

**CD/MP3 Quality Stereo 2:1 Multiplexer with Click and Pop Elimination**

The Intersil ISL54405 is a single supply, bidirectional, dual single-pole/double-throw (SPDT) ultra low distortion, high OFF-Isolation analog switch that can pass analog signals that are positive and negative with respect to ground. It is primarily targeted at consumer and professional audio switching applications such as Computer Sound Cards and Home Theater products. The inputs can accommodate ground referenced signals up to 2V<sub>RMS</sub> while operating from a single 3.3V or 5V DC supply. The digital logic inputs are 1.8V logic-compatible when using a single 3.3V or 5V supply. It can be used in both AC or DC coupled ground referenced applications.

The ISL54405 features a soft-switch feature and click/pop circuitry at each signal pin that eliminates clicks and pops associated with power-up/down conditions of the preceding amplifier outputs.

With -106dB THD+N performance with a 2V<sub>RMS</sub> signal into 20kΩ load, superior signal muting, high PSRR and very flat frequency response the ISL54405 meets the exacting requirements of consumer and professional audio engineers.

The ISL54405 is available in 16 Ld TSSOP, 16 Ld 3mmx3mm TQFN, and 16 Ld 2.6mmx1.8mm μTQFN packages. Its specified for operation over the -40°C to +85°C temperature range.

**TABLE 1. FEATURES AT A GLANCE**

	<b>ISL54405</b>
<b>Number of Switches</b>	2
<b>Switch Type</b>	SPDT or 2 to 1 MUX
<b>Insertion Loss</b>	±0.01dB
<b>THD+N, 2V<sub>RMS</sub>, 20kΩLoad</b>	-106dB
<b>OFF-Isolation (MUTE)</b>	125dB
<b>Packages</b>	16 Ld TSSOP, 16 Ld 3x3 TQFN, 16 Ld 2.6x1.8 μTQFN

**Related Literature**

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Application Note AN557 "Recommended Test Procedures for Analog Switches"

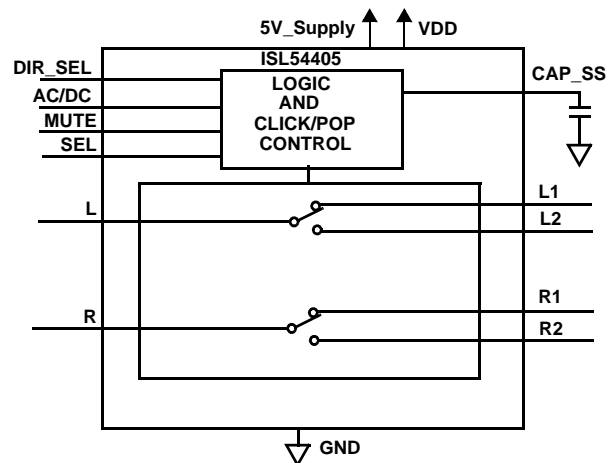
**Features**

- Clickless Audio Switching
- 2V<sub>RMS</sub> Signal Switching from 3.3V or 5V Supply
- -106dB THD+N into 20kΩ Load @ 2V<sub>RMS</sub>
- -108dB THD+N into 32Ω Load @ 3.9mW
- Signal to Noise . . . . . >124dBV
- ±0.01dB Insertion Loss at 1kHz, 20kΩ Load
- ±0.007dB Gain Variation 20Hz to 20kHz
- 125dB Signal Muting into 20kΩ Load
- 90dB PSRR 20Hz to 20kHz
- Single Supply Operation . . . . . 3.3V or 5V
- Available in 16 Ld TSSOP, 16 Ld TQFN, and 16 Ld μTQFN
- Pb-Free (RoHS Compliant)

**Applications**

- Computer Sound Cards
- Home Theater Audio Products
- SACD/DVD Audio
- DVD Player Audio Output Switching
- Headsets for MP3/Cellphone Switching
- Hi-Fi Audio Switching Application

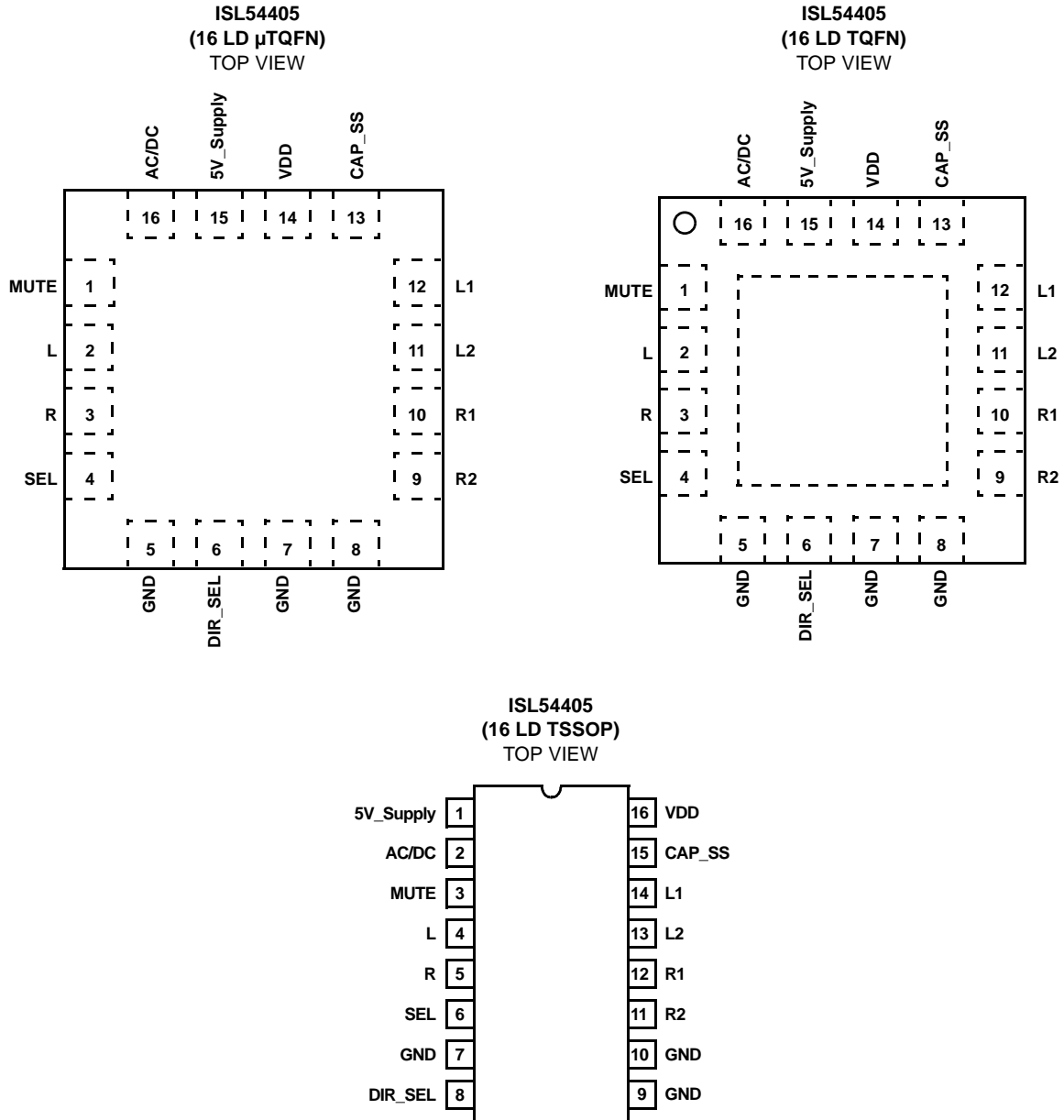
**Block Diagram**



For 5V operation connect the 5V\_Supply pin to 5V and float the VDD pin. For 3.3V operation connect the VDD pin to 3.3V and float the 5V\_Supply pin.

# ISL54405

## Pinouts (Note 1)



NOTE:

1. See Page 1 for ISL54405 Block Diagram.

**Truth Table**

INPUTS				OUTPUTS				
AC/DC	DIR	MUTE	SEL	L1, R1	L2, R2	COM (L,R) C/P Shunts	L1, R1 C/P Shunts	L2, R2 C/P Shunts
0	X	0	0	ON	OFF	OFF	OFF	OFF
0	X	0	1	OFF	ON	OFF	OFF	OFF
0	X	1	X	OFF	OFF	OFF	OFF	OFF
1	0	0	0	ON	OFF	OFF	OFF	ON
1	0	0	1	OFF	ON	OFF	ON	OFF
1	0	1	X	OFF	OFF	OFF	ON	ON
1	1	0	0	ON	OFF	OFF	OFF	OFF
1	1	0	1	OFF	ON	OFF	OFF	OFF
1	1	1	X	OFF	OFF	ON	OFF	OFF

NOTE: MUTE, AC/DC, DIR: Logic "0"  $\leq$  0.5V, Logic "1"  $\geq$  1.4V or Float with a 3.3V Supply or 5V supply.

SEL: Logic "0"  $\leq$  0.5V, Logic "1"  $\geq$  1.4V with a 3.3V Supply or 5V supply.

X = Don't Care

**Pin Descriptions**

PIN	FUNCTION
VDD	System Power Supply Pin (+3V to +3.6V) (Float pin for 5V applications)
5V_Supply	5V Supply Pin (+4.5V to +5.5V) (Float pin for 3.3V applications)
GND	Ground Connection
CAP_SS	Soft-Start Capacitor Pin
MUTE	Signal Mute Control Pin

**Pin Descriptions (Continued)**

PIN	FUNCTION
SEL	Input Select Control Pin
AC/DC	AC/DC Select Control Pin
DIR_SEL	DIRECTION Select Control Pin
R	Analog Switch Common Pin
L	Analog Switch Common Pin
L2, R2	Analog Switch Normally Open Pin
L1, R1	Analog Switch Normally Closed Pin

**Ordering Information**

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54405IVZ (Note 2)	54405 IVZ	-40 to +85	16 Ld TSSOP	M16.173
ISL54405IVZ-T* (Note 2)	54405 IVZ	-40 to +85	16 Ld TSSOP	M16.173
ISL54405IRTZ (Note 2)	05TZ	-40 to +85	16 Ld 3x3 TQFN	L16.3x3A
ISL54405IRTZ-T* (Note 2)	05TZ	-40 to +85	16 Ld 3x3 TQFN	L16.3x3A
ISL54405IRUZ-T* (Note 3)	GAD	-40 to + 85	16 Ld $\mu$ TQFN	L16.2.6x1.8A

\*Please refer to TB347 for details on reel specifications.

**NOTES:**

- These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

**Absolute Maximum Ratings**

VDD to GND	-0.3V to 4.0V
5V_Supply to GND	-0.3V to 6.0V
Input Voltages	
SEL, MUTE, AC/DC, DIR_SEL (Note 4)	-0.3 to ((V <sub>DD</sub> ) + 0.3V)
L1, L2, R1, R2 (Note 4)	-3.1 to ((V <sub>DD</sub> ) + 0.3V)
Output Voltages	
R, L (Note 4)	-3.1 to ((V <sub>DD</sub> ) + 0.3V)
Continuous Current L1, L2, R1, R2 or L, R	±300mA
Peak Current L1, L2, R1, R2 or L, R	
(Pulsed 1ms, 10% Duty Cycle, Max)	±500mA
ESD Rating:	
Human Body Model	>5kV
Machine Model	>200V
Charged Device Model	>2kV

**Thermal Information**

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
16 Ld TSSOP Package (Note 5)	150	N/A
16 Ld TQFN Package (Notes 6, 7)	75	11
16 Ld $\mu$ TQFN Package (Note 6)	93	N/A
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Pb-free reflow profile	see link below	
<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>		

**Operating Conditions**

Temperature Range	-40°C to +85°C
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*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

**NOTES:**

- Signals on L1, L2, R1, R2, MUTE, SEL, AC/DC, DIR\_SEL, R, and L exceeding V<sub>DD</sub> or GND by specified amount are clamped. Limit current to maximum current ratings.
- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

**Electrical Specifications - 3.3V Supply**

Test Conditions: V<sub>DD</sub> = +3.0V to +3.6V, GND = 0V, V<sub>DIR\_SEL</sub> = V<sub>AC/DC</sub> = GND, V<sub>5V\_SUPPLY</sub> = Float, V<sub>SIGNAL</sub> = 2V<sub>RMS</sub>, R<sub>LOAD</sub> = 20k $\Omega$ , f = 1kHz, V<sub>SELH</sub> = V<sub>MUTEH</sub> = 1.4V, V<sub>SELL</sub> = V<sub>MUTEL</sub> = 0.5V, CAP<sub>SS</sub> = 0.1 $\mu$ F, (Note 8), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	SUPPLY	TEMP (°C)	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNITS
<b>ANALOG SWITCH CHARACTERISTICS</b>							
Analog Signal Range, V <sub>ANALOG</sub>		3.3V, 5V	Full	-	2	-	V <sub>RMS</sub>
ON-Resistance, r <sub>ON</sub>	V <sub>DD</sub> = 3.3V, I <sub>R</sub> or I <sub>L</sub> = 80mA, V <sub>Lx</sub> or V <sub>Rx</sub> = -2.828V to +2.828V (See Figure 4)	3.3V	25	-	1.9	-	$\Omega$
			Full	-	2.6	-	$\Omega$
r <sub>ON</sub> Matching Between Channels, $\Delta$ r <sub>ON</sub>	V <sub>DD</sub> = 3.3V, I <sub>R</sub> or I <sub>L</sub> = 80mA, V <sub>Lx</sub> or V <sub>Rx</sub> = Voltage at max r <sub>ON</sub> over -2.828V to +2.828V (Note 13)	3.3V	25	-	0.023	-	$\Omega$
			Full	-	0.045	-	$\Omega$
r <sub>ON</sub> Flatness, r <sub>FLAT(ON)</sub>	V <sub>DD</sub> = 3.3V, I <sub>R</sub> or I <sub>L</sub> = 80mA, V <sub>Lx</sub> or V <sub>Rx</sub> = -2.828V, 0V, +2.828V (Note 11)	3.3V	25	-	0.003	0.01	$\Omega$
			Full	-	0.009	-	$\Omega$
L, R, Lx, Rx Pull-down Resistance	V <sub>DD</sub> = 3.6V, V <sub>Lx</sub> or V <sub>Rx</sub> = -2.83V, 2.83V, V <sub>L</sub> or V <sub>R</sub> = -2.83V, 2.83V, V <sub>AC/DC</sub> = 0V, V <sub>MUTE</sub> = 3.6V, Measure Current, calculate Resistance.	3.6V	25	225	300	375	k $\Omega$
			Full	-	345	-	k $\Omega$
<b>DYNAMIC CHARACTERISTICS</b>							
THD+N	V <sub>SIGNAL</sub> = 2V <sub>RMS</sub> , f = 1kHz, A-weighted Filter, R <sub>LOAD</sub> = 20k $\Omega$	3.3V, 5V	25	-	-106	-	dB
	V <sub>SIGNAL</sub> = 1.9V <sub>RMS</sub> , f = 1kHz, A-weighted Filter, R <sub>LOAD</sub> = 20k $\Omega$		25	-	-113	-	dB
	V <sub>SIGNAL</sub> = 1.8V <sub>RMS</sub> , f = 1kHz, A-weighted Filter, R <sub>LOAD</sub> = 20k $\Omega$		25	-	-116	-	dB
	V <sub>SIGNAL</sub> = 0.707V <sub>RMS</sub> , f = 1kHz, A-weighted Filter, R <sub>LOAD</sub> = 32 $\Omega$		25	-	-100	-	dB
SNR	f = 20Hz to 20kHz, A-weighted Filter, Inputs grounded, R <sub>LOAD</sub> = 20k $\Omega$ or 32 $\Omega$	3.3V, 5V	25	-	>124	-	dBV

**Electrical Specifications - 3.3V Supply** Test Conditions:  $V_{DD} = +3.0V$  to  $+3.6V$ ,  $GND = 0V$ ,  $V_{DIR\_SEL} = V_{AC/DC} = GND$ ,  $V_{5V\_SUPPLY} = Float$ ,  $V_{SIGNAL} = 2V_{RMS}$ ,  $R_{LOAD} = 20k\Omega$ ,  $f = 1kHz$ ,  $V_{SELH} = V_{MUTEH} = 1.4V$ ,  $V_{SELL} = V_{MUTEL} = 0.5V$ ,  $CAP\_SS = 0.1\mu F$ , (Note 8), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	SUPPLY	TEMP (°C)	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNITS
Insertion Loss, $G_{ON}$	$f = 1kHz$ , $R_{LOAD} = 20k\Omega$	3.3V	25	-	$\pm 0.01$	-	dB
Gain vs Frequency, $G_f$	$f = 20Hz$ to $20kHz$ , $R_{LOAD} = 20k\Omega$ , Reference to $G_{ON}$ at $1kHz$	3.3V	25	-	$\pm 0.007$	-	dB
Stereo Channel Imbalance L1 and R1, L2 and R2	$f = 20Hz$ to $20kHz$ , $R_{LOAD} = 20k\Omega$	3.3V	25	-	$\pm 0.003$	-	dB
OFF-Isolation (Muting)	$f = 20Hz$ to $22kHz$ , $L = R = 2V_{RMS}$ , $R_{LOAD} = 20k\Omega$ , $MUTE = AC/DC = 3.3V$ , $DIR\_SEL = GND$ , $SEL = "X"$	3.3V, 5V	25	-	120	-	dB
	$f = 20Hz$ to $22kHz$ , $L1, R1, L2, R2 = 2V_{RMS}$ , $R_{LOAD} = 20k\Omega$ , $MUTE = AC/DC = DIR\_SEL = 3.3V$ , $SEL = "X"$		25	-	120	-	dB
	$f = 20Hz$ to $22kHz$ , $V_L$ or $V_R = 0.7V_{RMS}$ , $R_{LOAD} = 32\Omega$		25	-	125	-	dB
Crosstalk (Channel-to-Channel)	$R_L = 20k\Omega$ , $f = 20Hz$ to $20kHz$ , $V_{SIGNAL} = 2V_{RMS}$ , Signal source impedance = $20\Omega$ , Note: Crosstalk is inversely proportional to source impedance.	3.3V	25	-	120	-	dB
	$R_L = 32\Omega$ , $f = 20Hz$ to $20kHz$ , $V_{SIGNAL} = 0.7V_{RMS}$ , Signal source impedance = $20\Omega$ , Note: Crosstalk is inversely proportional to source impedance.		25	-	120	-	dB
PSRR	$f = 1kHz$ , $V_{SIGNAL} = 100mV_{RMS}$ , Inputs Grounded	3.3V, 5V	25	-	110	-	dB
	$f = 20kHz$ , $V_{SIGNAL} = 100mV_{RMS}$ , Inputs Grounded		25	-	90	-	dB
Bandwidth, -3dB	$R_{LOAD} = 50\Omega$	3.3V	25	-	230	-	MHz
ON to Mute Time, $T_{TRANS-OM}$	$CAP\_SS = 0.1\mu F$	3.3V	25	-	50	-	ns
Mute to ON Time, $T_{TRANS-MO}$	$CAP\_SS = 0.1\mu F$ (Selectable via Soft-Start Capacitor Value)	3.3V	25	-	58	-	ms
Turn-ON Time, $t_{ON}$	$V_{DD} = 3.3V$ , $V_{Lx}$ or $V_{Rx} = 1.5V$ , $V_{MUTE} = 0V$ , $R_L = 20k\Omega$ , (See Figure 1)	3.3V	25	-	45	-	$\mu s$
Turn-OFF Time, $t_{OFF}$	$V_{DD} = 3.3V$ , $V_{Lx}$ or $V_{Rx} = 1.5V$ , $V_{MUTE} = 0V$ , $R_L = 20k\Omega$ , (See Figure 1)	3.3V	25	-	50	-	ns
Break-Before-Make Time Delay, $t_D$	$V_{DD} = 3.6V$ , $V_{Lx}$ or $V_{Rx} = 1.5V$ , $V_{MUTE} = 0V$ , $R_L = 20k\Omega$ , See Figure 2	3.6V	25	-	45	-	$\mu s$
OFF-Isolation	$R_L = 50\Omega$ , $f = 1MHz$ , $V_L$ or $V_R = 1V_{RMS}$ , (See Figure 3)	3.3V	25	-	100	-	dB
Crosstalk (Channel-to-Channel)	$R_L = 50\Omega$ , $f = 1MHz$ , $V_L$ or $V_R = 1V_{RMS}$ , (See Figure 5)	3.3V	25	-	70	-	dB
Lx, Rx OFF Capacitance, $C_{OFF}$	$f = 1MHz$ , $V_{Lx}$ or $V_{Rx} = V_L$ or $V_R = 0V$ (See Figure 6)	3.3V	25	-	10	-	pF
L, R ON Capacitance, $C_{COM(ON)}$	$f = 1MHz$ , $V_{Lx}$ or $V_{Rx} = V_{COM} = 0V$ (See Figure 6)	3.3V	25	-	27	-	pF
<b>POWER SUPPLY CHARACTERISTICS</b>							
Power Supply Range, VDD	$5V\_Supply = Float$	3.3V	Full	3	-	3.6	V
Power Supply Range, $5V\_Supply$	$V_{DD} = Float$	5V	Full	4.5	-	5.5	V

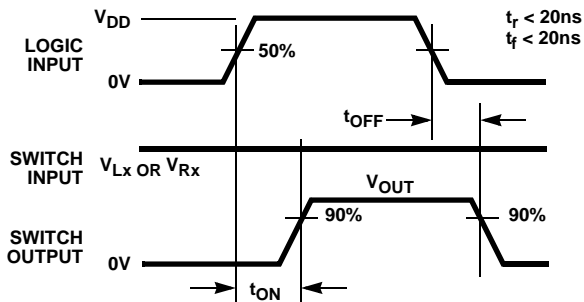
**Electrical Specifications - 3.3V Supply** Test Conditions:  $V_{DD} = +3.0V$  to  $+3.6V$ ,  $GND = 0V$ ,  $V_{DIR\_SEL} = V_{AC/DC} = GND$ ,  $V_{5V\_SUPPLY} = \text{Float}$ ,  $V_{SIGNAL} = 2V_{RMS}$ ,  $R_{LOAD} = 20k\Omega$ ,  $f = 1kHz$ ,  $V_{SELH} = V_{MUTEH} = 1.4V$ ,  $V_{SELL} = V_{MUTEL} = 0.5V$ ,  $CAP\_SS = 0.1\mu F$ , (Note 8), Unless Otherwise Specified. (Continued)

PARAMETER	TEST CONDITIONS	SUPPLY	TEMP (°C)	MIN (Notes 9, 10)	TYP	MAX (Notes 9, 10)	UNITS
Positive Supply Current, $I_+$	$V_{DD} = +3.6V$ , $V_{MUTE} = 0V$ , $V_{SEL} = 0V$ or $V_{DD}$	3.6V	25	-	54	65	$\mu A$
			Full	-	59	-	$\mu A$
	$V_{DD} = +3.6V$ , $V_{MUTE} = V_{DD}$ , $V_{SEL} = 0V$ or $V_{DD}$	3.6V	25	-	14	18	$\mu A$
		3.6V	Full	-	15	-	$\mu A$
	$V_{DD} = +3.6V$ , $V_{MUTE} = 0V$ , $V_{SEL} = 1.8V$	3.6V	25	-	55	65	$\mu A$
		3.6V	Full	-	58	-	$\mu A$
<b>DIGITAL INPUT CHARACTERISTICS</b>							
Input Voltage Low, $V_{SELL}$ , $V_{MUTEL}$		3.3V, 5V	Full	-	-	0.5	V
Input Voltage High, $V_{SELH}$ , $V_{MUTEH}$		3.3V, 5V	Full	1.4	-	-	V
Input Current, $I_{SELH}$ , $I_{SELL}$	$V_{DD} = 3.6V$ , $V_{MUTE} = 0V$ , $V_{SEL} = 0V$ or $V_{DD}$	3.6V	Full	-0.5	0.01	0.5	$\mu A$
Input Current, $I_{AC/DCL}$ , $I_{DIR\_SELL}$	$V_{DD} = 3.6V$ , $V_{AC/DC}$ , $V_{DIR\_SEL} = 0V$ , $V_{MUTE} = \text{Float}$ , $V_{SEL} = V_{DD}$	3.6V	Full	-1.3	-0.7	0.3	$\mu A$
Input Current, $I_{AC/DCH}$ , $I_{DIR\_SELH}$	$V_{DD} = 3.6V$ , $V_{AC/DC}$ , $V_{DIR\_SEL} = V_{DD}$ , $V_{MUTE} = 0V$ , $V_{SEL} = 0V$	3.6V	Full	-0.5	0.01	0.5	$\mu A$
Input Current, $I_{MUTEL}$	$V_{DD} = 3.6V$ , $V_{SEL} = V_{DD}$ , $V_{MUTE} = 0V$	3.6V	Full	-1.3	-0.7	0.3	$\mu A$
Input Current, $I_{MUTEH}$	$V_{DD} = 3.6V$ , $V_{SEL} = 0V$ , $V_{MUTE} = V_{DD}$	3.6V	Full	-0.5	0.01	0.5	$\mu A$

NOTES:

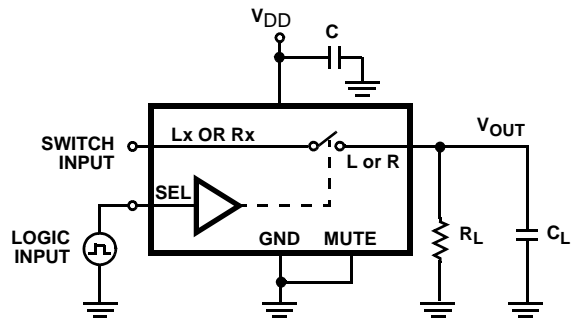
- $V_{IN}$  = input voltage to perform proper function.
- The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.
- Limits established by characterization and are not production tested.
- $r_{ON}$  matching between channels is calculated by subtracting the channel with the highest max  $r_{ON}$  value from the channel with lowest max  $r_{ON}$  value.

**Test Circuits and Waveforms**



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches.  $C_L$  includes fixture and stray capacitance.

$$V_{OUT} = V_{(Lx \text{ or } Rx)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

Test Circuits and Waveforms (Continued)

FIGURE 1. SWITCHING TIMES

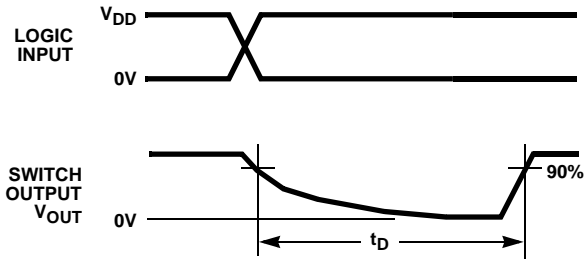
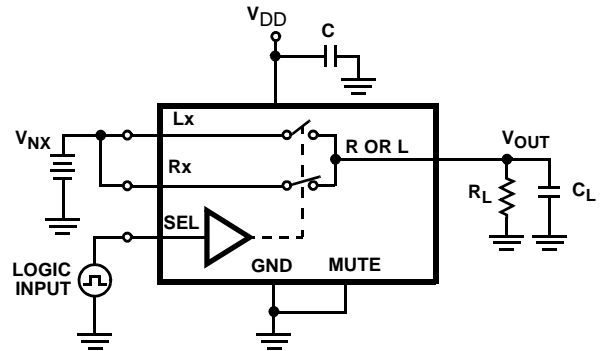


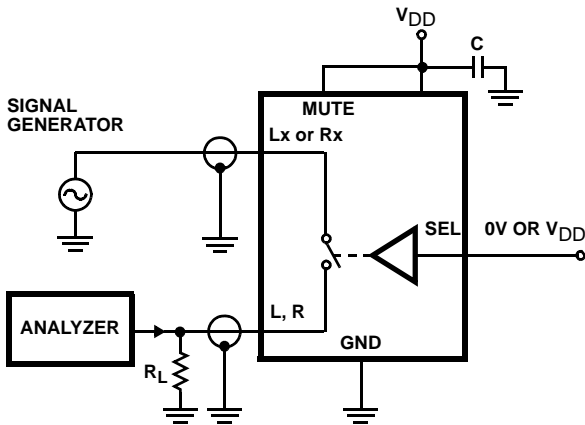
FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C<sub>L</sub> includes fixture and stray capacitance.

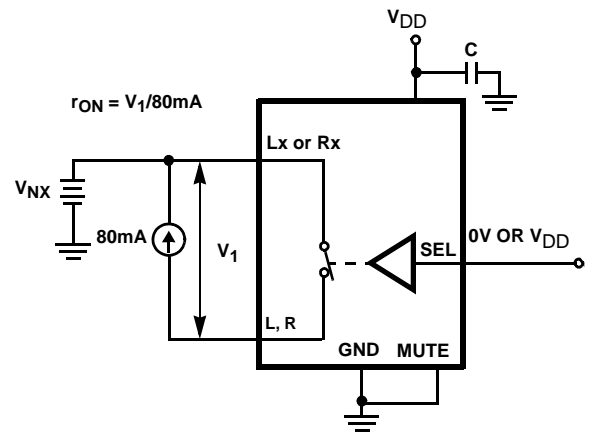
FIGURE 2B. TEST CIRCUIT

FIGURE 2. BREAK-BEFORE-MAKE TIME



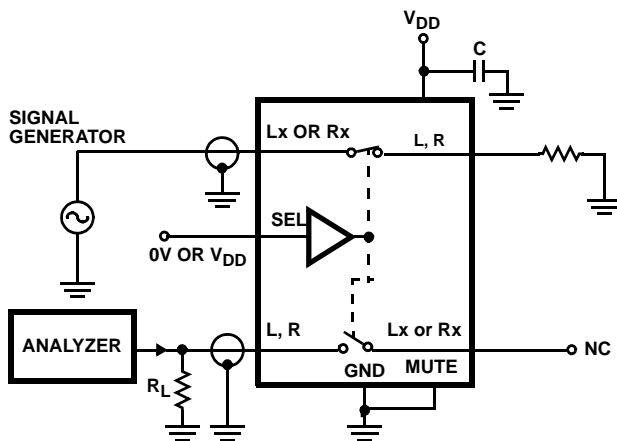
Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 3. OFF-ISOLATION TEST CIRCUIT



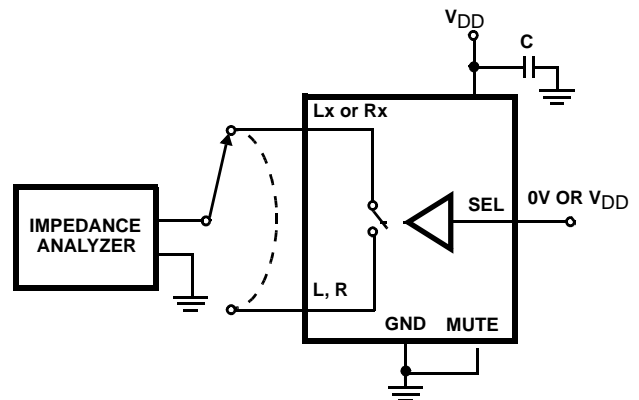
Repeat test for all switches.

FIGURE 4. r<sub>ON</sub> TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

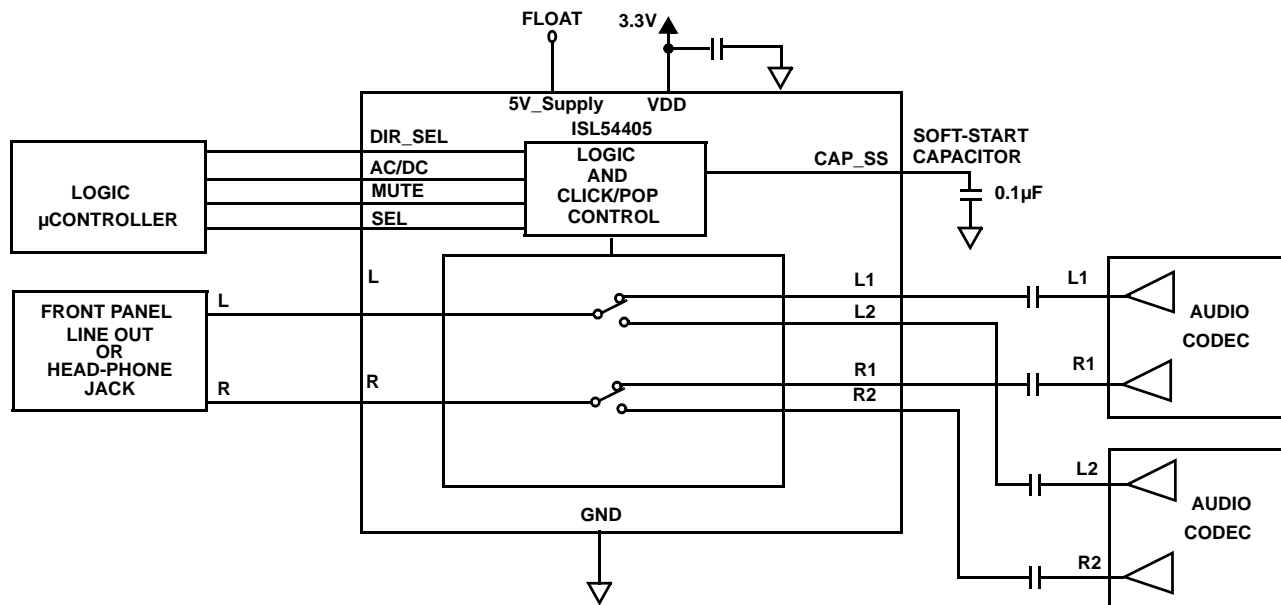
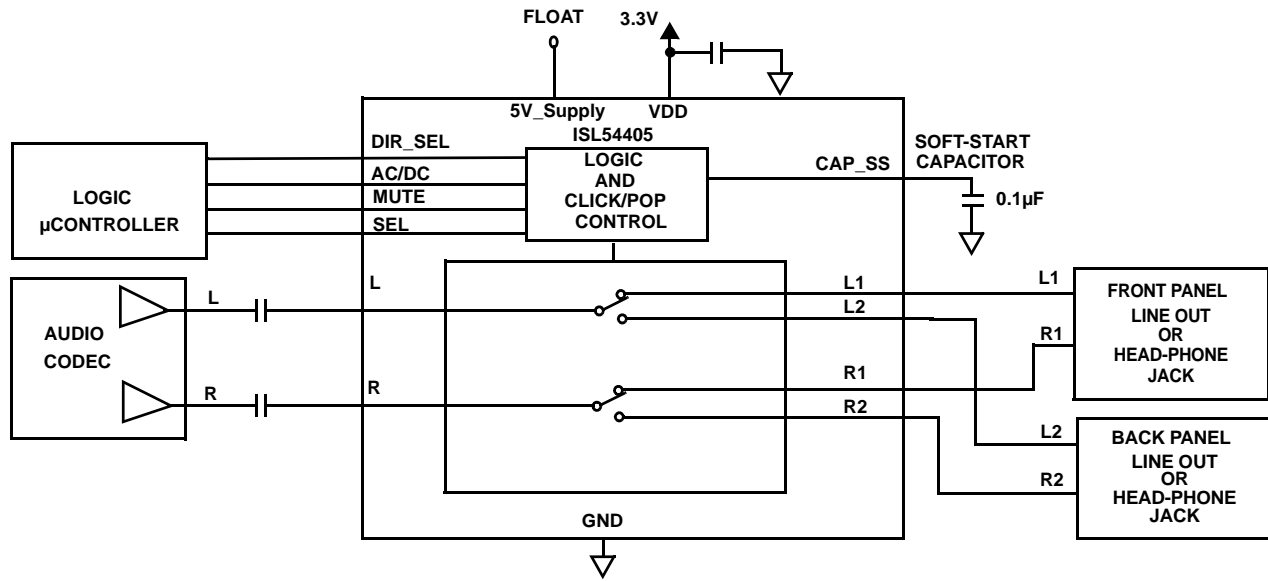
FIGURE 5. CROSSTALK TEST CIRCUIT



Repeat test for all switches.

FIGURE 6. CAPACITANCE TEST CIRCUIT

## Sound Card AC Coupled Application Block Diagrams



### Detailed Description

The ISL54405 is a single supply, bi-directional, dual single pole/double throw (SPDT) ultra low distortion, high off-isolation analog switch. It was designed to operate from either a 3.3V or 5V single supply. When operated with a 3.3V or 5V single supply, the switches can accommodate  $\pm 2.83V_{PEAK}$  ( $2V_{RMS}$ ) ground reference analog signals. The switch  $r_{ON}$  flatness across this range is extremely small resulting in excellent THD+N performance (0.0006% with 20k $\Omega$  load and 0.0014% with 32 $\Omega$  load at 707mV $_{RMS}$ ). The T-Type configuration of the switch cells prevents signals from getting through to the output when a switch is in the OFF-state providing for superior mute performance (>120dB) in audio applications.

The ISL54405 has special circuitry to eliminate click and pops in the speakers during power-up and power-down of the audio CODEC drivers, during removal and insertion of headphones, and while switching between sources and loads.

The ISL54405 was designed primarily for consumer and professional audio switching applications such as computer sound cards and home theater products. The "Application Block Diagrams" on this page show two typical sound card applications. In the upper block diagram the ISL54405 is being used to route a single stereo source to either the front or back panel line outs of the computer sound card. In the lower block diagram the ISL54405 is being used to multiplex two stereo sources to a single line out of the computer sound card.



### SPDT Switch Cell Architecture and Performance Characteristics

The normally open ( $L_2$ ,  $R_2$ ) and normally closed ( $L_1$ ,  $R_1$ ) of the SPDT switches are T-Type switches that have a typical  $r_{ON}$  of  $1.9\Omega$  and an off-isolation of  $>120\text{dB}$ . The low on-resistance ( $1.9\Omega$ ) and  $r_{ON}$  flatness ( $0.003\Omega$ ) provide very low insertion loss and minimal distortion to applications that require hi-fidelity signal reproduction.

The SPDT switch cells have internal charge pumps that allow for signals to swing below ground. They were specifically designed to pass audio signals that are ground referenced and have a swing of  $\pm 2.828V_{PEAK}$  while driving either  $10\text{k}/20\text{k}\Omega$  (receiver) or  $32\Omega$  (headphone) loads.

Each switch cell incorporates special circuitry to gradually decrease the switch resistance when transitioning from the OFF-state (high impedance) to the ON state ( $1.9\Omega$ ). The gradual decrease in the switch resistance provides for a slow ramp of the voltage at the load side of the switch which helps to eliminate click and pops in the speaker by suppressing the transient during switching events. The output voltage ramp time is determined by the capacitor value of the soft-start capacitor connected at the CAP\_SS pin. With a  $0.1\mu\text{F}$  ceramic chip capacitor the ramp time is approximately  $4.6\text{V/s}$ . The slow ramping of the signal at the output can be disabled by floating the CAP\_SS pin.

In addition to the slow ramp feature (soft-start feature) of the in line switches, the part has special click and pop (C/P) shunt circuitry at each of the signal pins ( $L$ ,  $R$ ,  $L_1$ ,  $L_2$ ,  $R_1$ , and  $R_2$ ). A pin's C/P shunt circuitry is activated or deactivated depending on the logic levels applied at the AC/DC and DIR\_SEL control pins. This shunt circuitry serves two functions:

1. In an AC coupled application they are activated and directed to the source side of the switch to suppress or eliminate click/pop noise in the speaker load when powering up or down of the audio CODEC drivers.
2. For superior muting the C/P shunt circuitry is activated and directed to the load side of the switch which gives  $>120\text{dB}$  of off-isolation when driving a  $10\text{k}/20\text{k}\Omega$  receiver load with an audio signal in the range of  $20\text{Hz}$  to  $22\text{kHz}$ .

If the AC/DC pin is driven LOW, all C/P shunt circuitry at all the signal pins ( $L$ ,  $R$ ,  $L_1$ ,  $R_1$ ,  $L_2$ , and  $R_2$ ) are deactivated and not operable.

If the AC/DC pin is driven HIGH then the logic at the DIR\_SEL pin will determine whether the L and R (COM) C/P shunt circuitry is activated or the  $L_1$ ,  $L_2$ ,  $R_1$ , and  $R_2$  (NOx, NCx) C/P shunt circuitry is activated. When the DIR\_SEL is driven LOW, the  $L_1$ ,  $R_1$ ,  $L_2$ ,  $R_2$  C/P shunt circuitry will be activated while the L and R C/P shunt circuitry will be deactivated. When the DIR\_SEL is driven HIGH the L and R C/P shunt circuitry will be activated while the  $L_1$ ,  $R_1$ ,  $L_2$ ,  $R_2$  C/P shunt circuitry will be deactivated. Note: Shunt circuitry that is activated will be turned ON when a switch cell is turned OFF and will be OFF when a switch cell is turned ON.

### Supply Voltage, Signal Amplitude, Grounding

The power supply connected at VDD or the 5V\_SUPPLY pin provides power to the ISL54405 part. The ISL54405 is a single supply device that was designed to be operated with a  $3.3\text{V} \pm 10\%$  DC supply connected at the VDD pin or a  $5\text{V} \pm 10\%$  DC supply connected at the 5V\_SUPPLY pin.

It was specifically designed to accept ground referenced  $2V_{RMS}$  ( $\pm 2.828V_{PEAK}$ ) audio signals at its signal pins while driving either  $10\text{k}/20\text{k}\Omega$  receiver loads or  $32\Omega$  headphone loads.

When using the part in a  $3.3\text{V}$  application the 5V\_Supply pin should be left floating. A  $0.1\mu\text{F}$  decoupling capacitor should be connected from the VDD pin to ground to minimize power supply noise and transients. This capacitor should be located as close to the pin as possible.

The part also has a 5V supply pin (5V\_Supply) to allow it to be used in  $5\text{V} \pm 10\%$  applications. Special circuitry within the device converts the 5V, connected at the 5V\_Supply pin, to  $3.3\text{V}$  to properly power the internal circuitry of the device.

When using the part in a  $5\text{V}$  application the VDD pin should be left floating. A  $0.1\mu\text{F}$  decoupling capacitor should be connected from the 5V\_Supply pin to ground to minimize power supply noise. This capacitor should be located as close to the pin as possible.

Grounding of the ISL54405 should follow a star configuration (see Figure 7). All grounds of the IC should be directly connected to the power supply ground return without cascading to other grounds. This configuration isolates shunt currents of the Click and Pop transients from the IC ground and optimizes device performance.

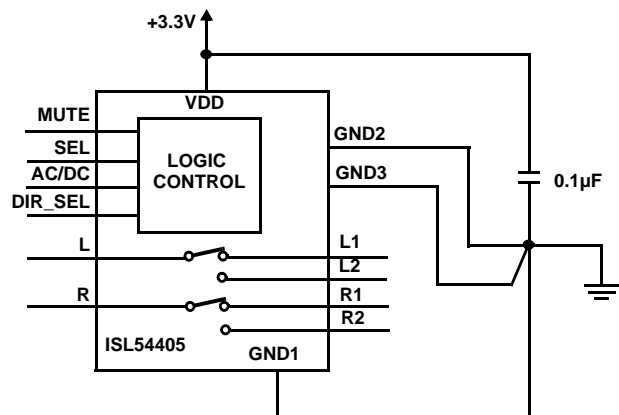


FIGURE 7. STAR GROUNDING CONFIGURATION

### Mute Operation

When the MUTE logic pin is driven HIGH the part will go into the Mute State. In the Mute State all switches of the SPDTs are OPEN while the T-Shunt switches are closed. In addition any activated click and pop shunt circuitry at the signal pins is turned ON.

See "Logic Control" on page 10 for more details.

## MUTE TO ON

When the Mute pin is driven LOW the ISL54405 will transition to the ON-state in the following sequence:

1. All active shunt switches turn-off quickly.
2. The resistance of the switches selected by the SEL pin will gradually decrease in resistance. They will decrease from their high OFF-resistance to their ON-resistance of  $1.9\Omega$ . This gradual decrease in resistance will allow for the voltage at the load to increase gradually. The voltage ramp rate at the load is determined by the value of the capacitor connected at the CAP\_SS pin. See Figures 27 and 28 in the "Typical Performance Curves" beginning on page 13.

Table 2 indicates how the signal ramp rate at the load changes as you change the CAP\_SS capacitor value. It also shows how the mute turn-on time is affected.

**TABLE 2. SIGNAL RAMP-RATE LOAD CHANGE WITH CAP SS**

CAPACITOR VALUE	RAMP RATE	TURN-ON TIME
No Capacitor	6250V/s	65 $\mu$ s
0.05 $\mu$ F	10.3V/s	30ms
0.1 $\mu$ F	4.6V/s	58ms

## ON TO MUTE

When the Mute pin is driven HIGH the switches will turn OFF quickly (50ns) and the active shunt switches will turn ON quickly. Note: There is no gradual ramping of the switch resistance in this direction.

## OFF-ISOLATION IN THE MUTE STATE

When in the mute state, the level of OFF-Isolation across the audio band is dependent on the signal amplitude, external loading, and location of the activated C/P (click/pop) shunt circuitry. During muting the logic of the ISL54405 can be configured to activate the C/P shunt circuitry on the load side of the switch or on the source side of the switch, or deactivated on both sides of the switch.

With a  $0.707V_{RMS}$  signal driving a  $32\Omega$  headphone load the location of the C/P shunt circuitry has little effect on the off-isolation performance (> 120dB of off-isolation in all configurations). See Figure 11 in the "Typical Performance Curves" beginning on page 13.

With a  $2V_{RMS}$  signal driving a  $20k\Omega$  amplifier load the best off-isolation is achieved by placing the C/P shunt circuitry on the load side of the switch (>120dB across the audio band). The off-isolation decreases when placing the C/P shunt circuitry on the source side of the switch (>85dB across the audio band). See Figure 10 in the "Typical Performance Curves" beginning on page 13.

Note: For AC coupled applications when powering up or down of the audio codecs the C/P shunts should be

activated on the source side of the switch. See "Click and Pop Operation" on page 11.

When using the switch for muting of the audio signal the C/P shunt circuitry should be de-activated on the source side of the switch and directed to the load side of the switch for best possible off-isolation.

## Logic Control

The ISL54405 has four logic control pins; the AC/DC, DIR\_SEL, MUTE, and SEL. The MUTE and SEL control pins determine the state of the switches. The AC/DC and DIR\_SEL control pins determine the location of the C/P (click/pop) shunt circuitry and if it will be active or not. See "Truth Table" on page 3.

The ISL54405 logic is 1.8V CMOS compatible (Low  $\leq 0.5V$  and High  $\geq 1.4V$ ) over a supply range of 3.0V to 3.6V at the VDD pin or 4.5V to 5.5V at the 5V\_SUPPLY pin. This allows control via 1.8V or 3V  $\mu$ controller.

## SEL, MUTE CONTROL PINS

The state of the SPDT switches of the ISL54405 device is determined by the voltage at the MUTE pin and the SEL pin.

The SEL control pin is only active when MUTE is logic "0". The MUTE has an internal pull-up resistor to the internal 3.3V supply rail and can be driven high or tri-stated(floated) by the  $\mu$ processor.

These pins are 1.8V logic compatible. When powering the part by the VDD pin the logic voltage can be as high as the VDD voltage which is typically 3.3V. When powering the part by the 5V\_SUPPLY pin the logic voltage can be as high as the 5V\_SUPPLY voltage which is typically 5V.

Logic Levels:

MUTE = Logic "0" (Low) when  $\leq 0.5V$

MUTE = Logic "1" (High) when  $\geq 1.4V$  or Floating

SEL = Logic "0" (Low) when  $\leq 0.5V$

SEL = Logic "1" (High) when  $\geq 1.4V$

## AC/DC AND DIR\_SEL CONTROL PINS

The ISL54405 contains C/P (click/pop) shunt circuitry on its COM pins (L, R) and on its signal pins (L1, R1, L2, R2). The activation of this circuitry and whether it is located on the COM or signal side of the switch is determined by the logic levels applied at the AC/DC and DIR\_SEL pins. The DIR\_SEL control pin is only active when AC/DC is logic "1". Note: Any activated C/P shunt circuitry is ON when in the mute state (MUTE = Logic "1") and OFF in the audio state (MUTE = Logic "0").

When AC/DC is logic "0", all of the C/P shunt circuitry on both sides of the switch is deactivated and not operable.

When AC/DC is logic "1" then the DIR\_SEL logic level determines whether the shunt circuitry will be activated on the COM side of the switch or on the signal side of the switch. When DIR\_SEL = Logic "1" the C/P shunts on the

COM side (L,R) are activated and inoperable on the signal side (L1, R1, L2, R2) of the switch. When DIR\_SEL = Logic "0" the C/P shunts are activated on the signal side (L1, R1, L2, R2) and inoperable on the COM side (L, R).

Logic Levels:

AC/DC, DIR\_SEL = Logic "0" (Low) when  $\leq 0.5V$

AC/DC, DIR\_SEL = Logic "1" (High) when  $\geq 1.4V$  or Floating.

The AC/DC and DIR\_SEL have internal pull-up resistors to the internal 3.3V supply rail and can be driven high or tri-stated (floated by the  $\mu$ processor). They should be driven to ground for a logic "0" (Low). Note: For 5V applications, the AC/DC and DIR\_SEL pins should never be driven to the external 5V rail. They need to be driven with 1.8V logic or 3V logic circuit.

### **AC Coupled or DC Coupled Operation**

The Audio CODEC drivers can be directly coupled to the ISL54405 when the audio signals from the drivers are ground referenced or do not have a significant DC offset voltage,  $< 50mV$ . Otherwise the signal should be AC coupled to the ISL54405 part.

### **CLICK AND POP OPERATION**

The ISL54405 has special circuitry to eliminate click and pops in the speakers during power-up and power-down of the Audio CODEC Drivers and during removal and insertion of headphones.

A different click and pop scheme is required depending on whether the audio CODEC drivers are AC coupled or DC coupled to the inputs of the ISL54405 part.

### **AC COUPLED CLICK AND POP OPERATION**

Single supply audio drivers have their signal biased at a DC offset voltage, usually at 1/2 the DC supply voltage of the driver. As this DC bias voltage comes up or goes down during power up or down of the driver a transient can be coupled into the speaker load through the DC blocking capacitor (see the "Application Block Diagrams" on page 8).

When a driver is OFF and suddenly turned ON the rapidly changing DC bias voltage at the output of the driver will cause an equal voltage at the input side of the switch due to the fact that the voltage across the blocking capacitor cannot change instantly. If the switch is in Audio mode or there is no low impedance path to discharge the capacitor voltage at the input of the switch, before turning on the switch, a transient discharge will occur in the speaker, generating a Click and pop noise.

Proper elimination of a click/pop transient at the speaker load while powering up or down of the audio driver requires that the ISL54405 have its C/P shunts activated on the source side of the switch and then placed in Mute mode. This allows the transient generated by the audio drivers to be discharged through the Click and Pop shunt circuitry.

Once the driver DC bias has reached  $V_{DD}/2$  and the transient on the switch side of the DC blocking capacitor has been discharged to ground through the C/P shunt circuitry, the switches can be turned ON and connected through to the speaker loads without generating an undesirable click/pop in the speakers.

With a typical DC blocking capacitor of  $220\mu F$  and the C/P shunt circuitry designed to have a resistance of  $40\Omega$ , allowing a 100ms wait time to discharge the transient before placing the switch in the Audio mode will prevent the transient from getting through to the speaker load. See Figures 25 and 26 in the "Typical Performance Curves" beginning on page 13.

### **DC COUPLED CLICK AND POP OPERATION**

The ISL54405 can pass ground referenced audio signals which allows it to be directly connected to audio drivers that output ground referenced audio signals, eliminating the need for a DC blocking capacitor.

Audio drivers that swing around ground however do generate some DC offset, from a few millivolts to tens of millivolts. When switching between audio channels or muting the audio signal these small DC offset levels of the drivers can generate a transient that can cause un-wanted clicks and pops in the speaker loads.

In a DC coupled application the C/P shunt resistors placed at the source side of the switch have no effect in eliminating the transients at the speaker loads when transitioning in and out of the mute state or switching between channels. In fact having these C/P shunts active on the source side only increase un-necessary power consumption. So, for DC coupled connection the C/P shunt circuitry should not be applied at the source (driver) side of the switch.

For DC coupled applications the ISL54405 has a special soft-start feature that slowly ramps the DC offset voltage from the audio driver to the speaker load when turning ON a switch channel. The ramp rate at the load is determined by the capacitor value connected at the CAP\_SS pin.

Lab experimentation has shown that if you can slow the voltage ramp rate at the speaker to  $< 10V/s$ , you can eliminate click/pop noise in a speaker. A soft-start capacitor value of  $0.1\mu F$  provides for  $4.5V/s$  ramp rate and is recommended. See Figures 27 and 28 in the "Typical Performance Curves" beginning on page 13.

See "MUTE to ON" section on page 10 for more detail of how soft-start works.

### **Supply Sequencing and Overvoltage Protection**

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes or diode stacks from the pin to  $V_{DD}$  and to GND (see Figure 8). To prevent forward biasing these

diodes,  $V_{DD}$  must be applied before any input signals, and the signal voltages must remain between  $V_{DD}$  and  $-3V$  and the logic voltage must remain between  $V_{DD}$  and ground.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provide additional protection to limit the current in the event that the voltage at a signal pin goes below ground by more than  $-3V$  or above the  $V_{DD}$  rail and the logic pin goes below ground or above the  $V_{DD}$  rail.

Logic inputs can be protected by adding a  $1k\Omega$  resistor in series with the logic input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low  $r_{ON}$  switch. Connecting Schottky diodes to the signal pins (as shown in Figure 8) will shunt the fault current to the supply or to ground thereby protecting the switch. These Schottky diodes must be sized to handle the expected fault current and to clamp when the voltage reaches the overvoltage limit.

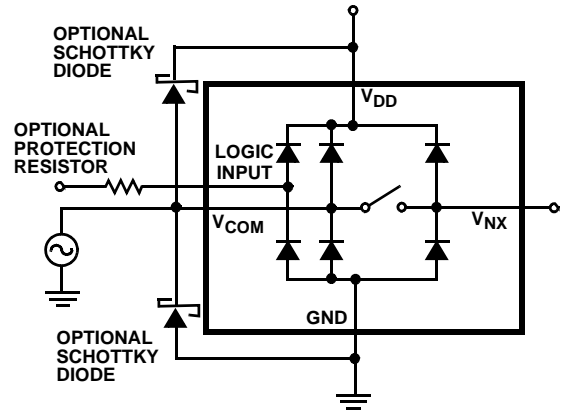


FIGURE 8. OVERVOLTAGE PROTECTION

### High-Frequency Performance

In  $50\Omega$  systems, the ISL54405 has a  $-3dB$  bandwidth of  $230MHz$  (see Figure 29). The frequency response is very consistent over varying analog signal levels.

An OFF-switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off-Isolation is the resistance to this feedthrough, while crosstalk indicates the amount of feedthrough from one switch to another. Figure 30 details the high Off-Isolation and crosstalk rejection provided by this part. At  $1MHz$ , Off-Isolation is about  $100dB$  in  $50\Omega$  systems, decreasing approximately  $20dB$  per decade as frequency increases. Higher load impedances decrease off-Isolation and Crosstalk rejection due to the voltage divider action of the switch off impedance and the load impedance.

Typical Performance Curves  $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified

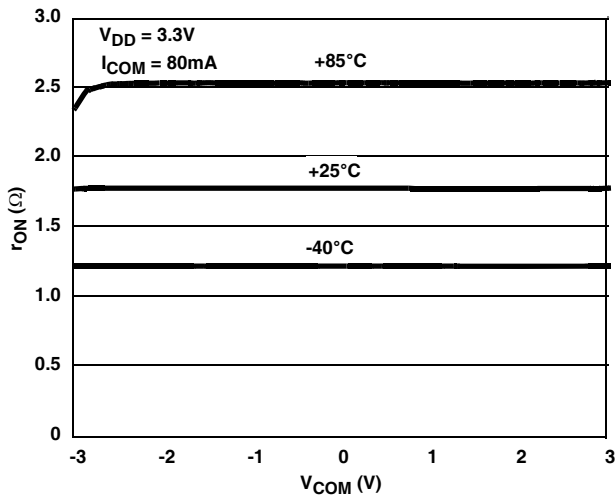


FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE

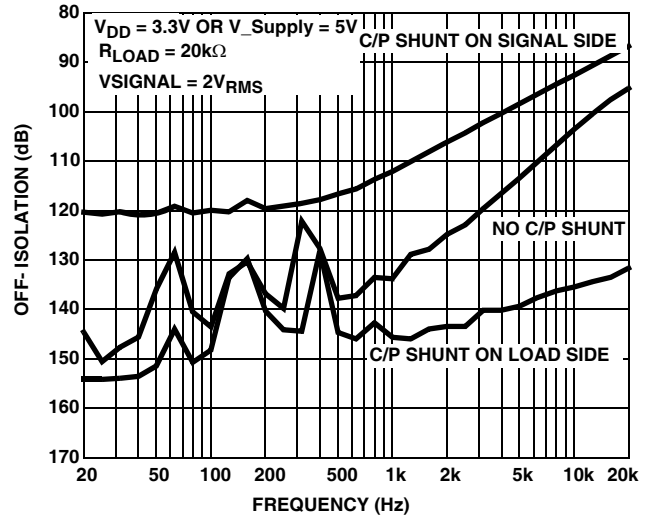


FIGURE 10. OFF-ISOLATION,  $2V_{RMS}$  SIGNAL,  $20k\Omega$  Load

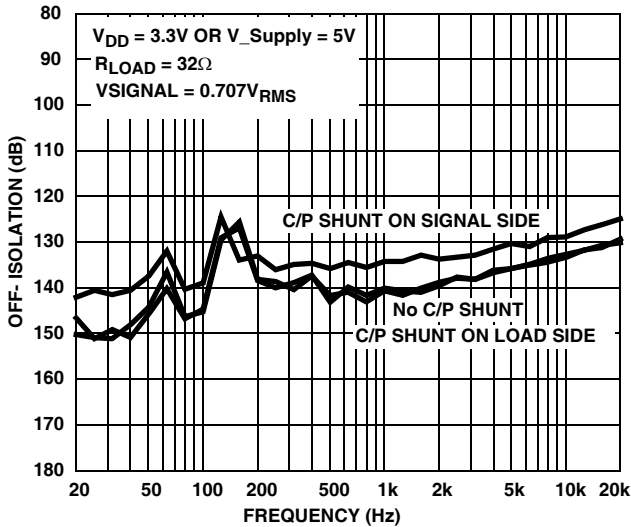


FIGURE 11. OFF-ISOLATION,  $0.707V_{RMS}$  SIGNAL,  $32\Omega$  LOAD

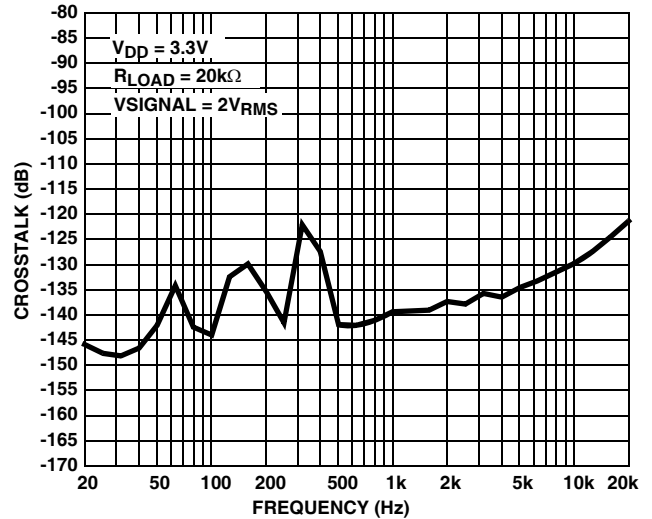


FIGURE 12. CHANNEL-TO-CHANNEL CROSSTALK

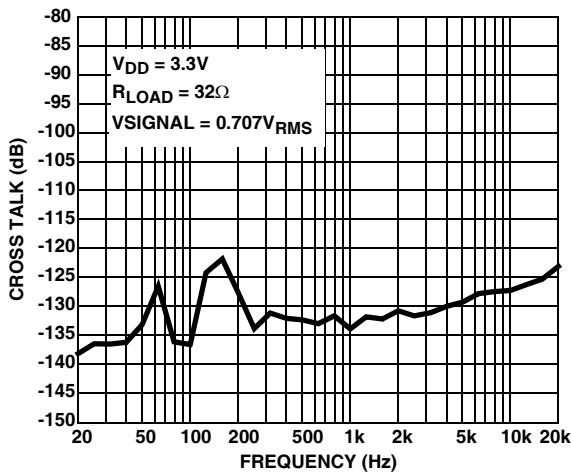


FIGURE 13. CHANNEL-TO-CHANNEL CROSSTALK

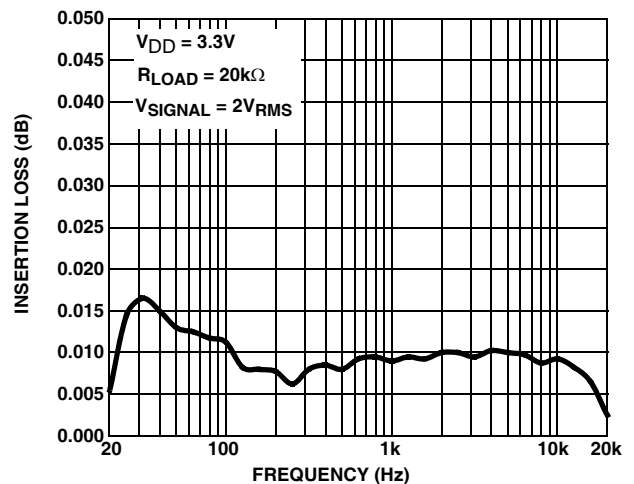


FIGURE 14. INSERTION LOSS vs FREQUENCY

Typical Performance Curves  $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

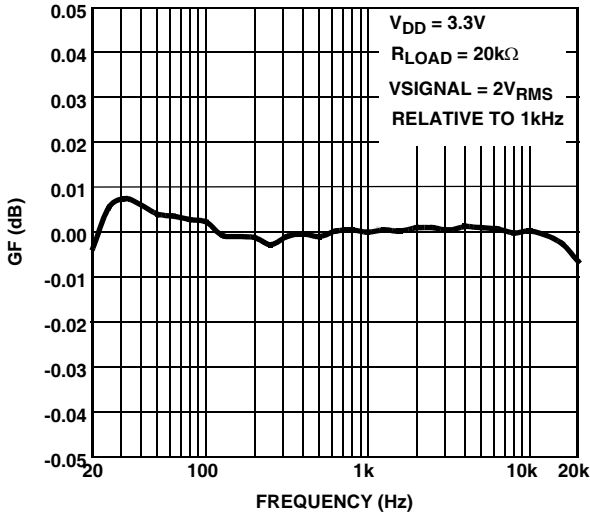


FIGURE 15. GAIN vs FREQUENCY

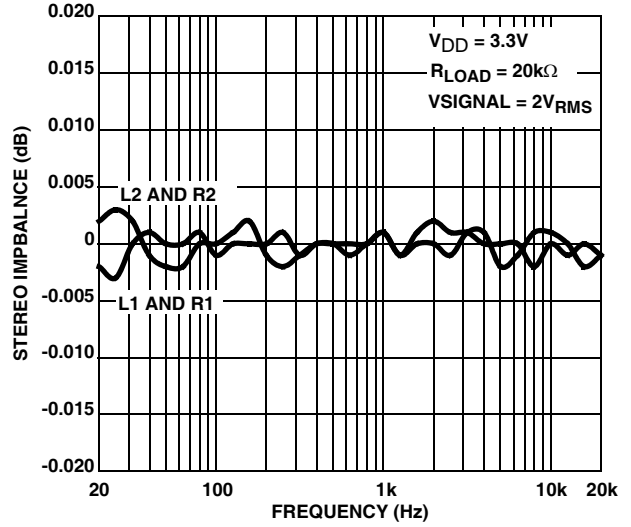


FIGURE 16. STEREO IMBALANCE vs FREQUENCY

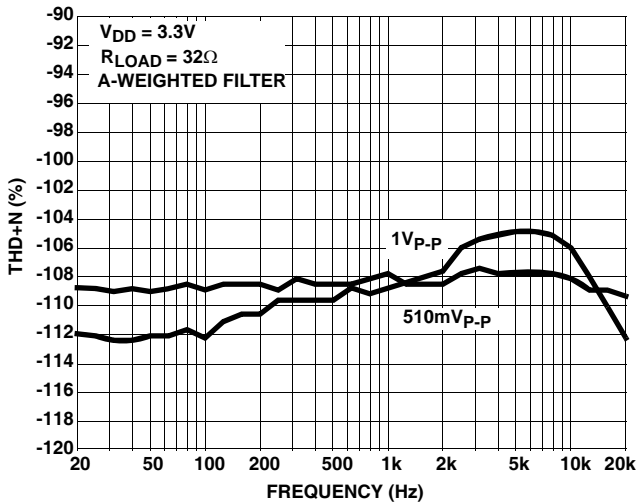


FIGURE 17. THD+N vs SIGNAL LEVELS vs FREQUENCY

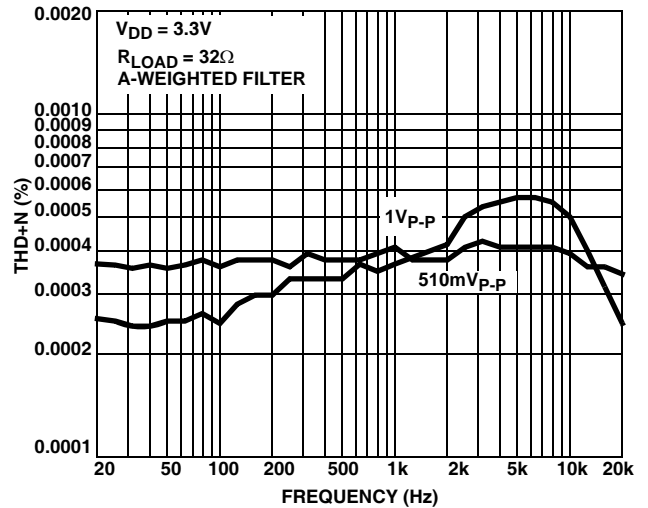


FIGURE 18. THD+N vs SIGNAL LEVELS vs FREQUENCY

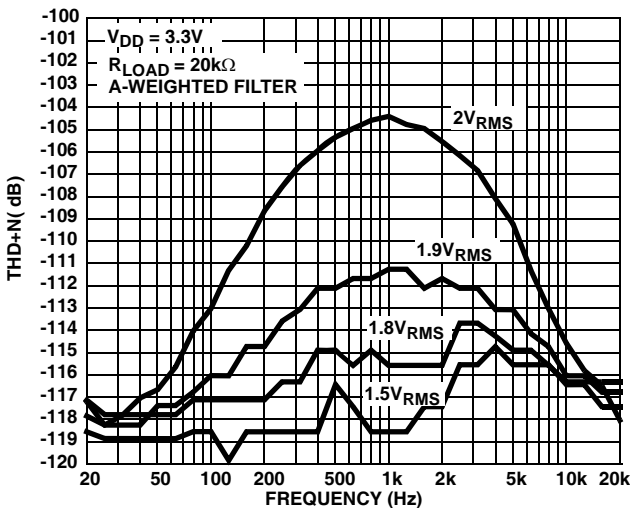


FIGURE 19. THD+N vs SIGNAL LEVELS vs FREQUENCY

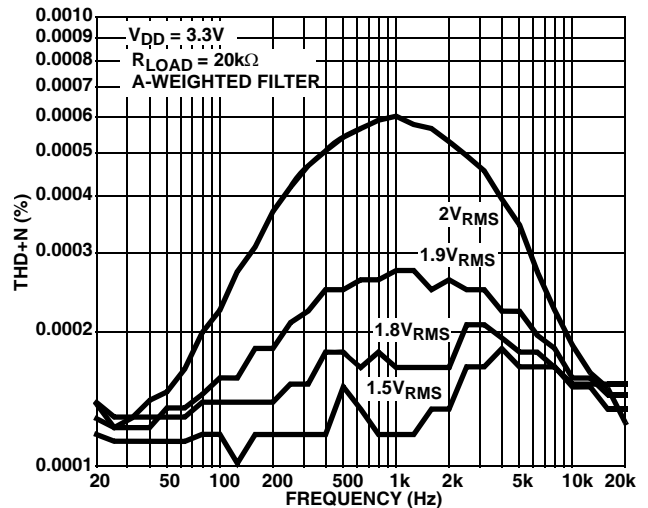


FIGURE 20. THD+N vs SIGNAL LEVELS vs FREQUENCY



Typical Performance Curves  $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

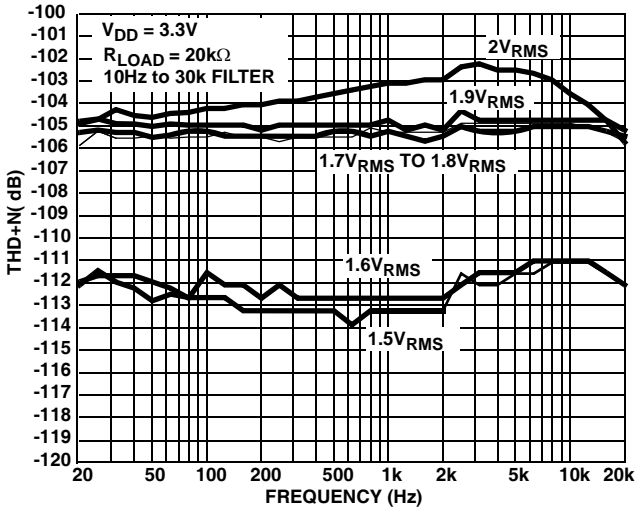


FIGURE 21. THD+N vs SIGNAL LEVELS vs FREQUENCY

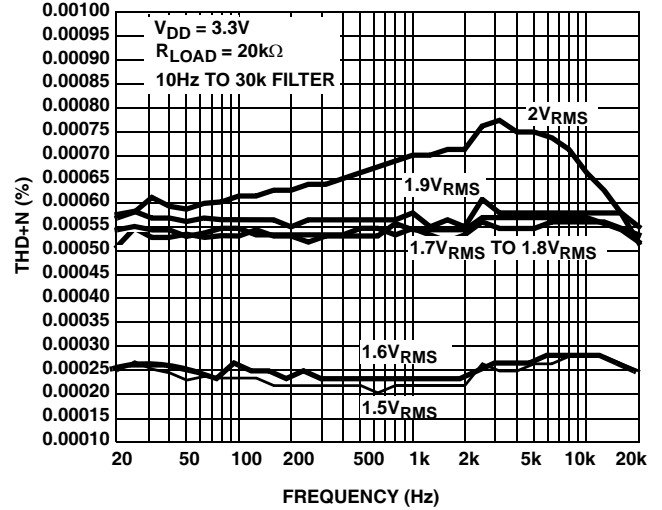


FIGURE 22. THD+N vs SIGNAL LEVELS vs FREQUENCY

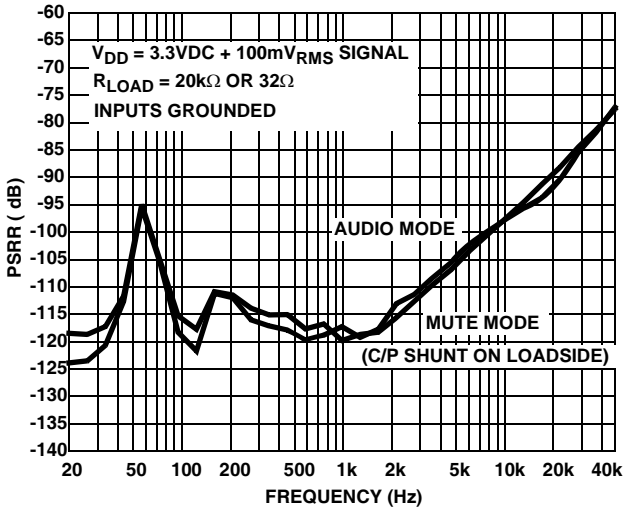


FIGURE 23. PSRR vs FREQUENCY

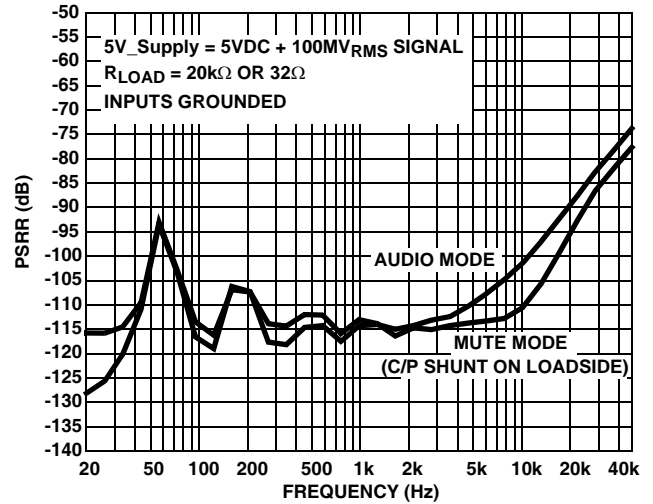


FIGURE 24. PSRR vs FREQUENCY

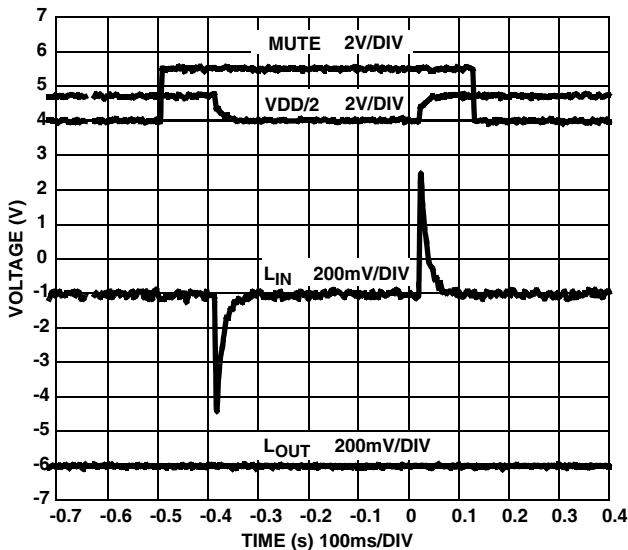


FIGURE 25. 20kΩ AC COUPLED CLICK/POP REDUCTION

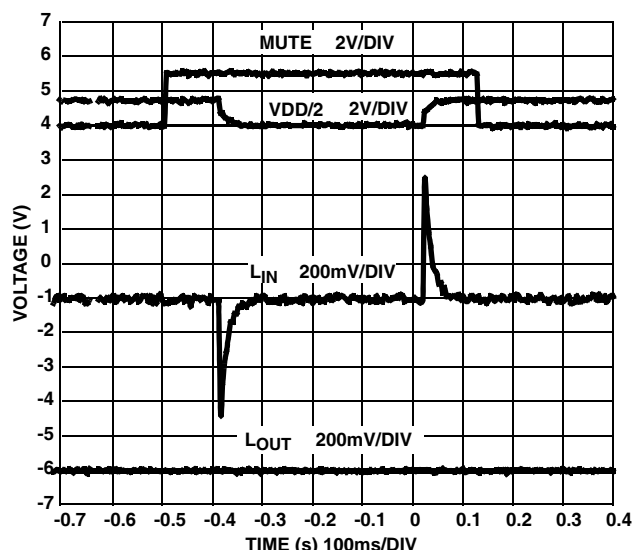


FIGURE 26. 32Ω AC COUPLED CLICK/POP REDUCTION

**Typical Performance Curves**  $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

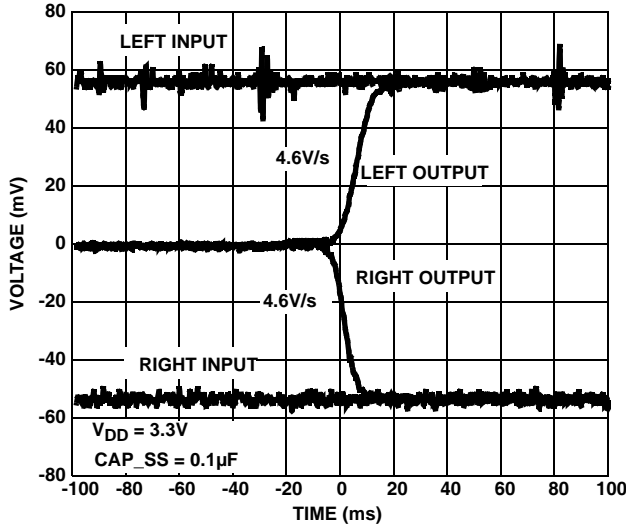


FIGURE 27. SOFT-START (0.1µF) CLICK/POP REDUCTION

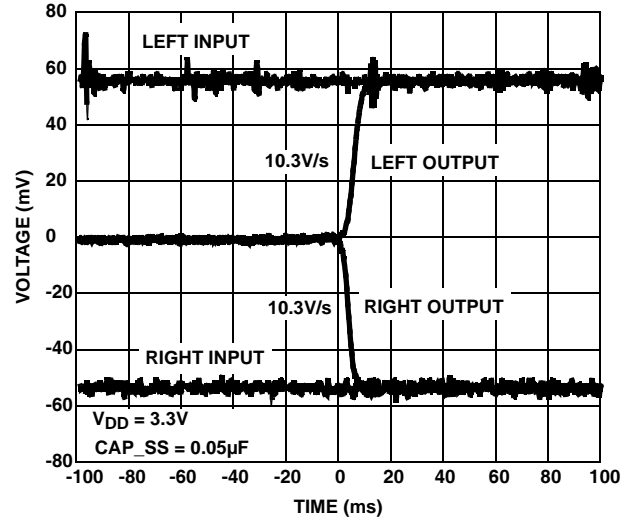


FIGURE 28. SOFT-START (0.05µF) CLICK/POP REDUCTION

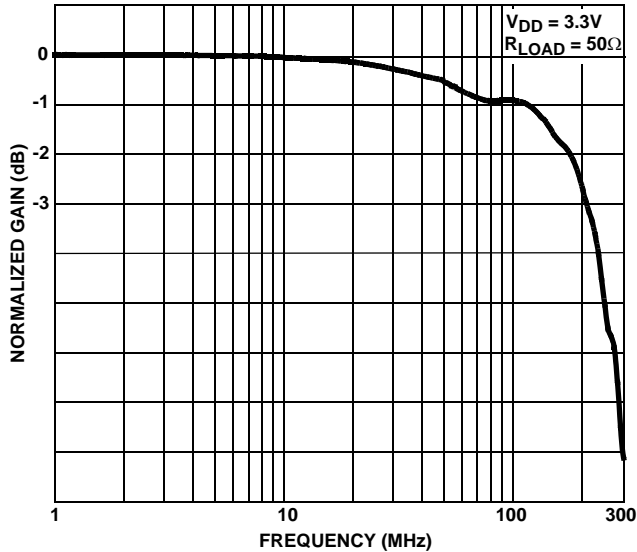


FIGURE 29. FREQUENCY RESPONSE

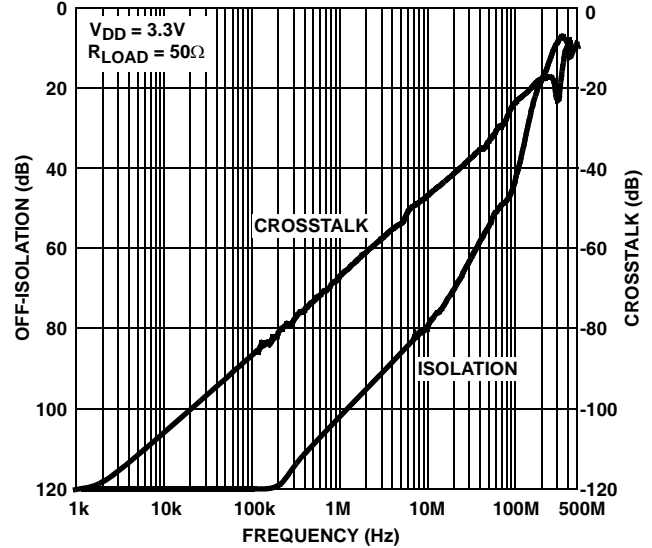


FIGURE 30. CROSSTALK AND OFF-ISOLATION

**Die Characteristics**

**SUBSTRATE POTENTIAL (POWERED UP):**

GND

**TRANSISTOR COUNT:**

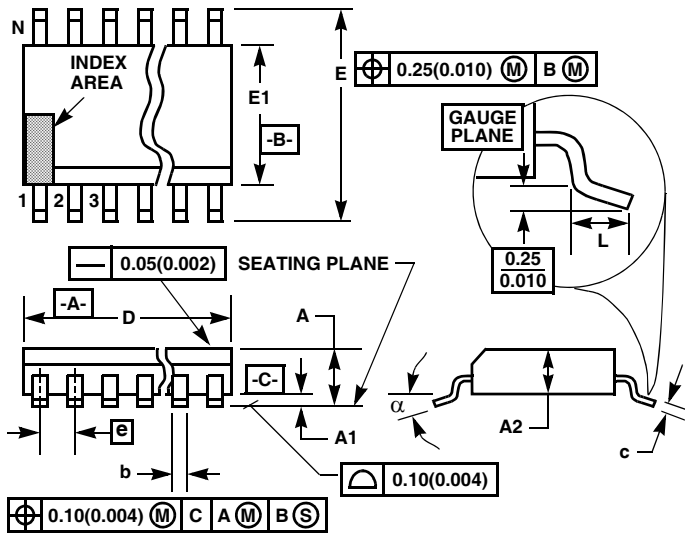
3376

**PROCESS:**

Submicron CMOS



Thin Shrink Small Outline Plastic Packages (TSSOP)



M16.173  
16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

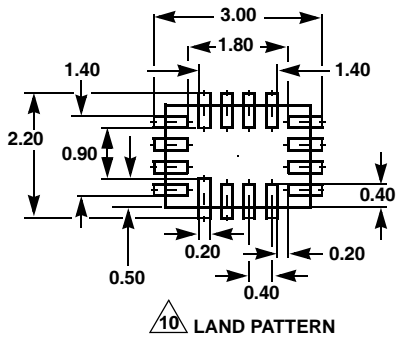
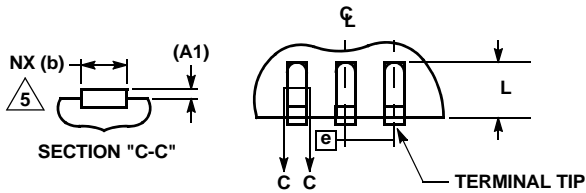
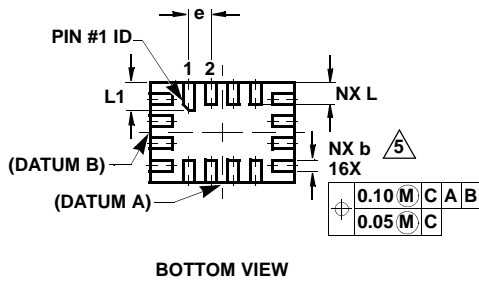
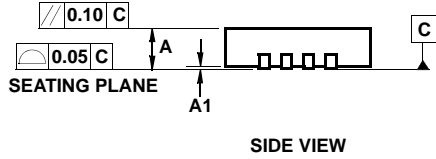
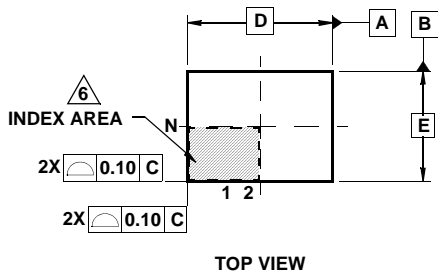
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
$\alpha$	0°	8°	0°	8°	-

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

Rev. 1 2/02

Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



L16.2.6x1.8A

16 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

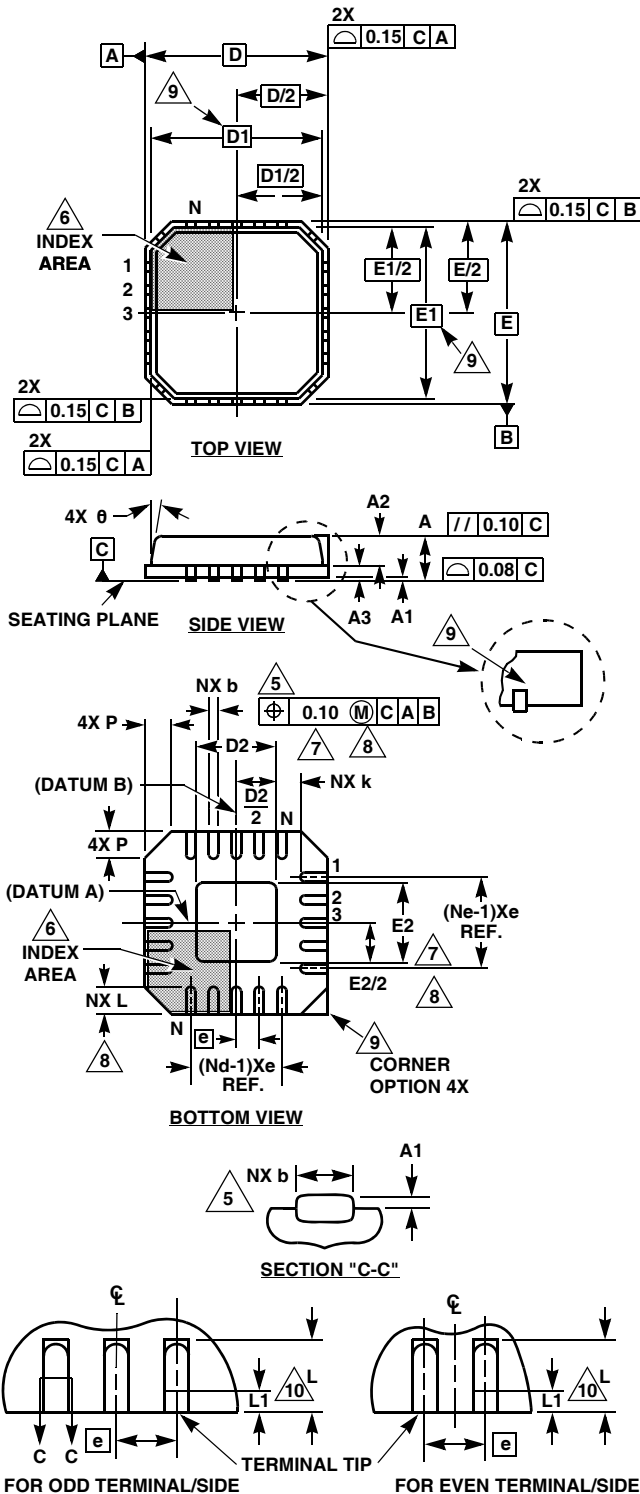
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	5
D	2.55	2.60	2.65	-
E	1.75	1.80	1.85	-
e	0.40 BSC			-
L	0.35	0.40	0.45	-
L1	0.45	0.50	0.55	-
N	16			2
Nd	4			3
Ne	4			3
θ	0	-	12	4

Rev. 4 8/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

**Thin Quad Flat No-Lead Plastic Package (TQFN)**  
**Thin Micro Lead Frame Plastic Package (TMLFP)**



**L16.3x3A**

**16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A2	-	-	0.80	9
A3	0.20 REF			9
b	0.18	0.23	0.30	5, 8
D	3.00 BSC			-
D1	2.75 BSC			9
D2	1.35	1.50	1.65	7, 8, 10
E	3.00 BSC			-
E1	2.75 BSC			9
E2	1.35	1.50	1.65	7, 8, 10
e	0.50 BSC			-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N	16			2
Nd	4			3
Ne	4			3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 0 6/04

**NOTES:**

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220WEED-2 Issue C, except for the E2 and D2 MAX dimension.

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