Data Sheet | October 18, 2007 | FN6033.5

Low-Voltage, Single Supply, Dual SPST Analog Switches

The Intersil ISL43120, ISL43121 and ISL43122 devices are precision, bidirectional, dual analog SPST switches designed to operate from a single +2.7V to +12V supply. Targeted applications include battery powered equipment that benefit from the devices' low power consumption (5µW), low leakage currents (100pA max) and fast switching speeds (t_{ON} = 28ns, t_{OFF} = 20ns). Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This family of parts may be used to "mux-in" additional functionality while reducing ASIC design risk. Some of the smallest packages are available, alleviating board space limitations, and making Intersil's newest line of low-voltage switches an ideal solution.

The ISL43120, ISL43121, ISL43122 are dual single-pole/single-throw (SPST) devices. The ISL43120 has two normally open (NO) switches; the ISL43121 has two normally closed (NC) switches; the ISL43122 has one NO and one NC switch and can be used as an SPDT.

TABLE 1. FEATURES AT A GLANCE

	ISL43120	ISL43121	ISL43122
SW 1/SW 2	NO/NO	NC/NC	NO/NC
3.3V r_{ON}	32Ω	32Ω	32Ω
3.3V t_{ON}/t_{OFF}	40ns/20ns	40ns/20ns	40ns/20ns
5V r_{ON}	19Ω	19Ω	19Ω
5V t_{ON}/t_{OFF}	28ns/20ns	28ns/20ns	28ns/20ns
12V r_{ON}	11Ω	11Ω	11Ω
12V t_{ON}/t_{OFF}	25ns/17ns	25ns/17ns	25ns/17ns
Packages	8 Ld SOT-23		

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Application Note AN557 "Recommended Test Procedures for Analog Switches"

Features

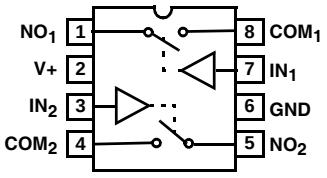
- Fully specified at 12V, 5V, and 3.3V supplies for 10% tolerances
- ON-resistance (r_{ON}) 19Ω
- r_{ON} matching between channels . . . . . <1Ω
- Low charge injection . . . . . 5pC (Max)
- Single supply operation . . . . . +2.7V to +12V
- Low power consumption (P_D) . . . . . <5µW
- Low leakage current 10nA
- Fast switching action
  - t_{ON} 28ns
  - t_{OFF} 20ns
- Guaranteed break-before-make (ISL43122 only)
- Minimum 2000V ESD protection per method 3015.7
- TTL, CMOS compatible
- Available in SOT-23 packaging
- Pb-Free Available (RoHS Compliant)

Applications

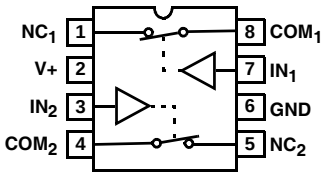
- Battery-powered, handheld and portable equipment
  - Cellular/mobile phones
  - Pagers
  - Laptops, notebooks, palmtops
- Communications systems
  - Radios, ADSL Modems
  - PBX, PABX
- Test and measurement equipment
  - Ultrasound
  - Computerized Tomography (CT) Scanner
  - Magnetic Resonance Image (MRI)
  - Position Emission Tomography (PET) Scanner
  - Electrocardiograph
- Heads-up displays
- Audio and video switching
- Various circuits
  - +3V/+5V DACs and ADCs
  - Sample and hold circuits
  - Digital filters
  - Operational amplifier gain switching networks
  - High frequency analog switching
  - High speed multiplexing
  - Integrator reset circuits

Pinouts (Note 1)

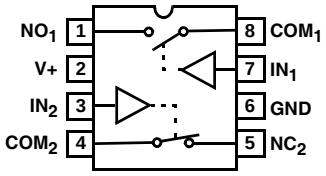
ISL43120
(8 LD SOT-23)
TOP VIEW



ISL43121
(8 LD SOT-23)
TOP VIEW



ISL43122
(8 LD SOT-23)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

IN1	IN2	ISL43120		ISL43121		ISL43122	
		NO1	NO2	NC1	NC2	NO1	NC2
0	0	OFF	OFF	ON	ON	OFF	ON
0	1	OFF	ON	ON	OFF	OFF	OFF
1	0	ON	OFF	OFF	ON	ON	ON
1	1	ON	ON	OFF	OFF	ON	OFF

NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+2.7V to +12V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (TAPE AND REEL)	PKG. DWG. #
ISL43120IH-T*	120I	-40 to +85	8 Ld SOT-23	P8.064
ISL43120IHZ-T* (Note)	120Z	-40 to +85	8 Ld SOT-23 (Pb-free)	P8.064
ISL43121IH-T*	121I	-40 to +85	8 Ld SOT-23	P8.064
ISL43121IHZ-T* (Note)	121Z	-40 to +85	8 Ld SOT-23 (Pb-free)	P8.064
ISL43122IH-T*	122I	-40 to +85	8 Ld SOT-23	P8.064
ISL43122IHZ-T* (Note)	122Z	-40 to +85	8 Ld SOT-23 (Pb-free)	P8.064

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

V+ to GND . . . . . -0.3V to 15V
Input Voltages
IN (Note 2). . . . . -0.3V to ((V+) + 0.3V)
NO, NC (Note 2) . . . . . -0.3V to ((V+) + 0.3V)
Output Voltages
COM (Note 2) . . . . . -0.3V to ((V+) + 0.3V)
Continuous Current (Any Terminal) 30mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) 40mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015) . . . . .>2kV

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
8 Ld SOT-23 Package 215
Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range
ISL43XXXIH-T . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V (See Figure 5)	25	-	19	30	Ω
		Full	-	23	40	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V	25	-	0.8	2	Ω
		Full	-	1	4	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V	Full	-	7	8	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V	25	-0.1	0.01	0.1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, 1V, V_{NO} or V_{NC} = 1V, 4.5V	25	-0.1	-	0.1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, or V_{NO} or V_{NC} = 1V, 4.5V, or Floating	25	-0.2	-	0.2	nA
		Full	-10	-	10	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 3V, R_L =1kΩ, C_L = 35pF, V_{IN} = 0V to 3V (See Figure 1, Note 7)	25	-	28	75	ns
		Full	-	40	150	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 3V, R_L =1kΩ, C_L = 35pF, V_{IN} = 0V to 3V (See Figure 1, Note 7)	25	-	20	50	ns
		Full	-	30	100	ns
Break-Before-Make Time Delay (ISL43122 only), t_D	R_L = 300Ω, C_L = 35pF, V_{NO} = V_{NC} = 3V, V_{IN} = 0V to 3V (See Figure 3, Note 7)	Full	3	10	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2, Note 7)	25	-	3	5	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz (See Figure 4)	25	-	76	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz (See Figure 6)	25	-	-105	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	60	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	8	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	8	-	pF

Electrical Specifications - 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	21	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	2.7	-	12	V
Positive Supply Current, I+	V+ = 5.5V, V_{IN} = 0V or V+, all channels on or off	Full	-1	0.0001	1	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Voltage High, V_{INH}		Full	2.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{IN} = 0V or V+	Full	-1	-	1	µA

Electrical Specifications - 3.3V Supply

Test Conditions: V+ = +3.0V to +3.6V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V	25	-	32	50	Ω
		Full	-	40	60	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 3.3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V	25	-	0.8	2	Ω
		Full	-	1	4	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 3.3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 0.5V, 1V, 1.5V	25	-	6	8	Ω
		Full	-	7	12	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.6V, V_{COM} = 1V, 3V, V_{NO} or V_{NC} = 3V, 1V	25	-0.1	0.01	0.1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 3V, 1V, V_{NO} or V_{NC} = 1V, 3V	25	-0.1	0.01	0.1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.6V, V_{COM} = 1V, 3V, or V_{NO} or V_{NC} = 1V, 3V, or floating	25	-0.2	-	0.2	nA
		Full	-10	-	10	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 1.5V, R_L = 1kΩ, C_L = 35pF, V_{IN} = 0V to 3V (Note 7)	25	-	40	120	ns
		Full	-	60	200	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 1.5V, R_L = 1kΩ, C_L = 35pF, V_{IN} = 0V to 3V (Note 7)	25	-	20	50	ns
		Full	-	30	120	ns
Break-Before-Make Time Delay (ISL43122 only), t_D	R_L = 300Ω, C_L = 35pF, V_{NO} or V_{NC} = 1.5V, V_{IN} = 0V to 3V (Note 7)	Full	3	20	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (Note 7)	25	-	1	5	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	76	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	-105	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	56	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V	25	-	8	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V	25	-	8	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	21	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V_{IN} = 0V or V+, all channels on or off	Full	-1	-	1	µA

Electrical Specifications - 3.3V Supply

Test Conditions: V+ = +3.0V to +3.6V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Voltage High, V_{INH}		Full	2.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+	Full	-1	-	1	µA

Electrical Specifications - 12V Supply

Test Conditions: V+ = +10.8V to +13V, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 10V	25	-	11	20	Ω
		Full	-	15	25	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 12V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 10V	25	-	0.8	2	Ω
		Full	-	1	4	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 12V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V, 6V, 9V	25	-	1	4	Ω
		Full	-	-	6	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 13V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 12V, 1V	25	-0.1	0.01	0.1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 13V, V_{COM} = 12V, 1V, V_{NO} or V_{NC} = 1V, 12V	25	-0.1	0.01	0.1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 13V, V_{COM} = 1V, 12V, or V_{NO} or V_{NC} = 1V, 12V, or floating	25	-0.2	-	0.2	nA
		Full	-10	-	10	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{NO} or V_{NC} = 10V, R_L = 1kΩ, C_L = 35pF, V_{IN} = 0V to 4V (Note 7)	25	-	25	35	ns
		Full	-	35	55	ns
Turn-OFF Time, t_{OFF}	V_{NO} or V_{NC} = 10V, R_L = 1kΩ, C_L = 35pF, V_{IN} = 0V to 4V (Note 7)	25	-	17	30	ns
		Full	-	26	50	ns
Break-Before-Make Time Delay (ISL43122 only), t_D	R_L = 300Ω, C_L = 35pF, V_{NO} or V_{NC} = 10V, V_{IN} = 0 to 4V	Full	0	2		ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (Note 7)	25	-	5	15	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	76	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	-105	-	dB
Power Supply Rejection Ratio	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	63	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V	25	-	8	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V	25	-	8	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	21	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13V, V_{IN} = 0V or V+, all channels on or off	Full	-1	-	1	µA

Electrical Specifications - 12V Supply

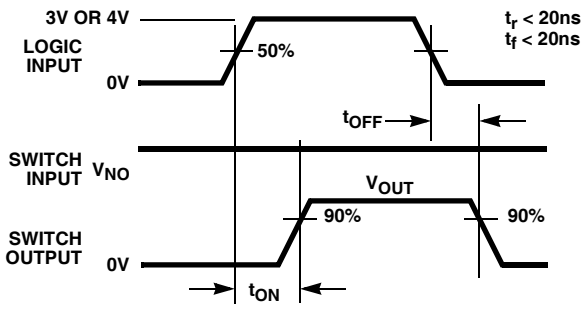
Test Conditions: V+ = +10.8V to +13V, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.8	V
Input Voltage High, V_{INH}		Full	4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 13V, V_{IN} = 0V or V+	Full	-1	-	1	µA

NOTES:

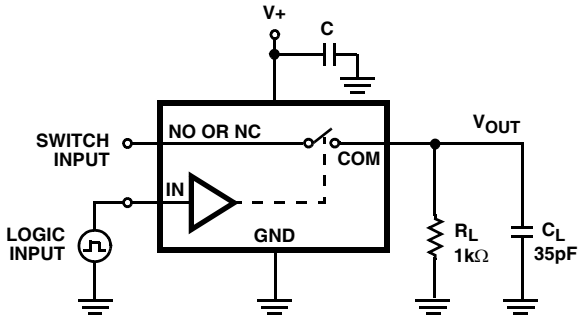
4. V_{IN} = input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Parts are 100% tested at +25°C Over-temperature limits established by characterization and are not production tested.
7. Limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

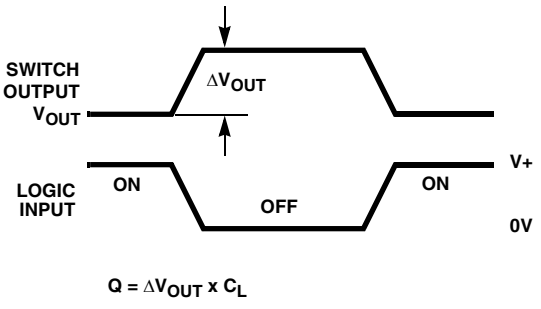


Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



$Q = \Delta V_{OUT} \times C_L$

FIGURE 2A. MEASUREMENT POINTS

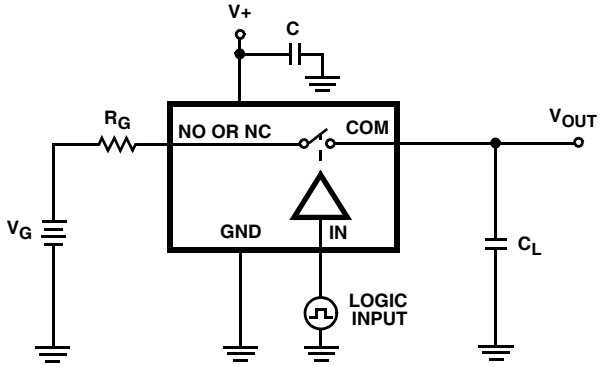


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

Test Circuits and Waveforms (Continued)

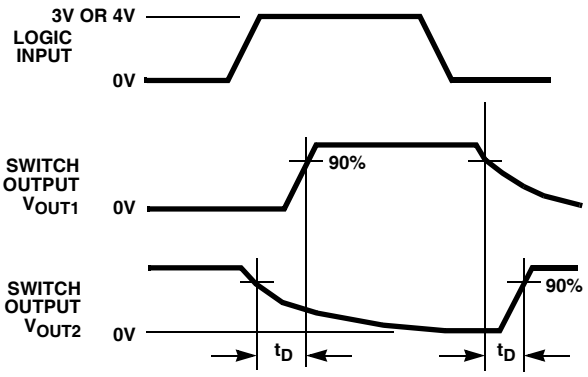
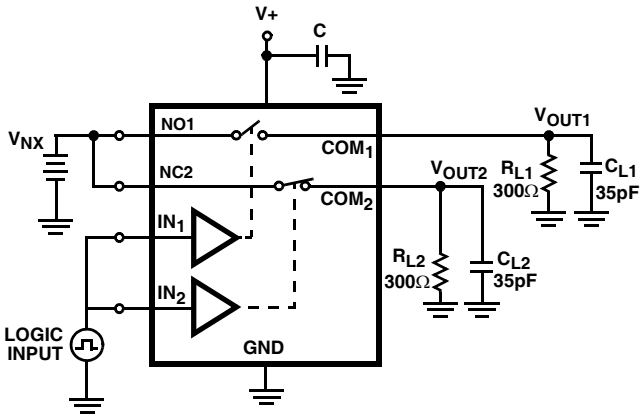


FIGURE 3A. MEASUREMENT POINTS (ISL43122 ONLY)



C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT (ISL43122 ONLY)

FIGURE 3.

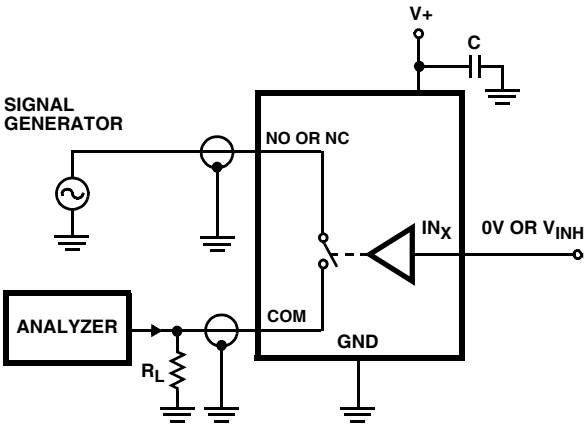


FIGURE 4. OFF ISOLATION TEST CIRCUIT

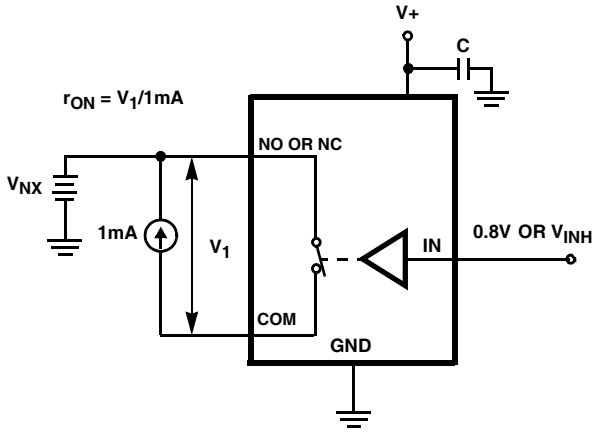


FIGURE 5. r_{ON} TEST CIRCUIT

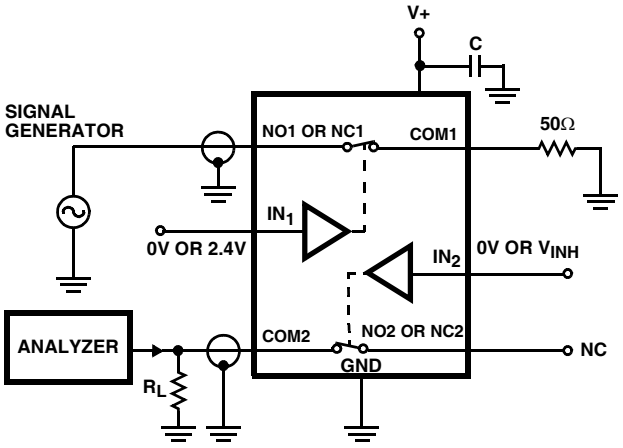


FIGURE 6. CROSSTALK TEST CIRCUIT

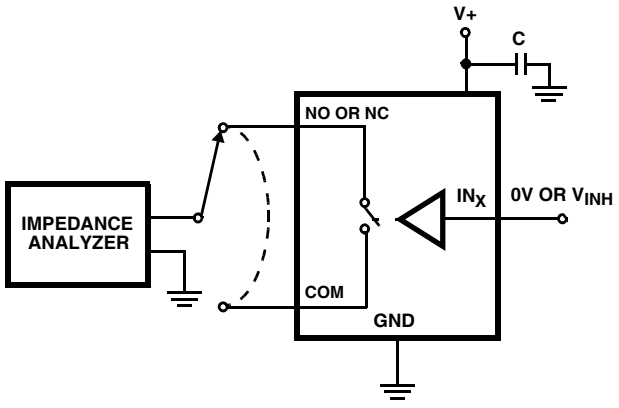


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43120, ISL43121, ISL43122 bidirectional dual SPST analog switches offer precise switching capability from a single 2.7V to 12V supply with low ON-resistance (19Ω) and high speed operation (t_{ON} = 28ns, t_{OFF} = 20ns). The devices are especially well suited to portable battery-powered equipment thanks to the low operating supply voltage (2.7V), low power consumption (5µW), low leakage currents (100pA max), and the tiny SOT-23 packaging. High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents, which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

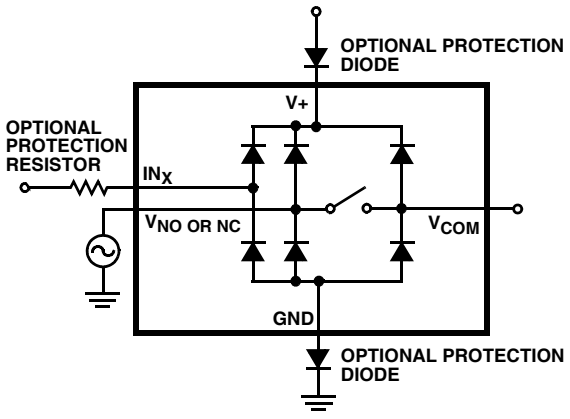


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL43120, ISL43121, ISL43122 construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 13V maximum supply voltage, the ISL43120, ISL43121, ISL43122 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 2.7V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the “Electrical Specifications” tables starting on page 3 and “Typical Performance Curves” (starting on page 9) for details.

V+ and GND also power the internal logic and level shifter. The level shifter convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is TTL compatible (0.8V and 2.4V) over a supply range of 3V to 11V (see Figure 15). At 12V the V_{IH} level is about 2.5V. This is still below the TTL guaranteed high output minimum level of 2.8V, but noise margin is reduced. For best results with a 12V supply, use a logic family the provides a V_{OH} greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 300MHz (see Figure 16). Figure 16 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch’s input to its output. Off isolation is the resistance to this feedthrough, while crosstalk indicates the amount of feedthrough from one switch to another. Figure 17 details the high off isolation and crosstalk rejection provided by this family. At 10MHz, off isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off isolation and crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

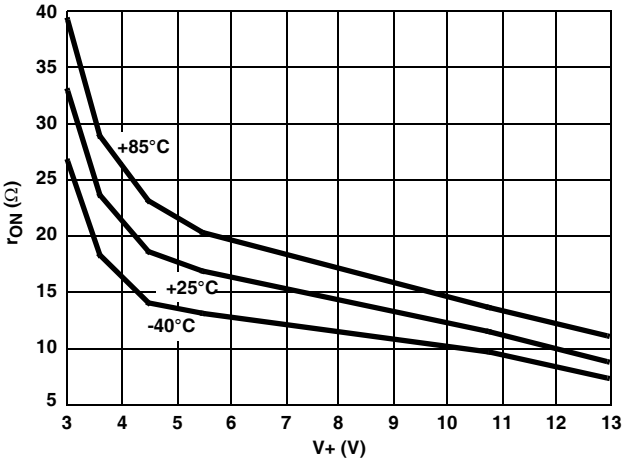


FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE

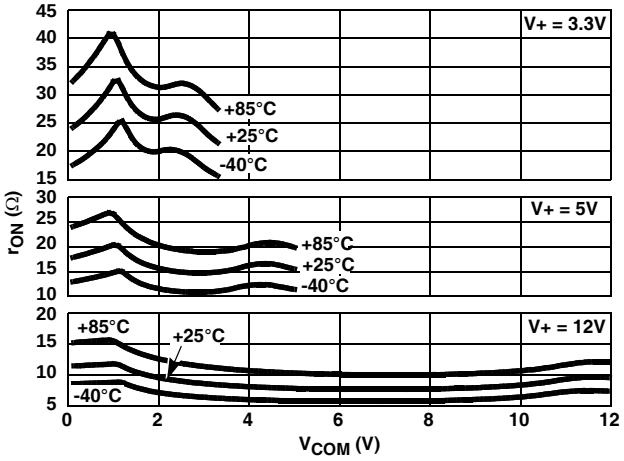


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

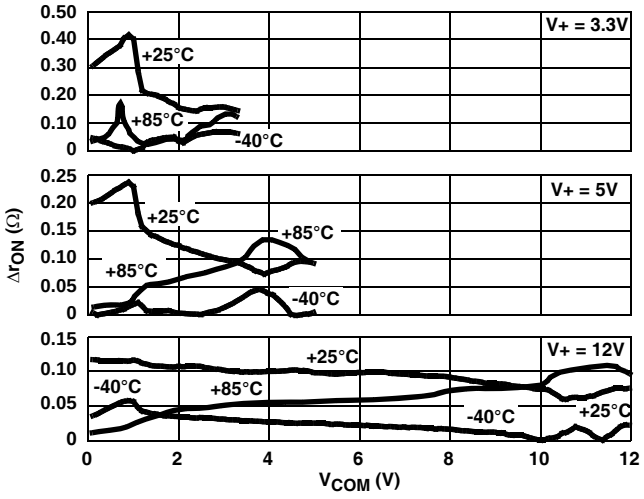


FIGURE 11. r_{ON} MATCH vs SWITCH VOLTAGE

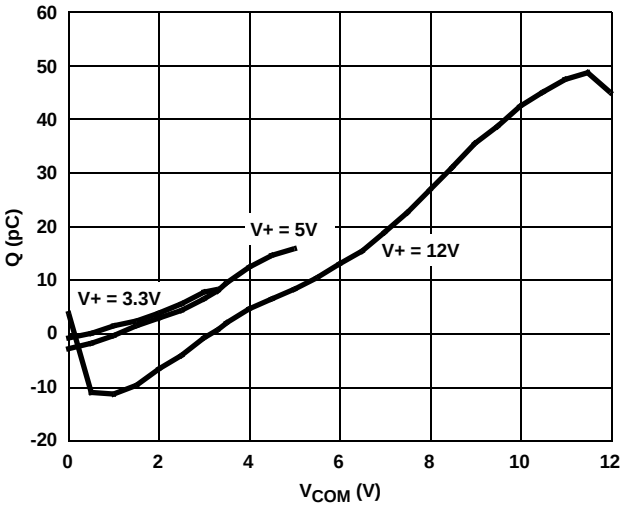


FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

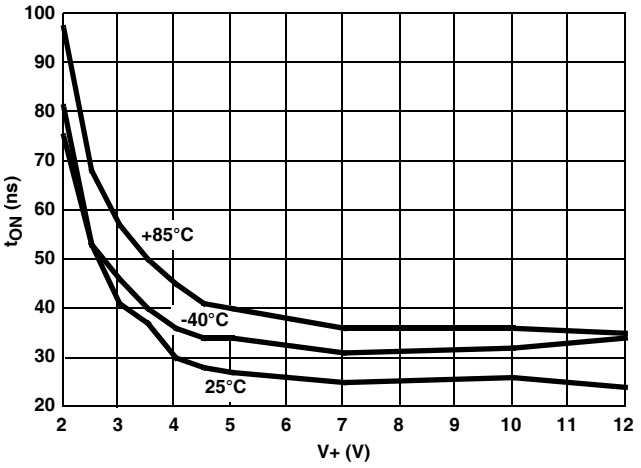


FIGURE 13. TURN-ON TIME vs SUPPLY VOLTAGE

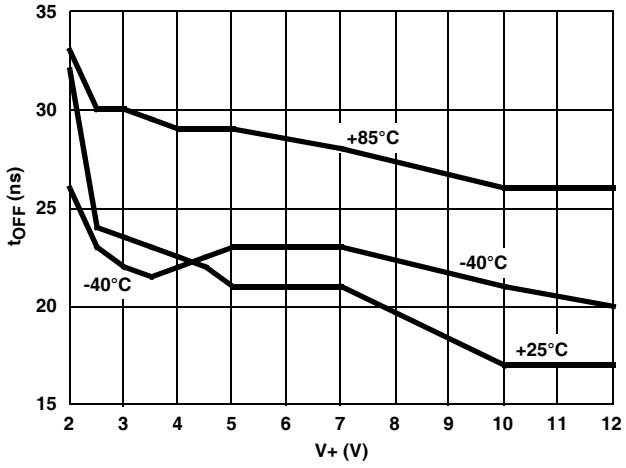


FIGURE 14. TURN-OFF TIME vs SUPPLY VOLTAGE

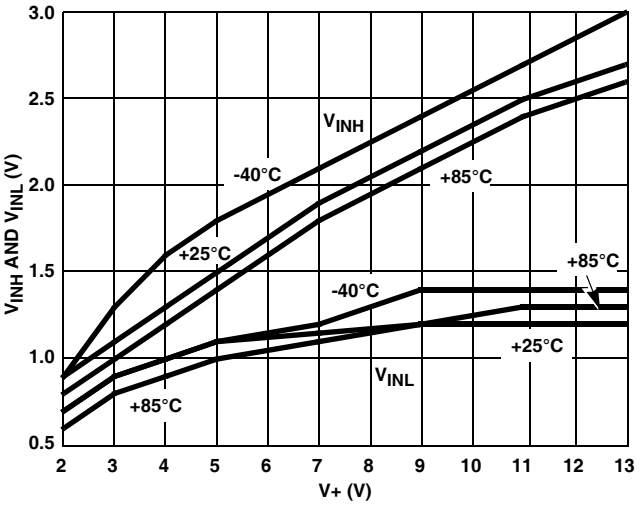


FIGURE 15. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

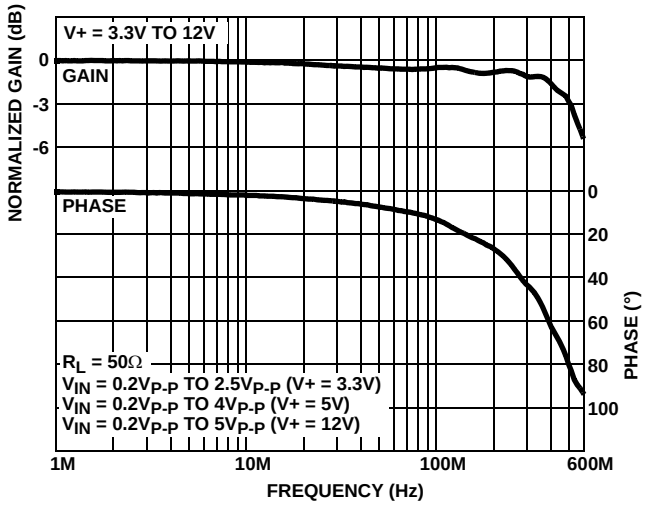


FIGURE 16. FREQUENCY RESPONSE

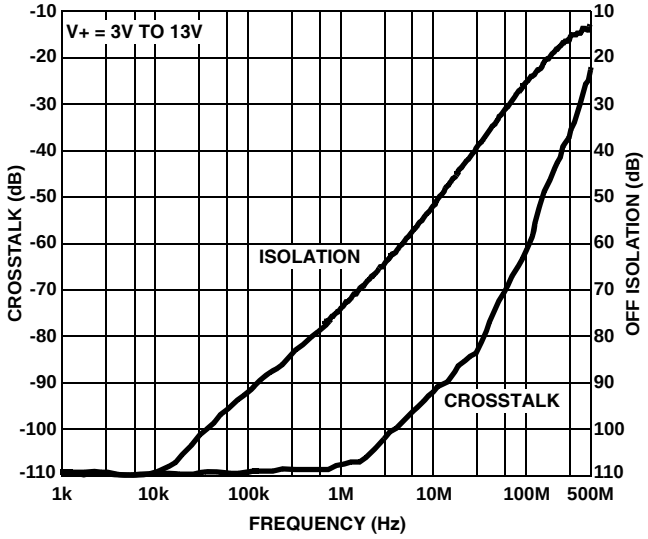


FIGURE 17. CROSSTALK AND OFF ISOLATION

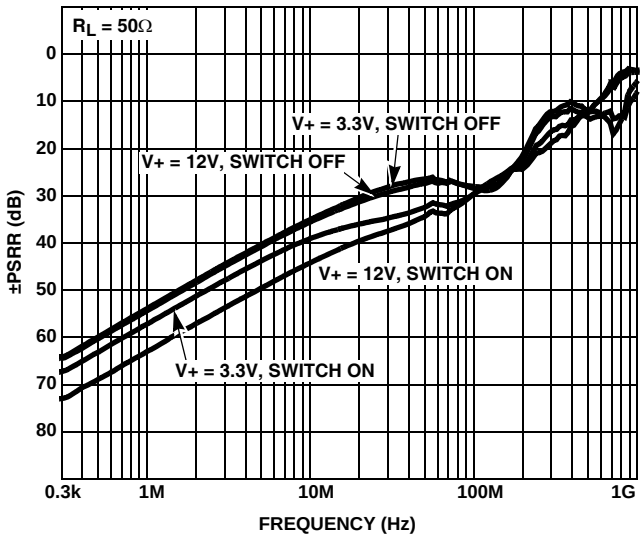


FIGURE 18. ±PSRR vs FREQUENCY

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

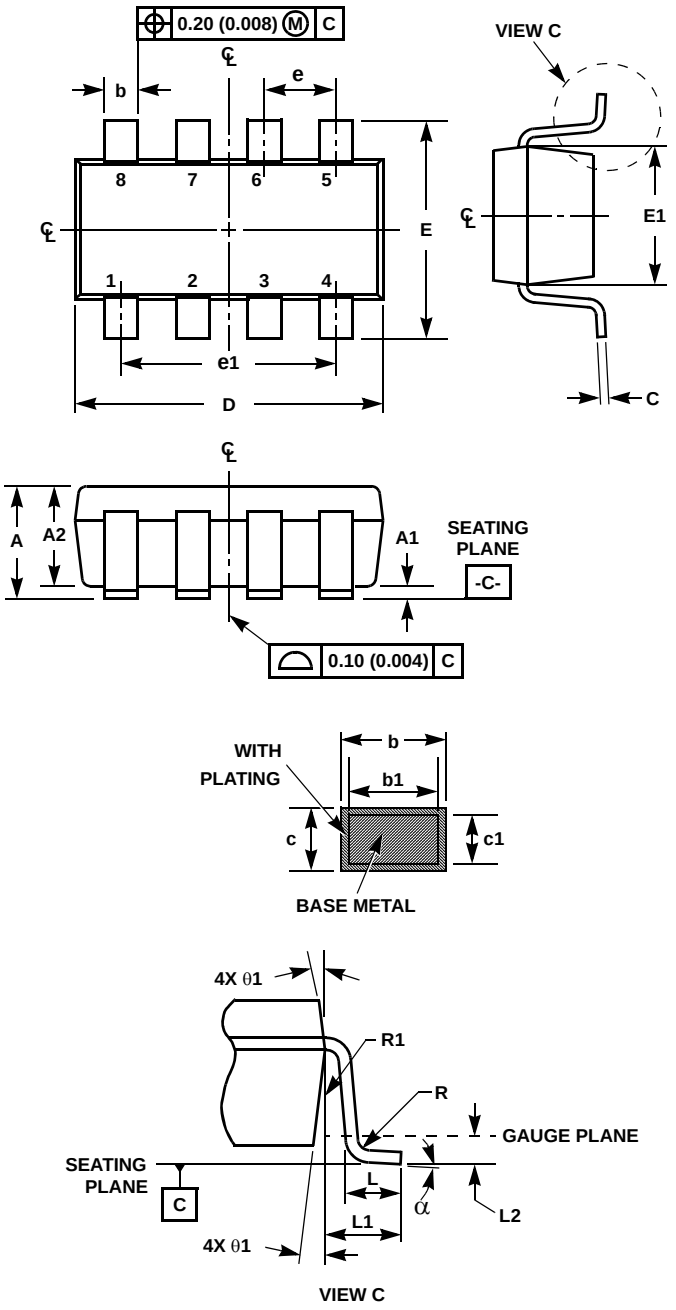
TRANSISTOR COUNT:

ISL43120: 66
ISL43121: 66
ISL43122: 66

PROCESS:

Si Gate CMOS

Small Outline Transistor Plastic Packages (SOT23-8)



P8.064

8 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.036	0.057	0.90	1.45	-
A1	0.000	0.0059	0.00	0.15	-
A2	0.036	0.051	0.90	1.30	-
b	0.009	0.015	0.22	0.38	-
b1	0.009	0.013	0.22	0.33	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.008	0.08	0.20	6
D	0.111	0.118	2.80	3.00	3
E	0.103	0.118	2.60	3.00	-
E1	0.060	0.067	1.50	1.70	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0768 Ref		1.95 Ref		-
L	0.014	0.022	0.35	0.55	4
L1	0.024 Ref.		0.60 Ref.		
L2	0.010 Ref.		0.25 Ref.		
N	8		8		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.10	0.25	
α	0^o	8^o	0^o	8^o	-

Rev. 2 9/03

NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178BA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only