

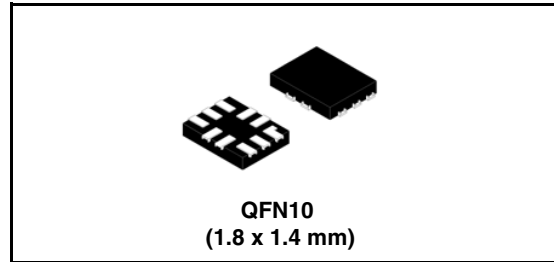
Low voltage high bandwidth dual SPDT switch

Features

- Ultra low power dissipation:
 - $I_{CC} = 1 \mu\text{A}$ (max.) at $T_A = 85 \text{ }^\circ\text{C}$
- Low "ON" resistance:
 - $R_{ON} = 4.8 \Omega$ ($T_A = 25 \text{ }^\circ\text{C}$) at $V_{CC} = 4.3 \text{ V}$
 - $R_{ON} = 5.9 \Omega$ ($T_A = 25 \text{ }^\circ\text{C}$) at $V_{CC} = 3.0 \text{ V}$
- Wide operating voltage range:
 - $V_{CC} \text{ (opr)} = 1.65 \text{ V to } 4.3 \text{ V}$
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at $V_{CC} = 2.3 \text{ V to } 3.0 \text{ V}$
- Typical bandwidth (-3 dB) at 800 MHz on all channels
- USB (2.0) high speed (480 Mbps) signal switching compliant
- Integrated fail safe function
- Interrupt function to indicate to the processor that the device is in dedicated port charging mode
- Latch-up performance exceeds 500 mA per JESD 78, Class II
- ESD performance exceeds JESD22:
 - Dn pins: 4000-V human body model (A114-A)
 - All other pins: 2000-V human body model (A114-A)

Applications

- Mobile phones



Description

The STG3220 is a high-speed CMOS low voltage dual analog SPDT (single pole dual throw) switch or 2:1 multiplexer/de-multiplexer switch fabricated in silicon gate C^2 MOS technology. It is designed to operate from 1.65 V to 4.3 V, making this device ideal for portable applications.

The SEL input is provided to control the switch. The switch nS1 is ON (connected to common ports Dn) when the SEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch nS2 is ON (it is connected to common port Dn) when the SEL input is held low and OFF (high impedance state exists between the two ports) when SEL is held high. STG3220 has an integrated fail safe function to withstand over-voltage condition when the device is powered off.

The STG3220 also has an interrupt pin which sends a signal to the processor when the device is in dedicated port charging mode. Additional key features are fast switching speed, break-before-make-delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

Order code	Package	Packaging
STG3220QTR	QFN10 (1.8 x 1.4 mm)	Tape and reel

Contents

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1 Pin settings

Figure 1. Pin connection (top through view)

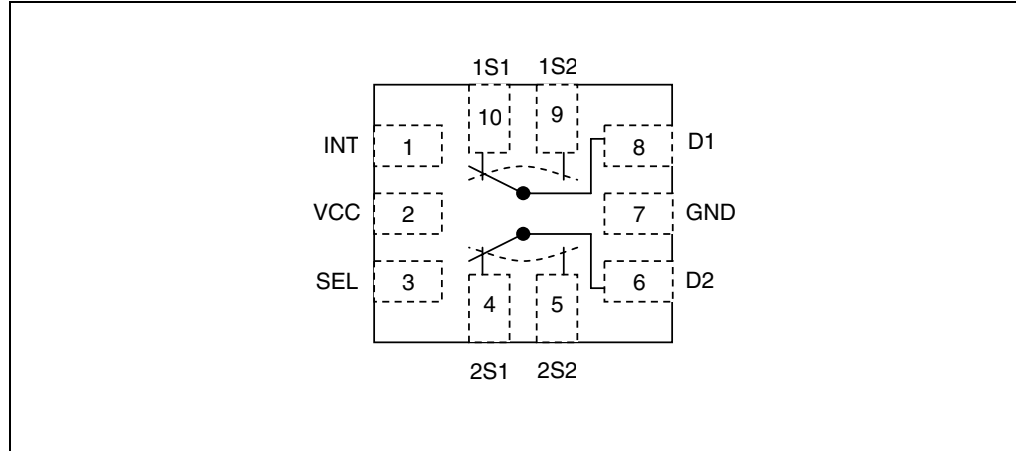


Table 2. Pin description

Pin number	Symbol	Name and function
1	INT	Interrupt
2	VCC	Positive supply voltage
3	SEL	Control
4	2S1	Independent channel for switch 2
5	2S2	Independent channel for switch 2
6	D2	Common channel for switch 2
7	GND	Ground (0 V)
8	D1	Common channel for switch 1
9	1S2	Independent channel for switch 1
10	1S1	Independent channel for switch 1

2 Logic diagram

Figure 2. Logic block diagram

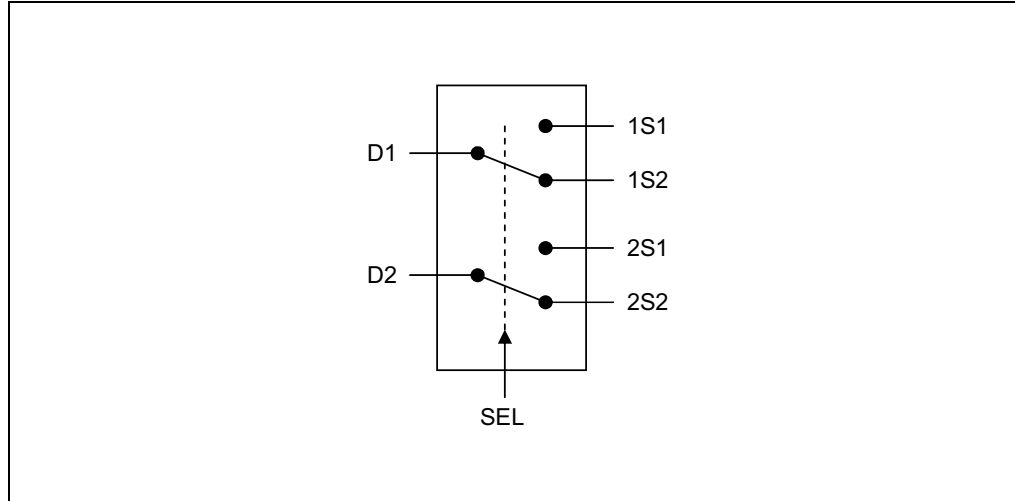


Figure 3. Logic equivalent circuit

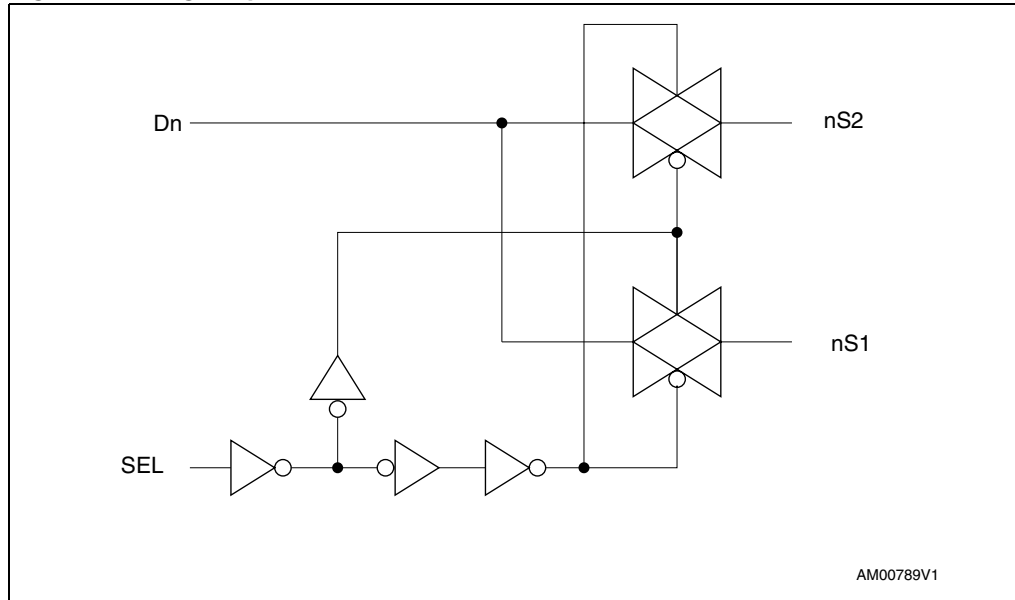


Table 3. Truth table

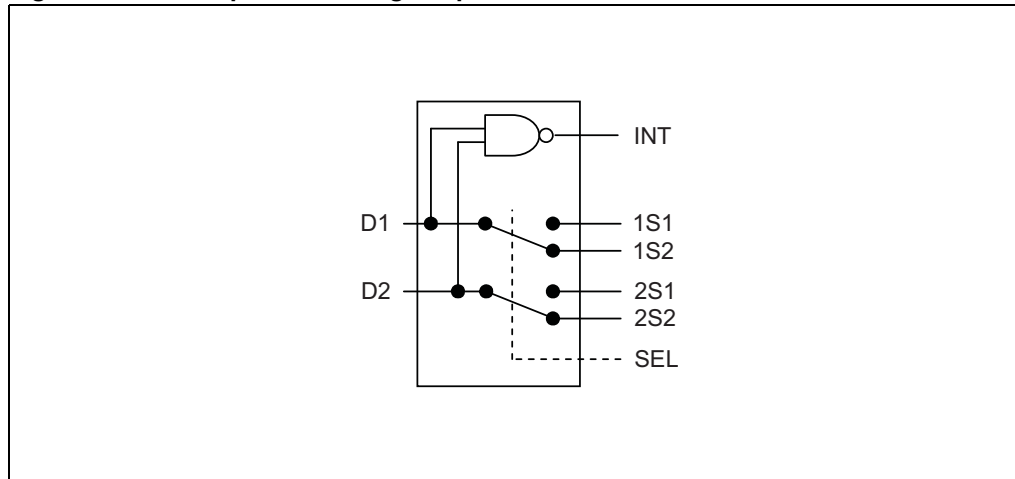
SEL	Switch nS1	Switch nS2
H	ON	OFF ⁽¹⁾
L	OFF ⁽¹⁾	ON

1. High impedance.

3 Dedicated port charging detection

The STG3220 has a built-in dedicated port charging detection circuit to detect the condition when the USB D+/D- lines are both in high state. When this occurs, the device sends an interrupt signal to the processor to indicate that the connected USB device is in dedicated port charging mode.

Figure 4. Interrupt function logic representation



4 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IKC}	DC input diode current on control pin ($V_{SEL} < 0V$)	-50	mA
I_{IK}	DC input diode current ($V_{SEL} < 0V$)	± 50	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 128	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	± 300	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 100	mA
P_D	Power dissipation at $T_A = 70\text{ °C}$ ⁽¹⁾	1120	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

1. Derate above 70 °C by 18.5 mW/°C.

4.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.65 to 4.3	V
V_I	Input voltage	0 to V_{CC}	V
V_{IC}	Control input voltage	0 to 4.3	V
V_O	Output voltage	0 to V_{CC}	V
T_{op}	Operating temperature	-40 to 85	°C
dt/dv	Input rise and fall time control input	$V_L = 1.65\text{ V to }2.7\text{ V}$	0 to 20
		$V_L = 3.0\text{ to }4.3\text{ V}$	0 to 10

5 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V _{CC} (V)	Test conditions	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
V _{IH}	High level input voltage	1.65 – 1.95	–	0.65 V _{CC}	–	–	0.65V _{CC}	–	V
		2.3 – 2.5		1.2	–	–	1.2	–	
		2.7 – 3.0		1.3	–	–	1.3	–	
		3.3 – 3.6		1.4	–	–	1.4	–	
		4.3		1.6	–	–	1.6	–	
V _{IL}	Low level input voltage	1.65 – 1.95	–	–	–	0.25	–	0.25	V
		2.3 – 2.5		–	–	0.25	–	0.25	
		2.7 – 3.0		–	–	0.25	–	0.25	
		3.3 – 3.6		–	–	0.30	–	0.30	
		4.3		–	–	0.40	–	0.40	
V _{IH-INT}	High level input voltage for INT	4.3	–	2.4	–	–	2.4	–	V
V _{IL-INT}	Low level input voltage for INT	4.3	–	–	–	0.9	–	0.9	V
V _{OL-INT}	Low level output voltage for INT	4.3	I _O = 4 mA	–	–	0.40	–	0.50	V
R _{PEAK}	Switch ON peak resistance	1.8	V _S = 0 V to V _{CC} I _S = 8 mA	–	15.1	17.8	–	–	Ω
		2.7		–	6.4	8.0	–	–	
		3.0		–	5.9	7.5	–	–	
		3.7		–	5.0	6.5	–	–	
		4.3		–	4.8	6.1	–	–	
R _{ON}	Switch ON resistance	3.0	V _S = 3 V I _S = 8 mA	–	4.2	5.4	–	–	Ω
		3.0	V _S = 0.4 V I _S = 8 mA	–	5.7	7.0	–	–	

Table 6. DC specifications (continued)

Symbol	Parameter	V _{CC} (V)	Test conditions	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
ΔR _{ON}	ON resistance match between channels ⁽¹⁾	1.8	V _S at R _{ON} max I _S = 8 mA	–	–	–	–	–	Ω
		2.7		–	–	–	–		
		3.0		–	0.1	–	–		
		3.7		–	–	–	–		
		4.3		–	–	–	–		
R _{FLAT}	ON resistance flatness ⁽²⁾	1.8	V _S = 0 V to 0.4 V I _S = 8 mA	–	4.5	–	–	–	Ω
		1.8	V _S = 0 V to V _{CC} I _S = 8 mA	–	9.0	–	–	–	
		2.7		–	2.2	–	–	–	
		3.0		–	1.8	–	–	–	
		3.7		–	1.6	–	–	–	
		4.3		–	1.6	–	–	–	
I _{OFF}	OFF state leakage current (Sn), (D)	4.3	V _S = 0.3 or 4 V	-20	–	20	-100	100	nA
I _{IN}	Input leakage current	0 to 4.3	V _{SEL} = 0 to 4.3 V	-0.2	–	0.2	-1.0	1.0	μA
I _{CC}	Quiescent supply current	1.65 to 4.3	V _{SEL} = V _{CC} or GND	-0.2	–	0.2	-1.0	1.0	μA
I _{CCLV}	Quiescent supply current for low voltage driving	4.3	V _{SEL} = 1.65 V	–	±37	±50	–	±100	μA
			V _{SEL} = 1.80 V	–	±33	±40	–	±50	
			V _{SEL} = 2.60 V	–	±11	±20	–	±30	

1. ΔR_{ON} = max I_{mSN}-nSNI, where m = 1, 2 and n = 1, 2, N = 1, 2

2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC characteristics ($C_L = 35 \text{ pf}$, $R_L = 50 \Omega$, $T_R = T_f \leq 5 \text{ ns}$)

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				$T_A = 25 \text{ }^\circ\text{C}$			$-40 \text{ to } 85 \text{ }^\circ\text{C}$		
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation delay	1.65 - 1.95	-	-	0.21	-	-	-	ns
		2.3 - 2.7		-	0.15	-	-	-	
		3.0 - 3.3		-	0.14	-	-	-	
		3.6 - 4.3		-	0.13	-	-	-	
t_{ON}	Turn on time	1.65 - 1.95	$V_S = 0.8 \text{ V}$	-	34	-	-	-	ns
		2.3 - 2.7	$V_S = 1.5 \text{ V}$	-	20	23	-	26	
		3.0 - 3.3		-	15	17	-	20	
		3.6 - 4.3		-	13	15	-	17	
t_{OFF}	Turn off time	1.65 - 1.95	$V_S = 0.8 \text{ V}$	-	27	-	-	-	ns
		2.3 - 2.7	$V_S = 1.5 \text{ V}$	-	19	22	-	25	
		3.0 - 3.3		-	14	16	-	18	
		3.6 - 4.3		-	11	13	-	14	
t_D	Break-before-make time delay	1.65 - 1.95	$C_L = 35 \text{ pF}$ $R_L = 50 \Omega$ $V_S = 1.5 \text{ V}$	-	10	-	-	-	ns
		2.3 - 2.7		-	6	-	-	-	
		3.0 - 3.3		-	4	-	-	-	
		3.6 - 4.3		-	3	-	-	-	

Table 8. AC electrical characteristics ($C_L = 5 \text{ pF}$, $R_L = 50 \text{ } \Omega$, $T_A = 25 \text{ } ^\circ\text{C}$)

Symbol	Parameter	V_{CC} (V)	Test conditions	Value					Unit
				$T_A = 25 \text{ } ^\circ\text{C}$			$-40 \text{ to } 85 \text{ } ^\circ\text{C}$		
				Min	Typ	Max	Min	Max	
Q	Charge injection	1.65	$C_L = 100 \text{ pF}$ $V_{GEN} = 0 \text{ V}$ $R_{GEN} = 0 \text{ } \Omega$	-	3.9	-	-	-	pC
		2.3		-	4.8	-	-	-	
		3.0		-	5.2	-	-	-	
		4.3		-	6.4	-	-	-	
OIRR	OFF isolation ⁽¹⁾	1.65 – 4.3	$V_S = 1 \text{ V}_{RMS}$, $f = 1 \text{ MHz}$ Signal = 0 dBm	-	-78	-	-	-	dB
				$V_S = 1 \text{ V}_{RMS}$, $f = 10 \text{ MHz}$ Signal = 0 dBm	-	-57	-	-	
Xtalk	Crosstalk	1.65 – 4.3	$V_S = 1 \text{ V}_{RMS}$, $f = 1 \text{ MHz}$ Signal = 0 dBm	-	-78	-	-	-	dB
				$V_S = 1 \text{ V}_{RMS}$, $f = 10 \text{ MHz}$ Signal = 0 dBm	-	-58	-	-	
BW	-3dB bandwidth	3.0 – 4.3	$R_L = 50 \text{ } \Omega$ Signal = 0 dBm	-	800	-	-	-	MHz
C_{IN}	Control pin input capacitance		$V_{CC} = 0 \text{ V}$	-	2	-	-	-	pF
C_{ON}	Sn port capacitance when switch is enabled	3.3	$f = 240 \text{ MHz}$	-	6	-	-	-	
C_{OFF}	Sn port capacitance when switch is disabled	3.3	$f = 240 \text{ MHz}$	-	2	-	-	-	

1. Off isolation = $20 \text{ Log}_{10}(V_D/V_S)$, V_D = output, V_S = input to off switch.

Table 9. USB related AC electrical characteristics

Symbol	Parameter	V _{CC} (V)	Test conditions	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
t _{SK(0)}	Channel-to-channel skew	3.0 - 3.6	C _L = 10 pF	–	26	–	–	–	ps
t _{SK(P)}	Skew of opposite transition of the same output	3.0 - 3.6	C _L = 10 pF	–	60	–	–	–	ps
T _J	Total jitter	3.0 - 3.6	R _L = 50 Ω C _L = 10 pF t _R = t _F = 750 ps at 480 Mbps	–	130	–	–	–	ps

6 Test circuit

Figure 5. ON resistance

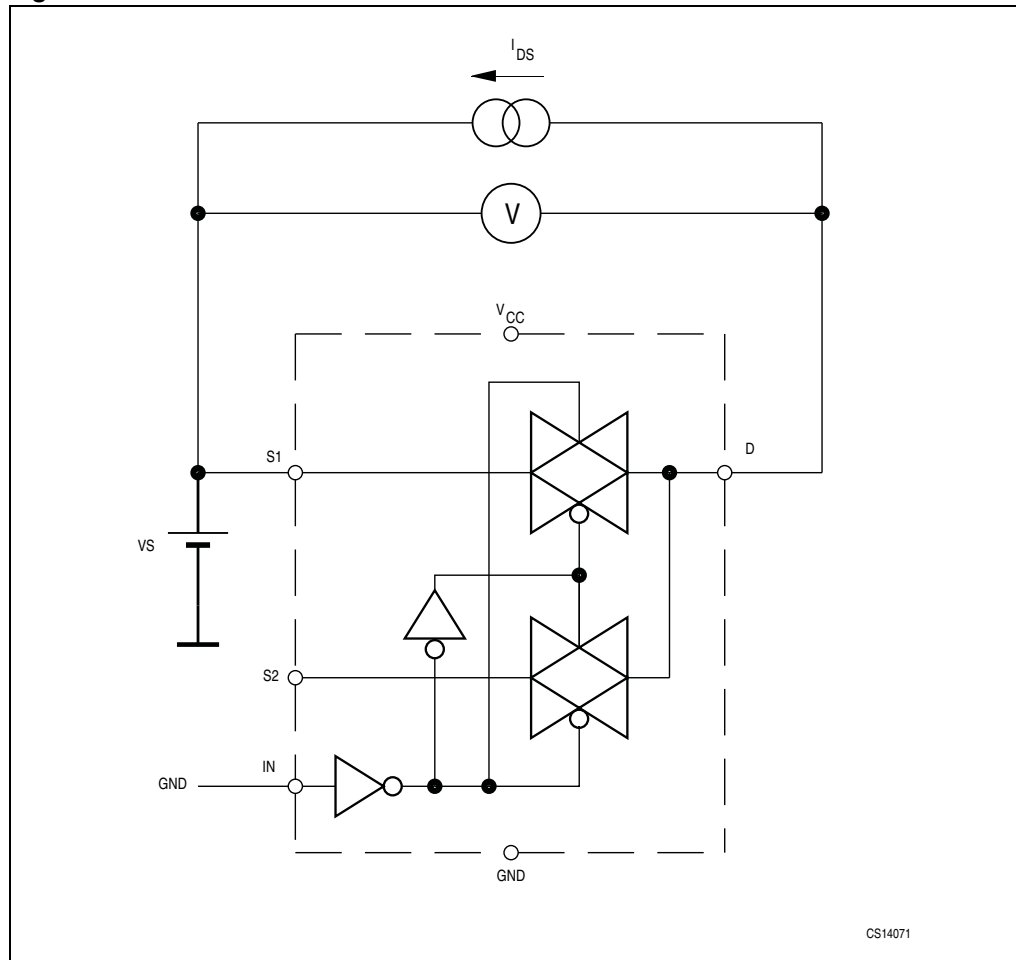


Figure 6. OFF leakage

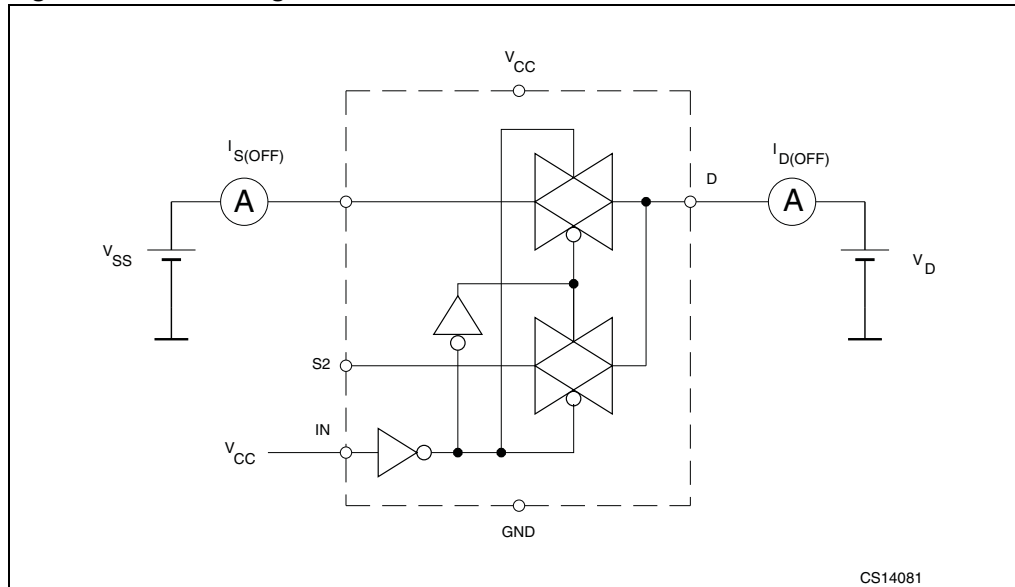


Figure 7. OFF isolation

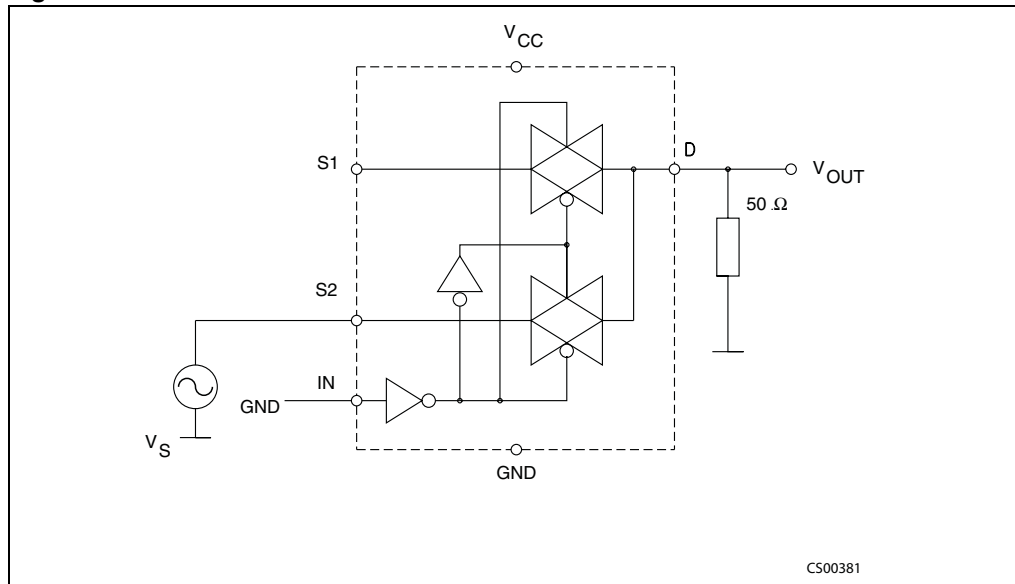


Figure 8. Bandwidth

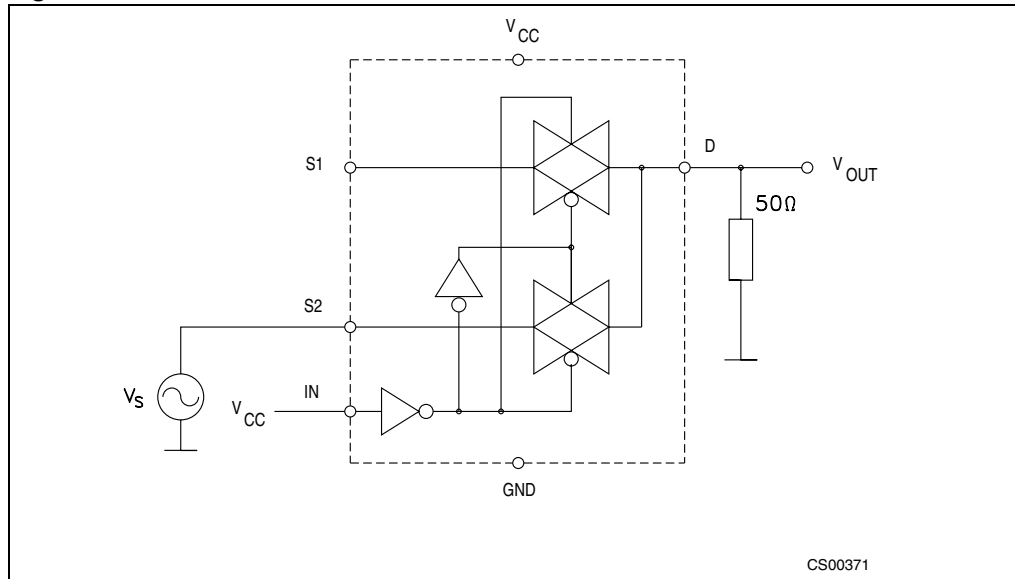


Figure 9. Channel-to-channel crosstalk

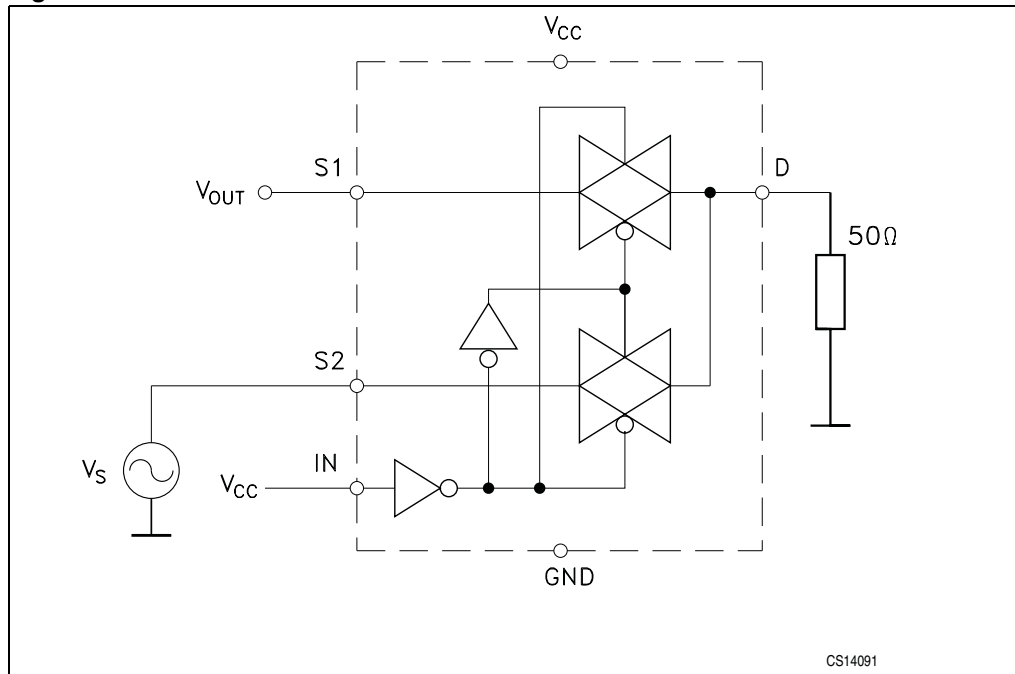
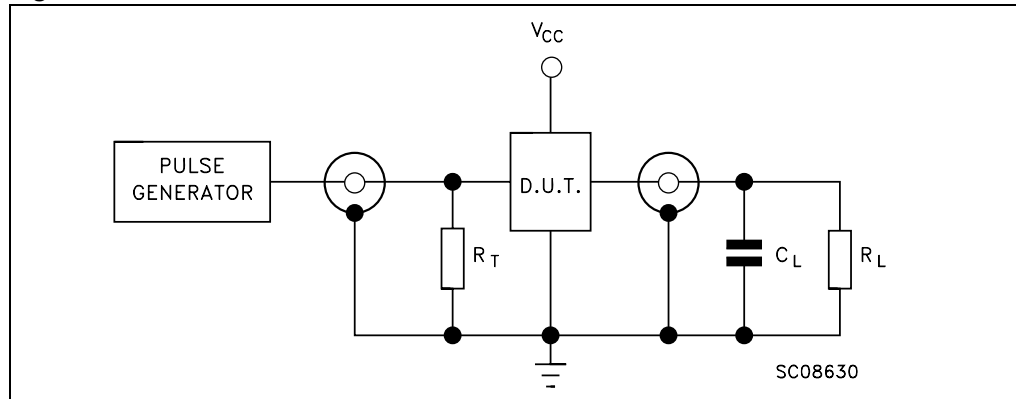


Figure 10. Test circuit



1. $C_L = 5/35$ pF or equivalent (includes jig and probe capacitance)
2. $R_L = 50 \Omega$ or equivalent
3. $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 11. Break-before-make time delay

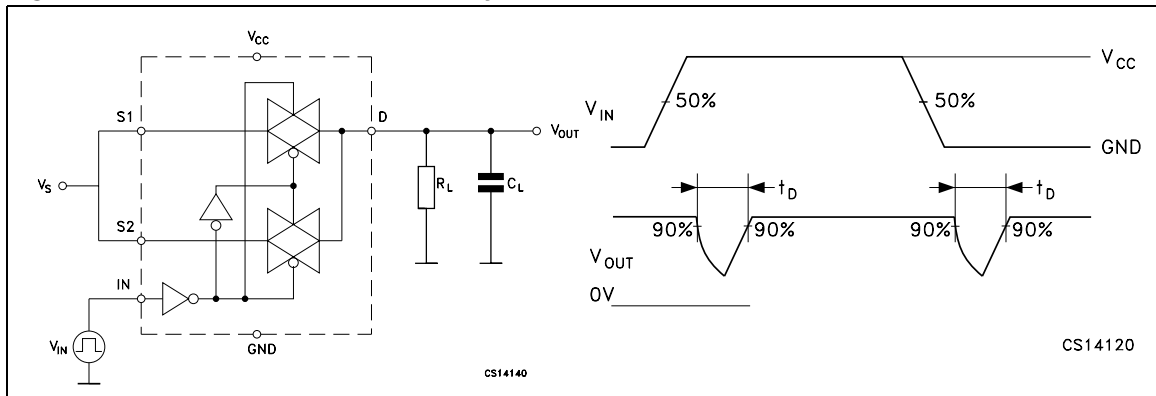


Figure 12. Switching time and charge injection
 ($V_{GEN} = 0\text{ V}$, $R_{GEN} = 0\ \Omega$, $R_L = 1\ \text{M}\Omega$, $C_L = 100\ \text{pF}$)

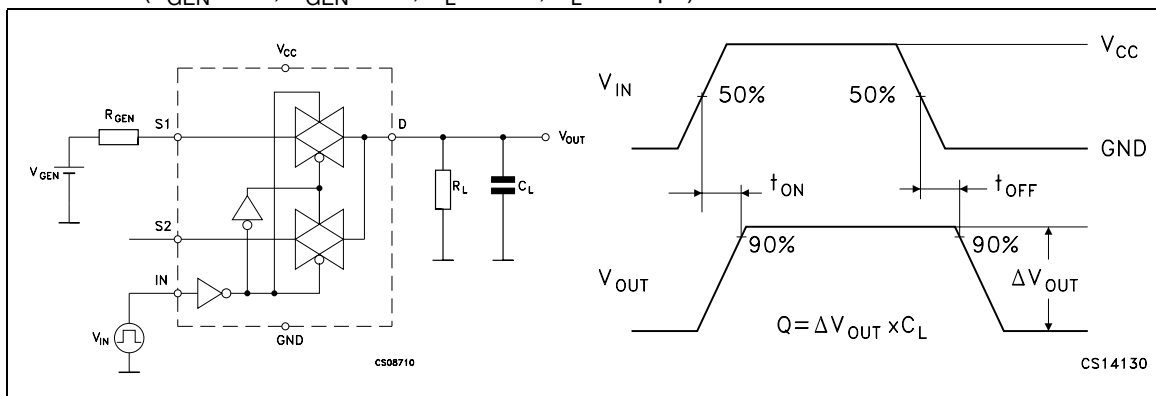
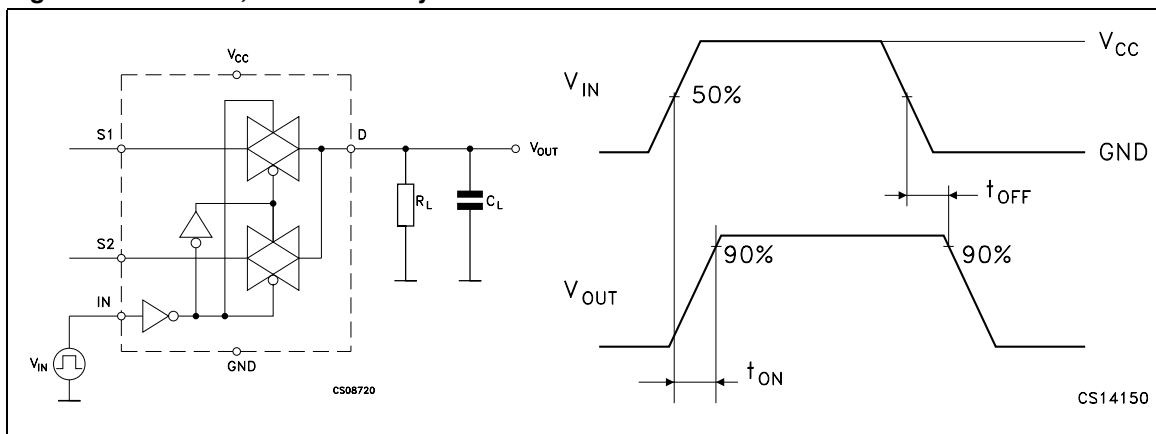


Figure 13. Turn ON, turn OFF delay time



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 14. Package outline for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch

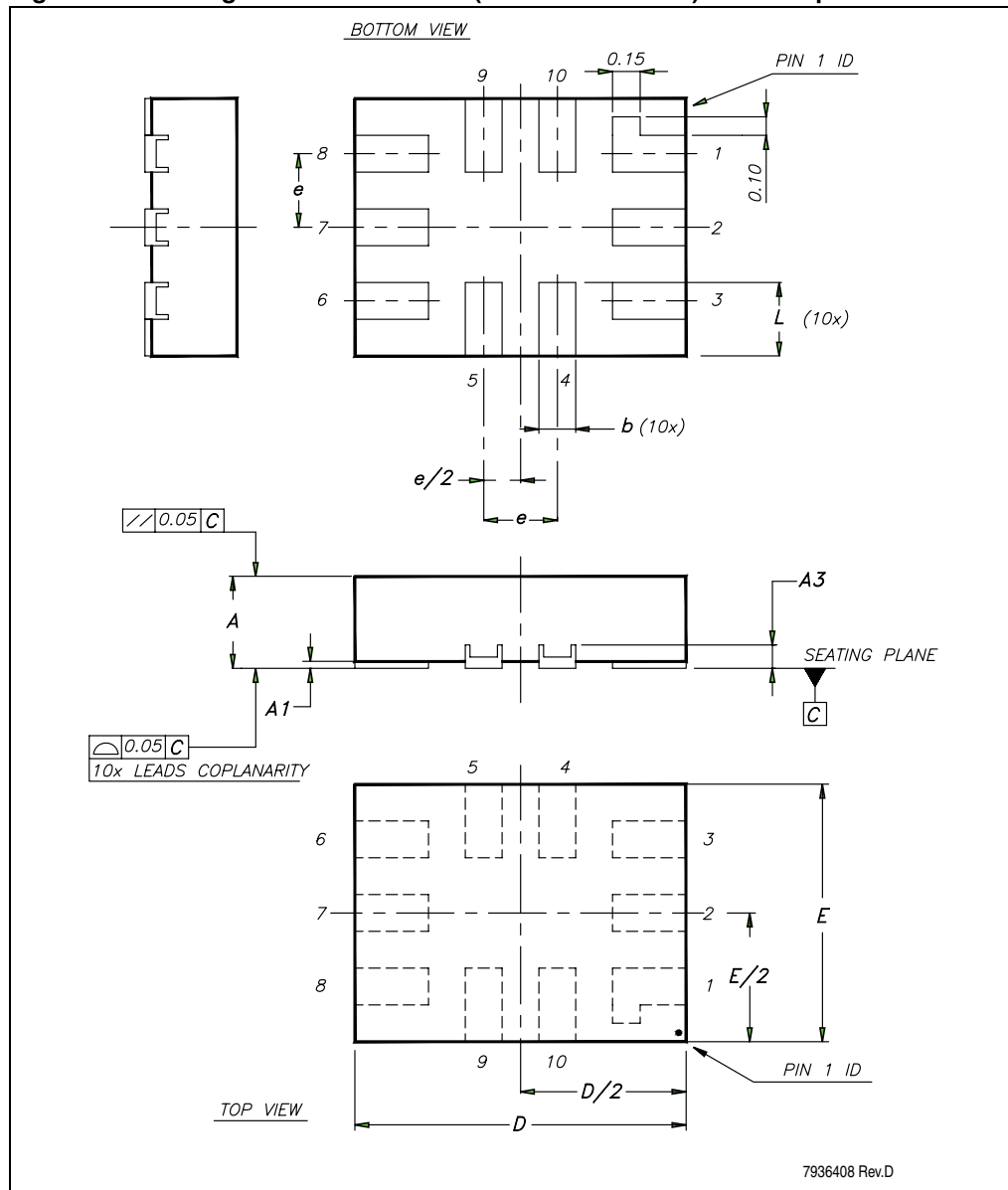


Table 2. Mechanical data for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch

Symbol	Millimeters		
	Min	Typ	Max
A	0.45	0.50	0.55
A1	0	0.02	0.05
A3		0.127	
b	0.15	0.20	0.25
D	1.75	1.80	1.85
E	1.35	1.40	1.45
e		0.40	
L	0.35	0.40	0.45

Figure 15. Footprint recommendations for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch

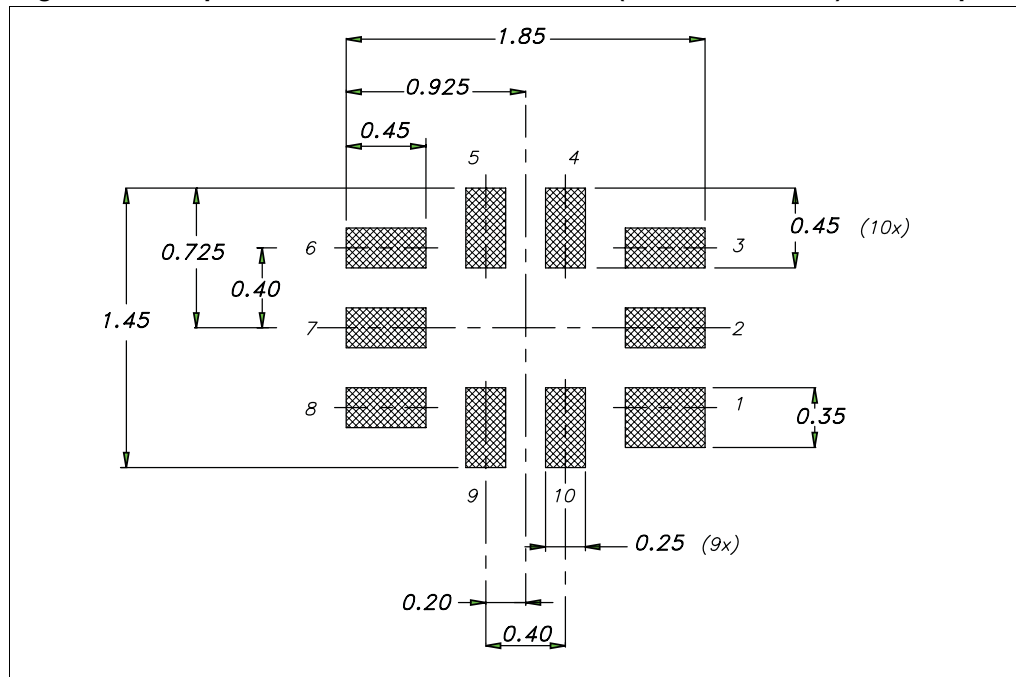


Figure 16. Carrier tape for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch

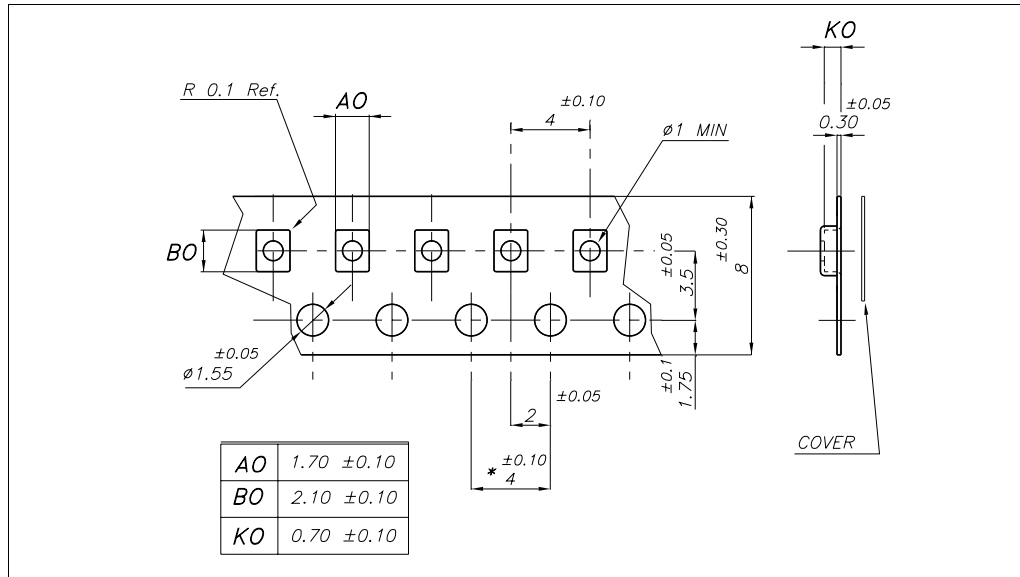


Figure 17. Reel information (front side) for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch

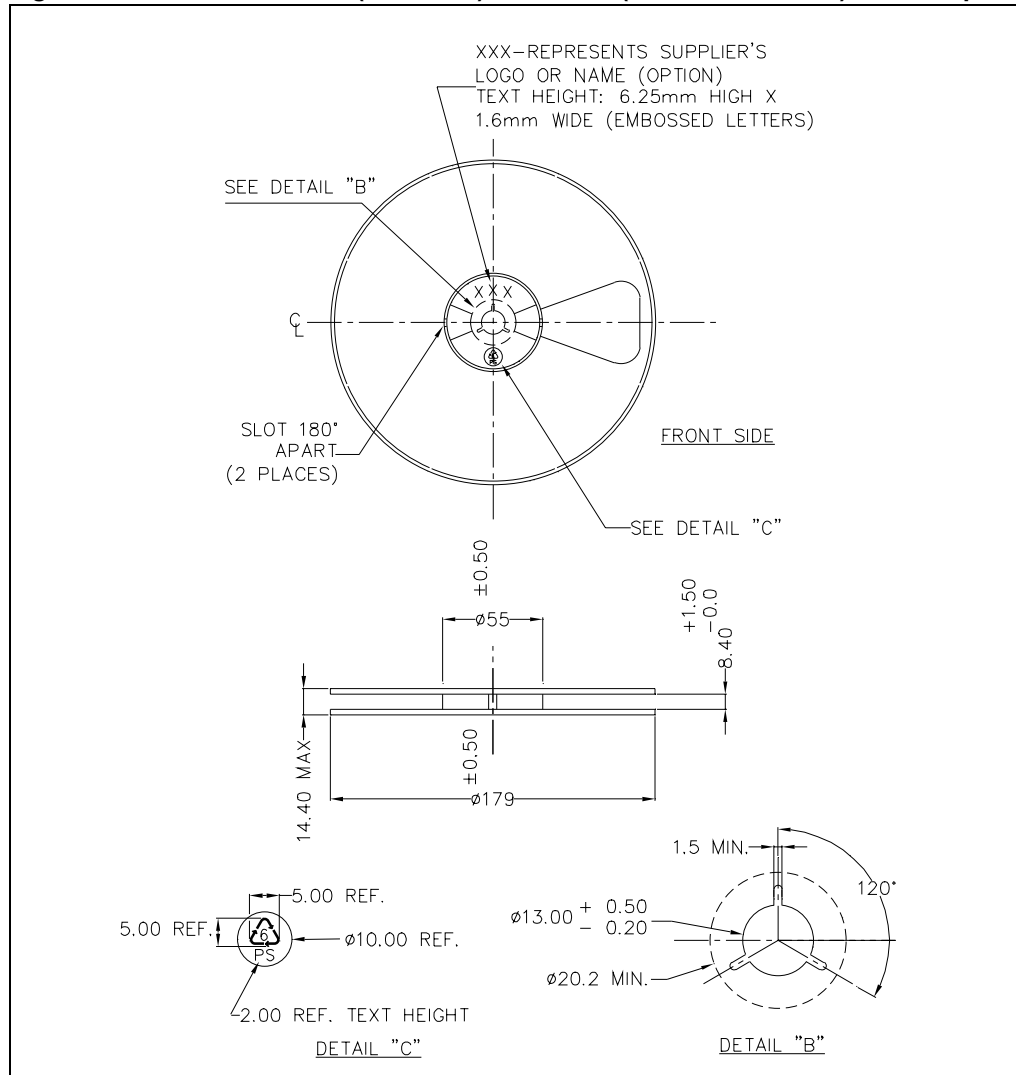
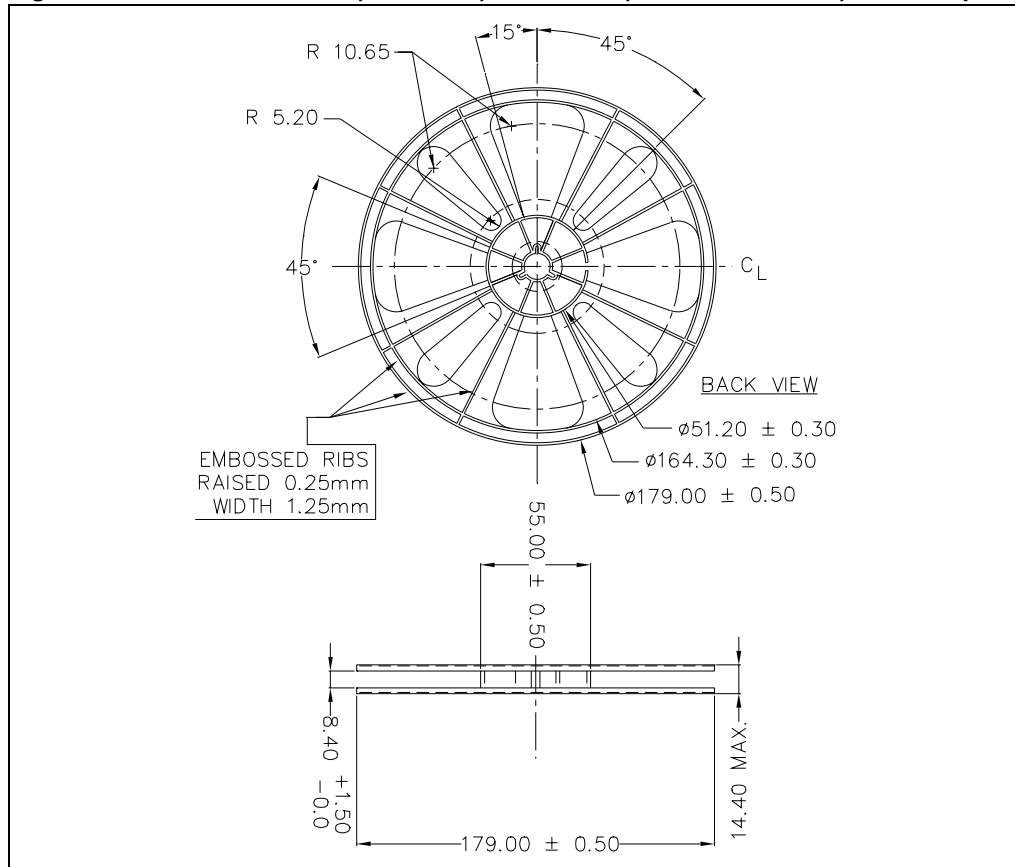


Figure 18. Reel information (back view) for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.4 mm pitch



8 Revision history

Table 10. Document revision history

Date	Revision	Changes
14-May-2009	1	Initial release.

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