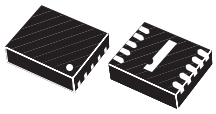
STG3684A

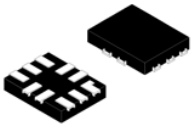
Low voltage 0.5 Ω max dual SPDT switch with break-before-make

Features

- Ultra low power dissipation:
  I_{CC} = 0.2 µA (max.) at T_A = 85 °C
- Low ON resistance V_{IN} = 0 V:
  - R_{ON} = 0.50 Ω (max. T_A = 25 °C) at V_{CC} = 4.3 V
  - R_{ON} = 0.50 Ω (max. T_A = 25 °C) at V_{CC} = 3.6 V
- Wide operating voltage range:
  V_{CC} (OPR) = 1.65 to 4.3 V single supply
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 2.3 to 4.3 V
- Latch-up performance exceeds 300 mA (JESD 17)
- ESD performance:
  HMB > 2 kV (MIL STD 883 method 3015)



DFN10L
(2.3 x 2 mm)



QFN10L
(1.8 x 1.4 mm)

Table 1. Device summary

Order code	Package	Packing
STG3684AUTR	QFN10L (1.8 x 1.4 mm)	Tape and reel
STG3684ADTR	DFN10L (2.3 x 2 mm)	Tape and reel

Contents

1 Description 5

2 Pin settings 6

2.1 Pin connection 6

2.2 Pin description 7

3 Input equivalent circuit and truth table 8

4 Maximum rating 9

Recommended operating conditions 9

5 Electrical characteristics 10

6 Test circuit 13

7 Package mechanical data 19

8 Revision history 28

List of tables

Table 1. Device summary . . . 1
Table 2. Pin description . . . 7
Table 3. Truth table . . . 8
Table 4. Absolute maximum ratings . . . 9
Table 5. Recommended operating conditions . . . 9
Table 6. DC specifications . . . 10
Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq 6$ ns) . . . 11
Table 8. Analog switch characteristics (C_L = 5 pF, R_L = 50 Ω, T_A = 25 °C) . . . 12
Table 9. QFN10L (1.8 x 1.4 mm) mechanical data . . . 20
Table 10. DFN10L (2 x 2.3 mm) mechanical data . . . 24
Table 11. Document revision history . . . 28

List of figures

Figure 1. Pin connection (top through view) . . . 6
Figure 2. Input equivalent circuit . . . 8
Figure 3. ON resistance . . . 13
Figure 4. OFF leakage . . . 14
Figure 5. OFF isolation . . . 14
Figure 6. Bandwidth . . . 15
Figure 7. Channel-to-channel crosstalk . . . 15
Figure 8. Test circuit . . . 16
Figure 9. Break-before-make time delay . . . 16
Figure 10. Charge injection (V_{GEN} = 0 V, R_{GEN} = 0 Ω, R_L = 1 MΩ, C_L = 100 pF) . . . 17
Figure 11. Turn-on, turn-off delay time . . . 18
Figure 12. QFN10L (1.8 x 1.4 mm) package outline . . . 19
Figure 13. QFN10L (1.8 x 1.4 mm) footprint recommendations. . . . 20
Figure 14. QFN10L (1.8 x 1.4 mm) carrier type . . . 21
Figure 15. QFN10L (1.8 x 1.4 mm) reel information - back view . . . 22
Figure 16. QFN10L (1.8 x 1.4 mm) reel information - front side . . . 23
Figure 17. DFN10L (2 x 2.3 mm) package outline . . . 24
Figure 18. DFN10L (2 x 2.3 mm) carrier type . . . 25
Figure 19. DFN10L (2 x 2.3 mm) reel information - back view. . . . 26
Figure 20. DFN10L (2 x 2.3 mm) reel information - front side . . . 27

1 Description

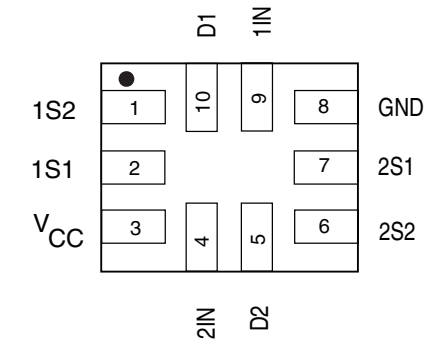
The STG3684A is a high-speed CMOS dual analog SPDT (single-pole dual-throw) switch or dual 2:1 multiplexer/demultiplexer bus switch fabricated using silicon gate C^2MOS technology. Designed to operate from 1.65 to 4.3 V, this device is ideal for portable applications.

It offers very low ON resistance (R_{ON} < 0.5 Ω) at V_{CC} = 3.6 V. The nIN inputs are provided to control the independent channel switches nS1 and nS2. The switches nS1 are ON (connected to common ports Dn) when the nIN input is held high and OFF (state of high impedance exists between the two ports) when nIN is held low. The switches nS2 are ON (connected to common ports Dn) when the nIN input is held low and OFF (state of high impedance exists between the two ports) when IN is held high. Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD and excess transient voltage immunity.

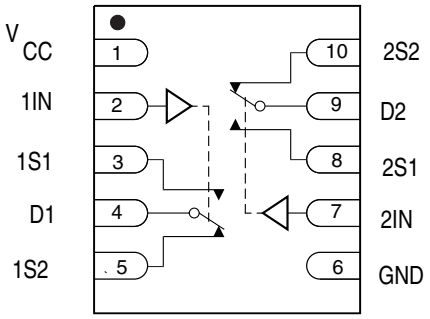
2 Pin settings

2.1 Pin connection

Figure 1. Pin connection (top through view)



QFN10L (1.8 x 1.4 mm)



DFN10L (2.3 x 2 mm)

2.2 Pin description

Table 2. Pin description

Pin number		Symbol	Name and function
QFN10L	DFN10L		
1	5	1S2	Independent channel
2	3	1S1	Independent channel
3	1	V_{CC}	Positive voltage supply
4	7	2IN	Control
5	9	D2	Common channel
6	10	2S2	Independent channel
7	8	2S1	Independent channel
8	6	GND	Ground (0 V)
9	2	1IN	Control
10	4	D1	Common channel

Note: Exposed pad must be soldered to a floating plane. Do NOT connect to power or ground.

3 Input equivalent circuit and truth table

Figure 2. Input equivalent circuit

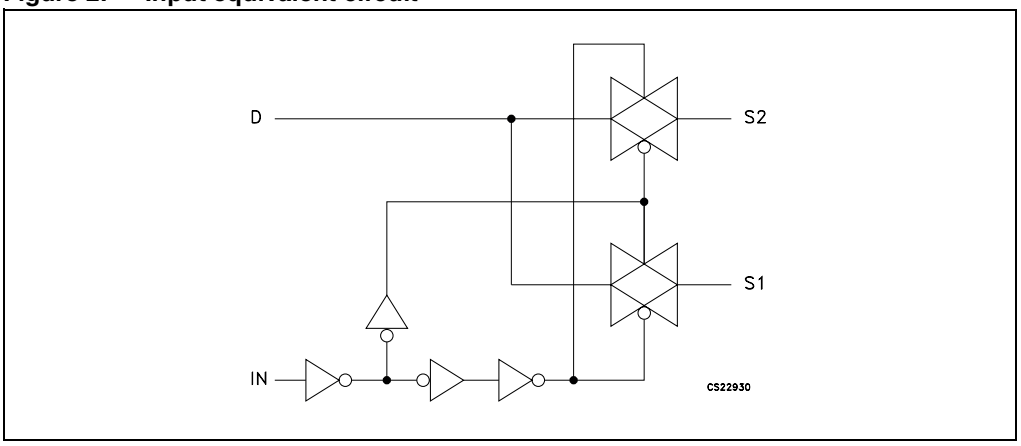


Table 3. Truth table

IN	Switch S1	Switch S2
H	ON	OFF(1)
L	OFF(1)	ON

1. High impedance.

4 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{IN} < 0 V)	-50	mA
I_{IK}	DC Input diode current (V_{IN} < 0 V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±300	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	±500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70 °C	1120	mW
T_{STG}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.3	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65 to 2.7 V	0 to 20	ns/V
		V_{CC}= 3.0 to 4.3 V	0 to 10	

5 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
V_{IH}	High level input voltage	1.65 –1.95		0.65 V_{CC}			0.65 V_{CC}		V
		2.3 –2.5		1.2			1.2		
		2.7 –3.0		1.3			1.3		
		3.0 –3.6		1.4			1.4		
		4.3		1.5			1.5		
V_{IL}	Low level input voltage	1.65 –1.95				0.25		0.25	V
		2.3 –2.5				0.25		0.25	
		2.7 –3.0				0.25		0.25	
		3.0 –3.6				0.30		0.30	
		4.3				0.40		0.40	
R_{ON}	Switch ON resistance	4.3	V_S = 0 V to V_{CC} I_S = 100 mA		0.45	0.50		0.60	Ω
		3.6			0.45	0.50		0.60	
		3.0			0.50	0.55		0.60	
		2.3			0.60	0.70		0.80	
		1.8			0.80	0.9		1.0	
ΔR_{ON}	ON resistance match between channels(1),(2)	2.7	V_S = 1.5 V I_S = 100 mA		0.1				Ω
R_{FLAT}	ON resistance flatness (3)	4.3	V_S = 1.5 V I_S = 100 mA		0.15	0.20		0.20	Ω
		3.6			0.15	0.20		0.20	
		3.0			0.15	0.20		0.20	
		2.7			0.15	0.20		0.20	
		2.3			0.20	0.25		0.25	
		1.65			0.35	0.45		0.45	
I_{OFF}	OFF state leakage current (nSn), (Dn)	4.3	V_S = 0.3 or 4 V			±20		±100	nA
I_{IN}	Input leakage current	0 –4.3	V_{IN} = 0 to 4.3 V			±0.05		±1	µA
I_{CC}	Quiescent supply current (1)	1.65 –4.3	V_{IN} = V_{CC} or GND			±0.05		±0.2	µA

Table 6. DC specifications (continued)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
I_{CCLV}	Quiescent supply current low voltage driving	4.3	V_{1IN}, V_{2IN} = 1.65 V		±37	±50		±100	µA
			V_{1IN}, V_{2IN} = 1.80 V		±33	±40		±50	
			V_{1IN}, V_{2IN} = 2.60 V		±12	±20		±30	

1. Guaranteed by design.
2. $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$.
3. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq$ 6 ns)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation delay	1.65 –1.95			0.45				ns
		2.3 –2.7			0.40				
		3.0 –3.3			0.30				
		3.6 –4.3			0.30				
t_{ON}	Turn-ON time	1.65 –1.95	V_S = 0.8 V		120				ns
		2.3 –2.7	V_S = 1.5 V		65	85		90	
		3.0 –3.3			42	55		65	
		3.6 –4.3			40	55		65	
t_{OFF}	Turn-OFF time	1.65 –1.95	V_S = 0.8 V		45				ns
		2.3 –2.7	V_S = 1.5 V		18	30		40	
		3.0 –3.3			16	30		40	
		3.6 –4.3			15	30		40	
t_D	Break-before make time delay	1.65 –1.95	C_L = 35 pF R_L = 50 Ω V_S = 1.5 V	2	80				ns
		2.3 –2.7		2	60				
		3.0 –3.3		2	55				
		3.6 –4.3		2	50				

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq$ 6 ns) (continued)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
Q	Charge injection	1.65 –1.95	C_L = 100 pF R_L = 1 MΩ V_{GEN} = 0 V R_{GEN} = 0 Ω		43				pC
		2.3 –2.7			51				
		3.0 –3.3			51				
		3.6 –4.3			49				

Table 8. Analog switch characteristics (C_L = 5 pF, R_L = 50 Ω, T_A = 25 °C)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
OIRR	Off isolation(1)	1.65 –4.3	V_S = 1 V_{RMS} f = 100 kHz		-66				dB
Xtalk	Crosstalk	1.65 –4.3	V_S = 1 V_{RMS} f = 100 kHz		-72				dB
THD	Total harmonic distortion	2.3 –4.3	R_L = 600 Ω V_{IN} = 2V_{PP} f = 20 Hz to 20 kHz		0.02				%
BW	-3 dB bandwidth	1.65 –4.3	R_L= 50 Ω		55				MHz
C_{IN}	Control pin input capacitance				5				pF
C_{Sn}	Sn port capacitance	3.3	f = 1 MHz		40				
C_D	D port capacitance when switch is enabled	3.3	f = 1 MHz		114				

1. Off Isolation = 20 Log_{10} (V_D/V_S), V_D = output. V_S = input at off switch.

6 Test circuit

Figure 3. ON resistance

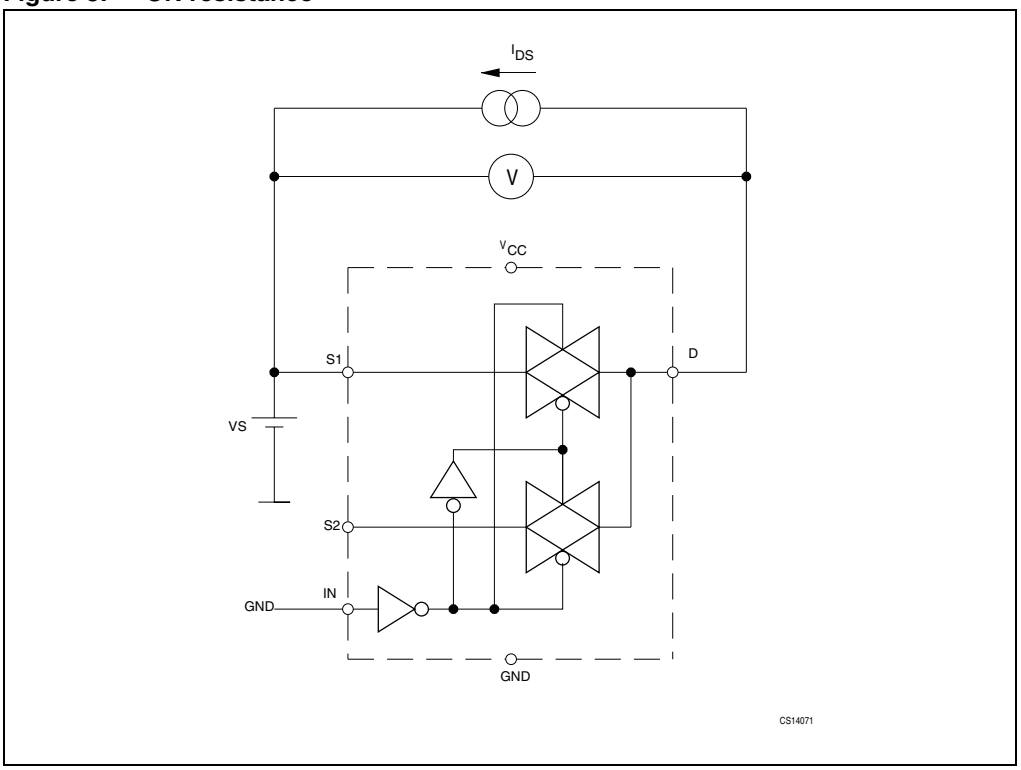


Figure 4. OFF leakage

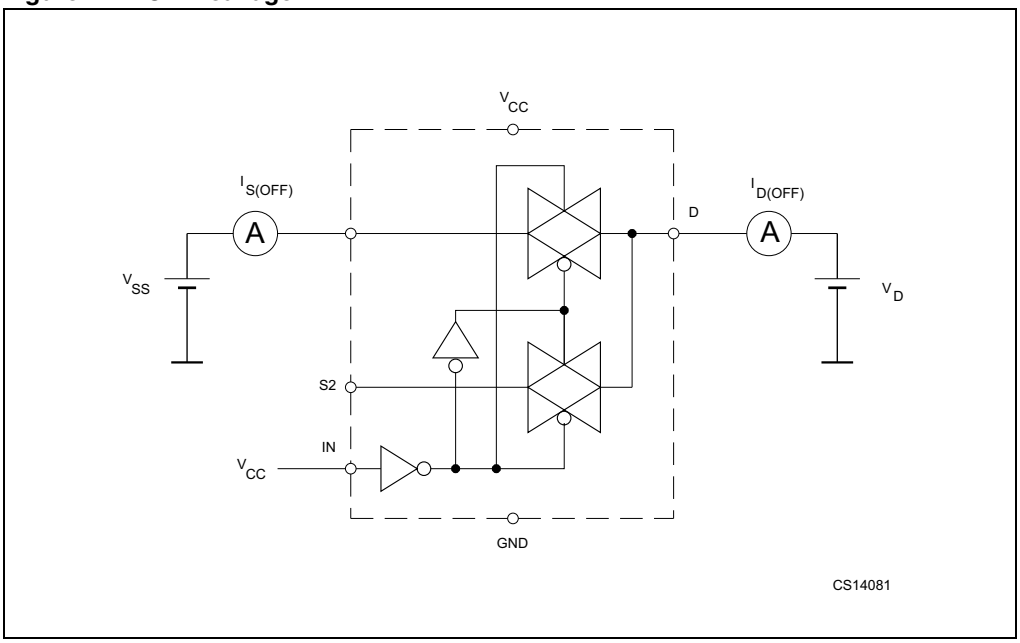


Figure 5. OFF isolation

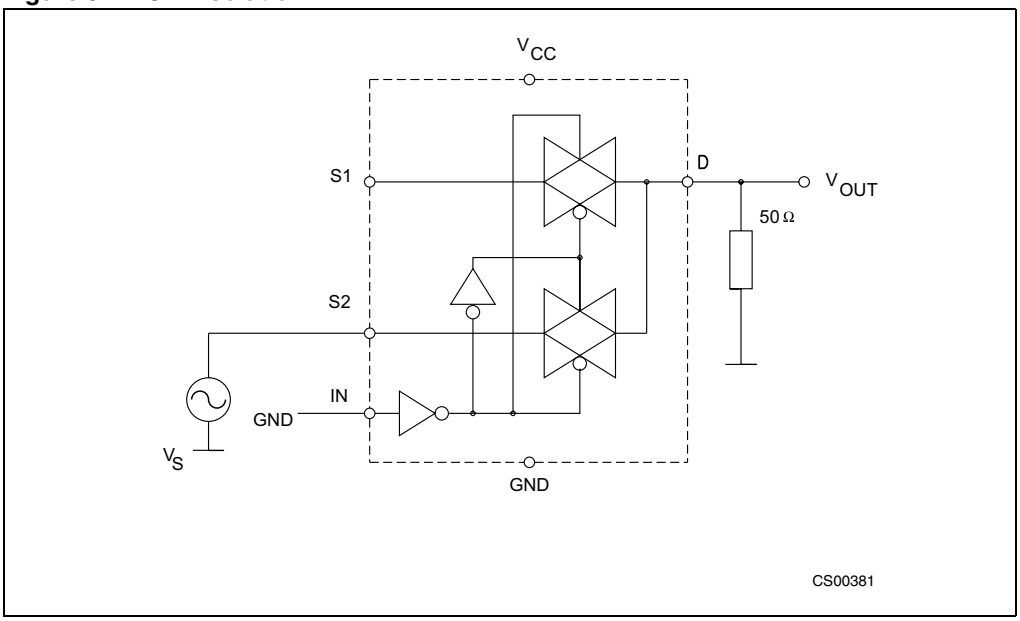


Figure 6. Bandwidth

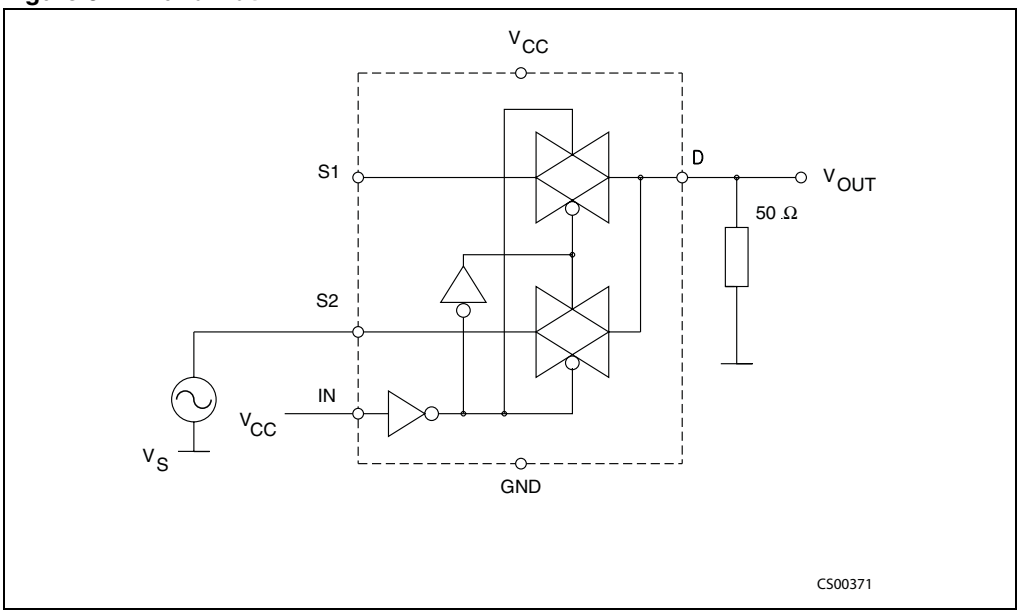


Figure 7. Channel-to-channel crosstalk

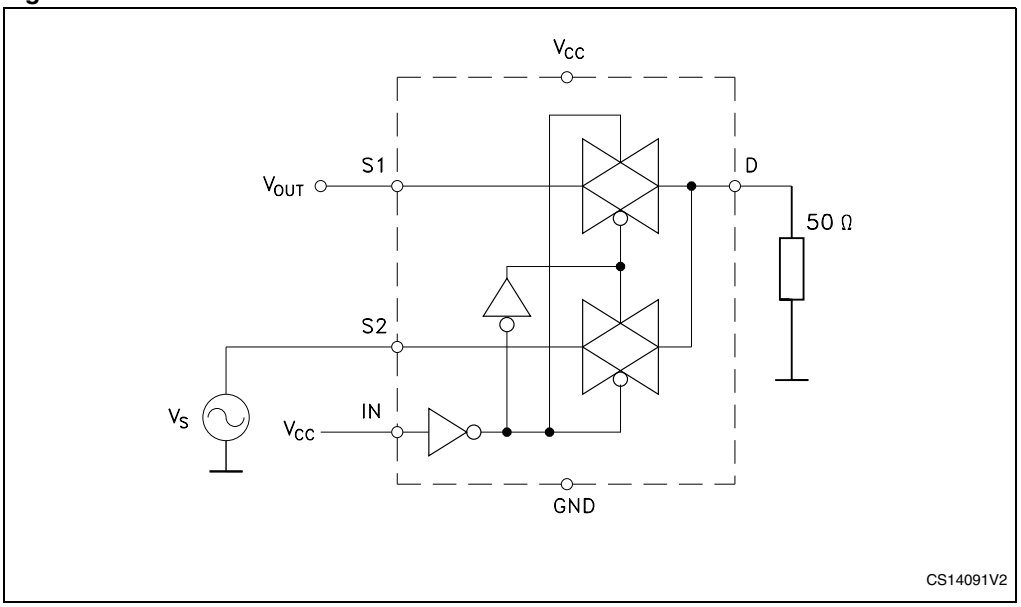
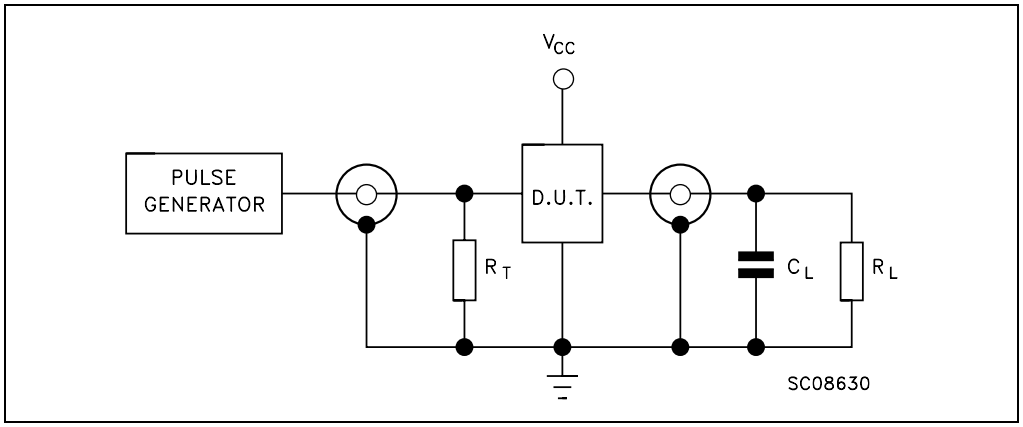


Figure 8. Test circuit



1. C_L = 5/35 pF or equivalent (includes jig and probe capacitance).
   R_L = 50 Ω or equivalent.
   $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω).

Figure 9. Break-before-make time delay

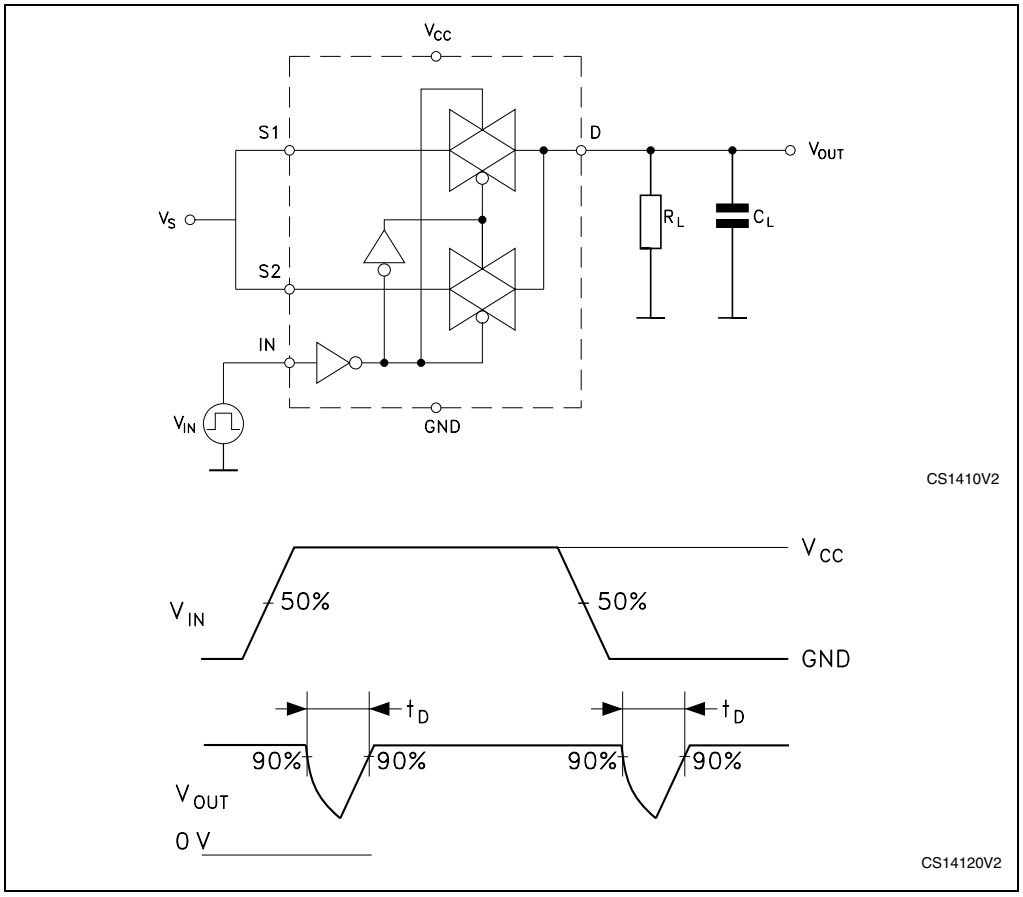


Figure 10. Charge injection (V_{GEN} = 0 V, R_{GEN} = 0 Ω, R_L = 1 MΩ, C_L = 100 pF)

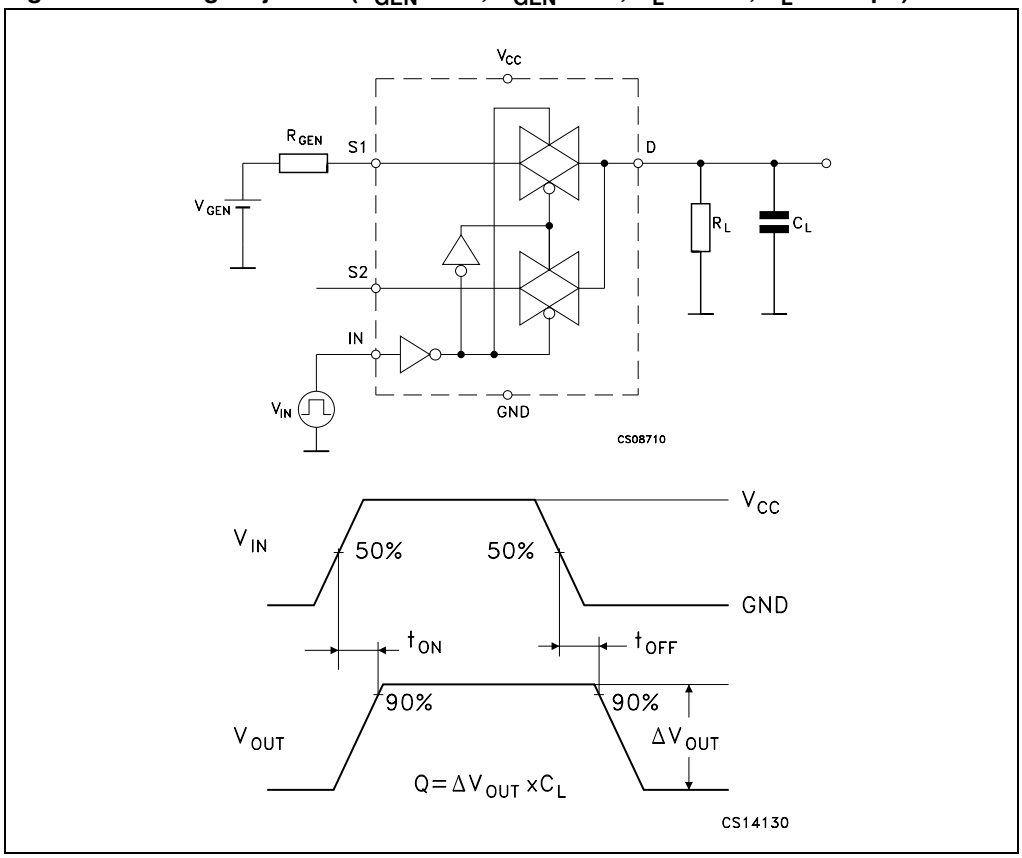
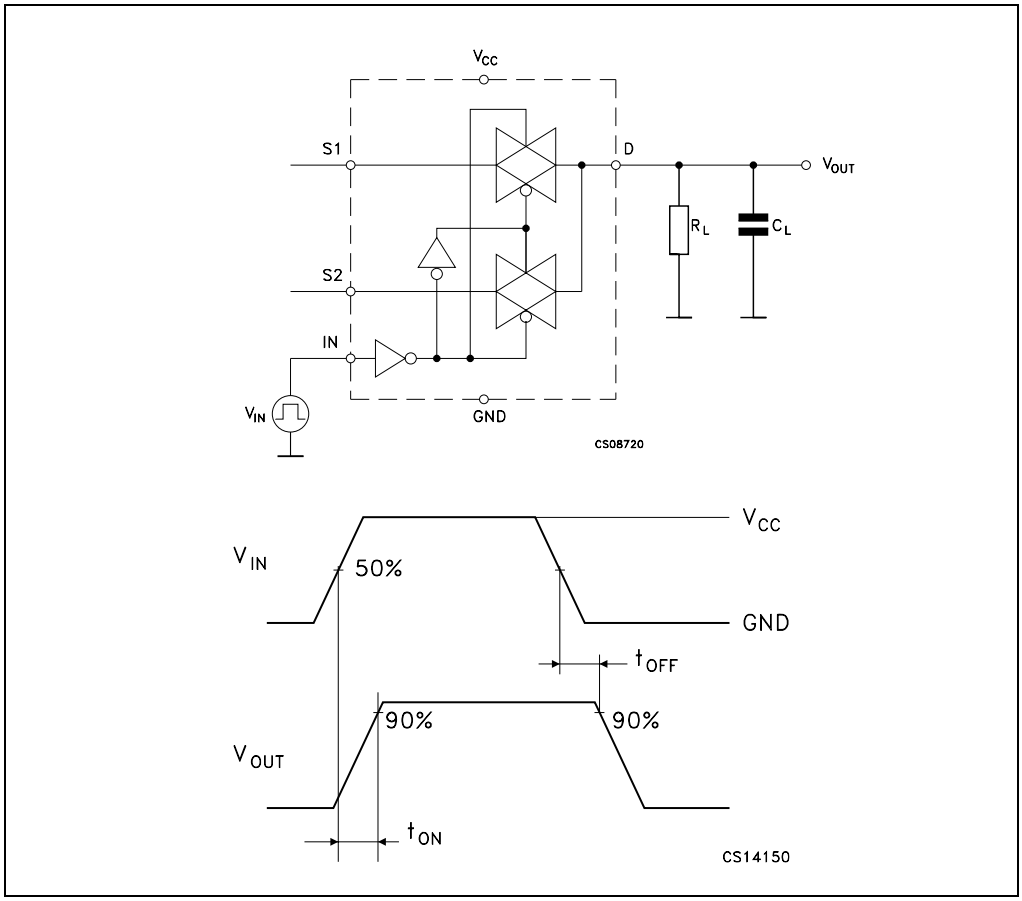


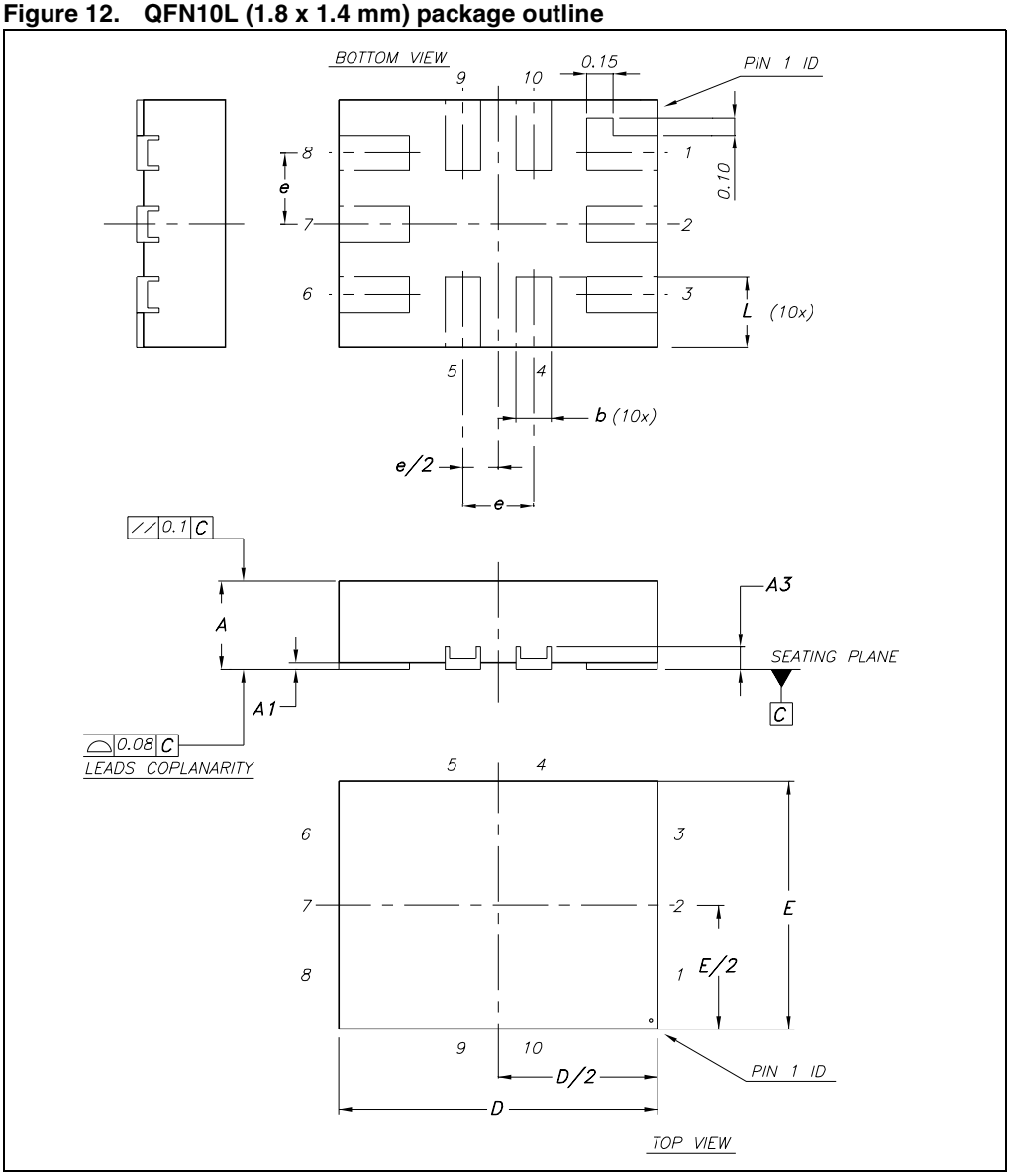
Figure 11. Turn-on, turn-off delay time



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 12. QFN10L (1.8 x 1.4 mm) package outline

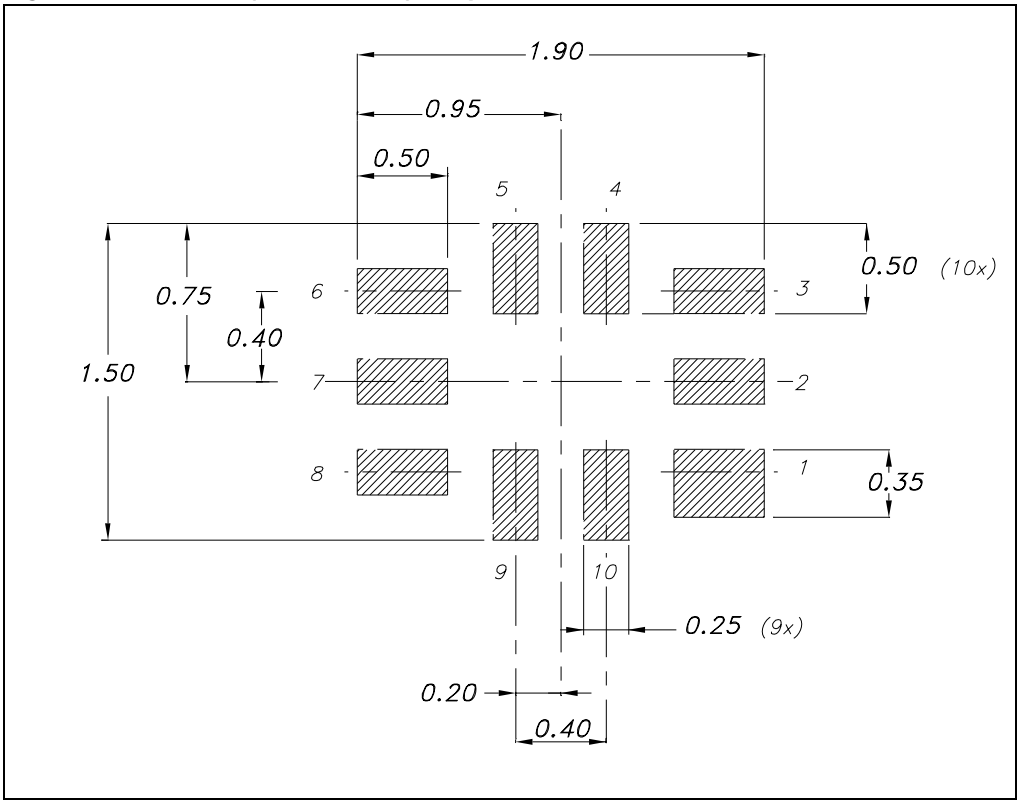


1. Drawing not to scale.

Table 9. QFN10L (1.8 x 1.4 mm) mechanical data

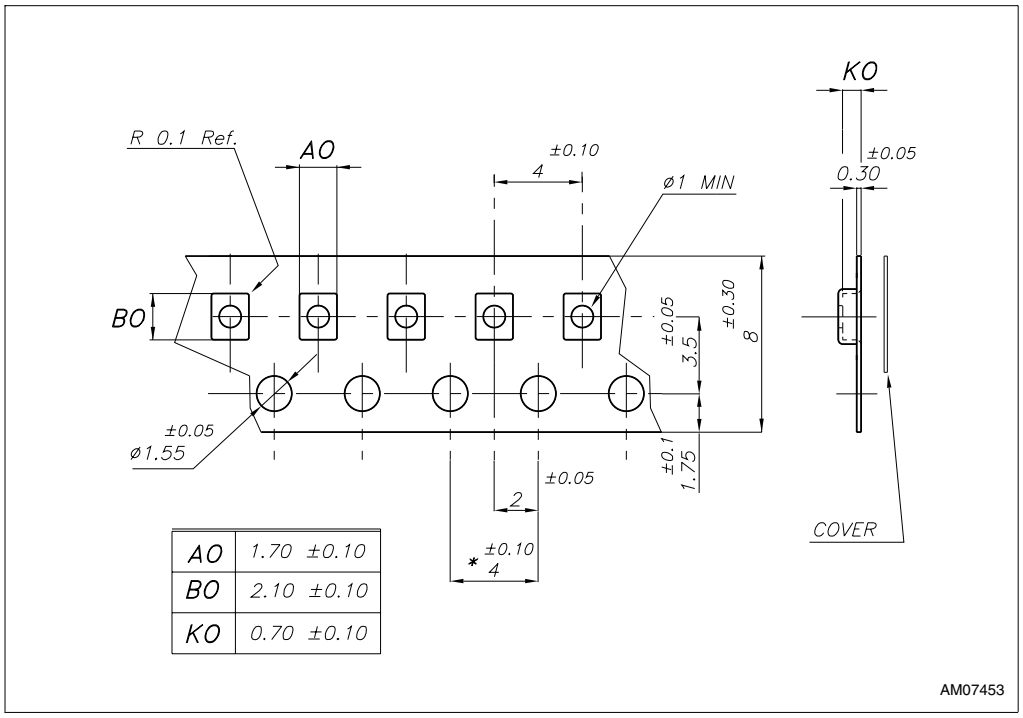
Symbol	millimeters			inches		
	Nom	Min	Max	Nom	Min	Max
A	0.50	0.45	0.55	0.020	0.017	0.021
A1	0.02	0	0.05	0.001	0	0.002
A3	0.127			0.005	0	0
b	0.20	0.15	0.25	0.007	0.006	0.010
D	1.80	1.70	1.90	0.070	0.066	0.074
E	1.40	1.30	1.50	0.055	0.051	0.059
e	0.40			0.015		
L	0.40	0.30	0.50	0.015	0.011	0.020

Figure 13. QFN10L (1.8 x 1.4 mm) footprint recommendations



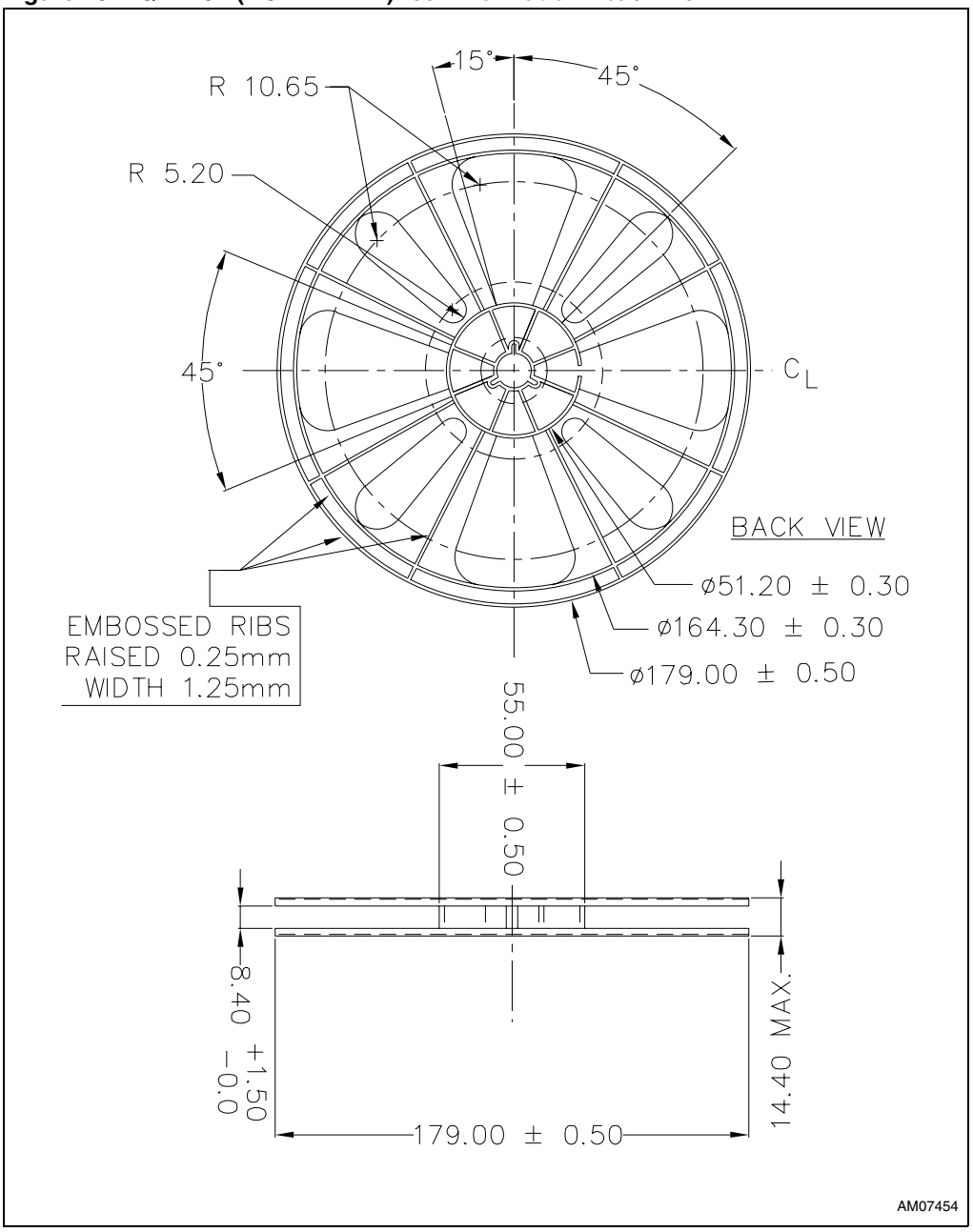
1. Drawing not to scale.

Figure 14. QFN10L (1.8 x 1.4 mm) carrier type



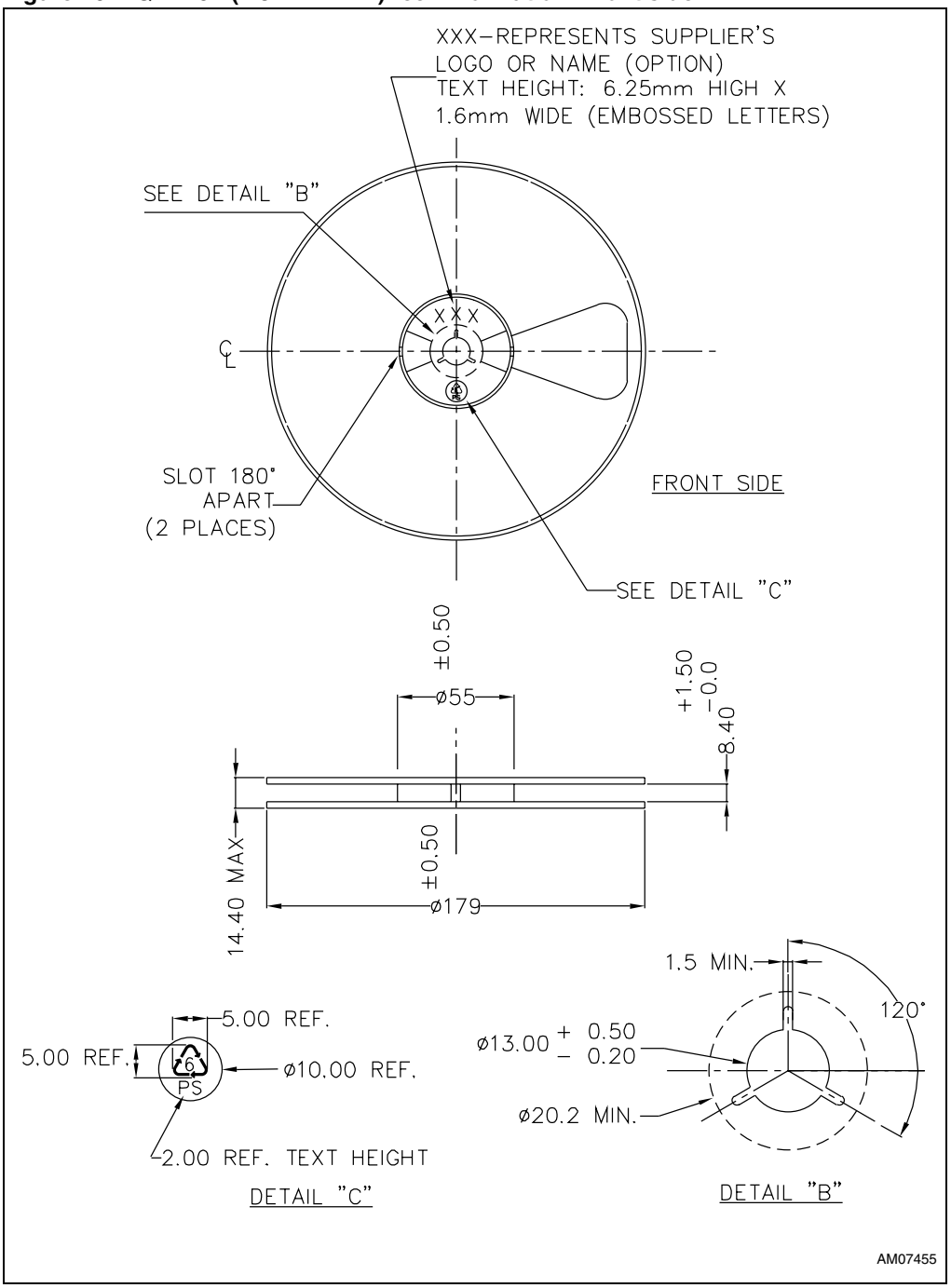
1. Drawing not to scale.

Figure 15. QFN10L (1.8 x 1.4 mm) reel information - back view



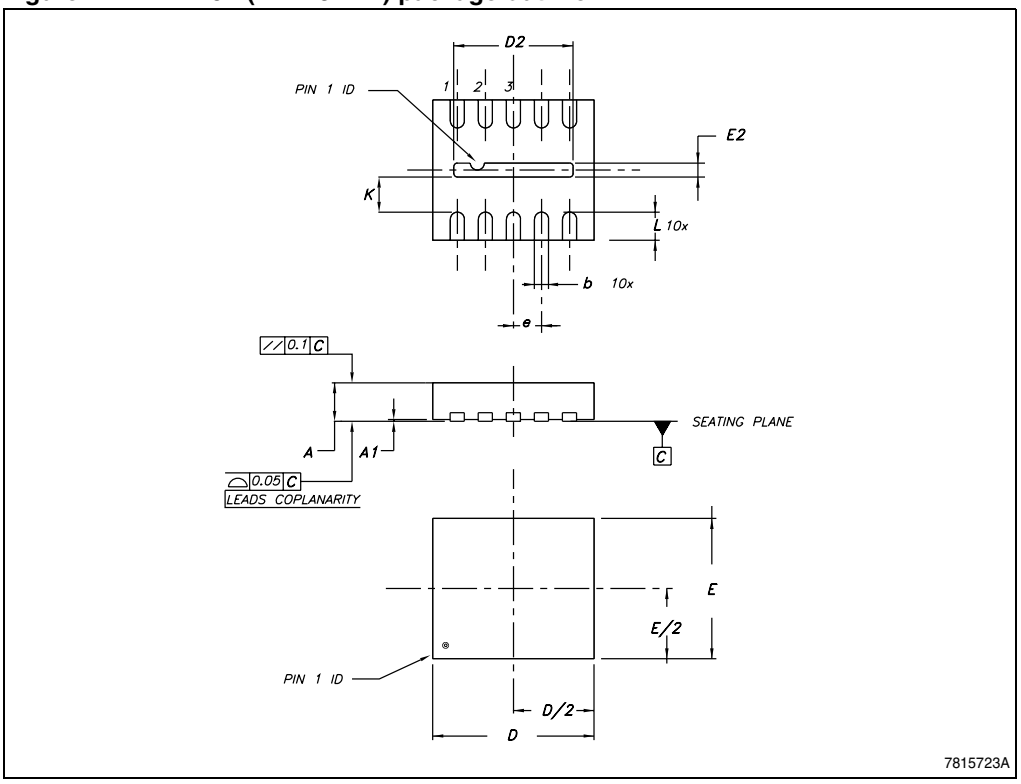
1. Drawing not to scale.

Figure 16. QFN10L (1.8 x 1.4 mm) reel information - front side



1. Drawing not to scale.

Figure 17. DFN10L (2 x 2.3 mm) package outline

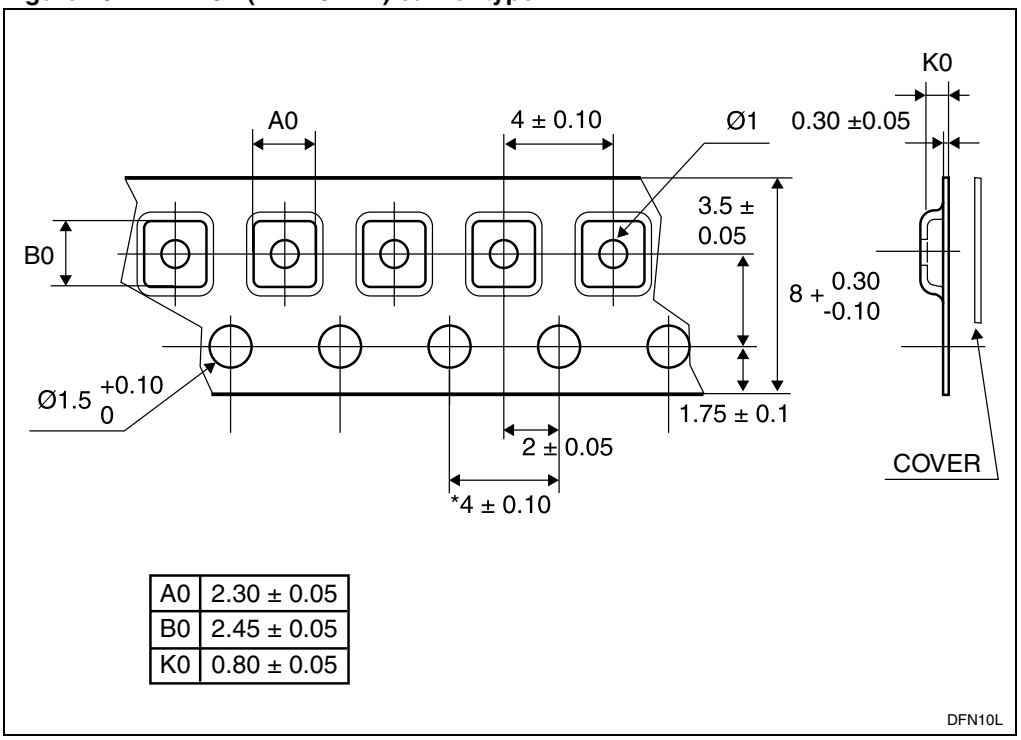


1. Drawing not to scale.

Table 10. DFN10L (2 x 2.3 mm) mechanical data

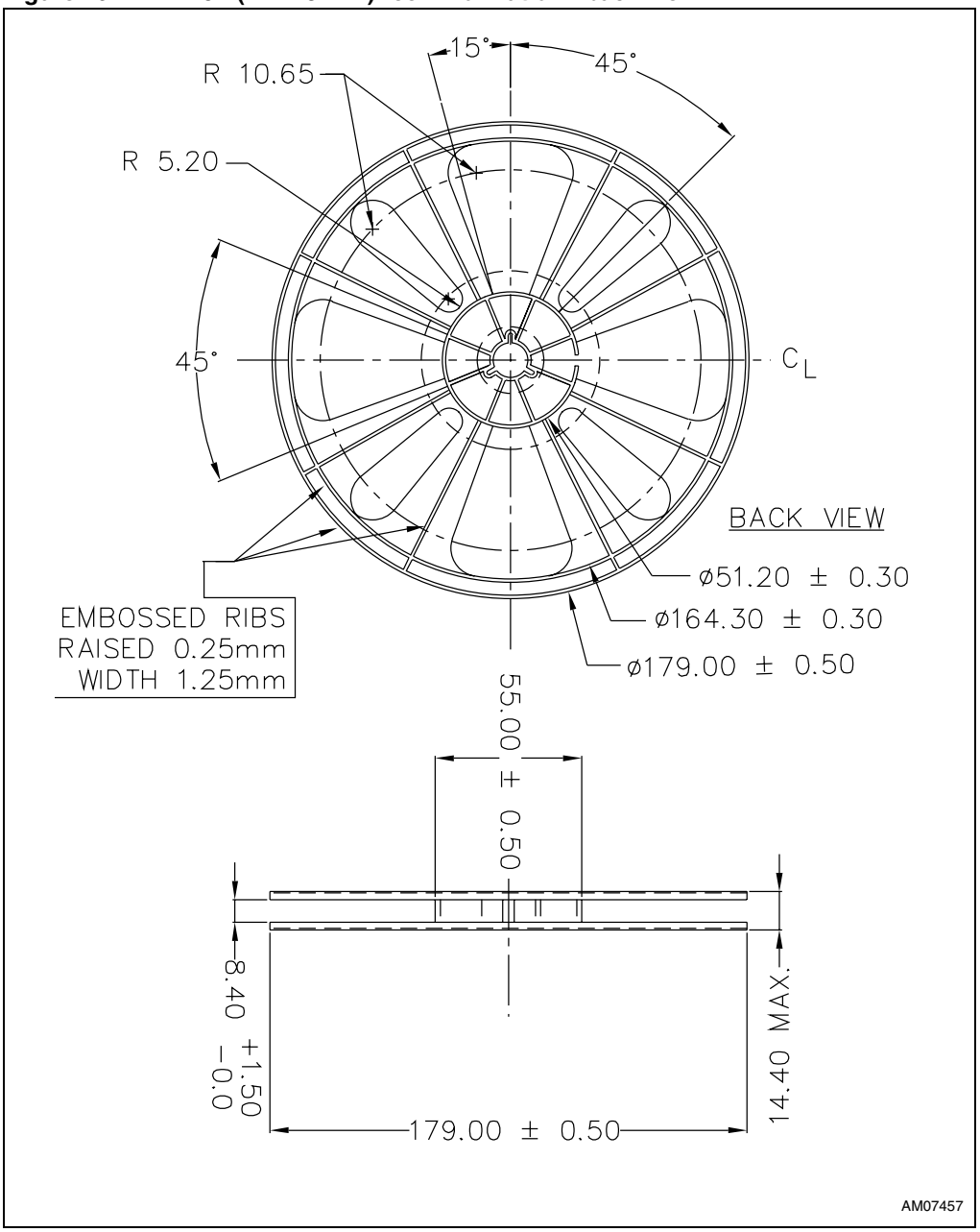
Symbol	millimeters			mils		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.60	19.7	21.7	23.6
A1		0.02	0.05		0.8	2.0
b	0.15	0.20	0.25	5.9	7.9	9.8
D	2.20	2.30	2.40	86.6	90.6	94.5
D2	1.65	1.70	1.75	65.0	66.9	68.9
E	1.90	2	2.10	74.8	78.7	82.7
E2	0.15	0.20	0.25	5.9	7.9	9.8
e		0.40			15.7	
L	0.35	0.40	0.45	13.8	15.7	17.7
K	0.20			7.9		

Figure 18. DFN10L (2 x 2.3 mm) carrier type



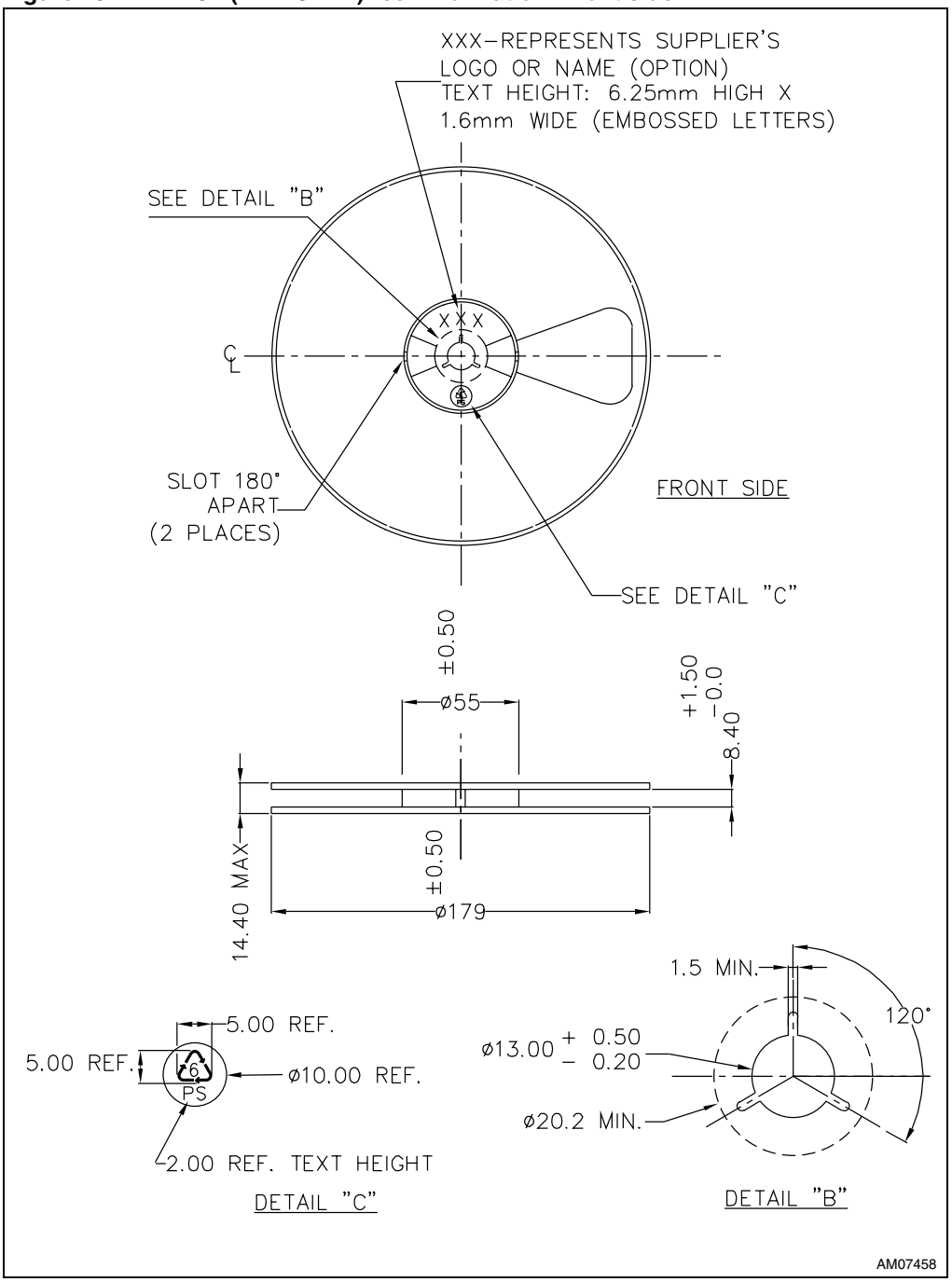
1. Drawing not to scale.

Figure 19. DFN10L (2 x 2.3 mm) reel information - back view



1. Drawing not to scale.

Figure 20. DFN10L (2 x 2.3 mm) reel information - front side



1. Drawing not to scale.

8 Revision history

Table 11. Document revision history

Date	Revision	Changes
04-Jul-2005	1	First release.
22-Aug-2005	2	The V_{CC} and V_{IC} values has been changed on *Table 4 on page 9*.
15-May-2006	3	New template, few updates.
21-Jun-2006	4	Mechanical data updated.
10-Sept-2007	5	Removed STG3684QTR order code, small text changes, updated *Figure 3 on page 13*, *Figure 4 on page 14*, *Figure 5 on page 14*, *Figure 6 on page 15*, layout restructured.
15-Nov-2007	6	Added list of tables and list of figures, updated *Features Section on page 1* and T_{op} value in *Table 5 on page 9*, removed the -55 to -125 ° C values in *Table 6 on page 10* and *Table 7 on page 11*, minor changes to the text and layout.
04-Feb-2011	7	Document reformatted, updated *Features*, *Section 1: Description*, *Table 6*, ECOPACK text, corrected typo in *Table 2* to *Table 8*, *Figure 7*, *Figure 9*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com