

### FEATURES

- 44 V supply maximum ratings**
- V<sub>SS</sub> to V<sub>DD</sub> analog signal range**
- Low on resistance (<70 Ω)**
- Low ΔR<sub>ON</sub> (9 Ω max)**
- Low R<sub>ON</sub> match (3 Ω max)**
- Low power dissipation**
- Fast switching times**
  - t<sub>ON</sub> < 110 ns
  - t<sub>OFF</sub> < 60 ns
- Low leakage currents (3 nA max)**
- Low charge injection (6 pC max)**
- Break-before-make switching action**
- Latch-up proof A grade**
- Plug-in upgrade for DG201A/ADG201A, DG202A/ADG202A, DG211/ADG211A**
- Plug-in replacement for DG441/DG442/DG444**

### APPLICATIONS

- Audio and video switching**
- Automatic test equipment**
- Precision data acquisition**
- Battery-powered systems**
- Sample-and-hold systems**
- Communication systems**

### GENERAL DESCRIPTION

The ADG441, ADG442, and ADG444 are monolithic CMOS devices that comprise of four independently selectable switches. They are designed on an enhanced LC<sup>2</sup>MOS process that provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals. High switching speed also makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments. The ADG441, ADG442, and ADG444 contain four independent SPST switches. Each switch of the ADG441 and ADG444 turns on when a logic low is applied to the appropriate control input. The ADG442 switches are turned on with logic high on the appropriate control input. The ADG441 and ADG444 switches

#### Rev. A

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### FUNCTIONAL BLOCK DIAGRAM

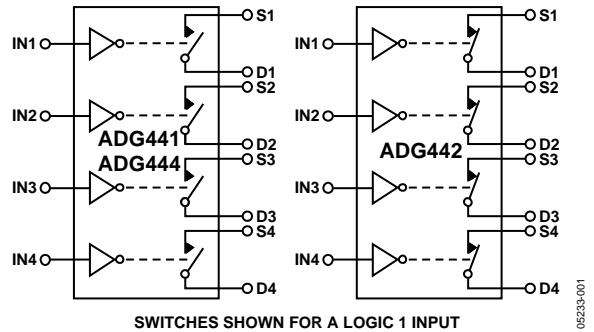


Figure 1.

differ in that the ADG444 requires a 5 V logic power supply that is applied to the V<sub>L</sub> pin. The ADG441 and ADG442 do not have a V<sub>L</sub> pin, the logic power supply is generated internally by an on-chip voltage generator.

Each switch conducts equally well in both directions when ON and has an input signal range that extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is the low charge injection for minimum transients when switching the digital inputs.

### PRODUCT HIGHLIGHTS

1. Extended signal range. The ADG441A/ADG442A/ADG444A are fabricated on an enhanced LC<sup>2</sup>MOS, trench-isolated process, giving an increased signal range that extends to the supply rails.
2. Low power dissipation.
3. Low R<sub>ON</sub>.
4. Trench isolation guards against latch-up for A grade parts. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
5. Break-before-make switching. This prevents channel shorting when the switches are configured as a multiplexer.
6. Single-supply operation. For applications where the analog signal is unipolar, the ADG441/ADG442/ADG444 can be operated from a single-rail power supply. The parts are fully specified with a single 12 V power supply.

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**REVISION HISTORY**

**5/05—Data Sheet Changed from Rev. 0 to Rev. A**

Changes to Format .....	Universal
Deleted CERDIP Package and T Grade .....	Universal
Changes to Features and Product Highlights .....	1
Changes to Test Conditions in Table 2 .....	4
Changes to Figure 11 .....	8
Changes to Trench Isolation Section .....	12
Updated Outline Dimensions .....	13
Changes to Ordering Guide .....	14

**4/94—Revision 0: Initial Version**

# SPECIFICATIONS

## DUAL SUPPLY<sup>1</sup>

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $V_L = +5\text{ V} \pm 10\%$  (ADG444), GND = 0 V, unless otherwise noted.

**Table 1.**

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		$V_{SS}$ to $V_{DD}$	V	
$R_{ON}$	40		$\Omega$ typ	$V_D = \pm 8.5\text{ V}$ , $I_S = -10\text{ mA}$
	70	85	$\Omega$ max	$V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
$\Delta R_{ON}$		4	$\Omega$ typ	$-8.5\text{ V} \leq V_D \leq +8.5\text{ V}$
		9	$\Omega$ max	
$R_{ON}$ Match		1	$\Omega$ typ	$V_D = 0\text{ V}$ , $I_S = -10\text{ mA}$
		3	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
	$\pm 0.5$	$\pm 3$	nA max	$V_D = \pm 15.5\text{ V}$ , $V_S = \mp 15.5\text{ V}$
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$		nA typ	See Figure 15
	$\pm 0.5$	$\pm 3$	nA max	$V_D = \pm 15.5\text{ V}$ , $V_S = \mp 15.5\text{ V}$
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.08$		nA typ	See Figure 15
	$\pm 0.5$	$\pm 3$	nA max	$V_S = V_D = \pm 15.5\text{ V}$
			nA max	See Figure 16
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current				
$I_{INL}$ or $I_{INH}$		$\pm 0.00001$	$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.5$	$\mu\text{A}$ max	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	85		ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$ ;
	110	170	ns max	$V_S = \pm 10\text{ V}$ ; see Figure 17
$t_{OFF}$	45		ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$ ;
	60	80	ns max	$V_S = \pm 10\text{ V}$ ; see Figure 17
$t_{OPEN}$	30		ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$ ;
Charge Injection	1		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ;
	6		pC max	$V_{DD} = +15\text{ V}$ , $V_{SS} = -15\text{ V}$ ; see Figure 18
OFF Isolation	60		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; $f = 1\text{ MHz}$ ; see Figure 19
Channel-to-Channel Crosstalk	100		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; $f = 1\text{ MHz}$ ; see Figure 20
$C_S$ (OFF)	4		pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	4		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	16		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$				$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
ADG441/ADG442		80	$\mu\text{A}$ max	Digital Inputs = 0 V or 5 V
ADG444	0.001		$\mu\text{A}$ typ	
	1	2.5	$\mu\text{A}$ max	
$I_{SS}$	0.0001		$\mu\text{A}$ typ	
	1	2.5	$\mu\text{A}$ max	
$I_L$ (ADG444 Only)	0.001		$\mu\text{A}$ typ	$V_L = 5.5\text{ V}$
	1	2.5	$\mu\text{A}$ max	

<sup>1</sup> Temperature range is: B Version: -40°C to +85°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

# ADG441/ADG442/ADG444

## SINGLE SUPPLY<sup>1</sup>

$V_{DD} = +12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $V_L = +5\text{ V} \pm 10\%$  (ADG444),  $GND = 0\text{ V}$ , unless otherwise noted.

Table 2.

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
ANALOG SWITCH				
Analog Signal Range		0 to $V_{DD}$	V	
$R_{ON}$	70		$\Omega$ typ	$V_D = +3\text{ V}$ , $+8\text{ V}$ , $I_S = -5\text{ mA}$
	110	130	$\Omega$ max	$V_{DD} = 10.8\text{ V}$
$\Delta R_{ON}$		4	$\Omega$ typ	$3\text{ V} \leq V_D \leq 8\text{ V}$
		9	$\Omega$ max	
$R_{ON}$ Match		1	$\Omega$ typ	$V_D = +6\text{ V}$ , $I_S = -5\text{ mA}$
		3	$\Omega$ max	
<b>LEAKAGE CURRENT</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		nA typ	$V_{DD} = 13.2\text{ V}$ $V_D = 12.2\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/12.2\text{ V}$
	$\pm 0.5$	$\pm 3$	nA max	See Figure 15
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$		nA typ	$V_D = 12.2\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/12.2\text{ V}$
	$\pm 0.5$	$\pm 3$	nA max	See Figure 15
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.08$		nA typ	$V_S = V_D = 12.2\text{ V}/1\text{ V}$
	$\pm 0.5$	$\pm 3$	nA max	Figure 16
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current				
$I_{INL}$ or $I_{INH}$		$\pm 0.00001$	$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.5$	$\mu\text{A}$ max	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	105		ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$
	150	220	ns max	$V_S = 8\text{ V}$ ; Figure 17
$t_{OFF}$	40		ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$
	60	100	ns max	$V_S = 8\text{ V}$ ; Figure 17
$t_{OPEN}$	50		ns typ	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$
Charge Injection	2		pC typ	$V_S = 6\text{ V}$ , $R_S = 0\text{ }\Omega$ , $C_L = 1\text{ nF}$
	6		pC max	$V_{DD} = 12\text{ V}$ , $V_{SS} = 0\text{ V}$ ; see Figure 18
OFF Isolation	60		dB typ	$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 19
Channel-to-Channel Crosstalk	100		dB typ	$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 20
$C_S$ (OFF)	7		pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	10		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	16		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$				$V_{DD} = 13.2\text{ V}$ Digital Inputs = 0 V or 5 V
ADG441/ADG442		80	$\mu\text{A}$ max	
ADG444	0.001		$\mu\text{A}$ typ	
	1	2.5	$\mu\text{A}$ max	
$I_L$ (ADG444 Only)	0.001		$\mu\text{A}$ typ	$V_L = 5.5\text{ V}$
	1	2.5	$\mu\text{A}$ max	

<sup>1</sup> Temperature range is: B Version: -40°C to +85°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	44 V
$V_{DD}$ to GND	-0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to -25 V
$V_L$ to GND	-0.3 V to $V_{DD} + 0.3$ V
Analog, Digital Inputs	$V_{SS} - 2$ V to $V_{DD} + 2$ V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	100 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature, Soldering (10 sec)	300°C
Plastic Package, Power Dissipation	470 mW
$\theta_{JA}$ , Thermal Impedance	177°C/W
Lead Temperature, Soldering (10 sec)	260°C
SOIC Package, Power Dissipation	600 mW
$\theta_{JA}$ , Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

**Table 4. Truth Table**

ADG441/ADG444 IN	ADG442 IN	Switch Condition
0	1	ON
1	0	OFF

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# ADG441/ADG442/ADG444

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Figure 2. ADG441/ADG442 (DIP/SOIC)

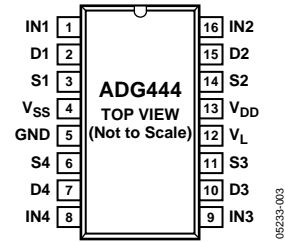


Figure 3. ADG444 (DIP/SOIC)

Table 5. ADG441/ADG442 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16	IN1 to IN4	Logic Control Input.
2, 7, 10, 15	D1 to D4	Drain Terminal. May be an input or output.
3, 6, 11, 14	S1 to S4	Source Terminal. May be an input or output.
4	V <sub>SS</sub>	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it may be connected to ground.
5	GND	Ground (0 V) Reference.
12	NC	No Connect.
13	V <sub>DD</sub>	Most Positive Power Supply Potential.

Table 6. ADG444 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16	IN1 to IN4	Logic Control Input.
2, 7, 10, 15	D1 to D4	Drain Terminal. May be an input or output.
3, 6, 11, 14	S1 to S4	Source Terminal. May be an input or output.
4	V <sub>SS</sub>	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it may be connected to ground.
5	GND	Ground (0 V) Reference.
12	V <sub>L</sub>	Logic Power Supply (5 V).
13	V <sub>DD</sub>	Most Positive Power Supply Potential.

### TYPICAL PERFORMANCE CHARACTERISTICS



Figure 4.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Dual Supply

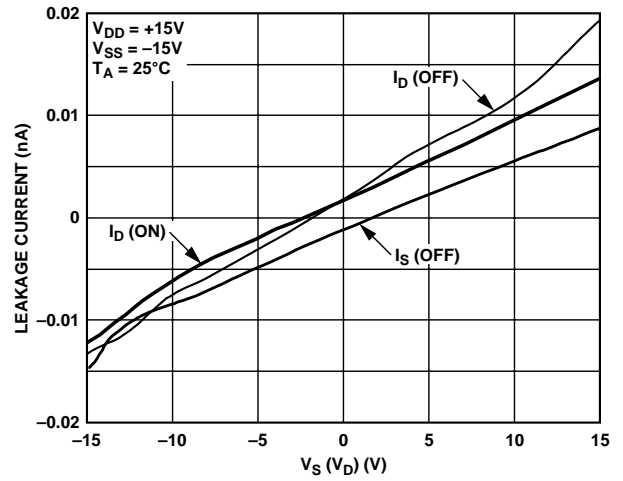


Figure 7. Leakage Currents as a Function of  $V_S$  ( $V_D$ )

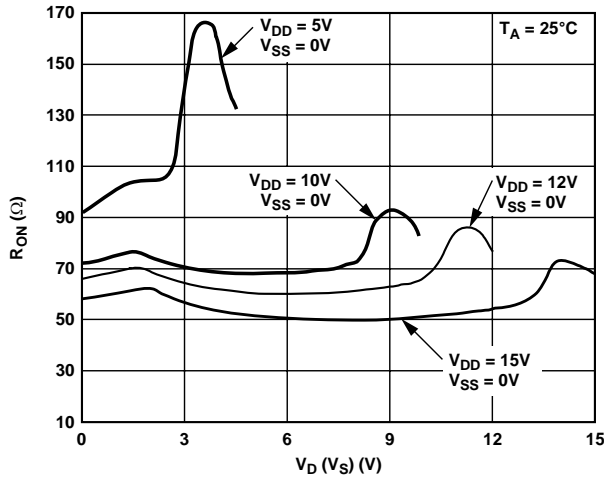


Figure 5.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Single Supply

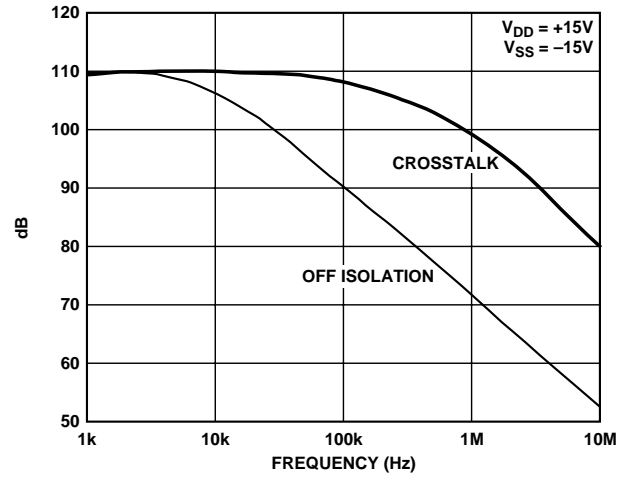


Figure 8. Crosstalk and Off Isolation vs. Frequency

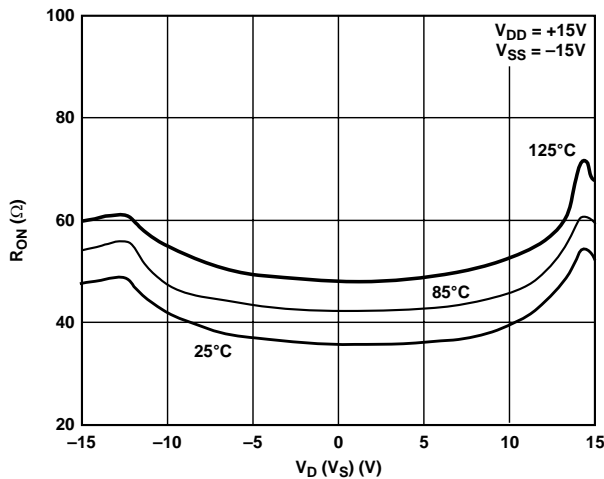


Figure 6.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

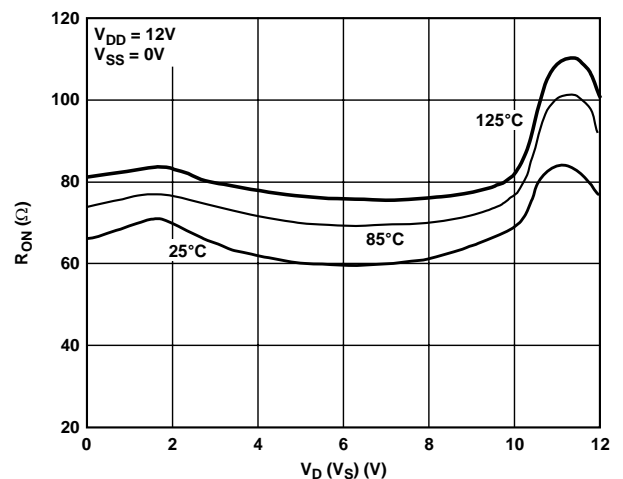


Figure 9.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

# ADG441/ADG442/ADG444

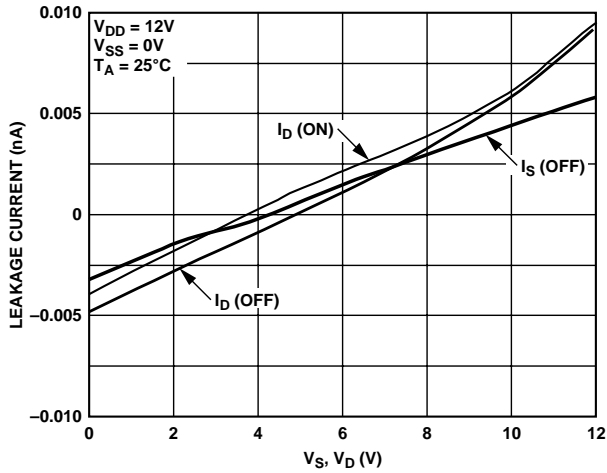


Figure 10. Leakage Currents as a Function of  $V_S$  ( $V_D$ )

05233-011

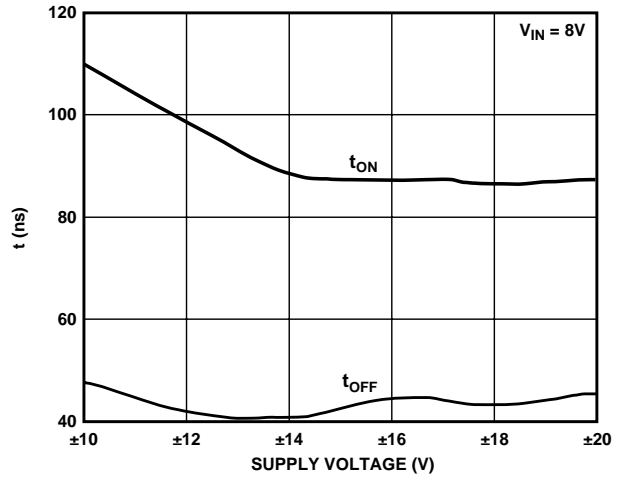


Figure 12. Switching Time vs. Bipolar Supply

05233-013

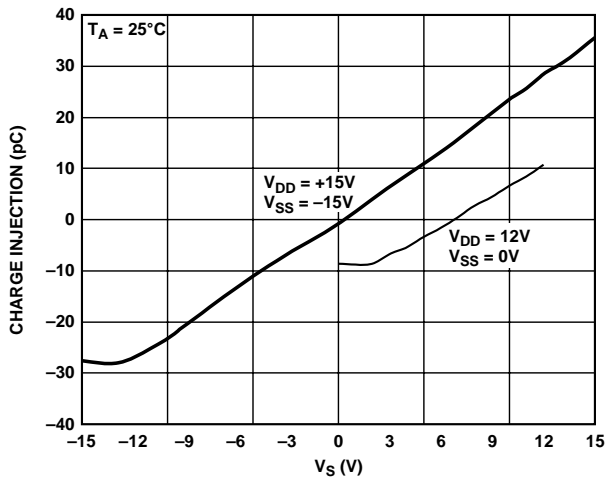


Figure 11. Charge Injection vs. Source Voltage

05233-012

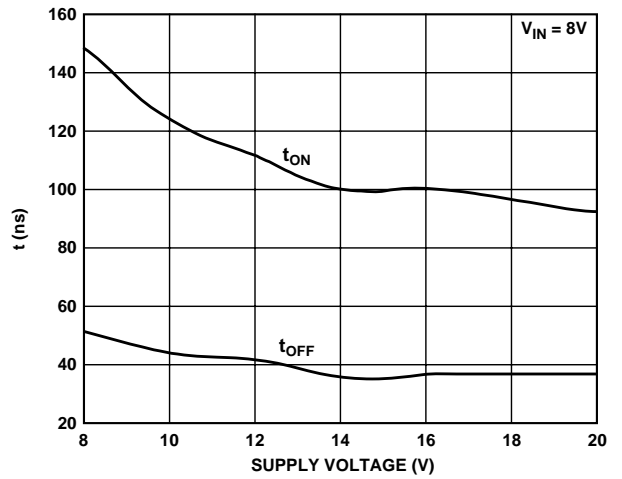


Figure 13. Switching Time vs. Single Supply

05233-014



## TEST CIRCUITS

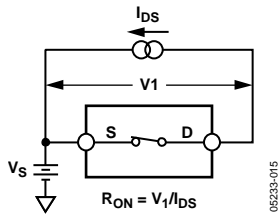


Figure 14. On Resistance

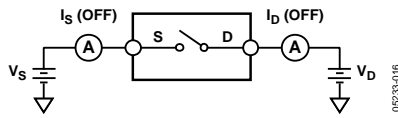


Figure 15. Off Leakage

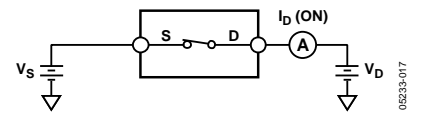


Figure 16. On Leakage

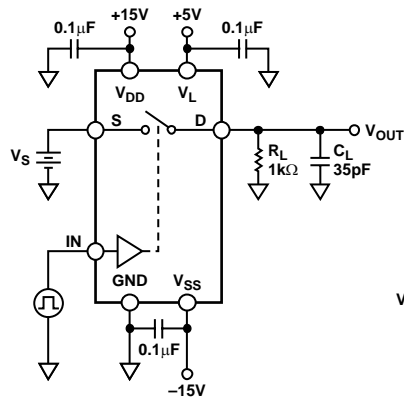


Figure 17. Switching Times

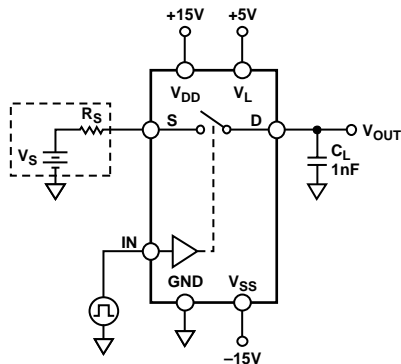
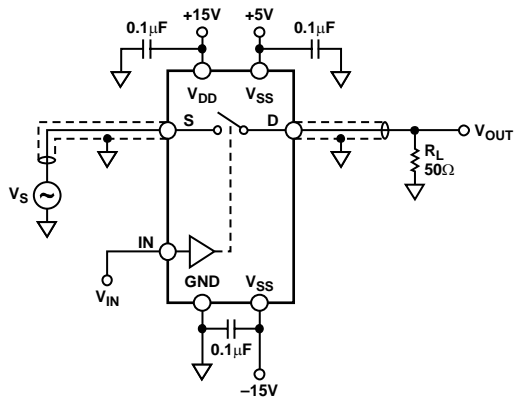


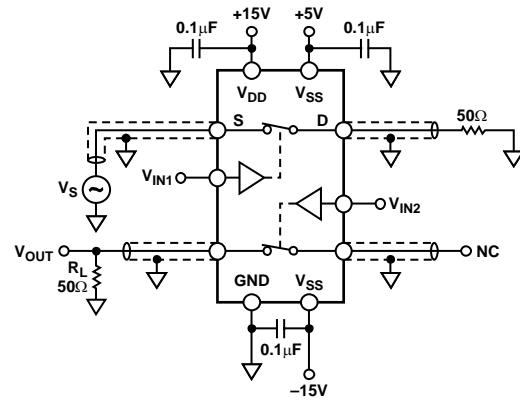
Figure 18. Charge Injection

# ADG441/ADG442/ADG444



06233-021

Figure 19. Off Isolation



06233-022

$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \times \text{LOG} |V_S/V_{OUT}|$$

Figure 20. Channel-to-Channel Crosstalk

## TERMINOLOGY

**R<sub>ON</sub>**

Ohmic resistance between D and S.

**R<sub>ON Match</sub>**

Difference between the R<sub>ON</sub> of any two channels.

**I<sub>S</sub> (OFF)**

Source leakage current with the switch OFF.

**I<sub>D</sub> (OFF)**

Drain leakage current with the switch OFF.

**I<sub>D</sub>, I<sub>S</sub> (ON)**

Channel leakage current with the switch ON.

**V<sub>D</sub> (V<sub>S</sub>)**

Analog voltage on Terminals D, S.

**C<sub>S</sub> (OFF)**

OFF switch source capacitance.

**C<sub>D</sub> (OFF)**

OFF switch drain capacitance.

**C<sub>D</sub>, C<sub>S</sub> (ON)**

ON switch capacitance.

**t<sub>ON</sub>**

Delay between applying the digital control input and the output switching on.

**t<sub>OFF</sub>**

Delay between applying the digital control input and the output switching off.

**t<sub>OPEN</sub>**

Break-before-make delay when switches are configured as a multiplexer.

**Crosstalk**

A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

**Off Isolation**

A measure of unwanted signal coupling through an OFF switch.

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

## TRENCH ISOLATION

In the ADG441A, ADG442A, and ADG444A, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward-biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

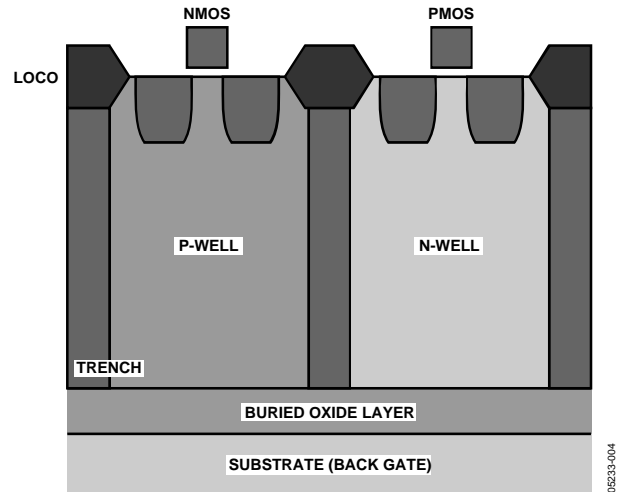
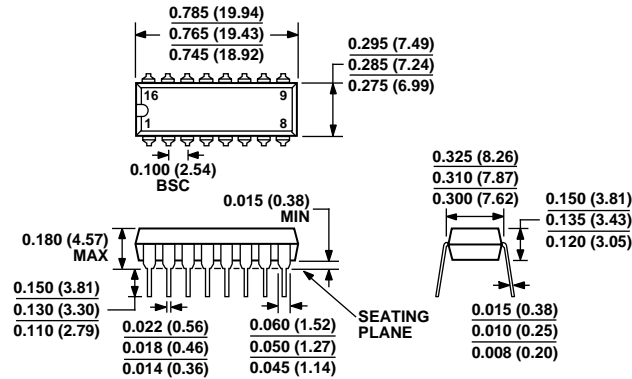


Figure 21. Trench Isolation

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-095AC  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 22. 16-Lead Plastic Dual In-Line Package [PDIP]  
 (N-16)  
 Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012AC  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 23. 16-Lead Standard Small Outline Package [SOIC]  
 (R-16)  
 Dimensions shown in millimeters and (inches)

# ADG441/ADG442/ADG444

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG441BN	-40°C to +85°C	16-Lead Plastic Dual In-Line Package (PDIP)	N-16
ADG441BR	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG441BR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG441BRZ <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG441BRZ-REEL <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG441BCHIPS		DIE	
ADG441ABCHIPS <sup>2</sup>		DIE	
ADG441ABN <sup>2</sup>	-40°C to +85°C	16-Lead Plastic Dual In-Line Package (PDIP)	N-16
ADG441ABR <sup>2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG441ABR-REEL <sup>2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG441ABRZ-REEL <sup>1,2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG442BN	-40°C to +85°C	16-Lead Plastic Dual In-Line Package (PDIP)	N-16
ADG442BR	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG442BR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG442BRZ <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG442BRZ-REEL <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG442ABN <sup>2</sup>	-40°C to +85°C	16-Lead Plastic Dual In-Line Package (PDIP)	N-16
ADG442ABR <sup>2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG442ABR-REEL <sup>2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG442ABRZ <sup>1,2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG442ABRZ-REEL <sup>1,2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG444BN	-40°C to +85°C	16-Lead Plastic Dual In-Line Package (PDIP)	N-16
ADG444BR	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG444BR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG444BRZ <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG444BRZ-REEL <sup>1</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG444ABN <sup>2</sup>	-40°C to +85°C	16-Lead Plastic Dual In-Line Package (PDIP)	N-16
ADG444ABR <sup>2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG444ABR-REEL <sup>2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG444ABRZ <sup>1,2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16
ADG444ABRZ-REEL <sup>1,2</sup>	-40°C to +85°C	16-Lead Standard Small Outline Package (SOIC)	R-16

<sup>1</sup> Z = Pb-free part.

<sup>2</sup> A = Trench isolated.

**NOTES**

**ADG441/ADG442/ADG444**

**NOTES**