Winbond
LPC I/O
W83637HF
W83637HG

Revision: 1.6 Date: 2006/03/22

Winbond Electronics Corp.

Revision History

	PAGES	DATES	VERSION	MAIN CONTENTS
1	N. A.	03/25/2001	0.50	No Released. For Winbond Internal use only.
2		08/09/2001	0.60	First published.
3		02/18/2002	0.70	Update Chapter 10. (Hardware Monitor Device)
4		08/28/2002	1.0	New update
5		09/27/2002	1.1	ADD Secure Digital Function Description
6	7 100~101	04/15/2003	1.2	ADD Block Digram ADD Chapter 4.1 Plug and Play Configuration
7	130~137	06/25/2003	1.3	Add Chapter 9 DC Specification
8	N.A.	11/23/2005	1.4	Add Pb-free package
9	N.A.	02/10/2006	1.5	Remove 5VSB H/W monitor sensor function.
10	Page.5	03/23/2006	1.6	Correct GPIO pins to 21-pin, not 40-pin

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Winbond Electronics Corp.

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1. GENERAL DESCRIPTION

W83637HF/HG is the new generation of Winbond's LPC I/O products. It is an evolving product from Winbond's most popular LPC I/O chip W83627HF/HG – which integrates the disk driver adapter, serial port (UART), keyboard controller (KBC), SIR, CIR, game port, MIDI port, hardware monitor, ACPI, On Now Wake-Up – plus additional new features: the Smart Card reader interface and Memory Stick ™ reader interface.

The Smart Card application is gaining more and more attention; it provides a very high-grade security and convenience in Internet transaction, banking, telephony, electronic payments, etc. W83637HF/HG supports a smart card reader interface featuring Smart wake-up function. This smart card reader interface fully meets the ISO7816 and PC/SC (Personal Computer/Smart Card Workgroup) standards. W83637HF/HG provides a minimum external components and lowest cost solution for smart card applications.

W83637HF/HG implements a standard Memory Stick™ reader interface. The Memory Stick™ has been a new mainstream media for storing and transferring data. It's ultra-small size and high storage capacity make it can be used in very wide variety products, including the Audio, Video and PC.

The disk drive adapter functions of W83637HF/HG include a floppy disk drive controller compatible with the industry standard 82077/765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83637HF/HG greatly reduces the number of components required for interfacing with floppy disk drives. W83637HF/HG supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s.

W83637HF/HG provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupts system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of 230k, 460k, or 921k bps, which support higher speed modems. In addition, W83637HF/HG provides IR functions: IrDA 1.0 (SIR for 1.152K bps) and TV remote IR (Consumer IR, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

W83637HF/HG supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

W83637HF/HG provides functions that comply with ACPI (*Advanced Configuration and Power Interface*), which includes support of legacy and ACPI power management through PME# or PSOUT# function pins. For OnNow keyboard Wake-Up, OnNow mouse Wake-Up, and OnNow CIR Wake-Up. W83637HF/HG also has auto power management to reduce the power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware are available with optional AMIKEY™ -2, Phoenix MultiKey/42™, or customer code.

W83637HF/HG provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O port. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function.

W83637HF/HG is made to fully comply with Microsoft PC98 and PC99 Hardware Design Guide. Moreover, W83637HF/HG is made to meet the specification of PC2001's requirement in the power management: ACPI 1.0/1.0b/2.0 and DPM (Device Power Management).

W83637HF/HG contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices. They are very important for an entertainment or consumer computer.

W83637HF/HG supports hardware status monitoring for personal computers. It can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and properly. Moreover, W83637HF/HG support the Smart Fan control system, including the "Thermal Cruise™" and "Speed Cruise™" functions. Smart Fan can make system more stable and user friendly.

2. FEATURES

General

- Meet LPC Spec. 1.01
- Support LDRQ#(LPC DMA), SERIRQ (serial IRQ)
- Compliant with Microsoft PC2000/PC2001 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD, and its Win95/98 driver

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  - --- 5, 6, 7 or 8-bit characters
  - --- Even, odd or no parity bit generation/detection
  - --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  - --- Loop-back controls for communications link fault isolation
  - --- Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate up to 921k bps for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Keyboard Controller

- 8042 based with optional F/W from AMIKKEY™-2, Phoenix MultiKey/42™ or customer code with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6 MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

Game Port

- Support two separate Joysticks
- Support every Joystick two axis (X, Y) and two button (A, B) controllers

MIDI Port

- The baud rate is 31.25 K baud
- 16-byte input FIFO
- 16-byte output FIFO

General Purpose I/O Ports

- 21 programmable general purpose I/O ports
- General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watching dog timer output, power LED output, infrared I/O pins, KBC control I/O pins, suspend LED output, RSMRST# signal, PWROK signal, STR (suspend to DRAM) function, VID control function,

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- CIR Wake-Up by programmable keys
- SMART Card Wake-up by SCPSNT
- On Now Wake-Up from all of the ACPI sleeping states (S1-S5)

Smart Card Reader Interface

- PC/SC T=0, T=1 compliant
- ISO7816 protocol compliant
- With 16-byte send/receive FIFOs
- Programmable baud generator
- Standard drivers for Windows 98 ME™, Windows 2000™

Memory Stick™ Reader Interface

- Meet SONY Memory Stick™ Specification Version 1.03

Hardware Monitor Functions

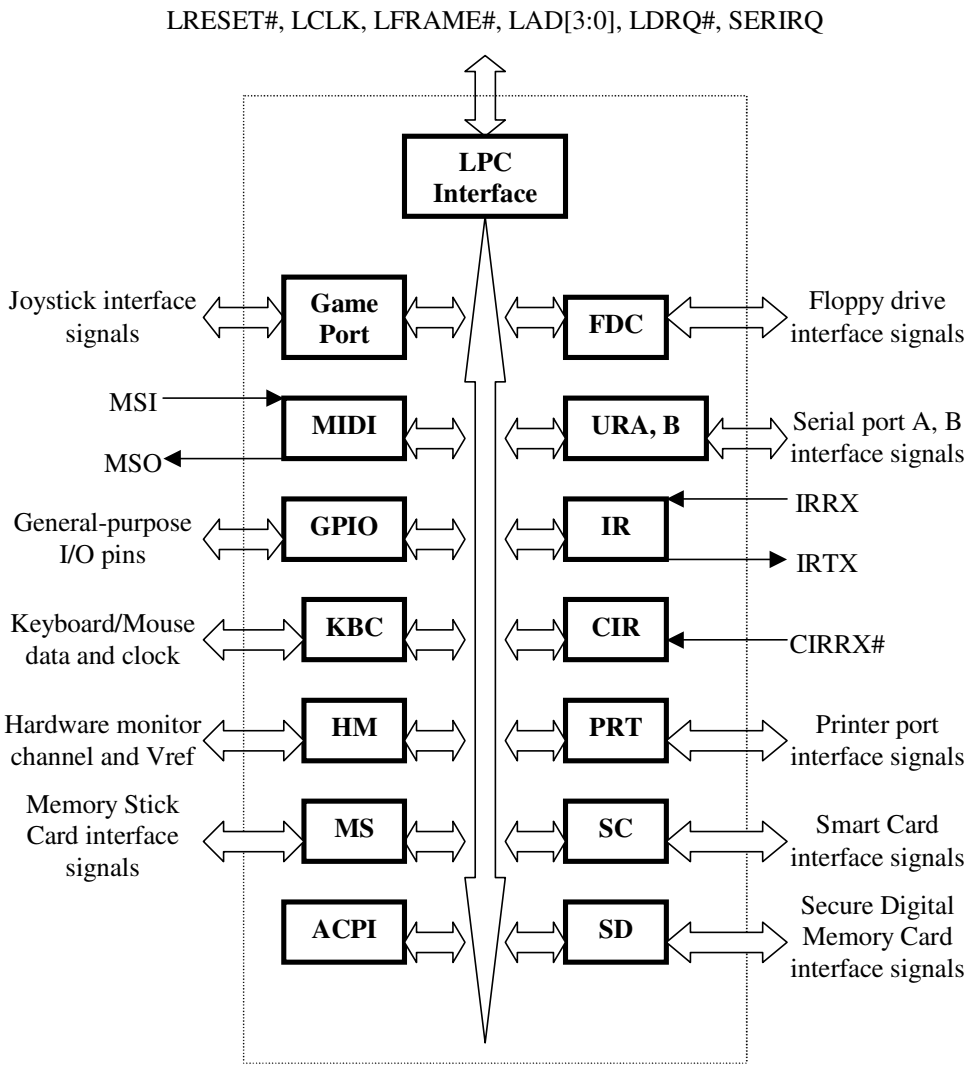
- Smart fan control system, support "Thermal Cruise™" and "Speed Cruise™"
- 3 thermal inputs from optionally remote thermistors or 2N3904 transistors or Pentium™ II/III/4 thermal diode output
- 3 positive voltage inputs (typical for +5V, +3.3V, Vcore)
- 1 intrinsic voltage monitoring (typical for Vbat)
- 3 fan speed monitoring inputs
- 3 fan speed control
- Build in Case open detection circuit
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points for all monitored items
- Over temperature indicate output

- Automatic Power On voltage detection Beep
- Issue SMI#, IRQ, OVT# to activate system protection
- Winbond Hardware Doctor™ Support
- Intel LDCM™ / Acer ADM™ compatible

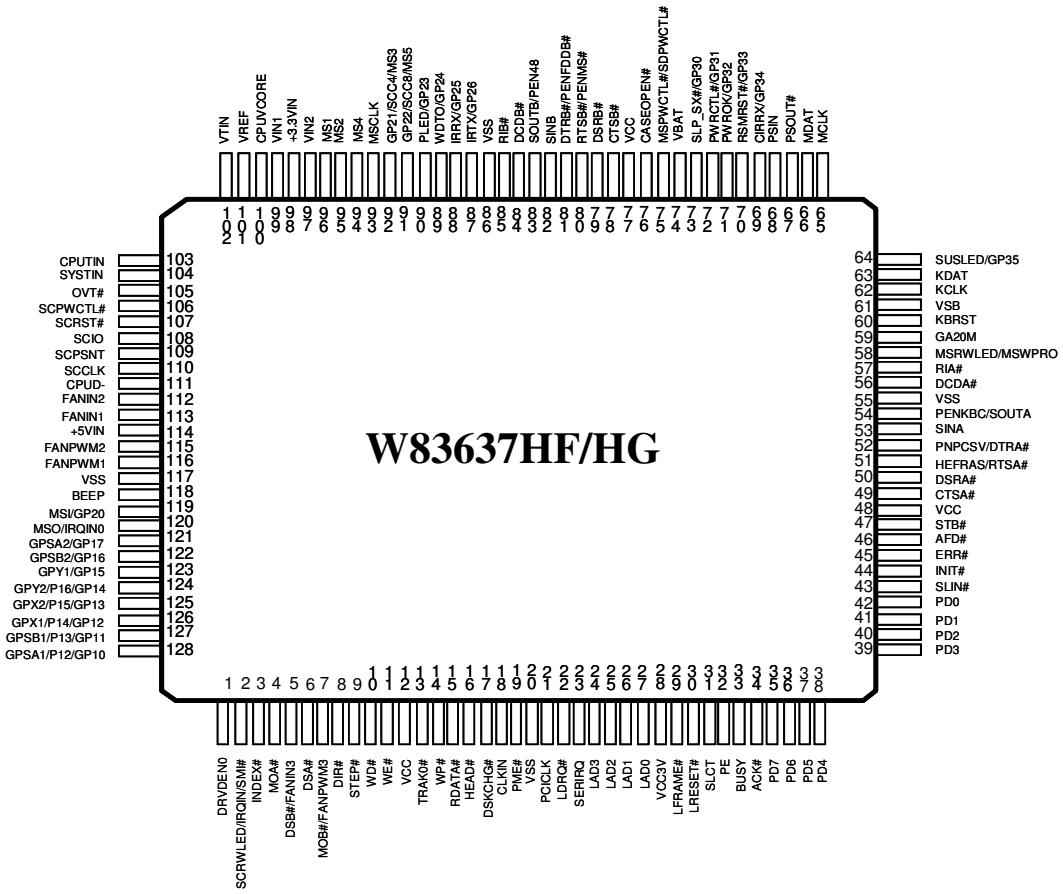
Package

- 128-pin PQFP

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



5. PIN DESCRIPTION

PIN DESCRIPTION	
I/O12t	TTL level bi-directional pin with 12 mA source-sink capability.
I/O24t	TTL level bi-directional pin with 24 mA source-sink capability.
I/O12ts	TTL level Schmitt-trigger bi-directional pin with 12 mA source-sink capability.
I/O24ts	TTL level Schmitt-trigger bi-directional pin with 24 mA source-sink capability.
I/OD12t	TTL level bi-directional pin and open drain output with 12 mA sink capability.
I/OD24t	TTL level bi-directional pin and open drain output with 24 mA sink capability.
I/OD12ts	TTL level Schmitt-trigger bi-directional pin and open drain output with 12 mA sink capability.
I/OD24ts	TTL level Schmitt-trigger bi-directional pin and open drain output with 24 mA sink capability.
I/OD12cs	CMOS level Schmitt-trigger bi-directional pin and open drain output with 12 mA sink capability.
I/OD16cs	CMOS level Schmitt-trigger bi-directional pin and open drain output with 16 mA sink capability.
I/OD12csd	CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open drain output with 12 mA sink capability.
I/OD12csu	CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open drain output with 12 mA sink capability.
O4t	TTL level output pin with 4 mA source-sink capability.
O12t	TTL level output pin with 12 mA source-sink capability.
O16t	TTL level output pin with 16 mA source-sink capability.
O24t	TTL level output pin with 24 mA source-sink capability.
O24ts	TTL level Schmitt-trigger output pin with 24 mA source-sink capability.
OD12t	TTL level open drain output pin with 12 mA sink capability.
OD24t	TTL level open drain output pin with 24 mA sink capability.
O8c	CMOS level output pin with 8 mA source-sink capability.
INt	TTL level input pin.
INts	TTL level Schmitt-trigger input pin.
INtu	TTL level input pin with internal pull up resistor.
INc	CMOS level input pin.
INcd	CMOS level input pin with internal pull down resistor.
INcsu	CMOS level Schmitt-trigger input pin with internal pull up resistor.

5.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
CLKIN	18	IN_t	System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input.
PME#	19	OD_{12t}	Generated PME event.
PCICLK	21	IN_{ts}	PCI clock input.
LDRQ#	22	O_{12t}	Encoded DMA Request signal.
SERIRQ	23	I/O_{12t}	Serial IRQ input/Output.
LAD[3:0]	24-27	I/O_{12t}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	29	IN_{ts}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	30	IN_{ts}	Reset signal. It can connect to PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24t}	Drive Density Select bit 0.
INDEX#	3	IN_{csu}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
MOA#	4	OD_{24t}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSB# FANIN3	5	OD_{24t} I/O_{24ts}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output. 0V to +5V amplitude fan tachometer input
DSA#	6	OD_{24t}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
MOB# FANPWM3	7	OD_{24t} OD_{24t}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output. Fan speed control. Use the Pulse Width Modulation (**PWM**) technical knowledge to control the Fan's RPM.
DIR#	8	OD_{24t}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24t}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
WD#	10	OD_{24t}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24t}	Write enable. An open drain output.
TRACK0#	13	IN_{csu}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
WP#	14	IN_{csu}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
RDATA#	15	IN_{csu}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
HEAD#	16	OD_{24t}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1

FDC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
DSKCHG#	17	IN_{csu}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

5.3 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT WE2#	31	IN_{ts} OD_{12t}	PRINTER MODE: An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: WE2# This pin is for Extension FDD B; its function is the same as the WE# pin of FDC. EXTENSION 2FDD MODE: WE2# This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC.
PE WD2#	32	IN_{ts} OD_{12t}	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: WD2# This pin is for Extension FDD B; its function is the same as the WD# pin of FDC. EXTENSION 2FDD MODE: WD2# This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC.
BUSY MOB2#	33	IN_{ts} OD_{12t}	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: MOB2# This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC. EXTENSION 2FDD MODE: MOB2# This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
ACK#	34	IN_{ts}	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSB2#		OD_{12t}	EXTENSION FDD MODE: DSB2# This pin is for the Extension FDD B; its functions is the same as the DSB# pin of FDC. EXTENSION 2FDD MODE: DSB2# This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC.
PD7	35	I/O_{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSA2#		OD_{12t}	EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: DSA2# This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.
PD6	36	I/O_{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
MOA2#		OD_{12t}	EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION. 2FDD MODE: MOA2# This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC.
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: This pin is a tri-state output.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD4	38	I/O_{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSKCHG2#		IN_{ts}	EXTENSION FDD MODE: DSKCHG2# This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: DSKCHG2# This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
PD3	39	I/O_{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
RDATA2#		IN_{ts}	EXTENSION FDD MODE: RDATA2# This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: RDATA2# This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC. It is pulled high internally.
PD2	40	I/O_{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
WP2#		IN_{ts}	EXTENSION FDD MODE: WP2# This pin is for Extension FDD B; its function is the same as the WP# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: WP2# This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC. It is pulled high internally.
PD1	41	I/O_{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
TRAK02#		IN_{ts}	EXTENSION FDD MODE: TRAK02# This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: TRAK02# This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
INDEX2#		IN_{ts}	EXTENSION FDD MODE: INDEX2# This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: INDEX2# This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.
SLIN#	43	OD_{12t}	PRINTER MODE: SLIN# Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
STEP2#		OD_{12t}	EXTENSION FDD MODE: STEP2# This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC. EXTENSION 2FDD MODE: STEP2# This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.
INIT#	44	OD_{12t}	PRINTER MODE: INIT# Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DIR2#		OD_{12t}	EXTENSION FDD MODE: DIR2# This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC. EXTENSION 2FDD MODE: DIR2# This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
ERR#	45	IN_{ts}	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
HEAD2#		OD_{12t}	EXTENSION FDD MODE: HEAD2# This pin is for Extension FDD B; its function is the same as the HEAD# pin of FDC. EXTENSION 2FDD MODE: HEAD2# This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.
AFD#	46	OD_{12t}	PRINTER MODE: AFD# An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DRVDEN0		OD_{12t}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC. EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.
STB#	47	OD_{12t}	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output EXTENSION 2FDD MODE: This pin is a tri-state output.

5.4 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA# CTSB#	49 78	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
DSRA# DSRB#	50 79	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
RTSA# HEFRAS	51	O_{8c} INcd	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address)
RTSB# ENGMTO	80	O_{8c} INcd	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Watch Dog Time-Out enable.
DTRA PNPCVS	52	O_{8c} INcd	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as PNPCVS, which provides the power-on value for CR24 bit 0 (PNPCVS). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, PRT, Game port and MIDI port)

Serial Port Interface, continued

SYMBOL	PIN	I/O	FUNCTION
DTRB#	81	O_{8c}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	53 82	IN_t	Serial Input. It is used to receive serial data through the communication link.
SOUTA PENKBC	54	O_{8c} IN_{cd}	UART A Serial Output. It is used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PENKBC, which provides the power-on value for CR24 bit 2 (PENKBC). A 4.7 kΩ resistor is recommended if intends to pull up. (enable KBC)
SOUTB PEN48	83	O_{8c} IN_{cd}	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up.
DCDA# DCDB#	56 84	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
RIA# RIB#	57 85	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

5.5 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
GA20M	59	O_{16t}	Gate A20 output. This pin is high after system reset. (KBC P21)
KBRST	60	O_{16t}	Keyboard reset. This pin is high after system reset. (KBC P20)
KCLK	62	I/OD_{16cs}	Keyboard Clock.
KDAT	63	I/OD_{16cs}	Keyboard Data.
MCLK	65	I/OD_{16cs}	PS2 Mouse Clock.
MDAT	66	I/OD_{16cs}	PS2 Mouse Data.

5.6 ACPI Interface

SYMBOL	PIN	I/O	FUNCTION
PSOUT#	67	OD_{12t}	Panel Switch Output. This signal is used for Wake-Up system from $S5_{cold}$ state. This pin is pulse output, active low.
PSIN	68	IN_{cd}	Panel Switch Input. This pin is high active with an internal pull down resistor.
VBAT	74	pvdf_rc1000_vbat	Battery voltage input.

5.7 Hardware Monitor Interface

SYMBOL	PIN	I/O	FUNCTION
CASEOPEN#	76	IN_t	CASE OPEN. An active low input from an external device when case is opened. This signal can be latched if pin VBAT is connect to battery, even W83637HF is power off.
VIN2	97	AIN	0V to 4.096V FSR Analog Inputs.
VIN1	99	AIN	0V to 4.096V FSR Analog Inputs.
CPUVCORE	100	AIN	0V to 4.096V FSR Analog Inputs.
VREF	101	AOUT	Reference Voltage for temperature maturation.
VTIN	102	AIN	Temperature sensor 3 inputs. It is used for temperature maturation.
CPUTIN	103	AIN	Temperature sensor 2 inputs. It is used for CPU1 temperature maturation.
SYSTIN	104	AIN	Temperature sensor 1 input. It is used for system temperature maturation.
OVT# SMI#	105	OD_{24t}	Over temperature Shutdown Output. It indicated the temperature is over temperature limit. System Management Interrupt channel input.
FANIN2 FANIN1	112 113	I/O_{12ts}	0V to +5V amplitude fan tachometer input.
FANPWM1 FANPWM2	116 115	O_{12t} (OD_{12t})	Fan speed control. Use the Pulse Width Modulation (PWM) technical knowledge to control the Fan's RPM.
BEEP	118	OD_{12t}	Beep function for hardware monitor. This pin is low after system reset.

5.8 Game Port & MIDI Port

SYMBOL	PIN	I/O	FUNCTION
MSI GP20	119	INtu I/OD_{12t}	MIDI serial data input .(Default) General purpose I/O port 2 bit 0.
MSO IRQIN0	120	O_{8c} INc	MIDI serial data output. (Default) Alternate Function input: Interrupt channel input.
GPSA2 GP17	121	Incsu I/OD_{12csu}	Active-low, Joystick I switch input 2. This pin has an internal pull-up resistor. (Default) General purpose I/O port 1 bit 7.
GPSB2 GP16	122	Incsu I/OD_{12csu}	Active-low, Joystick II switch input 2. This pin has an internal pull-up resistor. (Default) General purpose I/O port 1 bit 6.
GPY1 GP15	123	I/OD_{12csd} I/OD_{12cs}	Joystick I timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default) General purpose I/O port 1 bit 5.
GPY2 GP14 P16	124	I/OD_{12csd} I/OD_{12cs}	Joystick II timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default) General purpose I/O port 1 bit 4. Alternate Function Output: KBC P16 I/O port.
GPX2 GP13 P15	125	I/OD_{12csd} I/OD_{12cs}	Joystick II timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default) General purpose I/O port 1 bit 3. Alternate Function Output: KBC P15 I/O port.
GPX1 GP12 P14	126	I/OD_{12csd} I/OD_{12cs}	Joystick I timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default) General purpose I/O port 1 bit 2. Alternate Function Output: KBC P14 I/O port.
GPSB1 GP11 P13	127	Incsu I/OD_{12csu}	Active-low, Joystick II switch input 1. (Default) General purpose I/O port 1 bit 1. Alternate Function Output: KBC P13 I/O port.
GPSA1 GP10 P12	128	Incsu I/OD_{12csu}	Active-low, Joystick I switch input 1. (Default) General purpose I/O port 1 bit 0. Alternate Function Output: KBC P12 I/O port.

5.9 Card Reader Interface

5.9.1 Smart Card Interface

SYMBOL	PIN	I/O	FUNCTION
SCRWLED SMI# IRQIN GP27	2	OD_{24t} OD_{24t} IN_t I/OD_{24t}	This pin outputs an oscillating clock signal of various frequencies depending on traffic of Smart Card interface. System Management Interrupt channel input. General purpose I/O port 3 bit 6.
SCPWCTL#	106	O_{24t}	Smart Card interface power control signal.
SCRST#	107	O_{24t}	Smart Card interface reset output
SCIO	108	I/O_{24t}	Smart Card interface data I/O channel.
SCPSNT	109	IN_{ts}	Smart Card interface card present detection Schmitt-trigger input.
SCCLK	110	$O4_{t(O24t)}$	Smart Card interface clock output

5.9.2 MS/SD Card Interface

SYMBOL	PIN	I/O	FUNCTION
MSLED SDLED SDWPRO	58	O_{24t} IN_t	This pin outputs an oscillating clock signal of various frequencies depending on traffic of secondary Memory Stick interface; SD Card Write Protect Detect Pin.
MSPWCTL# SDPWCTL#	75	O_{24t}	MS Card power control SD Card power control
MS5 SD5 SCC8 GP22	91	I/O_{24ts} I/OD_{24ts}	MS function SD Data Line 2(DAT2) Smart Card C8 PIN. General purpose I/O port 2 bit 2.
MS3 SD3 SCC4 GP21	92	I/O_{24ts} I/OD_{24ts}	MS function SD Data Line 0(DAT0) Smart Card C4 PIN General purpose I/O port 2 bit 1
MSCLK SDCLK	93	O_{24ts}	MS card CLK output SD Card CLK output
MS4 SD4	94	I/O_{24ts}	MS function SD Data Line 1(DAT 1)
MS2 SD2	95	I/O_{24ts}	MS function SD Command Line(CMD)
MS1 SD1	96	I/O_{24ts}	MS function SD Data Line 3(CD/DAT3)

5.10 General Purpose I/O Port

5.10.1 General Purpose I/O Port 1 (Power source is Vcc)

see 1.8 Game Port

5.10.2 General Purpose I/O Port 2 (Power source is Vcc)

SYMBOL	PIN	I/O	FUNCTION
IRTX GP26	87	O_{12t} I/OD_{12t}	General purpose I/O port 2 bit 6. Alternate Function Output: Infrared Transmitter Output. (Default)
IRRX GP25	88	IN_{ts} I/OD_{12ts}	General purpose I/O port 2 bit 5. Alternate Function Input: Infrared Receiver input. (Default)
WDTO GP24	89	O_{12t} I/OD_{12t}	General purpose I/O port 2 bit 4. Watch dog timer output. (Default)
PLED GP23	90	O_{24t} I/OD_{24t}	General purpose I/O port 2 bit 3. Power LED output, this signal is low after system reset. (Default)
GP22	91	I/OD_{24t}	General purpose I/O port 2 bit 2.
GP21	92	I/OD_{24t}	General purpose I/O port 2 bit 1.

5.10.3 General Purpose I/O Port 3 (Power source is VSB)

SYMBOL	PIN	I/O	FUNCTION
SUSLED GP35	64	O_{24t} I/OD_{24t}	Suspend LED output, it can program to flash when suspend state. This function can work without VCC. (Default) General purpose I/O port 3 bit 5
CIRRX SDDET GP34	69	IN_{ts} I/OD_{12ts}	Consumer IR receiving input. This pin can Wake-Up system from S5 (Default) SD Card External Card Detect. General purpose I/O port 3 bit 4
RSMRST# GP33	70	OD_{12t} I/OD_{12t}	This pin generates the RSMRST signal while the VSB come in. (Default) General purpose I/O port 3 bit 3
PWROK GP32	71	OD_{12t} I/OD_{12t}	This pin generates the PWROK signal while the VCC come in. (Default) General purpose I/O port 3 bit 2.
PWRCTL# GP31	72	O_{12t} I/OD_{12t}	This pin generates the PWRCTL# signal while the power failure. (Default) General purpose I/O port 3 bit 1.
SLP_SX# GP30	73	IN_{ts} I/OD_{12ts}	Chip Set sleep state input. General purpose I/O port 3 bit 0.

5.11 Power Pins

SYMBOL	PIN	FUNCTION
VCC	12, 48, 77	+5V power supply for the digital circuitry.
VSB	61	+5V stand-by power supply for the digital circuitry.
VCC3V	28	+3.3V power supply for driving 3V on host interface.
+3.3VIN	98	+3.3V power supply and to be monitored.
+5VIN	114	Analog VCC input. Internally supplier to all analog circuitry.
CPUD-	111	Internally connected to all analog circuitry. The ground reference for all analog inputs..
VSS	20, 55, 86, 117	Ground.

6. HARDWARE MONITOR

6.1 General Description

W83637HF/HG can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stable and properly. W83637HF/HG provides LPC interface to access hardware.

An 8-bit analog-to-digital converter (ADC) was built inside W83637HF/HG. W83637HF/HG can simultaneously monitor 5 analog voltage inputs (addition monitor 3.3V & 5V VDD power), 3 fan tachometer inputs, 3 remote temperature, one case-open detection signal. The remote temperature sensing can be performed by thermistors, or 2N3904 NPN-type transistors, or directly from Intel™ Deschutes CPU thermal diode output. Also the W83637HF/HG provides: 3 PWM (pulse width modulation) outputs for the fan speed control; beep tone output for warning; SMI# (through serial IRQ or OVT pin), OVT# signals for system protection events.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time. And a pop-up warning can be also activated when the monitored item was out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, or Intel™ LDCM (LanDesk Client Management), or other management application software. Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and to activate one programmable and maskable interrupts. An optional beep tone could be used as warning signal when the monitored parameters are out of the preset range.

6.2 Access Interface

W83637HF/HG provides two interface for microprocessor to read/write hardware monitor internal registers.

6.2.1 LPC interface

The first interface uses LPC Bus to access which the ports of low byte (bit2~bit0) are defined in the port 5h and 6h. The other higher bits of these ports are set by W83637HF/HG itself. The general decoded address is set to port 295h and port 296h. These two ports are described as following:

Port 295h: Index port.

Port 296h: Data port.

The register structure is showed as the Figure 6.1

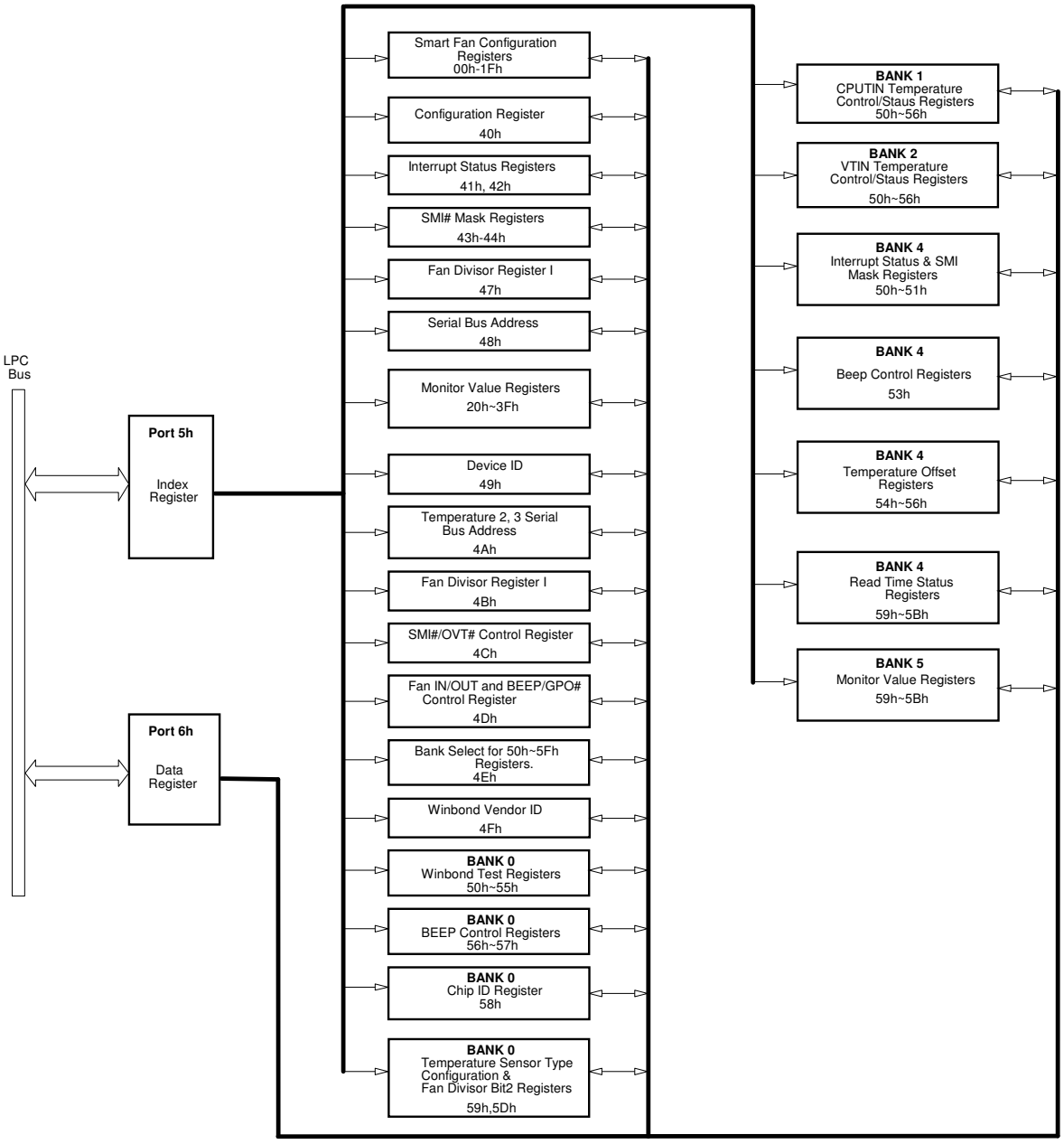


Figure 6.1: LPC interface access diagram

6.3 Analog Inputs

The maximum input voltage of the analog pin is 4.096V because the 8-bit ADC has a 16mv LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU V-core voltage, +3.3V, battery(pin 74) can directly connected to these analog inputs. The +12V voltage inputs should be reduced a factor with external resistors so as to obtain the input range. As Figure 6.2 shows.

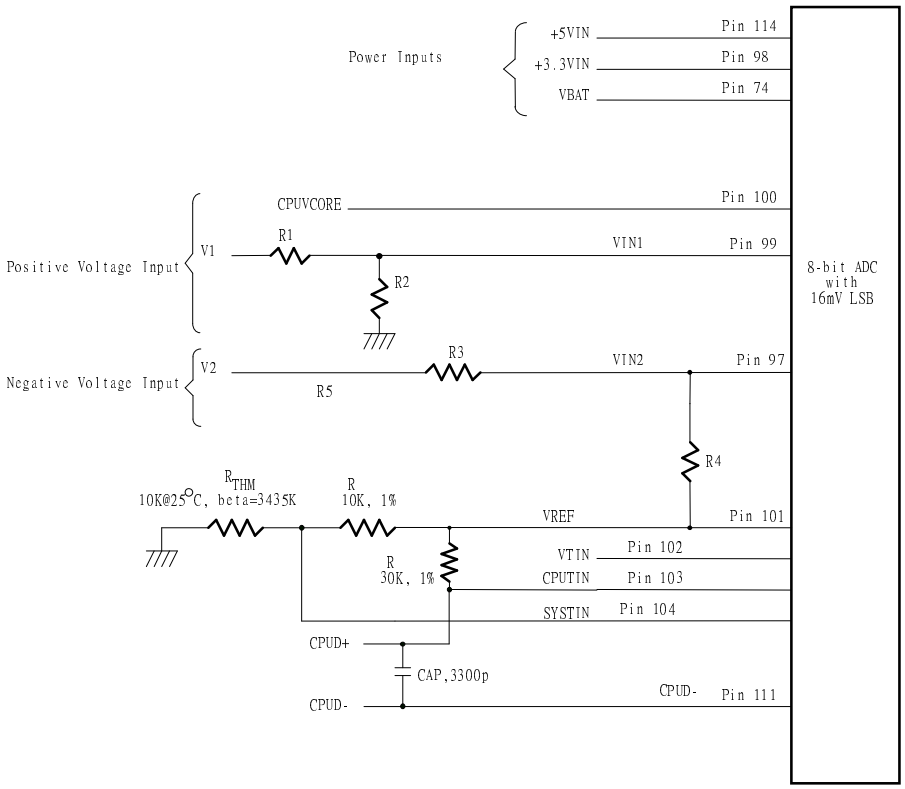


Figure. 6.2

6.3.1 Monitor over 4.096V voltage

The +12V input voltage can be expressed as following equation.

$$VIN1 = V_1 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage V1 is 12V. The node voltage of VIN1 can be subject to less than 4.096V for the maximun input range of the 8-bit ADC.

The -12V input voltage can be expressed as following equation.

$$VIN2 = (V_2 - 3.6) \times \frac{R_4}{R3 + R4} + 3.6, where V_2 = -12$$

The value of R3 and R4 can be selected to 56K Ohms and 232K Ohms, respectively, when the input voltage V2 is -12V. The node voltage of VIN2 can be subject to less than 4.096V for the maximun input range of the 8-bit ADC.

The Pin 114 is connected to the power supply VCC with +5V. There are two functions in this pin with 5V. The first function is to supply internal analog power in the W83637HF and the second function is that this voltage with 5V is connected to internal serial resistors to monitor the +5V voltage. The W83637HF internal two serial resistors are 34K ohms and 51K ohms so that input voltage to ADC is 3V which is less than 4.096V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{51K\Omega}{51K\Omega + 34K\Omega} \cong 3V$$

where VCC is set to 5V.

6.3.2 CPUVCORE voltage detection method

W83637HF provides two detection methods for CPUVCORE(pin100).

(1). VRM8 method:

The LSB of this mode is 16mV. This means that the detected voltage equals to the reading of this voltage register multiplies 16mV. The formula is as the following:

Detected Voltage = $\mathrm{Re}ading * 0.016$ V

(2). VRM9 method:

The LSB of this mode is 4.88mV which is especially designed the low voltage CPU. The formula is as the following:

Detected Voltage = $\mathrm{Re}ading * 0.00488 + 0.7$ V

6.3.3 Temperature Measurement Machine

The temperature data format is 8-bit two's-complement for sensor SYSTIN and 9-bit two's-complement for sensor CPUTIN and VTIN. The 8-bit temperature data can be obtained by reading the CR[27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the Bank1/Bank2 CR[50h] and the LSB from the Bank1/Bank2 CR[51h] bit 7. The format of the temperature data is show in Table 1.

Temperature	8-Bit Digital Output		9-Bit Digital Output	
	8-Bit Binary	8-Bit Hex	9-Bit Binary	9-Bit Hex
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

Table 1

6.3.3.1 Monitor temperature from thermistor:

The W83637HF can connect three thermistors to measure three different envirment temperature. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 6.2, the themistor is connected by a serial resistor with 10K Ohms, then connect to VREF (Pin 101).

6.3.3.2 Monitor temperature from Pentium II™/Pentium III™ thermal diode or bipolar transistor2N3904

The W83637HF can alternate the thermistor to Pentium II™/Pentium III™ thermal diode interface or transistor 2N3904 and the circuit connection is shown as Figure 6.3. The pin of Pentium II™/Pentium III™ D- is connected to pin 111(CPUD-) and the pin D+ is connected to temperature sensor pin in the W83637HF. The resistor R=30K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=3300pF should be added to filter the high frequency noise. The transistor 2N3904 should be connected to a form with a diode, that is, the Base (B) and Collector (C) in the 2N3904 should be tied together to act as a thermal diode.

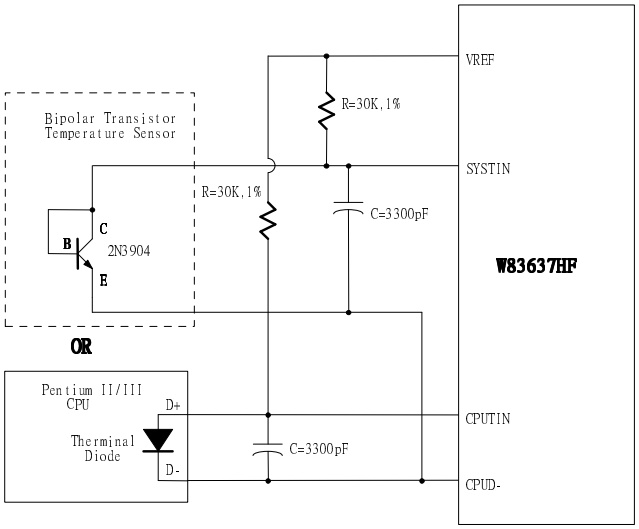


Figure 6.3

6.4 FAN Speed Count and FAN Speed Control

6.4.1 Fan speed count

Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as Figure 6.4.

Determine the fan counter according to:

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

In other words, the fan speed counter has been read from register CR28 or CR29 or CR2A, the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR47.bit7~4, CR4B.bit7~6, and Bank0 CR5D.bit5~7 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, PRM, and count.

Divisor	Nominal PRM	Time per Revolution	Counts	70% RPM	Time for 70%
1	8800	6.82 ms	*153*	6160	9.84 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms
128	68	872.64 ms	*153*	48	1246.72 ms

Table 2

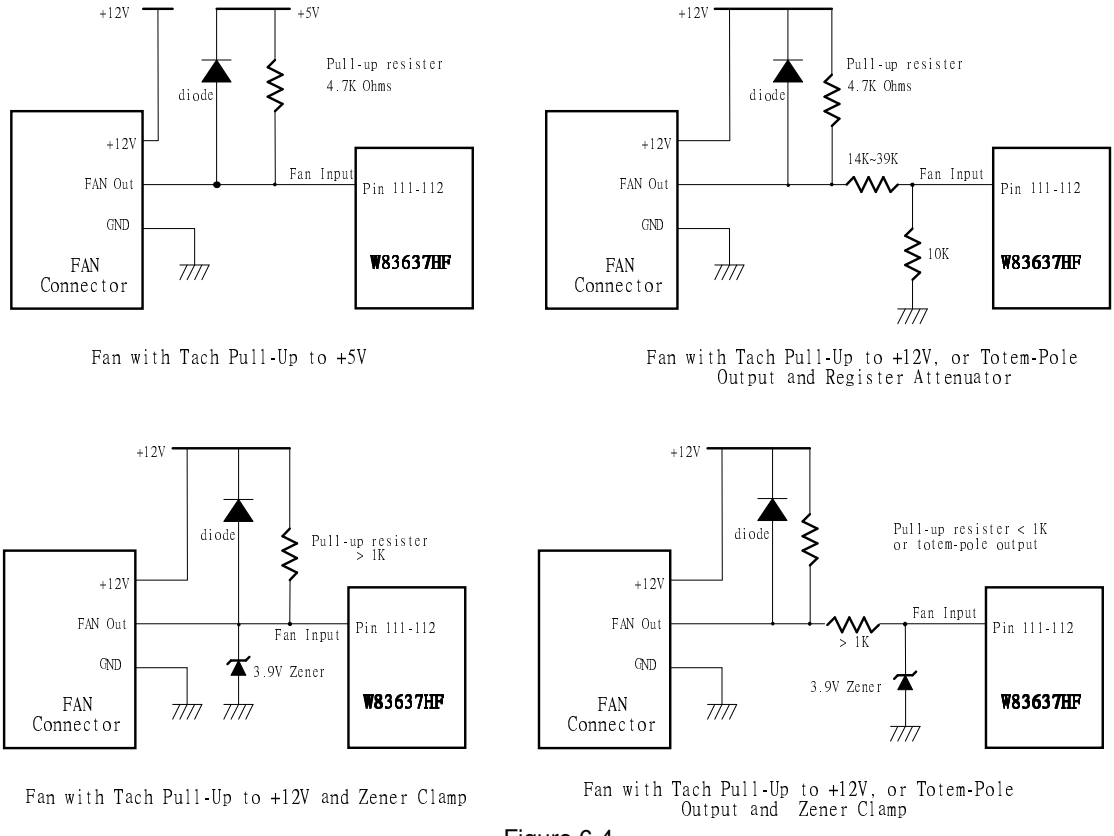


Figure 6.4

6.4.2 Fan speed control

The W83637HF provides maximum 3 sets for fan PWM speed control. The duty cycle of PWM can be programmed by a 8-bit registers which are defined in the Bank0 Index 01h, Index 03h and Index 11h. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty} - \text{cycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The PWM clock frequency also can be program and defined in the Bank0 Index 00h, Index 02h and Index 10h. The application circuit is shown as follows.

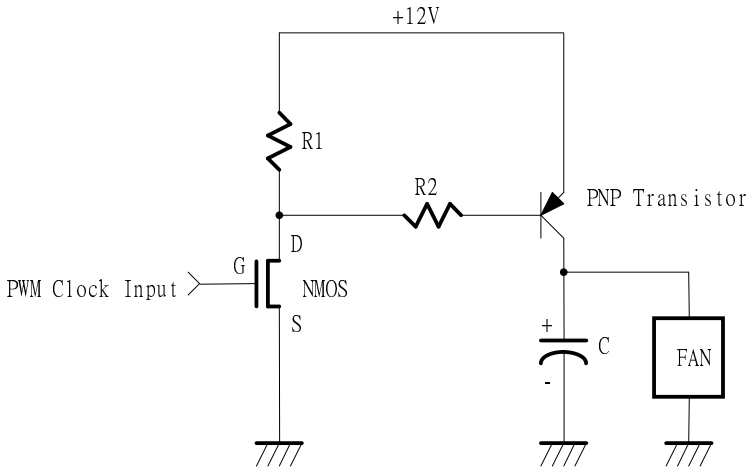


Figure 6.5

6.5 Smart Fan Control

Smart Fan Control provides two mechanisms. One is Thermal Cruise mode and the other is Fan Speed Cruise mode.

6.5.1 Thermal Cruise mode

There are maximum 3 pairs of Temperature/FanPWM control at this mode: SYSTIN with FANPWM1, CPUTIN with FANPWM2, VTIN with FANPWM3. At this mode, W83637HF provides the Smart Fan system which can control the fan speed automatically depend on current temperature to keep it with in a specific range. At first a wanted temperature and interval must be set (ex. 55 °C ±3 °C) by BIOS, as long as the real temperature remains below the setting value, the fan will be off. Once the temperature exceeds the setting high limit temperature (58°C), the fan will be turned on with a specific speed set by BIOS (ex: 80% duty cycle) and automatically controlled its PWM duty cycle with the temperature varying. Three conditions may occur:

(1) If the temperature still exceeds the high limit (ex: 58°C), PWM duty cycle will increase slowly. If the fan has been operating in its fully speed but the temperature still exceeds the high limit(ex: 58°C), a warning message will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target area(ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), PWM duty cycle will decrease slowly to 0 until the temperature exceeds the low limit.

Figure 6.6 and 6.7 give the illustration for Thermal Cruise Mode.

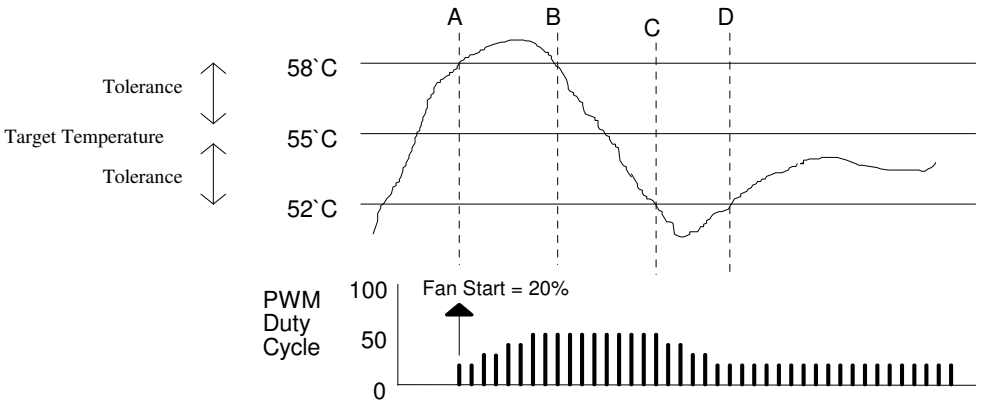


Figure 6.6

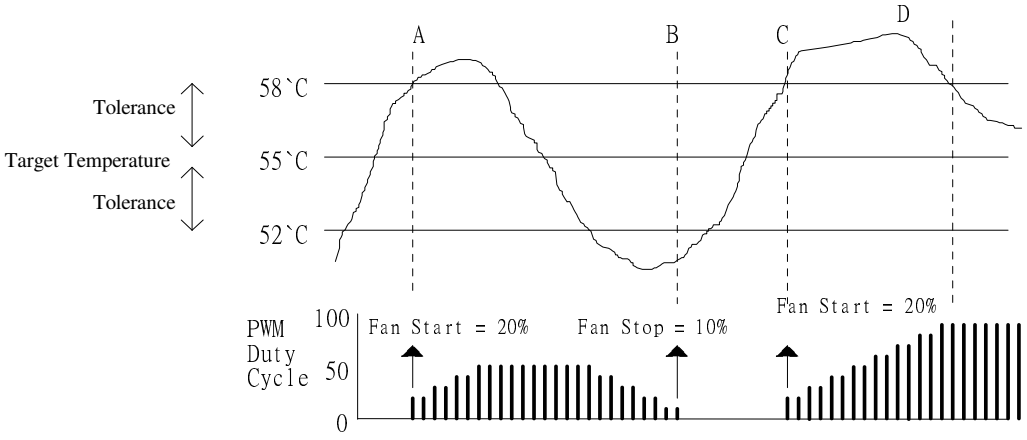


Figure 6.7

One more protection is provided that duty cycle will not be decreased to 0 in the above (3) situation in order to keep the fans running with a minimum speed. By setting CR[12h] bit3-5 to 1, FAN PWM duty cycle will be decreased to the “Stop Duty Cycle” which are defined at CR[08h],CR[09h] and CR[17h].

6.5.2 Fan Speed Cruise mode

There are 3 pairs of FanSpeed/FanPWM control at this mode: FANIN1 with FANPWM1, FANIN2 with FANPWM2, FANIN3 with FANPWM3.At this mode, W83637HF provides the Smart Fan system which can control the fan speed automatically depend on current fan spesed to keep it with in a specific range. A wanted fan speed count and interval must be set (ex. 160 ±10) by BIOS. As long as the fan speed count is the specific range, PWM duty will keep the current value. If current fan speed count is higher than the high limit (ex. 160+10), PWM duty will be increased to keep the count less than the high limit. Otherwise, if current fan speed is less than the low limit(ex. 160-10), PWM duty will be decreased to keep the count higher than the low limit. See Figure 6.8 example.

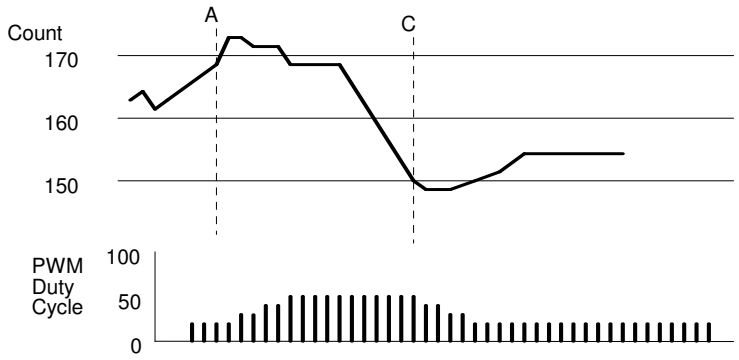


Figure 6.8

6.5.3 Manual Control Mode

Smart Fan control system can be disabled and the fan speed control algorithem can be progrmmed by BIOS or application software. The programming method is just as section 6.4.2.

6.6 SMI# Interrupt Mode

The SMI#/OVT# pin (pin105) is a multi-function pin. The function is selected at Configuration Register CR[28h] bit 6.

6.6.1 Voltage SMI# mode

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 6.9)

6.6.2 Fan SMI# mode

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit, will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 6.10)

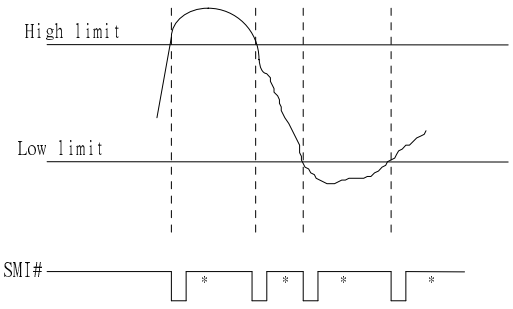
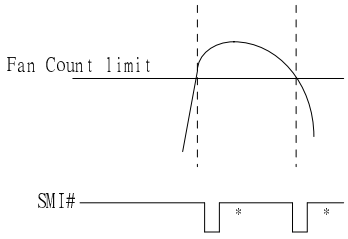


Figure 6.9



*Interrupt Reset when Interrupt Status Registers are read

Figure 6.10

6.6.3 The W83637HF temperature sensor 1(SYSTIN) SMI# interrupt has two modes

(1) Comparator Interrupt Mode

Setting the T_{HYST} (Temperature Hysteresis) limit to 127°C will set temperature sensor 1 SMI# to the Comparator Interrupt Mode. Temperature exceeds T_O (Over Temperature) Limit causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_O, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_O. (Figure 6.11)

Setting the T_{HYST} lower than T_O will set temperature sensor 1 SMI# to the Interrupt Mode. The following are two kinds of interrupt modes, which are selected by Index 4Ch bit5:

(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 6.12)

(3) One-Time Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below $T_{HYST,}$ an interrupt will not occur again until the temperature exceeding T_O. (Figure .6.13)

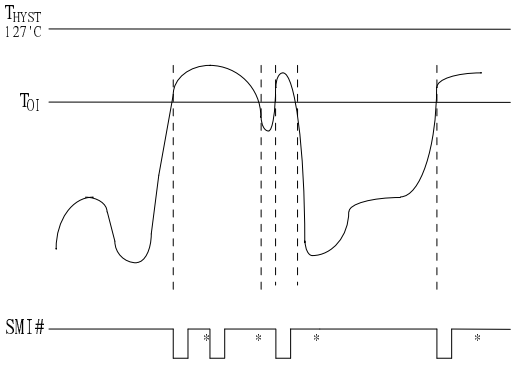


Figure 6.11

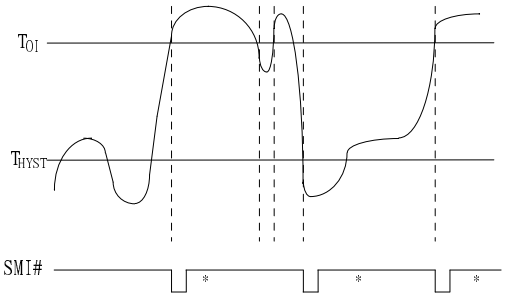
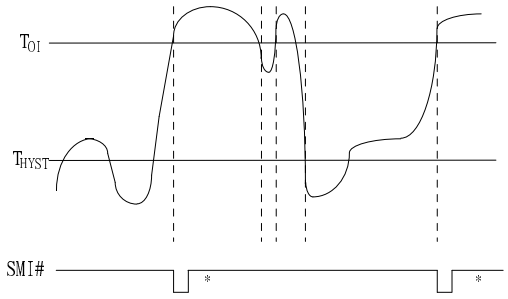


Figure 6.12

*Interrupt Reset when Interrupt Status Registers are read



*Interrupt Reset when Interrupt Status Registers are read

Figure 6.13

6.6.4 The W83637HF temperature sensor 2(CPUTIN) and sensor 3(VTIN) SMI# interrupt has two modes and it is programmed at CR[4Ch] bit 6.

(1) Comparator Interrupt Mode

Temperature exceeding T_O causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}. (Figure 6.14)

(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 6.15)

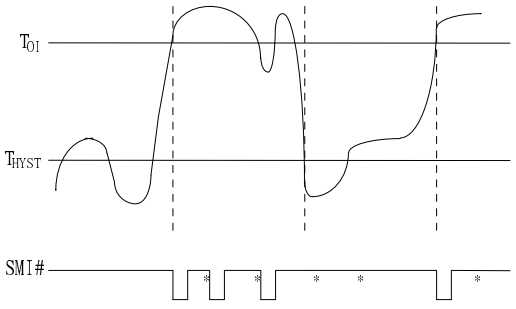
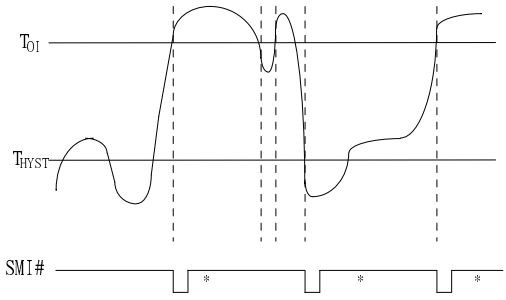


Figure 6.14



*Interrupt Reset when Interrupt Status Registers are read

Figure 6.15

6.7 OVT# Interrupt Mode

The SMI#/OVT# pin (pin105) is a multi-function pin. The function is selected at Configuration Register CR[28h] bit 6. The OVT# mode selection bits are at Bank0 Index18h bit4, Bank1 Index52h bit1and Bank2 Index52h bit1.

(1) Comparator Mode

Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. (Figure 6.16)

(2) Interrupt Mode

Temperature exceeding T_O causes the OVT# output activated indefinitely until reset by reading temperature sensor registers. Temperature exceeding T_O, then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor2 or sensor 3 registers. Once the OVT# is activated by exceeding T_O, then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again.(Figure 6.16)

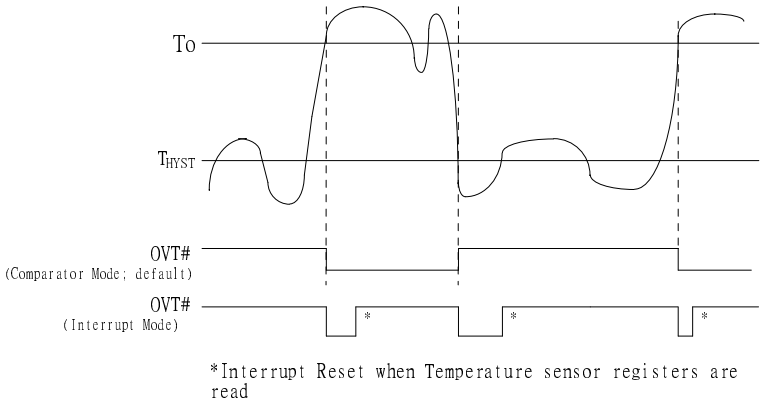


Figure 6.16

6.8 Registers and RAM

Address Port and Data Port are set in the register CR60 and CR61 of Device B which is Hardware Monitor Device. The value in CR60 is high byte and that in CR61 is low byte. For example, setting CR60 to 02 and CR61 to 90 cause the Address Port to be 0x295 and Data Port to be 0x296.

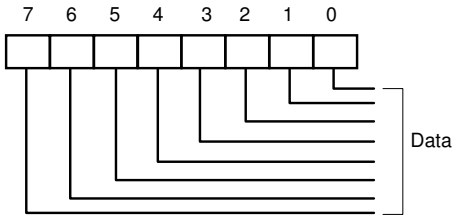
Address Port (Port x5h)

Address Port: Port x5h

Power on Default Value 00h

Attribute: Bit 6:0 Read/write , Bit 7: Reserved

Size: 8 bits



Bit7: Reserved

Bit 6-0: Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Address Pointer (Power On default 00h)						
(Power On default 0)	A6	A5	A4	A3	A2	A1	A0

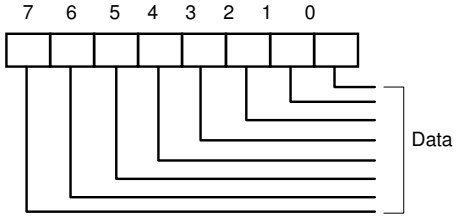
Data Port (Port x6h)

Data Port: Port x6h

Power on Default Value 00h

Attribute: Read/write

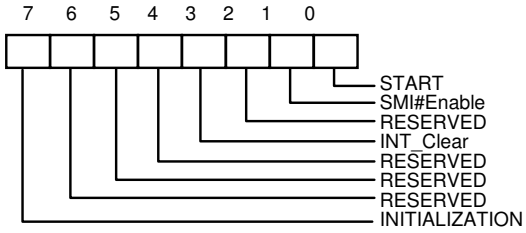
Size: 8 bits



Bit 7-0: Data to be read from or to be written to RAM and Register.

Configuration Register — Index 40h

Register Location: 40h
Power on Default Value 01h
Attribute: Read/write
Size: 8 bits



Bit 7: A one restores power on default value to all registers except the Serial Bus Address register. This bit clears itself since the power on default is zero.

Bit 6: Reserced

Bit 5: Reserved

Bit 4: Reserved

Bit 3: A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.

Bit 2: Reserved

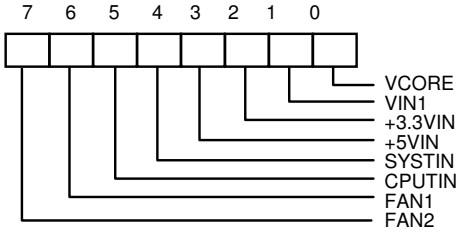
Bit 1: A one enables the SMI# Interrupt output.

Bit 0: A one enables startup of monitoring operations, a zero puts the part in standby mode.

Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

Interrupt Status Register 1— Index 41h

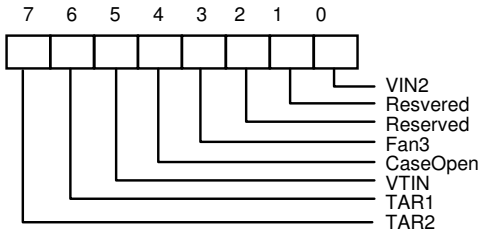
Register Location:	41h
Power on Default Value	00h
Attribute:	Read Only
Size:	8 bits



Bit 7: A one indicates the fan count limit of FAN2 has been exceeded.
Bit 6: A one indicates the fan count limit of FAN1 has been exceeded.
Bit 5: A one indicates a High limit of CPUTIN temperature has been exceeded.
Bit 4: A one indicates a High limit of SYSTIN temperature has been exceeded .
Bit 3: A one indicates a High or Low limit of +5VIN has been exceeded.
Bit 2: A one indicates a High or Low limit of +3.3VIN has been exceeded.
Bit 1: A one indicates a High or Low limit of VIN1 has been exceeded.
Bit 0: A one indicates a High or Low limit of VCORE has been exceeded.

Interrupt Status Register 2 — Index 42h

Register Location:	42h
Power on Default Value	00h
Attribute:	Read Only
Size:	8 bits



Bit 7: A one indicates that the CPUTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™.

Bit 6: A one indicates that the SYSTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™.

Bit 5: .A one indicates a High or Low limit of VTIN temperature has been exceeded.

Bit 4: A one indicates case has been opened.

Bit 3: A one indicates a High or Low limit of FAN3 has been exceeded .

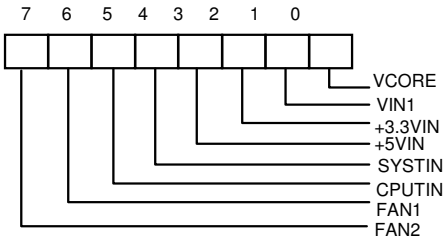
Bit 2: Reserved.

Bit 1: Reserved.

Bit 0: A one indicates a High or Low limit of VIN2 has been exceeded.

SMI# Mask Register 1 — Index 43h

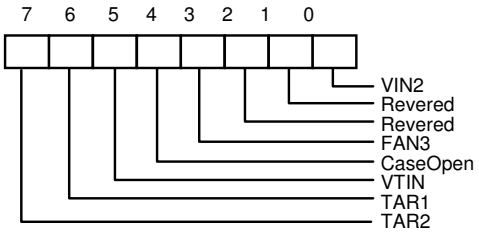
Register Location:	43h
Power on Default Value	FFh
Attribute:	Read/Write
Size:	8 bits



Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

SMI# Mask Register 2 — Index 44h

Register Location: 44h
Power on Default Value FFh
Attribute: Read/Write
Size: 8 bits

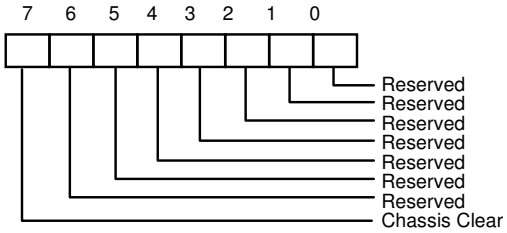


Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Reserved Register — Index 45h

Chassis Clear Register -- Index 46h

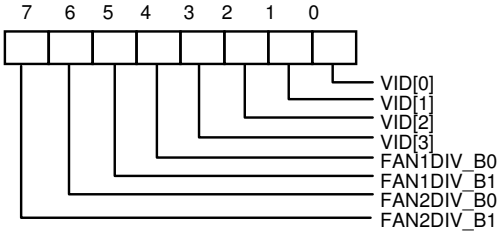
Register Location: 46h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: Set 1, clear case open event. This bit self clears after clearing case open event.
Bit 6-0:Reserved. This bit should be set to 0.

Fan Divisor Register I — Index 47h

Register Location: 47h
Power on Default Value: 5Fh
Attribute: Read/Write
Size: 8 bits



Bit 7-6: FAN2 Divisor bit1:0 .

Bit 5-4: FAN1 Divisor bit1:0.

Bit 3-0: CPU Vcore ID [3:0]. The VID value is written by BIOS if the VID value can be detected. After the VID value is written, Software/AP can use this information to identify the Vcore voltage of the CPU.

Note: Please refer to Bank0 CR[5Dh] , Fan divisor table.

Value RAM — Index 20h- 3Fh

Address A6-A0	Description
20h	VCORE reading
21h	VIN1 reading
22h	+3.3VIN reading
23h	+5VIN reading
24h	VIN2 reading
25h	Reserved
26h	Reserved
27h	SYSTIN temperature sensor reading
28h	FAN1 reading **Note:** This location stores the number of counts of the internal clock per revolution.
29h	FAN2 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Ah	FAN3 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Bh	VCORE High Limit
2Ch	VCORE Low Limit
2Dh	VIN1 High Limit
2Eh	VIN1 Low Limit
2Fh	+3.3VIN High Limit
30h	+3.3VIN Low Limit
31h	+5VIN High Limit
32h	+5VIN Low Limit
33h	VIN2 High Limit
34h	VIN2 Low Limit
35h	Reserved

Value RAM — Index 20h- 3Fh, continued

Address A6-A0	Description
36h	Reserved
37h	Reserved
38h	Reserved
39h	SYSTIN temperature sensor High Limit
3Ah	SYSTIN temperature sensor Hysteresis Limit
3Bh	FAN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Ch	FAN2 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh	FAN3 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3E- 3Fh	Reserved

Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.

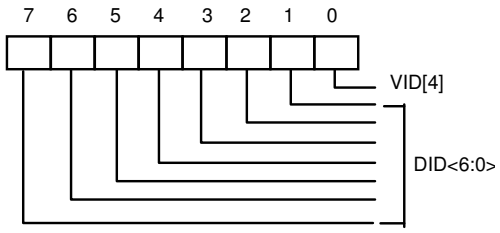
Device ID Register - Index 49h

Register Location: 49h

Power on Default Value 03h

Attribute: bit<7:1> Read Only; bit<0> Read/Write

Size: 8 bits

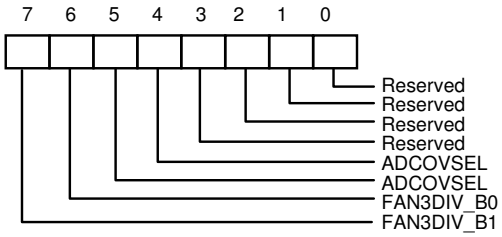


Bit 7-1: Read Only - Device ID<6:0>

Bit 0 : CPU Vcore ID [4]. The VID value is written by BIOS if the VID value can be detected. After the VID value is written, Software/AP can use this information to identify the Vcore voltage of the CPU.

Fan Divisor Register II - Index 4Bh

Register Location:	4Bh
Power on Default Value	<7:0> 44h.
Attribute:	Read/Write
Size:	8 bits



Bit 7-6:Fan3 speed divisor.

Please refer to Bank0 CR[5Dh] , Fan divisor table.

Bit 5-4: Select A/D Converter Clock Input.

<5:4> = 00 - default. ADC clock select 22.5 Khz.

<5:4> = 01- ADC clock select 5.6 Khz. (22.5K/4)

<5:4> = 10 - ADC clock select 1.4Khz. (22.5K/16)

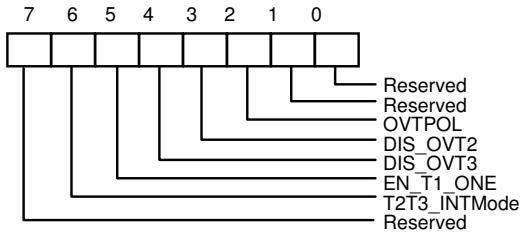
<5:4> = 11 - ADC clock select 0.35 Khz. (22.5K/64)

Bit 3-2: These two bits should be set to 01h. The default value is 01h.

Bit 1-0: Reserved.

SMI#/OVT# Control Register- Index 4Ch

Register Location:	4Ch
Power on Default Value	18h
Attribute:	Read/Write
Size:	8 bits



Bit 7: Reserved. User Defined.

Bit 6: Set to 1, the SMI# output type of Temperature CPUTIN/VTIN is set to Comparator Interrupt mode. Set to 0, the SMI# output type is set to Two-Times Interrupt mode. (default 0)

Bit 5: Set to 1, the SMI# output type of temperature SYSTIN is One-Time interrupt mode. Set to 0, the SMI# output type is Two-Times interrupt mode.

Bit 4: Disable temperature sensor VTIN over-temperature (OVT) output if set to 1. Default 0, enable VTIN OVT output through pin OVT#.

Bit 3: Disable temperature sensor CPUTIN over-temperature (OVT) output if set to 1. Default 0, enable CPUTIN OVT output through pin OVT#.

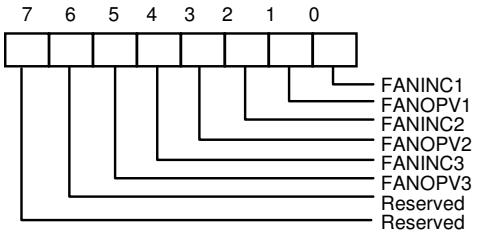
Bit 2: Over-temperature polarity. Write 1, OVT# active high. Write 0, OVT# active low. Default 0.

Bit 1: Reserved.

Bit 0: Reserved.

FAN IN/OUT and BEEP Control Register- Index 4Dh

Register Location:	4Dh
Power on Default Value	15h
Attribute:	Read/Write
Size:	8 bits



Bit 7~6: Reserved.

Bit 5: FAN 3 output value if FANINC3 sets to 0. Write 1, pin5 (DSB#/FANIN3) generates a logic high signal. Write 0, pin 5 generates a logic low signal. This bit is default 0. This bit is only valid when pin5 is set to FANIN3 function.

Bit 4: FAN 3 Input Control. Set to 1, pin 5(DSB#/FANIN3) acts as FAN tachmeter input, which is default value. Set to 0, this pin 5 acts as FAN control signal and the output value of FAN control is set by this register bit 5. This bit is only valid when pin5 is set to FANIN3 function.

Bit 3: FAN 2 output value if FANINC2 sets to 0. Write 1, then pin 115 always generate logic high signal. Write 0, pin 115 always generates logic low signal. This bit default 0.

Bit 2: FAN 2 Input Control. Set to 1, pin 112 acts as FAN clock input, which is default value. Set to 0, this pin 112 acts as FAN control signal and the output value of FAN control is set by this register bit 3.

Bit 1: FAN 1 output value if FANINC1 sets to 0. Write 1, then pin 116 always generate logic high signal. Write 0, pin 116 always generates logic low signal. This bit default 0.

Bit 0: FAN 1 Input Control. Set to 1, pin 113 acts as FAN clock input, which is default value. Set to 0, this pin 113 acts as FAN control signal and the output value of FAN control is set by this register bit 1.

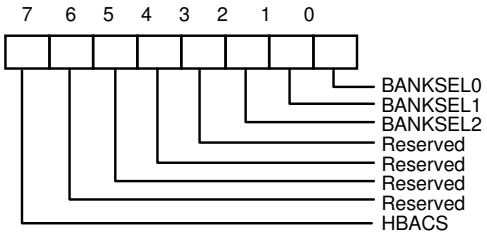
Register 50h ~ 5Fh Bank Select Register - Index 4Eh

Register Location: 4Eh

Power on Default Value 80h

Attribute: Read/Write

Size: 8 bits



Bit 7: HBACS- High byte access. Set to 1, access Register 4Fh high byte register.

Set to 0, access Register 4Fh low byte register. Default 1.

Bit 6-3: Reserved. This bit should be set to 0.

Bit 2-0: Index ports 0x50~0x5F Bank select.

Set to 0, select Bank0.

Set to 1, select Bank1.

Set to 2, select Bank2.

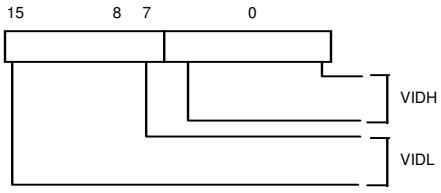
Winbond Vendor ID Register - Index 4Fh

Register Location: 4Fh

Power on Default Value <15:0> = 5CA3h

Attribute: Read Only

Size: 16 bits



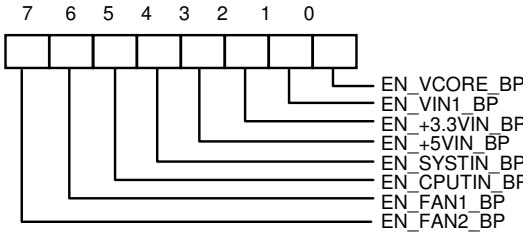
Bit 15-8: Vendor ID High Byte if CR4E.bit7=1.Default 5Ch.

Bit 7-0: Vendor ID Low Byte if CR4E.bit7=0. Default A3h.

Winbond Test Register -- Index 50h - 55h (Bank 0)

BEEP Control Register 1-- Index 56h (*Bank 0*)

Register Location:	56h
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits



Bit 7: BEEP output control for FAN 2 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 6: BEEP output control for FAN 1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 5: BEEP output control for temperature CPUTIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 4: BEEP output control for temperature SYSTIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 3: BEEP output control for +5VIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 2: BEEP output control for +3.3VIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 1: BEEP output control for VIN1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 0: BEEP output control for CPUVCORE if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

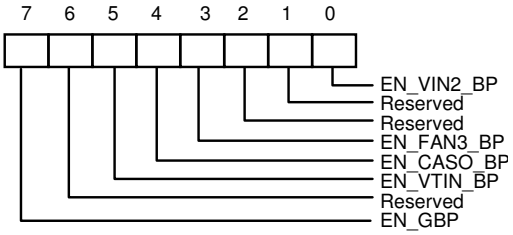
BEEP Control Register 2-- Index 57h (*Bank 0*)

Register Location: 57h

Power on Default Value 80h

Attribute: Read/Write

Size: 8 bits



Bit 7: Global BEEP Control. Write 1, enable global BEEP output. Default 1. Write 0, disable all BEEP output.

Bit 6: Reserved.

Bit 5: BEEP output control for temperature VTIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 4: BEEP output control for case open if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 3: BEEP output control for FAN 3 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 2-1: Reserved.

Bit 0: BEEP output control for VTIN2 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

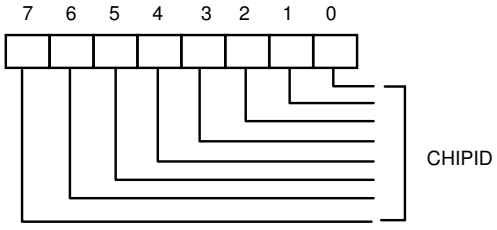
Chip ID -- Index 58h (*Bank 0*)

Register Location: 58h

Power on Default Value 80h

Attribute: Read Only

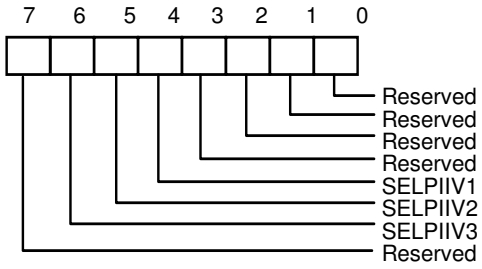
Size: 8 bits



Bit 7: Winbond Chip ID number. Read this register will return 80h.

Reserved Register -- Index 59h (*Bank 0*)

Register Location:	59h
Power on Default Value	70h
Attribute:	Read/Write
Size:	8 bits



Bit 7: Reserved

Bit 6: Diode mode selection of temperature VTIN if index 5Dh bit3 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode. Set this bit to 0, select 2N3904 bipolar diode.

Bit 5: Diode mode selection of temperature CPUTIN if index 5Dh bit2 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode. Set this bit to 0, select 2N3904 bipolar diode.

Bit 4: Diode mode selection of temperature SYSTIN if index 5Dh bit1 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode. Set this bit to 0, select 2N3904 bipolar diode.

Bit 3-0: Reserved

Reserved -- Index 5Ah (Bank 0)

Reserved -- Index 5Bh (Bank 0)

Reserved -- Index 5Ch (*Bank 0*)

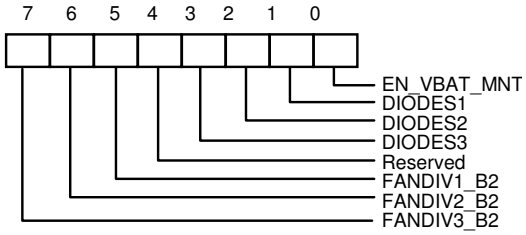
VBAT Monitor Control Register -- Index 5Dh (*Bank 0*)

Register Location: 5Dh

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: Fan3 divisor Bit2.

Bit 6: Fan2 divisor Bit2.

Bit 5: Fan1 divisor Bit2.

Bit 4: Reserved.

Bit 3: Sensor type selection of VTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 2: Sensor type selection of CPUTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 1: Sensor type selection of SYSTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 0: Set to 1, enable battery voltage monitor. Set to 0, disable battery voltage monitor. After set this bit from 0 to 1, the monitored value will be updated to the VBAT reading value register after one monitor cycle time.

Fan divisor table:

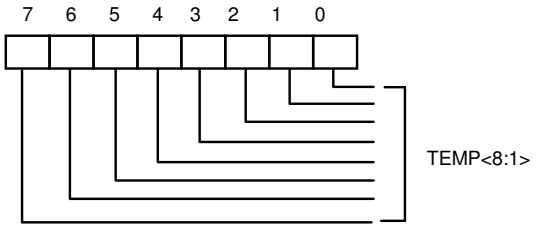
Bit 2	Bit 1	Bit 0	Fan Divisor	Bit 2	Bit 1	Bit 0	Fan Divisor
0	0	0	1	1	0	0	16
0	0	1	2	1	0	1	32
0	1	0	4	1	1	0	64
0	1	1	8	1	1	1	128

Reserved Register -- 5Eh (*Bank 0*)

Reserved Register -- 5Fh (*Bank 0*)

CPUTIN Temperature Sensor Temperature (High Byte) Register - Index 50h(*Bank1*)

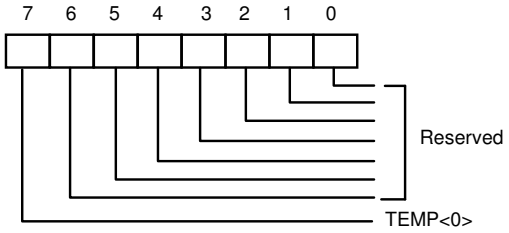
Register Location: 50h
Attribute: Read Only
Size: 8 bits



Bit 7: Temperature <8:1> of CPUTIN sensor, which is high byte, means 1°C.

CPUTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (*Bank1*)

Register Location: 51h
Attribute: Read Only
Size: 8 bits



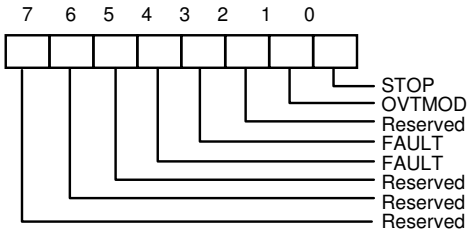
Bit 7: Temperature <0> of CPUTIN sensor, which is low byte, means 0.5°C.
Bit 6-0: Reserved.

CPUTIN Temperature Sensor Configuration Register - Index 52h (*Bank 1*)

Register Location: 52h

Power on Default Value 00h

Size: 8 bits



Bit 7-5: Read - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write - Number of faults to detect before setting OVT# output to avoid false tripping due to noise.

Bit 2: Read - Reserved. This bit should be set to 0.

Bit 1: Read/Write - OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

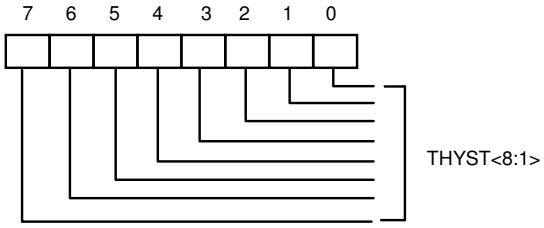
CPUTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (*Bank 1*)

Register Location: 53h

Power on Default Value 4Bh

Attribute: Read/Write

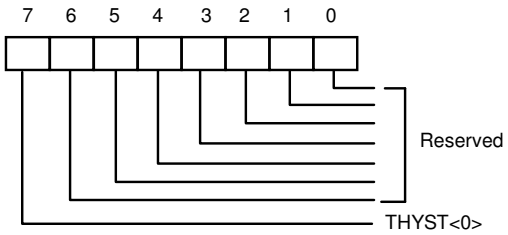
Size: 8 bits



Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

CPUTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (*Bank 1*)

Register Location:	54h
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits

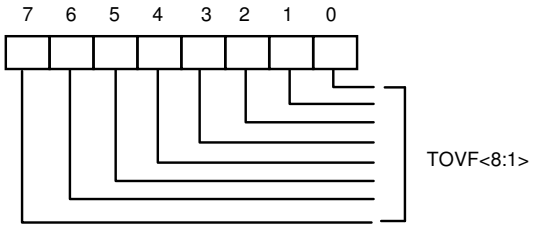


Bit 7: Hysteresis temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

CPUTIN Temperature Sensor Over-temperature (High Byte) Register - Index 55h (*Bank1*)

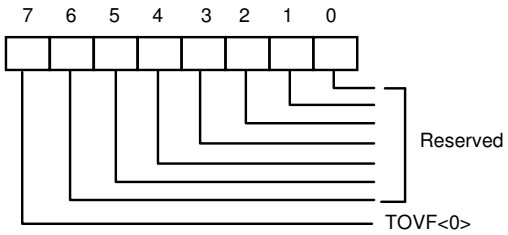
Register Location:	55h
Power on Default Value	50h
Attribute:	Read/Write
Size:	8 bits



Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

CPUTIN Temperature Sensor Over-temperature (Low Byte) Register - Index 56h (*Bank 1*)

Register Location:	56h
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits

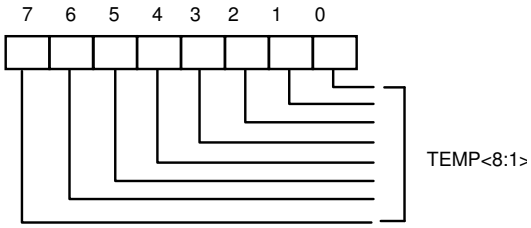


Bit 7: Over-temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

VTIN Temperature Sensor Temperature (High Byte) Register - Index 50h (*Bank 2*)

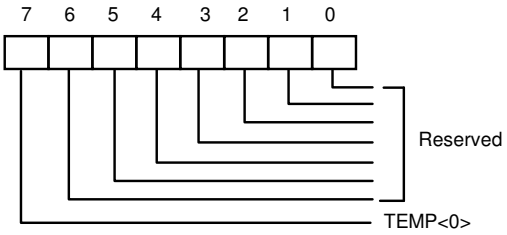
Register Location:	50h
Attribute:	Read Only
Size:	8 bits



Bit 7: Temperature <8:1> of sensor 2, which is high byte, means 1°C.

VTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (*Bank 2*)

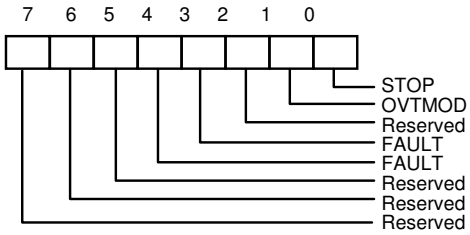
Register Location: 51h
Attribute: Read Only
Size: 8 bits



Bit 7: Temperature <0> of sensor3, which is low byte, means 0.5°C.
Bit 6-0: Reserved.

VTIN Temperature Sensor Configuration Register - Index 52h (*Bank 2*)

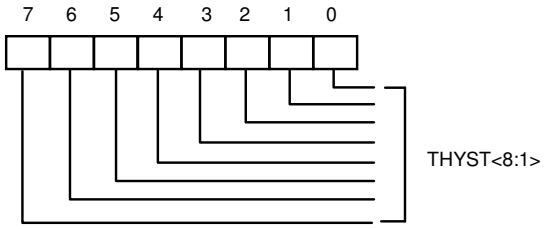
Register Location: 52h
Power on Default Value 00h
Size: 8 bits



Bit 7-5: Read - Reserved. This bit should be set to 0.
Bit 4-3: Read/Write - Number of faults to detect before setting OVT# output to avoid false tripping due to noise.
Bit 2: Read - Reserved. This bit should be set to 0.
Bit 1: Read/Write - OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.
Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

VTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (*Bank 2*)

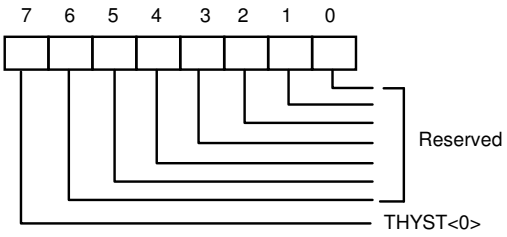
Register Location: 53h
Power on Default Value 4Bh
Attribute: Read/Write
Size: 8 bits



Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

VTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (*Bank 2*)

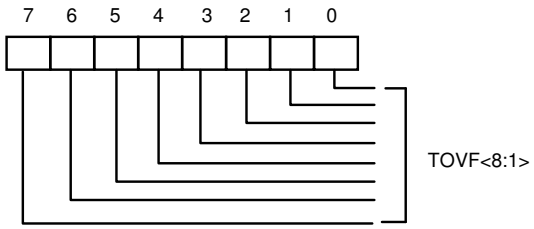
Register Location: 54h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: Hysteresis temperature bit 0, which is low Byte.
Bit 6-0: Reserved.

VTIN Temperature Sensor Over-temperature (High Byte)Register - Index 55 (*Bank 2*)

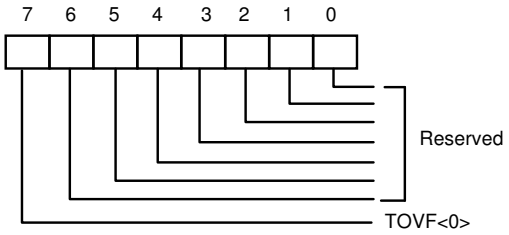
Register Location:	55h
Power on Default Value	50h
Attribute:	Read/Write
Size:	8 bits



Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

VTIN Temperature Sensor Over-temperature (Low Byte) Register - Index 56(*Bank2*)

Register Location:	56h
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits



Bit 7: Over-temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

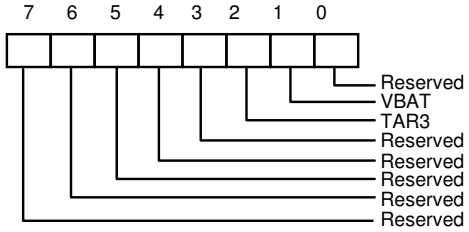
Interrupt Status Register 3 -- Index 50h (BANK4)

Register Location: 50h

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits



Bit 7-3: Reserved.

Bit 2: A one indicates that the VTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™ .

Bit 1: A one indicates a High or Low limit of VBAT has been exceeded.

Bit 0: Reserved.

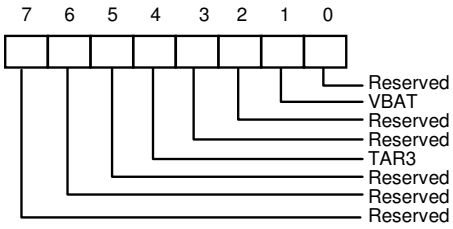
SMI# Mask Register 3 -- Index 51h (BANK 4)

Register Location: 51h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-5: Reserved.

Bit 4: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Bit 2-3: Reserved.

Bit 1: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Bit 0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Reserved Register -- Index 52h (*Bank 4*)

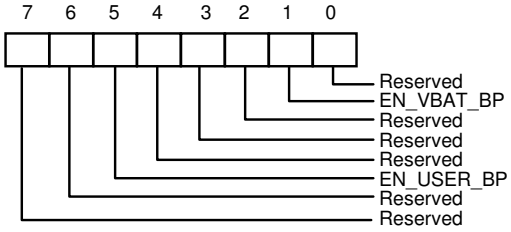
BEEP Control Register 3-- Index 53h (*Bank 4*)

Register Location: 53h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-6: Reserved.

Bit 5: User define BEEP output function. Write 1, the BEEP is always active. Write 0, this function is inactive. (Default 0)

Bit 4-2: Reserved.

Bit 1: BEEP output control for VBAT if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 0:Reserved.

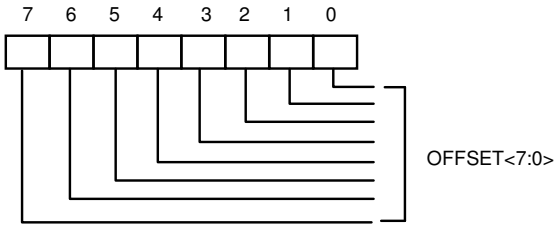
SYSTIN Temperature Sensor Offset Register -- Index 54h (*Bank 4*)

Register Location: 54h

Power on Default Value 00h

Attribute: Read/Write

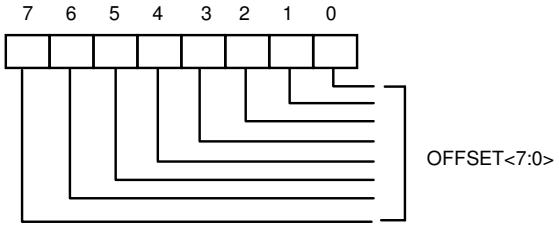
Size: 8 bits



Bit 7-0: SYSTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

CPUTIN Temperature Sensor Offset Register -- Index 55h (*Bank 4*)

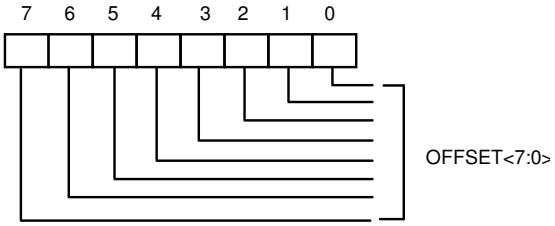
Register Location: 55h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



Bit 7-0: CPUTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

VTIN Temperature Sensor Offset Register -- Index 56h (*Bank 4*)

Register Location: 56h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits

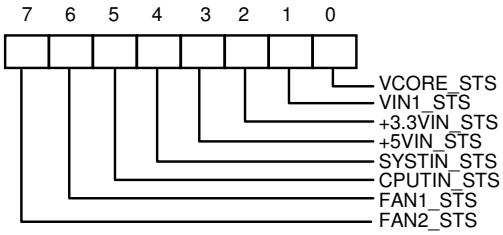


Bit 7-0: VTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

Reserved Register -- Index 57h--58h (*Bank4)*

Real Time Hardware Status Register I -- Index 59h (*Bank 4*)

Register Location:	59h
Power on Default Value	00h
Attribute:	Read Only
Size:	8 bits



Bit 7: FAN 2 Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

Bit 6: FAN 1 Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

Bit 5: CPUTIN temperature sensor status. Set 1, the temperature exceeds the over-temperature limit value. Set 0, the temperature is in under the hysteresis value.

Bit 4: SYSTIN temperature sensor status. Set 1, the temperature exceeds the over-temperature limit value. Set 0, the temperature is in under the hysteresis value.

Bit 3: +5VIN Voltage Status. Set 1, the voltage of +5VIN is over the limit value. Set 0, the voltage of +5VIN is in the limit range.

Bit 2: +3.3VIN Voltage Status. Set 1, the voltage of +3.3V is over the limit value. Set 0, the voltage of +3.3VIN is in the limit range.

Bit 1: VIN1 Voltage Status. Set 1, the voltage of VIN1 is over the limit value. Set 0, the voltage of VIN1 is in the limit range.

Bit 0: VCORE Voltage Status. Set 1, the voltage of VCORE is over the limit value. Set 0, the voltage of VCORE is in the limit range.

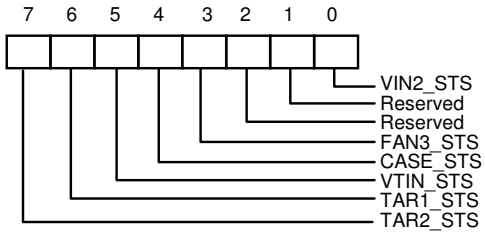
Real Time Hardware Status Register II -- Index 5Ah (*Bank 4*)

Register Location: 5Ah

Power on Default Value 00h

Attribute: Read Only

Size: 8 bits



Bit 7: Smart Fan 2 warning status. Set 1, the CPUTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Set 0, the temperature does not reach the warning range yet.

Bit 6: Smart Fan 1 warning status. Set 1, the SYSTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Set 0, the temperature does not reach the warning range yet.

Bit 5: VTIN temperature sensor status. Set 1, the temperature exceeds the over-temperature limit value. Set 0, the temperature is in under the hysteresis value.

Bit 4: Case Open Status. Set 1, the case open is detected and latched. Set 0, the case is not latched open.

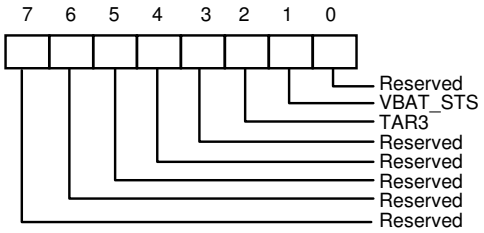
Bit 3: FAN 2 Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

Bit 2-1: Reserved.

Bit 0: Vin2 Voltage Status. Set 1, the voltage of VIN2 is over the limit value. Set 0, the voltage of VIN2 is in the limit range.

Real Time Hardware Status Register III -- Index 5Bh (*Bank 4*)

Register Location:	5Bh
Power on Default Value	00h
Attribute:	Read Only
Size:	8 bits



Bit 7-2: Reserved.

Bit 2: Smart Fan 3 warning status. Set 1, the VTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Set 0, the temperature does not reach the warning range yet.

Bit 1: VBAT Voltage Status. Set 1, the voltage of VBAT is over the limit value. Set 0, the voltage of VBAT is during the limit range.

Bit 0: Reserved.

Reserved Register -- Index 5Ch (*Bank 4*)

Reserved Register -- Index 5Dh (*Bank 4*)

Value RAM 2— Index 50h - 5Ah (auto-increment) ***(BANK 5)***

Address A6-A0 Auto-Increment	Description
50h	Reserved
51h	VBAT reading. The reading is meaningless if EN_VBAT_MNT bit(CR5D bit0) is not set.
52h	Reserved
53h	Reserved
54h	Reserved
55h	Reserved
56h	VBAT High Limit
57h	VBAT Low Limit

Winbond Test Register -- Index 50h (*Bank 6*)

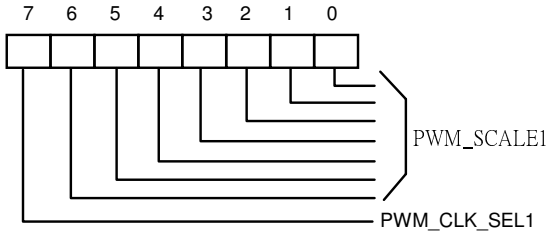
FANPWM1 Output Frequency Configuration Register—Index00h (*Bank 0*)

Register Location: 00h

Power on Default Value 01h

Attribute: Read/Write

Size: 8 bits



Bit 7: FANPWM1 Clock Source Select. This bit selects the clock source of FANPWM1 output frequency.

Set to 0, select 24 MHz.

Set to 1, select 180 KHz.

Bit 6-1: FANPWM1 Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

$$\text{PWM frequency} = \frac{SourceClock}{\text{Pr}e\_scaleDivider} * \frac{1}{256}$$

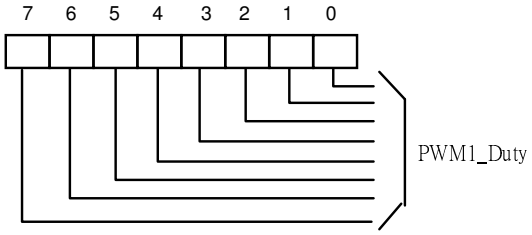
FANPWM1 Duty Cycle Select Register-- 01h (*Bank 0*)

Register Location: 01h

Power on Default Value FFh

Attribute: Read/Write

Size: 8 bits



Bit 7-0: FANPWM1 duty cycle control. Write FF, duty cycle is 100%. Write 00, duty cycle is 0%.

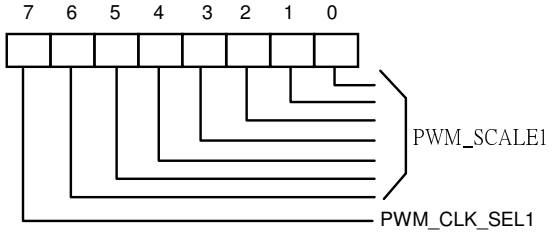
FANPWM2 Output Frequency Configuration Register—Index02h (*Bank 0*)

Register Location: 02h

Power on Default Value 01h

Attribute: Read Only

Size: 8 bits



Bit 7: FANPWM2 Clock Source Select. This bit selects the clock source of FANPWM2 output frequency.

Set to 0, select 24 MHz.

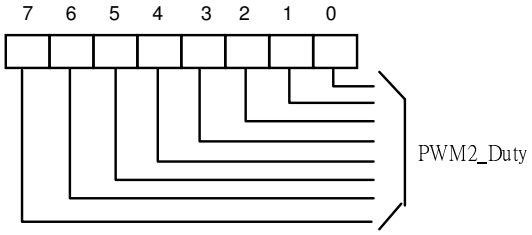
Set to 1, select 180 KHz.

Bit 6-1: FANPWM2 Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

$$\text{PWM frequency} = \frac{SourceClock}{\text{Pr}e\_scaleDivider} * \frac{1}{256}$$

FANPWM2 Duty Cycle Select Register-- 03h (*Bank 0*)

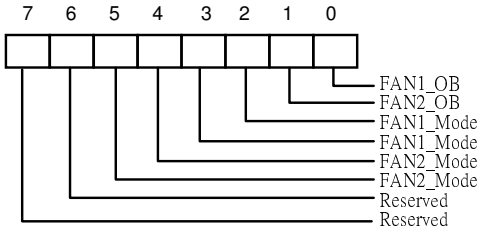
Register Location: 03h
Power on Default Value FFh
Attribute: Read/Write
Size: 8 bits



Bit 7-0: FANPWM2 duty cycle control. Write FF, duty cycle is 100%. Write 00, duty cycle is 0%.

FAN Configuration Register I -- Index 04h (*Bank 0*)

Register Location: 04h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



Bit7-6: Reserved

Bit5-4: FANPWM2 mode control.

Set 00, FANPWM2 is as Manual Mode. (Default).
Set 01, FANPWM2 is as Thermal Cruise Mode.
Set 10, FANPWM2 is as Fan Speed Cruise Mode.
Set 11, reserved and no function.

Bit3-2: FANPWM1 mode control.

Set 00, FANPWM1 is as Manual Mode. (Default).
Set 01, FANPWM1 is as Thermal Cruise Mode.

Set 10, FANPWM1 is as Fan Speed Cruise Mode.

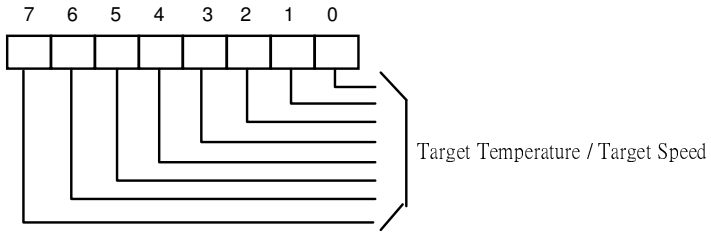
Set 11, reserved and no function.

Bit 1: FANPWM2 output mode selection. Set to 0, FANPWM2 pin is as output pin so that it can drive a logical high or low signal. Set to 1, FANPWM2 pin is as open-drain pin which can only drive a logical low signal.

Bit 0: FANPWM1 output mode selection. Set to 0, FANPWM1 pin is as output pin so that it can drive a logical high or low signal. Set to 1, FANPWM1 pin is as open-drain pin which can only drive a logical low signal.

SYSTIN Target Temperature Register/ Fan 1 Target Speed Register -- Index 05h (*Bank 0*)

Register Location:	05h
Power on Default Value	00h
Attribute:	Read/Write
Size:	8 bits



(1). When at Thermal Cruise mode:

Bit7: Reserved.

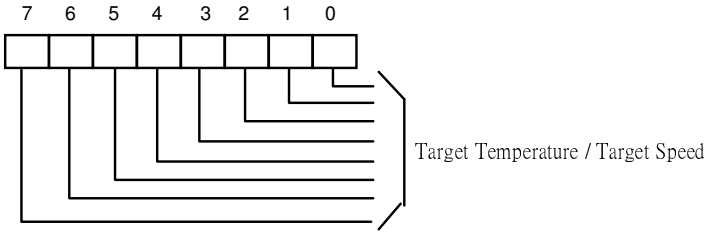
Bit6-0: SYSTIN Target Temperature.

(2). When at Fan Speed Cruise mode:

Bit7-0: Fan 1 Target Speed.

CPUTIN Target Temperature Register/ Fan 2 Target Speed Register -- Index 06h (*Bank 0*)

Register Location: 06h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



(1). When at Thermal Cruise mode:

Bit7: Reserved.

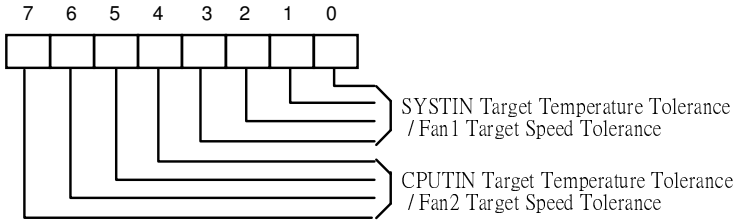
Bit6-0: CPUTIN Target Temperature.

(2). When at Fan Speed Cruise mode:

Bit7-0: Fan 2 Target Speed.

Tolerance of Target Temperature or Target Speed Register -- Index 07h (*Bank 0*)

Register Location: 07h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



(1). When at Thermal Cruise mode:

Bit7-4: Tolerance of CPUTIN Target Temperature.

Bit3-0: Tolerance of SYSTIN Target Temperature.

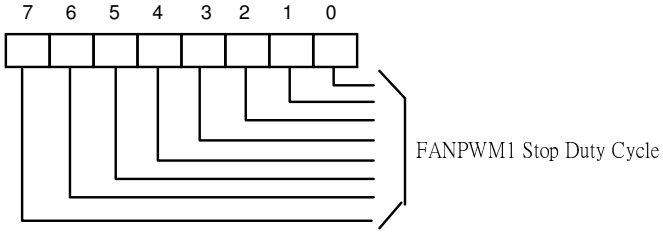
(2). When at Fan Speed Cruise mode:

Bit7-4: Tolerance of Fan 2 Target Speed.

Bit3-0: Tolerance of Fan 1 Target Speed.

FANPWM1 Stop Duty Cycle Register -- Index 08h (*Bank 0*)

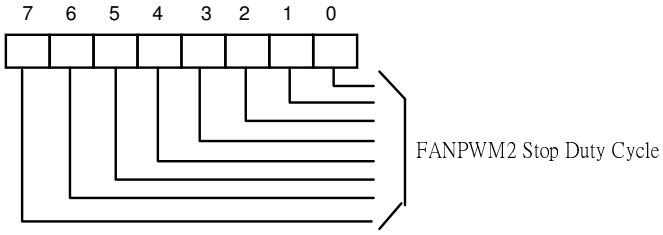
Register Location:	08h
Power on Default Value	01h
Attribute:	Read/Write
Size:	8 bits



When at Thermal Cruise mode, FANPWM1 duty cycle will be 0 if it decreases to below this value. This register should be written a non-zero minimum PWM stop duty cycle.

FANPWM2 Stop Duty Cycle Register -- 09h (*Bank 0*)

Register Location:	09h
Power on Default Value	01h
Attribute:	Read/Write
Size:	8 bits



When at Thermal Cruise mode, FANPWM2 duty cycle will be 0 if it decreases to below this value. This register should be written a non-zero minimum PWM stop duty cycle.

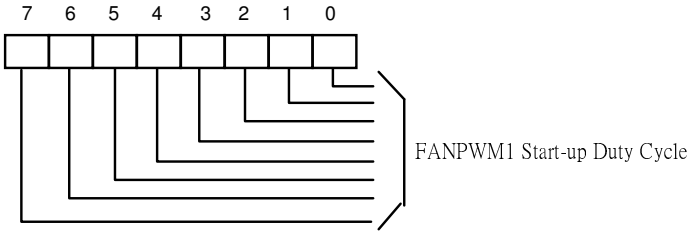
FANPWM1 Start-up Duty Cycle Register -- Index 0Ah (*Bank 0*)

Register Location: 0Ah

Power on Default Value 01h

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, FANPWM1 duty cycle will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan.

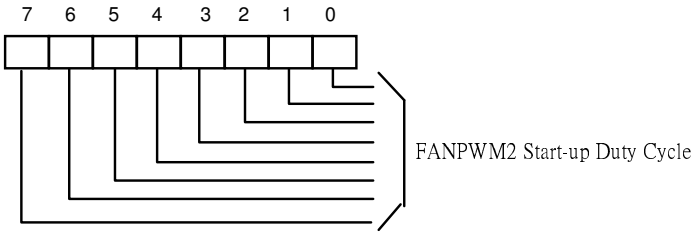
FANPWM2 Start-up Duty Cycle Register -- Index 0Bh (*Bank 0*)

Register Location: 0Bh

Power on Default Value 01h

Attribute: Read/Write

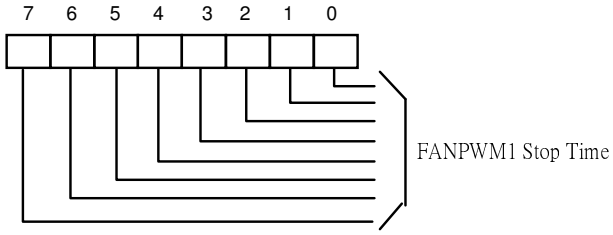
Size: 8 bits



When at Thermal Cruise mode, FANPWM2 duty cycle will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan.

FANPWM1 Stop Time Register -- Index 0Ch (*Bank 0*)

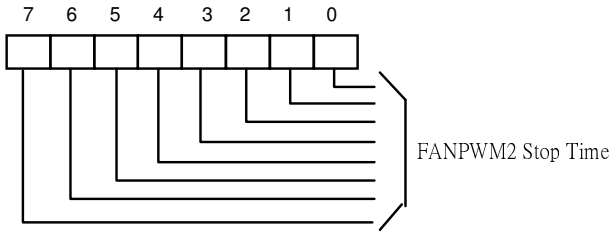
Register Location:	0Ch
Power on Default Value	3Ch
Attribute:	Read/Write
Size:	8 bits



When at Thermal Cruise mode, this register determines the time of which FANPWM1 duty is from stop duty cycle to 0 duty cycle. The unit of this register is 0.1 second. The default time is 6 seconds.

FANPWM2 Stop Time Register -- Index 0Dh (*Bank 0*)

Register Location:	0Dh
Power on Default Value	3Ch
Attribute:	Read/Write
Size:	8 bits



When at Thermal Cruise mode, this register determines the time of which FANPWM2 duty is from stop duty cycle to 0 duty cycle. The unit of this register is 0.1 second. The default time is 6 seconds.

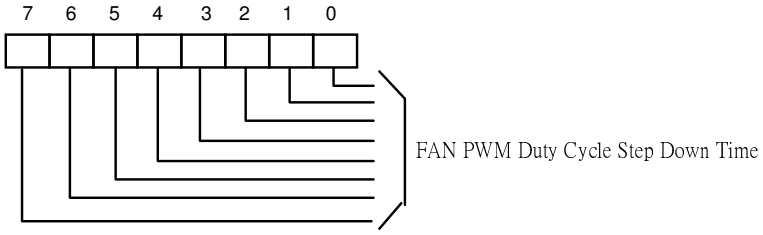
Fan PWM Duty Cycle Step Down Time Register -- Index 0Eh (*Bank 0*)

Register Location: 0Eh

Power on Default Value 0Ah

Attribute: Read/Write

Size: 8 bits



This register determines the speed of FAN PWM decreasing the duty cycle in Smart Fan Control mode.

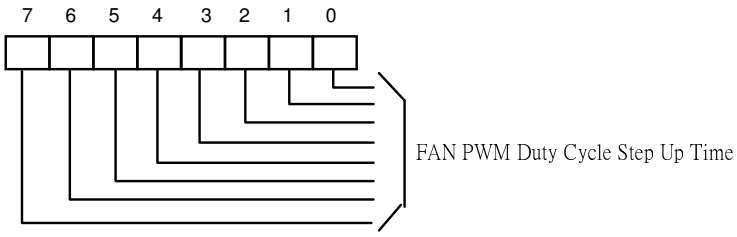
Fan PWM Duty Cycle Step Up Time Register -- Index 0Fh (*Bank 0*)

Register Location: 0Fh

Power on Default Value 0Ah

Attribute: Read/Write

Size: 8 bits



This register determines the speed of FAN PWM increasing the duty cycle in Smart Fan Control mode.

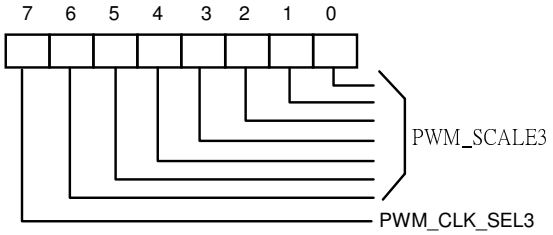
FANPWM3 Output Frequency Configuration Register—Index10h (*Bank 0*)

Register Location: 10h

Power on Default Value 01h

Attribute: Read Only

Size: 8 bits



Bit 7: FANPWM3 Clock Source Select. This bit selects the clock source of FANPWM3 output frequency.

Set to 0, select 24 MHz.

Set to 1, select 180 KHz.

Bit 6-1: FANPWM3 Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

$$\text{PWM frequency} = \frac{SourceClock}{Pre\_scaleDivider} * \frac{1}{256}$$

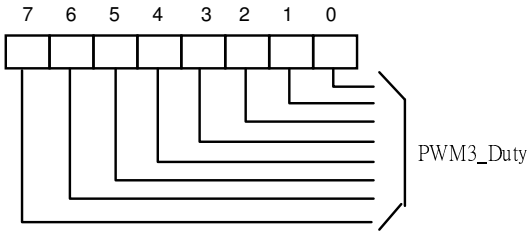
FANPWM3 Duty Cycle Select Register-- 11h (*Bank 0*)

Register Location: 11h

Power on Default Value FFh

Attribute: Read/Write

Size: 8 bits



Bit 7-0: FANPWM3 duty cycle control. Write FF, duty cycle is 100%. Write 00, duty cycle is 0%.

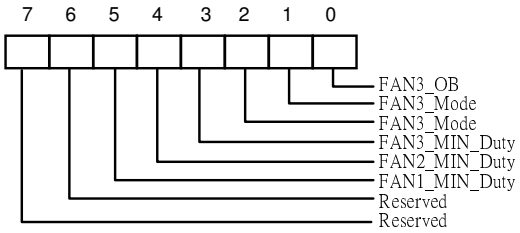
FAN Configuration Register II -- Index 12h (*Bank 0*)

Register Location: 12h

Power on Default Value 00h

Attribute: Read/Write

Size: 8 bits



Bit7-6: Reserved

Bit 5: Set 1, FANPWM1 duty cycle will decrease to and keep the value set in Index 08h when temperature goes below target range. This is to maintain the fan speed in a minimum value.

Set 0, FANPWM1 duty cycle will decrease to 0 when temperature goes below target range.

Bit 4: Set 1, FANPWM2 duty cycle will decrease to and keep the value set in Index 09h when temperature goes below target range. This is to maintain the fan speed in a minimum value.

Set 0, FANPWM2 duty cycle will decrease to 0 when temperature goes below target range.

Bit 3: Set 1, FANPWM3 duty cycle will decrease to and keep the value set in Index 17h when temperature goes below target range. This is to maintain the fan speed in a minimum value.

Set 0, FANPWM3 duty cycle will decrease to 0 when temperature goes below target range.

Bit2-1: FANPWM3 mode control.

Set 00, FANPWM3 is as Manual Mode. (Default).

Set 01, FANPWM3 is as Thermal Cruise Mode.

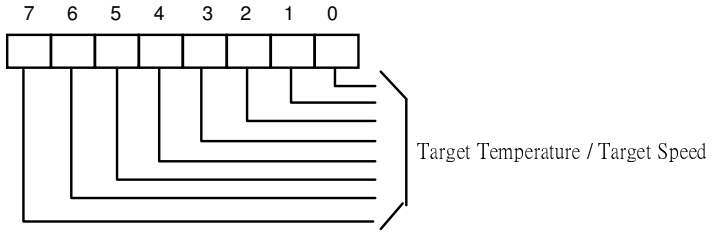
Set 10, FANPWM3 is as Fan Speed Cruise Mode.

Set 11, reserved and no function.

Bit 0: FANPWM3 output mode selection. Set to 0, FANPWM3 pin is as output pin so that it can drive a logical high or low signal. Set to 1, FANPWM3 pin is as open-drain pin which can only drive a logical low signal.

VTIN Target Temperature Register/ Fan 3 Target Speed Register -- Index 13h (*Bank0*)

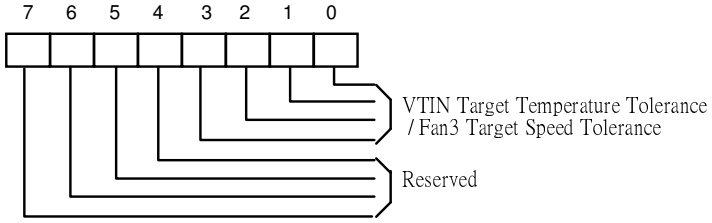
Register Location: 13h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



(1).When at Thermal Cruise mode:
Bit7: Reserved.
Bit6-0: VTIN Target Temperature.
(2).When at Fan Speed Cruise mode:
Bit7-0: Fan 3 Target Speed.

Tolerance of Target Temperature or Target Speed Register -- Index 14h (*Bank 0*)

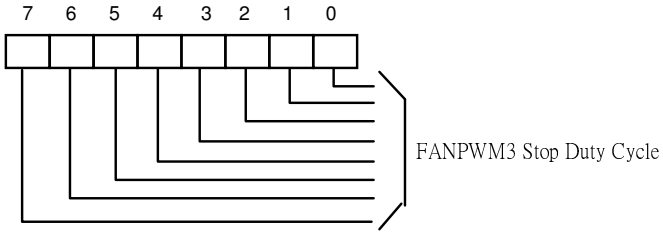
Register Location: 14h
Power on Default Value 00h
Attribute: Read/Write
Size: 8 bits



(1).When at Thermal Cruise mode:
Bit3-0: Tolerance of VTIN Target Temperature.
(2).When at Fan Speed Cruise mode:
Bit3-0: Tolerance of Fan 3 Target Speed.

FANPWM3 Stop Duty Cycle Register -- Index 15h (*Bank 0*)

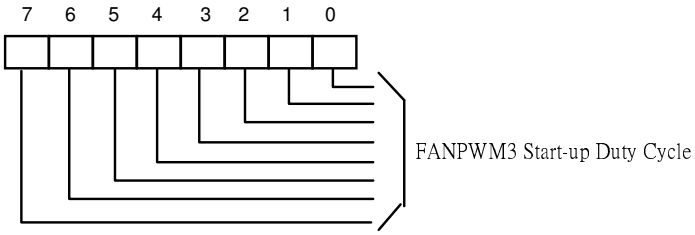
Register Location: 15h
Power on Default Value 01h
Attribute: Read/Write
Size: 8 bits



When at Thermal Cruise mode, FANPWM3 duty cycle will be 0 if it decreases to below this value. This register should be written a non-zero minimum PWM stop duty cycle.

FANPWM3 Start-up Duty Cycle Register -- Index 16h (*Bank 0*)

Register Location: 16h
Power on Default Value 01h
Attribute: Read/Write
Size: 8 bits



When at Thermal Cruise mode, FANPWM3 duty cycle will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan.

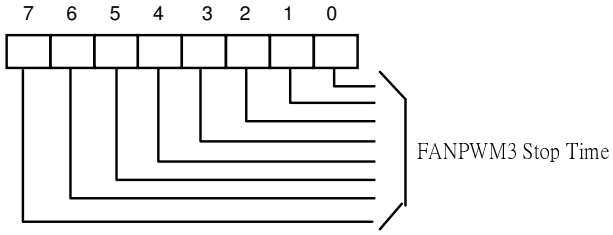
FANPWM3 Stop Time Register -- Index 17h (*Bank 0*)

Register Location: 17h

Power on Default Value 3Ch

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, this register determines the time of which FANPWM3 duty is from stop duty cycle to 0 duty cycle. The unit of this register is 0.1 second. The default time is 6 seconds.

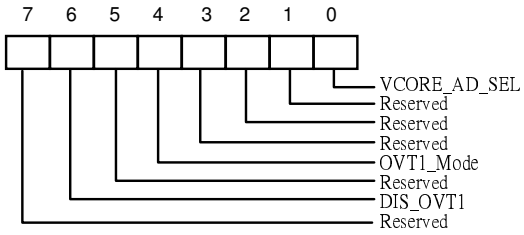
VRM & OVT Configuration Register -- Index 18h (*Bank 0*)

Register Location: 18h

Power on Default Value 43h

Attribute: Read/Write

Size: 8 bits



Bit 7: Reserved.

Bit 6: Set to 1, disable temperature sensor SYSTIN over-temperature (OVT) output. Set to 0, enable the SYSTIN OVT output.

Bit 5: Reserved.

Bit 4: SYSTIN OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

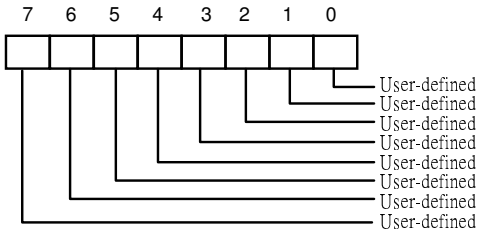
Bit 3-1: Reserved.

Bit 0: CPUVCORE pin voltage detection method selection. Set to 1, VRM9 formula is selected. Set to 0, VRM8 formula is selected. This bit default value is 1.

Reserved -- Index 19h (*Bank 0*)

User Defined Register -- Index 1A- 1Bh (*Bank 0*)

Register Location:	1A-1Bh
Power on Default Value	FFh
Attribute:	Read/Write
Size:	8 bits



Bit 7-0: User can write any value into these bits and read.

Reserved -- Index 1Ch-1Fh (*Bank 0*)

7. SMART CARD READER INTERFACE (SCR)

7.1 Features

Winbond's implementation of Smart Card Reader interface is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications 1.0. Except for pins specified in ISO/IEC 7816-3, W83637HF/HG's SCI also includes SCPSNT (Smart Card Present) monitoring status of card insertion/extraction, SCLED (Smart Card traffic LED display) which is active high when host is accessing information to/from card, and two general-purpose I/O pins SCC4 and SCC8 (only available in W83637HF/HG) for users to design application-specific functions.

Register file (control and status registers) of Winbond's Smart Card interface is designed in an UART-like structure so that users with previous UART experience should have no trouble to implement Winbond's SCI applications.

Power consumption is minimized by sophisticated device's operation scheme.

7.2 Register File

Complete register file table

Bit Number										
Register file		**Abbr.**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Base + 0 BDLAB = 0	Receiver Buffer Register (Read only)	RBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Base + 0 BDLAB = 0	Transmitter Buffer Register (Write only)	TBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Base + 1 BDLAB = 0	Interrupt Enable Register	IER	SCC8	SCC4	SCC8_IO (note)	SCC4_IO (note)	ESCPTI (note)	ESCSRI (note)	ETBREI (note)	ERDRI (note)
	default		x	x	0	0	0	0	0	0
Base + 2 BDLAB = 0	Interrupt Status Register (Read only)	ISR	FIFO enabled	FIFO enabled	SCPSNT	SCPTI (note)	INTS2 (note)	INTS1 (note)	INTS0 (note)	Interrupt pending
Base + 2 BDLAB = 0	Smart Card FIFO control Register (Write only)	SCFR	RxTL1 (note)	RxTL0 (note)	Reserved	Reserved	Reserved	TxFRST (note)	RxFRST (note)	Enable FIFO
	default		0	0	x	x	x	0	0	0
Base + 3	Smart Card Control Register	SCCR	BDLAB (note)	Reserved	Reserved	EPE (note)	PBE (note)	Reserved	Reserved	SC_SEL
	default		0	x	x	0	0	x	x	0
Base + 4	Clock Base Register	CBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	default		0	0	0	0	1	1	0	0
Base + 5	Smart Card Status Register (Read only)	SCSR	RxFEI (note)	TSRE (note)	TBRE (note)	SBD (note)	NSER (note)	PBER (note)	OER (note)	RDR (note)
Base + 6	Guard Time Register	GTR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	default		0	0	0	0	0	0	0	1
Base + 7	Extended Control Register	ECR	Cold reset	Reserved	SCKFS1 (note)	SCKFS0 (note)	CLKSTPL (note)	CLKSTP (note)	SCIODIR (note)	Warm reset
	default		0	x	0	1	0	0	1	0
Base + 0 BDLAB = 1	Baud rate divisor Latch Lower byte	BLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	default		0	0	0	1	1	1	1	1
Base + 1 BDLAB = 1	Baud rate divisor Latch Higher byte	BLH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	default		0	0	0	0	0	0	0	0
Base + 2 BDLAB = 1	Smart Card ID number (Read only)		0	1	1	1	0	0	0	0

Note:

Abbreviation explanation (in alphabetical order) –

BDLAB – Baud rate divisor latch access bit.

CLKSTP – Stop Smart Card interface's clock SCCLK.

CLKSTPL – Set SCCLK level when CLKSTP is "1".

EPE – Even parity enable.

ERDRI – Enable RBR (Receiver Buffer Register) data ready interrupt.

ESCPTI - Enable SCPSNT interrupt.

ESCSRI - Enable interrupts of SCSR (read only Smart Card Status Register at base address + 5) events.

ETBREI – Enable TBR (write only Transmitter Buffer Register at base address + 0) empty interrupt.

INTS2 ~ INTS0 – Interrupt status bits. Refer to description of ISR (read only Interrupt Status Register at base address + 2) for details.

NSER – No stop bit error.

OER – Overrun error.

PBE – Parity bit enable.

PBER – Parity bit error.

RDR – Receiver data ready status.

RxFEI – Receiver FIFO error indication.

RxFRST – Receiver FIFO reset.

RxTL1 ~ RxTL0 – Receiver threshold level setting bits. Refer to description of SCFR (write only Smart Card FIFO control register at base address + 2) for details.

SBD – Silent byte detected.

SCIODIR – SCIO direction bit (0/1 mean output/input respectively).

SCKFS1 ~ SCKFS0 – Smart Card interface clock frequency selection bits. Refer to description of ECR (Extended Control Register at base address + 7) for details.

SCPTI – SCPSNT toggle interrupt status.

SC_SEL – Smart Card socket selection.

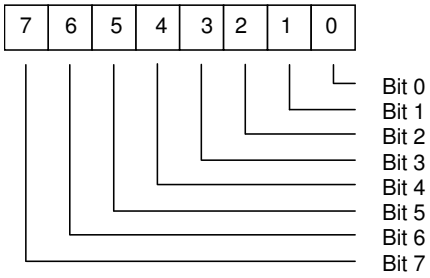
TBRE – TBR (write only Transmitter Buffer Register at base address + 0) empty status.

TSRE – TSR (Transmitter shift register) empty status.

TxFRST – Transmitter FIFO reset.

Receiver Buffer Register (RBR at base address + 0 when BDLAB = 0, read only)

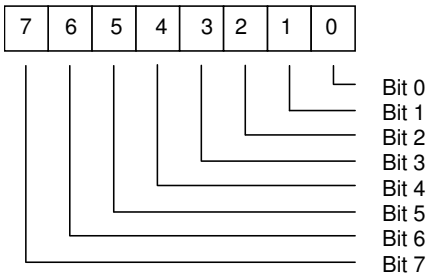
This register is the access port for receiver FIFO. It is active when Smart Card interface is in input mode with SCIODIR (bit 1 of ECR at base address + 7) set to "1". The depth of receiver FIFO is 16 bytes.



Bit 7 ~ bit 0: Access port for receiver FIFO.

Receiver Buffer Register (RBR at base address + 0 when BDLAB = 0, read only)

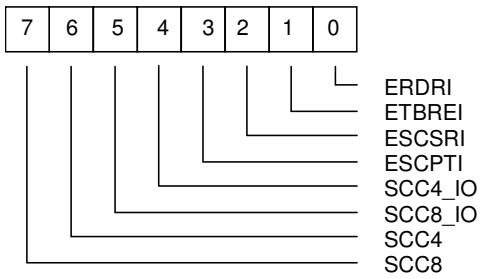
This register is the access port for transmitter FIFO. It is active when Smart Card interface is in output mode with SCIODIR (bit 1 of ECR at base address + 7) set to "0". The depth of transmitter FIFO is 16 bytes.



Bit 7 ~ bit 0: Access port for receiver FIFO.

Interrupt Enable Register (IER at base address + 1 when BDLAB = 0)

This register includes four control bits to enable interrupt events. The other four bits are allocated for control of general-purpose I/O pins which are usually connected to C4 and C8 pads of a smart card for application specific function.



Bit 7: SCC8 means Smart Card C8 pad. When SCC8_IO (bit 5) is set to "0" for output mode, this bit controls the voltage level of SCC8 pin which is high when SCC8 is set to "1" and low for setting of "0". Its value reflects what could be observed on SCC8 pin when SCC8_IO is set to "1" for input mode with the same convention as in output mode.

Bit 6: SCC4 means Smart Card C4 pad. When SCC4_IO (bit 4) is set to "0" for output mode, this bit controls the voltage level of SCC4 pin which is high when SCC4 is set to "1" and low for setting of "0". Its value reflects what is observed on SCC4 pin when SCC4_IO is set to "1" for input mode with the same convention as in output mode.

Bit 5: SCC8_IO means input/output direction control for SCC8 pin.

= 0 SCC8 is in output mode.

= 1 SCC8 is in input mode.

Bit 4: SCC4_IO means input/output direction control for SCC4 pin.

= 0 SCC4 is in output mode.

= 1 SCC4 is in input mode.

Bit 3: ESCPTI means SCPSNT toggle interrupt enable bit. A rising/falling edge of SCPSNT signal triggers an interrupt if this bit is set to "1".

= 0 SCPSNT toggle interrupt is disabled.

= 1 SCPSNT toggle interrupt is enabled.

Bit 2: ESCSRI means interrupt enable bit for SCSR-related events such as silent byte detected error, no stop bit error, parity bit error or overrun error. Any SCSR-related event as described above will trigger an interrupt if this bit is set to "1".

= 0 SCSR-related event interrupt is disabled.

= 1 SCSR-related event interrupt is enabled.

Bit 1: ETBREI means interrupt enable bit for TBR (Transmitter Buffer Register) empty condition. An interrupt is issued when TBR is empty and this bit is set to "1". It is used in output mode (SDIODIR = 0) to request host's attention to transfer data byte to card.

= 0 TBR empty interrupt is disabled.

= 1 TBR empty interrupt is enabled.

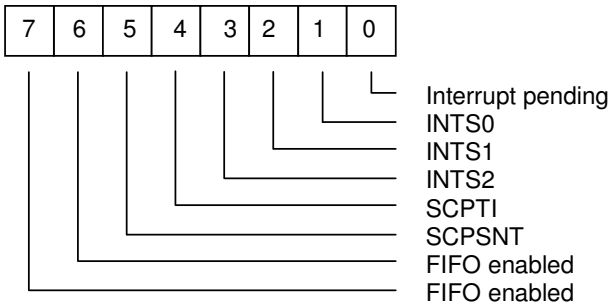
Bit 0: ERDRI means interrupt enable bit for receiver data ready status. The active FIFO threshold level for this kind of interrupt when FIFO is enabled is specified in RxTL1 and RxTL0 (bit 7 and bit 6 of SCFR at base address + 2. Refer to description of SCFR for details). An interrupt is issued if a data byte is ready for host to read when FIFO is disabled or incoming data from card reaches active FIFO threshold level when FIFO is enabled.

= 0 Receiver data ready interrupt is disabled.

= 1 Receiver data ready interrupt is enabled.

Interrupt Status Register (ISR at base address + 2 when BDLAB = 0, read only)

This register contains mainly interrupt status including transmission-related interrupts and SCPSNT toggle interrupt. Transmission-related interrupt status is coded and prioritized as in UART implementation. User may also find FIFO enable/disabled status reflecting what is set in bit 0 of SCFR (write only Smart Card FIFO Register at base address + 2 when BDLAB = 0) and SCPSNT line status.



Bit 7, 6: FIFO enabled status bits reflect what is set in bit 0 of SCFR (write only Smart Card FIFO Register at base address + 2 when BDLAB = 0).

Bit 5: SCPSNT line status. User may poll this bit to see SCPSNT pin's voltage level.

Bit 4: SCPTI means SCPSNT toggle interrupt status. A rising/falling edge of SCPSNT signal triggers an interrupt and set this status bit if ESCPTI (IER bit 3) is set to "1" to enable SCPSNT toggle interrupt.

= 0 No SCPSNT toggle interrupt.

= 1 SCPSNT toggle interrupt occurs.

Bit 3 ~ 1: INTS2 ~ INTS0 mean interrupt status bit 2 ~ 0. The combination indicates which kind of transmission-related interrupt has occurred. Refer to the following table for details.

ISR bit				Interrupt set and function			
3	2	1	0	Priority	Interrupt type	Interrupt source	Clear interrupt condition
0	0	0	1	-	-	No interrupt pending	-
0	1	1	0	first	Data receiving status	1. OER = 1 2. PBER = 1 3. NSER = 1 4. SBD = 1	Read SCSR
0	1	0	0	second	RBR data ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO is under active level
1	1	0	0	second	FIFO data time out	Data present in Rx FIFO for 4-character period of time since last access of Rx FIFO.	Read RBR
0	0	1	0	third	TBR empty	TBR empty	1. Write data to TBR 2. Read ISR (if priority is third)

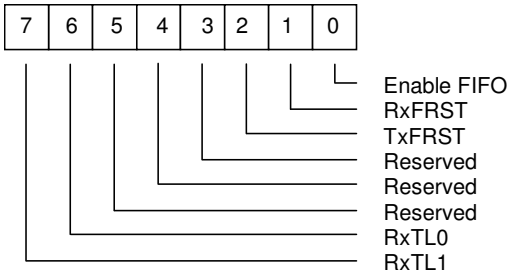
Bit 0: Interrupt pending status bit. This bit is a logical "1" if there is no interrupt pending. If one of the interrupt sources occurs, this bit will be set to a logical "0".

= 0 Interrupt pending.

= 1 No interrupt occurs.

Smart Card FIFO control Register (SCFR at base address + 2 when BDLAB = 0, write only)

This register controls FIFO function of Smart Card interface.



Bit 7, 6: RxTL1 and RxTL0 mean receiver FIFO active threshold level control bits. These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes, once there are at least 4 data characters in the receiver FIFO, an interrupt is activated to notify host to read data from FIFO. Default to be 00b.

RxTL1	RxTL0	Rx FIFO Interrupt Active Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 5 ~ 3: Reserved.

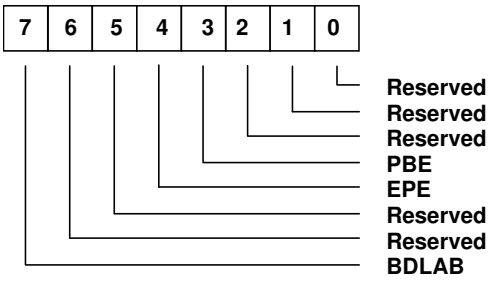
Bit 2: TxFRST means transmitter FIFO reset control bit. Setting this bit to a logical "1" resets the transmitter FIFO counter to initial state. This bit is self-cleared to "0" after being set to "1". Default is "0".

Bit 1: RxFRST means receiver FIFO reset control bit. Setting this bit to a logical "1" resets the receiver FIFO counter to initial state. This bit is self-cleared to "0" after being set to "1". Default is "0".

Bit 0: This bit enables FIFO of Smart Card interface. It should be set to a logical "1" before other bits of SCFR are programmed. Default is "0".

Smart Card Control Register (SCCR at base address + 3)

In contrast to its UART counterpart, Smart Card Control Register only controls parity bit setting because data length is fixed at 8-bit long for Smart Card interface protocol.



Bit 7: BDLAB means baud rate divisor latch access bit. When this bit is set to a logical "1", users may access baud rate divisor (in 16-bit binary format) through divisor latches (BLH and BLL) of baudrate generator during a read/write operation. A special Smart Card ID can also be read at base address + 2 when BDLAB is "1". When this bit is set to "0", accesses to base address + 0, 1 or 2 refer to RBR/TBR, IER or ISR/SCFR respectively.

Bit 6 ~ 5: Reserved.

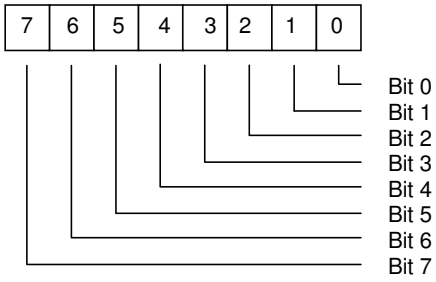
Bit 4: EPE means even parity enable. This bit is only available when bit 3 of SCCR is programmed to "1". It prescribes number of logical 1s in a data word including parity bit. When this bit is set to "1", even parity is required for transmission and reception. Odd parity is demanded when this bit is set to "0".

Bit 3: PBE means parity bit enable. When this bit is set, a parity bit is inserted between last data bit and stop bit for transmission integrity check.

Bit 2 ~ 0: Reserved.

Clock Base Register (CBR at base address + 4, default 0Ch)

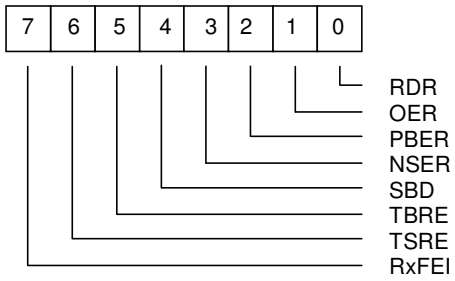
This register combining with BLH and BLL (baud rate latches) determine internal sampling clock frequency. For example, CBR defaults to be 0Ch and BLH, BLL default to be 1Fh which mean SCCLK clock frequency is 372 (12 x 31) times of internal sampling clock frequency. The default values of CBR, BLH and BLL are corresponding to default values of transmission factors F and D specified in ISO/IEC 7816-3. The value of 0Ch of CBR means there're 12 sampling clock pulses to detect a 1-etu (elementary time unit) data bit on SCIO signal. It is recommended that user sets CBR to be around 16 to maintain better data integrity and transmission stability.



Bit 7 ~ 0: Clock base value. It specifies number of internal sampling clock pulses for a data bit. Default to be 0Ch.

Smart Card Status Register (SCSR at base address + 5)

This 8-bit register provides information about status of data transfer during communication.



Bit 7: RxFEI means receiver FIFO error indication. This bit is set to "1" when there is at least one parity bit error, no stop bit error or silent byte detected error in receiver FIFO. It is cleared by reading from SCSR if there is no remaining error left in receiver FIFO.

Bit 6: TSRE means transmitter shift register empty. This bit is set to "1" when transmitter shift register is empty.

Bit 5: TBRE means transmitter buffer register empty. In non-FIFO mode, this bit will be set to a logical 1 when a data byte is transferred from TBR to TSR. If ETBREI of IER is a logical 1, an interrupt is generated to notify host to write the following data bytes. In FIFO mode, this bit is set to "1" when the transmitter FIFO is empty. It is cleared to "0" when host writes data bytes into TBR or FIFO.

Bit 4: SBD means silent byte detected. This bit is set to "1" to indicate that received data byte are kept in silent state for a full byte time, including start bit, data bits, parity bit, and stop bits. In FIFO mode, it indicates the same condition for the data on top of FIFO. When host reads SCSR, it clears this bit to "0".

Bit 3: NSER means no stop bit error. This bit is set to "1" to indicate that received data has no stop bit. In FIFO mode, it indicates the same condition for the data on top of FIFO. When host reads SCSR, it clears this bit to "0".

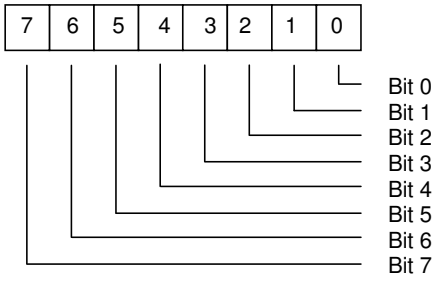
Bit 2: PBER means parity bit error. This bit is set to "1" to indicate that parity bit of received data is wrong. In FIFO mode, it indicates the same condition for the data on top of the FIFO. When host reads SCSR, it clears this bit to "0".

Bit 1: OER means overrun error. This bit is set to "1" to indicate previously received data is overwritten by the next received data before it is read by host. In FIFO mode, it indicates the same condition instead of FIFO full. When host reads SCSR, it clears this bit to "0".

Bit 0: RDR means receiver data ready. This bit is set to "1" to indicate received data is ready to be read by host in RBR or FIFO. If no data are left in RBR or FIFO, the bit is cleared to "0".

Guard Time Register (GTR at base address + 6, default 01h)

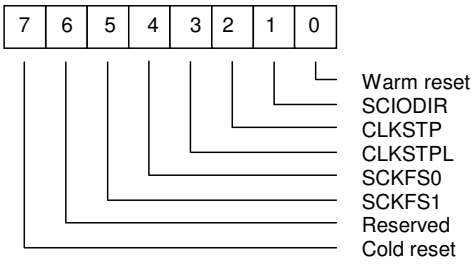
This register specifies number of stop bits appended in the end of data byte.



Bit 7 ~ 0: Guard time values. Default to be 01h.

Extended Control Register (ECR at base address + 7, default 12h)

This register contains reset control bits, clock frequency selection bits, clock stop control bits and SCIO direction control bit.



Bit 7: Cold reset. Setting "1" to this bit turns off power to Smart Card interface by pulling up SCPWR#. SCCLK is stopped, SCRST# kept low, SCIO in input mode and SCLED is inactive. ECR's SCIODIR, SCKFS1 and SCKFS0 control bits and control bits in CBR, GTR, BLH and BLL are cleared to default values. User must write a "0" to this bit to recover to normal state.

Bit 6: Reserved.

Bit 5, 4: SCKFS1 and SCKFS0 means SCCLK frequency selection bit 1 and 0. They selects working clock frequency as following table. Default values are 01h.

SCKFS1, SCKFS0	SCCLK frequency
00	1.5 MHz
01	3.0 MHz
10	6.0 MHz
11	12 MHz

Bit 3: CLKSTP means clock stop control bit. Setting "1" to this bit stops SCCLK at a voltage level specified by CLKSTPL (bit 2 of ECR).

Bit 2: CLKSTPL means clock stop voltage level.

= 0 SCCLK stops at low if CLKSTP is also set to "1".

= 1 SCCLK stops at high if CLKSTP is also set to "1".

Bit 1: SDIODIR means SDIO direction.

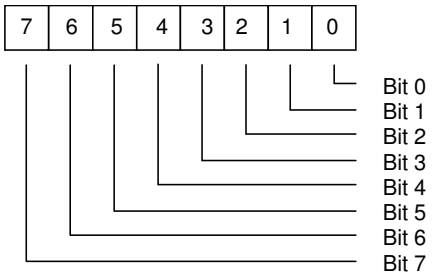
= 0 SDIO is in output mode.

= 1 SDIO is in input mode.

Bit 0: Warm reset. Setting "1" to this bit pulls down SCRST#. SCCLK is stopped, SCIO in input mode and SCLED is inactive. ECR's SCIODIR, SCKFS1 and SCKFS0 control bits and control bits in CBR, GTR, BLH and BLL are cleared to default values. User must write a "0" to this bit to recover to normal state. This bit is similar to cold reset except SCPWR# stays active low.

Baud rate divisor Latch Lower byte (BLL at base address + 0 when BDLAB = 1, default 1Fh)

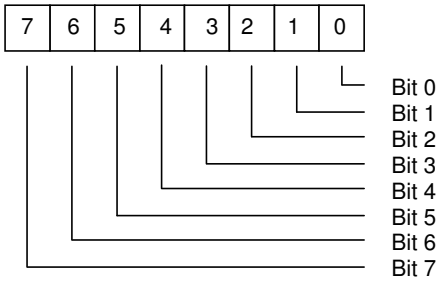
This register combining with BLH and CBR determine internal sampling clock frequency. Refer to section 2.2.8 for example.



Bit 7 ~ 0: Baud rate divisor latch lower byte values. Default to be 1Fh.

Baud rate divisor Latch Higher byte (BLH at base address + 1 when BDLAB = 1, default 00h)

This register combining with BLL and CBR determine internal sampling clock frequency. Refer to section 2.2.8 for example.



Bit 7 ~ 0: Baud rate divisor latch higher byte values. Default to be 00h.

7.3 Smart Card ID Number (base address + 2 when BDLAB = 1, fixed at 70h)

This register contains a specific value of 70h for driver to identify Smart Card interface.

7.4 Functional Description

The following description uses abbreviations to refer to control/status registers and their contents of Smart Card interface as seen in section 2.2. Also, PnP resources of Smart Card interface are assumed to have been programmed and allocated appropriately by system BIOS.

7.5 Initialization

User needs to program control registers so that ATR (Answer To Reset) data streams can be properly decoded after card insertion. Initialization settings include the following steps where sequential order is irrelevant.

1. BLH, BLL and CBR are written with 00h, 1Fh and 0Ch respectively to comply with default transmission factors Fd and Dd which are 372 and 1 as specified in ISO/IEC 7816-3.
2. GTR is programmed with 01h for one stop bit.
3. Set SCFR bit 1 to "1" to enable FIFO.
4. PBE needs to be "1" for parity bit enable but EPE is optional.
5. Set SDIODIR to "1" to put SDIO in reception mode.
6. Set SCKFS1 and SCKFS0 to "01" to select 3 MHz for SCCLK.

Most default values of above control bits are designed as specified in initialization step but it is recommended that user performs all the initialization sequence to avoid any ambiguity.

The relationship between transmission factors and settings of BLH, BLL and CBR is best described in the following example.

$$1\text{etu} = \frac{F}{D} \times \frac{1}{f} \qquad \text{(f means SCCLK frequency)}$$

Therefore,

$$\frac{Fd}{Dd} = \frac{372}{1} = (BLH, BLL) \times CBR = 31 \times 12$$

7.6 Activation

Card insertion pulls up SCPSNT (assuming SCPSNT is active high with CRF0 bit 0 SCPSNT_POL = 0) and in consequence SCPWR# is pulled down to activate power MOS to supply power to card slot after a delay of about 5 ms. This delay is for card slot mechanism to settle down before power is actually applied.

SCCLK starts to output clocks right after SCPWR# is active while SCIO is in reception mode and pulled up externally. SCRST# keeps low initially to reset card but will output high after 512 clock cycles to meet requirement of tb of more than 400 clock cycles (specified in ISO/IEC 7816-3).

To meet another timing requirement, tc of ISO/IEC 7816-3, a counter based on SCCLK is implemented to start counting on the rising edge of SCRST#. SCPWR# is deactivated if no ATR (Answer To Reset) is detected after 65536 clock cycles from the rising edge of SCRST#.

7.7 Answer-to-Reset

Answer-to-Reset (ATR) is the data streams sent by the card to the interface as an answer to a reset on SCRST# signal. Refer to ISO/IEC 7816-3 for detailed description of ATR.

There're two kind of cards specified in ISO/IEC 7816-3, inverse convention card and direct convention card. Although these two conventions treat logical meanings (0 or 1) of voltage levels (low or high) differently, Winbond's implementation of Smart Card interface decodes a high voltage level data bit as "1" and low voltage level data bit "0" nevertheless and resorts to software to interpret incoming data. Software driver needs to interpret initial character of ATR first to determine which convention is for inserted card and chooses a conversion procedure for it. Subsequent incoming data bytes must be passed through a conversion procedure before actually transfers these data bytes to host. Similar conversion procedure must be applied to outgoing data byte before writing to TBR too.

For example, the raw data byte for initial character of inverse-convention ATR would be 03h. Software driver therefore needs a conversion procedure to reverse bit-significance and polarity to process subsequent raw data bytes. On the other hand, initial character of direct-convention ATR is 3Bh which needs no conversion procedure to process data byte.

7.8 Data Transfer

Software driver might need to configure control registers again based on information contained in ATR before process subsequent data transfer. The following guidelines are provided for programming reference.

1. EPE should be set to "1" for direct-convention card and otherwise for inverse-convention card.
2. BLH, BLL and CBR should be set to comply with Fi and Di.
3. GTR is used for various stop bit requirement of different transmission protocols.
4. SCIODIR controls direction of data transfer.
5. Use interrupt resources to control communication sequence.
6. Monitor SCSR for transmission integrity.

7.9 Cold Reset and Warm Reset

Cold reset is achieved by writing a "1" to bit 7 of ECR. It deactivates SCPWR# to high. Consequentially, SCRST# is pulled down and SCCLK is stopped. User must write a "0" to ECR bit 7 to resume Smart Card interface to a normal activation state as described in section 2.3.2 assuming card is still present.

Writing a "1" to ECR bit 0 triggers a warm reset. This is a self-cleared reset operation unlike cold reset which needs explicit cancellation. Its effect is similar to cold reset except SCPWR# is kept activated and therefore power supply to card stays on.

7.10 Power States

W83637HF/HG employs a sophisticated algorithm to partition Smart Card interface's internal circuits to achieve optimal power utilization. However, users must pay extra care in the design of application circuits following guidelines stated below to prevent potential signal conflict and unnecessary power consumption.

There're four power states: disabled state, active state, idle state and power down state. Disabled state is the default state when power is first applied to the IC. Active state is entered by setting a "1" to enable bits at bit 0 of CR30 in logical device 0 (refer to Configuration Register section for details). Idle state means that I/O pins of deselected socket output a predetermined voltage level to disable power to socket and to prevent leakage from floating connections while Smart Card interface core circuits might still be servicing other selected socket. SCPWD (Smart Card Power Down, bit 7 of CR22 global control register) controls whether in active state (SCPWD = 0) or in power down state (SCPWD = 1).

7.11 Disabled State

Smart Card interface is in disabled state initially. Clock is stopped in this state and therefore it is the least power-consuming state. To prevent current leakage from floating connections, it is designed to output a predetermined voltage level on all the I/O pins of Smart Card interface as follows:

SCPWR# outputs high to disable power supply to socket;

SCRST#, SCCLK, SCIO, SCC4, SCC8 and SCLED output low;

SCPSNT is tri-stated.

These I/O conditions also apply to both socket A and socket B in power down state (SCPWD = 1) or deselected socket in idle state. Designers of application circuits must take extra care so that no contention occurs when Smart Card interface is in those power-saving states. Please refer to Winbond's recommended application circuit for example.

7.12 Active State

Active state is when Smart Card interface is actually performing all its functions: configuration of control and interrupt registers, detection of card insertion/extraction, reception of ATR (Answer to Reset) packet and communication of information between host and card. Refer to section 2.3 for detailed function description.

Smart Card interface enters active state by setting a "1" to bit 0 of CR30 in logical device 0. This is the most power-consuming state and actual power consumption is dependent on traffic of interface.

7.13 Idle State

W83637HF/HG supports up to two Smart Card sockets. Only one socket could be active at a time and the other deselected socket is considered to be in idle state. Selection of active socket is controlled through socket selection bits which are bits 0 at base address + 3. I/O pins of deselected socket also output a predetermined voltage level as described in section 2.4.1. Power consumption in this state is similar to active state because one of the two sockets is selected and core circuit is still functioning.

There is no idle state for W83637HF/HG because only one Smart Card socket is supported and it is always selected.

7.14 Power Down State

Transition from active state to power down state is accomplished by setting SCPWD to "1". Clock is stopped for most internal core circuits except detection circuit for SCPSNT toggle (card insertion/extraction). SCPWD could be reset by SCPSNT toggle and through this feature Smart Card interface in power down state can be waken up by card insertion/extraction. User may also directly write a "0" to SCPWD to wake up Smart Card interface.

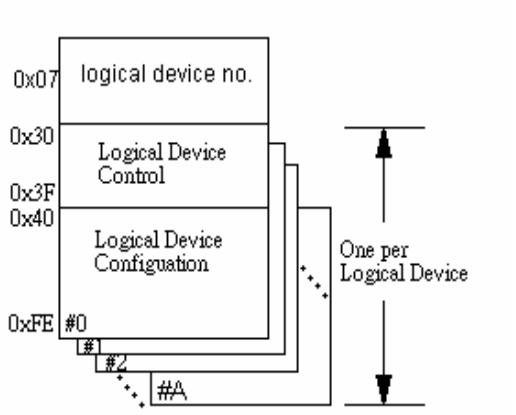
Smart Card interface spends a little bit more power to maintain SCPSNT toggle detection circuit in power down state than in disabled state while spares even more power than in active state by stopping clock to core circuit.

Users must make sure that all on-going transactions are concluded before putting Smart Card interface into power down state to prevent potential miss-operation of internal state machine.

8. CONFIGURATION REGISTER

8.1 Plug and Play Configuration

W83637HF/HG uses Compatible PNP protocol to access configuration registers for setting up different types of configurations. In W83637HF/HG, there are eleven Logical Devices (from Logical Device 0 to Logical Device B with the exception of logical device 4 for backward compatibility) which correspond to eleven individual functions: FDC (logical device 0), PRT (logical device 1), UART1 (logical device 2), UART2 (logical device 3), KBC (logical device 5), CIR (Consumer IR, logical device 6), GPIO1 (logical device 7), GPIO2 (logical device 8), GPIO3 (logical device 9), ACPI ((logical device A), and hardware monitor (logical device B). Each Logical Device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logical device number into logical device select register at CR7.



8.1.1 Compatible PnP

8.1.1.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

HEFRAS	Address and Value
0	Write 87h to the location 2Eh twice
1	Write 87h to the location 4Eh twice

After Power-on reset, the value on RTSA# (pin 43) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 2Eh or 4Eh). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Functions Index Register (I/O port address 2Eh or 4Eh same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 2Fh or 4Fh).

After programming of the configuration register is finished, an additional value (AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

8.1.1.2 Extended Functions Enable Registers (EFERs)

After a power-on reset, the W83637HF/HG enters the default operating mode. Before the W83637HF/HG enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 2Eh or 4Eh (as described in previous section).

8.1.1.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers (EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 2Eh or 4Eh (as described in section 12.2.1) on PC/AT systems; the EFDRs are read/write registers with port address 2Fh or 4Fh (as described in section 9.2.1) on PC/AT systems.

8.1.2 Configuration Sequence

To program W83637HF/HG configuration registers, the following configuration sequence must be followed:

(1). Enter the extended function mode

(2). Configure the configuration registers

(3). Exit the extended function mode

8.1.2.1 Enter the extended function mode

To place the chip into the extended function mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

8.1.2.2 Configuration the configuration registers

The chip selects the logical device and activates the desired logical devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). EFIR is located at the same address as EFER, and EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e., 0x07) to the EFIR and then write the number of the desired logical device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the logical device to the EFIR and then write (or read) the desired configuration register through EFDR.

8.1.2.3 Exit the extended function mode

To exit the extended function mode, one write of 0xAA to EFER is required. Once the chip exits the extended function mode, it is in the normal running mode and is ready to enter the configuration mode.

8.1.2.4 Software programming example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so EFIR is located at 2Eh and EFDR is located at 2Fh. If HEFRAS (CR26 bit 6) is set, 4Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;-------------------------------------------------------------------------------
; Enter the extended function mode ,interruptible double-write      |
;-------------------------------------------------------------------------------
MOV    DX,2EH
MOV    AL,87H
OUT    DX,AL
OUT    DX,AL
;-------------------------------------------------------------------------
; Configuration logical device 1, configuration register CRF0     |
;-------------------------------------------------------------------------
MOV    DX,2EH
MOV    AL,07H
OUT    DX,AL           ; point to Logical Device Number Reg.
MOV    DX,2FH
MOV    AL,01H
OUT    DX,AL           ; select logical device 1
;
MOV    DX,2EH
MOV    AL,F0H
OUT    DX,AL           ; select CRF0
MOV    DX,2FH
MOV    AL,3CH
OUT    DX,AL           ; update CRF0 with value 3CH
;-----------------------------------------
; Exit extended function mode       |
;-----------------------------------------
MOV    DX,2EH
MOV    AL,AAH
OUT    DX,AL
```

8.2 The PNP ID of the W83637HF/HG Card Reader Device (For BIOS Programming use)

SC (smart card reader)	**:**	**WEC0513**
MS (memory stick reader)	**:**	**WEC0515**

8.3 Chip (Global) Control Register

CR02 (Default 0x00)

Bit 7 - 1 : Reserved.
Bit 0 : SWRST --> Soft Reset.

CR07

Bit 7 - 0 : LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

CR20

Bit 7 - 0 : DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0 = 0x70 (read only).

CR21

Bit 7 - 0 : DEVREVB7 - DEBREVB0 --> Device Rev Bit 7 - Bit 0 = 0x8y (read only, y is version no).

CR22 (Default 0xff)

Bit 7 : Reserved.
Bit 6 : HMPWD
= 0 Power down
= 1 No Power down
Bit 5 : URBPWD
= 0 Power down
= 1 No Power down
Bit 4 : URAPWD
= 0 Power down
= 1 No Power down
Bit 3 : PRTPWD
= 0 Power down
= 1 No Power down
Bit 2 : MSPWD
= 0 Power down
= 1 No Power down
Bit 1 Reserved
Bit 0 : FDCPWD
= 0 Power down
= 1 No Power down

CR23 (Default 0x00)

Bit 7 - 1 : Reserved.

Bit 0 : IPD (Immediate Power Down). When set to 1, it will put the whole chip into power down mode immediately.

CR24 (Default 0b1s000s0s)

Bit 7 : EN16SA

= 0 12 bit Address Qualification

= 1 16 bit Address Qualification

Bit 6 :CLKSEL

= 0 The clock input on Pin 1 should be 24 Mhz.

= 1 The clock input on Pin 1 should be 48 Mhz.

The corresponding power-on setting pin is SOUTB (pin 83).

Bit 5 - 3 : Reserved

Bit 2 : ENKBC

= 0 KBC is disabled after hardware reset.

= 1 KBC is enabled after hardware reset.

This bit is read only, and set/reset by power-on setting pin. The corresponding power-on setting pin is SOUTA (pin 54).

Bit 1 : Reserved

Bit 0 : PNPCSV

= 0 The Compatible PnP address select registers have default values.

= 1 The Compatible PnP address select registers have no default value.

When trying to make a change to this bit, new value of PNPCVS must be complementary to the old one to make an effective change. For example, the user must set PNPCVS to 0 first and then reset it to 1 to reset these PnP registers if the present value of PNPCVS is 1. The corresponding power-on setting pin is NDTRA (pin 52).

CR25 (Default 0x00)

Bit 7 - 6 : Reserved

Bit 5 : URBTRI

Bit 4 : URATRI

Bit 3 : PRTTRI

Bit 2 - 1 : Reserved

Bit 0 : FDCTRI.

CR26 (Default 0b0s000000)

Bit 7 : SEL4FDD

= 0 Select two FDD mode.

= 1 Select four FDD mode.

Bit 6 : HEFRAS

These two bits define how to enable Configuration mode. The corresponding power-on setting pin is NRTSA (pin 51).

HEFRAS Address and Value

= 0 Write 87h to the location 2E twice.

= 1 Write 87h to the location 4Etwice.

Bit 5 : LOCKREG

= 0 Enable R/W Configuration Registers

= 1 Disable R/W Configuration Registers.

Bit 4 :Reserve

Bit 3 : DSFDLGRQ

= 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective on selecting IRQ

= 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective on selecting IRQ

Bit 2 : DSPRLGRQ

= 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ

= 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ

Bit 1 : DSUALGRQ

= 0 Enable UART A legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ

= 1 Disable UART A legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

Bit 0 : DSUBLGRQ

= 0 Enable UART B legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ

= 1 Disable UART B legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

CR28 (Default 0x00)

Bit 7 : PIN5S and PIN7S
= 0 pin5 and pin 7 is selected FDC(DSB and MOS) function
= 1 pin5 and pin 7 is selected FAN3(FANIN3 and FANPWM3) function

Bit 6 : PIN105S
= 0 pin105 is selected HM(OVT#) function
= 1 pin105 is selected HM(SMI#) function

Bit 5 : PIN91S and PIN92S
= Reserved
= 1 Select by CR2B Bit 7 & 6 for SCC4 & SCC8 or GPIO 21 & 22.

Bit 4 : PIN93S
= 0 pin 93 (MSCLK) is setting 8 fingers.
= 1 pin 93 (MSCLK) is setting 6 fingers.

Bit 3 : PIN91S, PIN92S, PIN94S, PIN95S and PIN96S
= 0 pin 91, 92, 94, 95 and 96 are setting 8 fingers.
= 1 pin 91, 92, 94, 95 and 96 are setting 6 fingers.

Bit 2 - 0 : PRTMODS2 - PRTMODS0
= 0xx Parallel Port Mode
= 100 Reserved
= 101 External FDC Mode
= 110 Reserved
= 111 External two FDC Mode

CR29 (GPIO3 multiplexed pin selection register. VBAT powered. Default 0x00)

Bit 7 : PIN64S
= 0 SUSLED (SUSLED control bits are in CRF3 of Logical Device 9)
= 1 GP35

Bit 6 : PIN69S
= 0 CIRRX#
= 1 GP34

Bit 5 : PIN70S
= 0 RSMRST#
= 1 GP33

Bit 4 : PIN71S
= 0 PWROK
= 1 GP32

Bit 3 : PIN72S
= 0 PWRCTL#
= 1 GP31

Bit 2 : PIN 73S
= 0 SLP_SX#
= 1 GP30

Bit 1 : Reserved

Bit 0 : Reserved

CR2A (GPIO multiplexed pin selection register 1. VCC powered. Default 0X7C)

Bit 7 : Port Select (select Game Port or General Purpose I/O Port 1)
= 0 Game Port
= 1 General Purpose I/O Port 1
pin121~128 select function GP10~GP17 or KBC Port 1)

Bit 6 : PIN128S
= 0 8042 P12
= 1 GP10

Bit 5 : PIN127S
= 0 8042 P13
= 1 GP11

Bit 4 : PIN126S
= 0 8042 P14
= 1 GP12

Bit 3 : PIN125S
= 0 8042 P15
= 1 GP13

Bit 2 : PIN124S
= 0 8042 P16
= 1 GP14

Bit 1 : PIN120S
= 0 MSO (MIDI Serial Output)
= 1 IRQIN0 (select IRQ resource through CRF4 Bit 7-4 of Logical Device 8)

Bit 0 : PIN119S
= 0 MS1 (MIDI Serial Input)
= 1 GP20

CR2B(GPIO multiplexed pin selection register 2. VCC powered. Default 0XC0)

Bit 7 : PIN92S
= 0 Reserved
= 1 GP21

Bit 6 : PIN91S
= 0 Reserved
= 1 GP22

Bit 5 : PIN90S
= 0 PLED (PLED0 control bits are in CRF5 of Logical Device 8)
= 1 GP23

Bit 4 : PIN89S
= 0 WDTO (Watch Dog Timer is controlled by CRF5, CRF6, CRF7 of Logical Device 8)
= 1 GP24

CR2B(GPIO multiplexed pin selection register 2. VCC powered. Default 0XC0), continued

Bit 3 : PIN88S
= 0 IRRX
= 1 GP25
Bit 2 : PIN87S
= 0 IRTX
= 1 GP26
Bit 1-0 :PIN 2S
= 00 SCLED.
= 01 SMI#.
= 10 IRQIN1 (select IRQ resource through CRF4 Bit 7-4 of Logical Device8) SMI#
= 11 Reserved.

CR2C (Default 0x00)

Bit 7-1 : Reserved
Bit 0 : MS/SD Multi-Function Pin Select(Pin 58,75,91-96)
= 0 Memory Stick
= 1 Secure Digital

CR2E (Default 0x00)

Test Modes: Reserved for Winbond.

CR2F (Default 0x00)

Test Modes: Reserved for Winbond.

8.3.1 Logical Device 0 (FDC)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 1 : Reserved.
Bit 0 = 1 Activates the logical device.
= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0xf0 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select FDC I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x06 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4 : Reserved.
Bit 3 - 0 : These bits select IRQ resource for FDC.

CR74 (Default 0x02 if PNPCSV = 0 during POR, default 0x04 otherwise)

Bit 7 - 3 : Reserved.

Bit 2 - 0 : These bits select DRQ resource for FDC.

= 0x00 DMA0
= 0x01 DMA1
= 0x02 DMA2
= 0x03 DMA3
= 0x04 - 0x07 No DMA active

CRF0 (Default 0x0E)

FDD Mode Register

Bit 7 : FIPURDWN

This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0, DSKCHG, and WP.

= 0 The internal pull-up resistors of FDC are turned on.(Default)
= 1 The internal pull-up resistors of FDC are turned off.

Bit 6 : INTVERTZ

This bit determines the polarity of all FDD interface signals.

= 0 FDD interface signals are active low.
= 1 FDD interface signals are active high.

Bit 5 : DRV2EN (PS2 mode only)

When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

Bit 4 : Swap Drive 0, 1 Mode

= 0 No Swap (Default)
= 1 Drive and Motor select 0 and 1 are swapped.

Bit 3 - 2 :Interface Mode

= 11 AT Mode (Default)
= 10 (Reserved)
= 01 PS/2
= 00 Model 30

Bit 1 : FDC DMA Mode

= 0 Burst Mode is enabled
= 1 Non-Burst Mode (Default)

Bit 0 : Floppy Mode

= 0 Normal Floppy Mode (Default)
= 1 Enhanced 3-mode FDD

CRF1 (Default 0x00)

Bit 7 - 6 : Boot Floppy
- = 00 FDD A
- = 01 FDD B
- = 10 FDD C
- = 11 FDD D

Bit 5, 4 : Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.

Bit 3 - 2 : Density Select
- = 00 Normal (Default)
- = 01 Normal
- = 10 1 (Forced to logic 1)
- = 11 0 (Forced to logic 0)

Bit 1 : DISFDDWR
- = 0 Enable FDD write.
- = 1 Disable FDD write(forces pins WE, WD stay high).

Bit 0 : SWWP
- = 0 Normal, use WP to determine whether the FDD is write protected or not.
- = 1 FDD is always write-protected.

CRF2 (Default 0xFF)

Bit 7 - 6 : FDD D Drive Type
Bit 5 - 4 : FDD C Drive Type
Bit 3 - 2 : FDD B Drive Type
Bit 1 - 0 : FDD A Drive Type

CRF4 (Default 0x00)

FDD0 Selection:

Bit 7 : Reserved.
Bit 6 : Pre-comp. Disable.
- = 1 Disable FDC Pre-compensation.
- = 0 Enable FDC Pre-compensation.

Bit 5 : Reserved.
Bit 4 - 3 : DRTS1, DRTS0: Data Rate Table select (Refer to TABLE A).
- = 00 Select Regular drives and 2.88 format
- = 01 3-mode drive
- = 10 2 Meg Tape
- = 11 Reserved

Bit 2 : Reserved.
Bit 1:0 : DTYPE0, DTYPE1: Drive Type select (Refer to TABLE B).

CRF5 (Default 0x00)

FDD1 Selection: Same as FDD0 of CRF4.

TABLE A

Drive Rate Table Select		Data Rate		Selected Data Rate		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0(pin 2)	DRVDEN1(pin 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5”“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

8.3.2 Logical Device 1 (Parallel Port)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 1 : Reserved.
Bit 0 = 1 Activates the logical device.
= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0x78 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Parallel Port I/O base address.
[0x100:0xFFC] on 4 byte boundary (EPP not supported) or
[0x100:0xFF8] on 8 byte boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR70 (Default 0x07 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4 : Reserved.
Bit [3:0] : These bits select IRQ resource for Parallel Port.

CR74 (Default 0x04)

Bit 7 - 3 : Reserved.
Bit 2 - 0 : These bits select DRQ resource for Parallel Port.
0x00 = DMA0
0x01 = DMA1
0x02 = DMA2
0x03 = DMA3
0x04 - 0x07= No DMA active

CRF0 (Default 0x3F)

Bit 7 : Reserved.
Bit 6 - 3 : ECP FIFO Threshold.
Bit 2 - 0 : Parallel Port Mode (CR28 PRTMODS2 = 0)
= 100 Printer Mode (Default)
= 000 Standard and Bi-direction (SPP) mode
= 001 EPP - 1.9 and SPP mode
= 101 EPP - 1.7 and SPP mode
= 010 ECP mode
= 011 ECP and EPP - 1.9 mode
= 111 ECP and EPP - 1.7 mode.

8.3.3 Logical Device 2 (UART A)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 1 : Reserved.
Bit 0 = 1 Activates the logical device.
= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 1 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x04 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4 : Reserved.
Bit 3 - 0 : These bits select IRQ resource for Serial Port 1.

CRF0 (Default 0x00)

Bit 7 - 2 : Reserved.
Bit 1 - 0 : SUACLKB1, SUACLKB0
= 00 UART A clock source is 1.8462 Mhz (24MHz/13)
= 01 UART A clock source is 2 Mhz (24MHz/12)
= 10 UART A clock source is 24 Mhz (24MHz/1)
= 11 UART A clock source is 14.769 Mhz (24 MHz/1.625)

8.3.4 Logical Device 3 (UART B)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 1 : Reserved.
Bit 0 = 1 Activates the logical device.
= 0 Logical device is inactive.

CR60, CR 61 (Default 0x02, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 2 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x03 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4 : Reserved.
Bit [3:0] : These bits select IRQ resource for Serial Port 2.

CRF0 (Default 0x00)

Bit 7 - 4 : Reserved.

Bit 3 : RXW4C

= 0 No reception delay when SIR is changed from TX mode to RX mode.

= 1 Reception delays 4 characters-time (40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2 : TXW4C

= 0 No transmission delay when SIR is changed from RX mode to TX mode.

= 1 Transmission delays 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.

Bit 1 - 0 : SUBCLKB1, SUBCLKB0

= 00 UART B clock source is 1.8462 MHz (24MHz/13)

= 01 UART B clock source is 2 MHz (24MHz/12)

= 10 UART B clock source is 24 MHz (24MHz/1)

= 11 UART B clock source is 14.769 MHz (24 MHz/1.625)

CRF1 (Default 0x00)

Bit 7 : Reserved.

Bit 6 : IRLOCSEL. IR I/O pins' location select.

= 0 Through SINB/SOUTB.

= 1 Through IRRX/IRTX.

Bit 5 : IRMODE2. IR function mode selection bit 2.

Bit 4 : IRMODE1. IR function mode selection bit 1.

Bit 3 : IRMODE0. IR function mode selection bit 0.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

Bit 2 : HDUPLX. IR half/full duplex function select.
= 0 The IR function is Full Duplex.
= 1 The IR function is Half Duplex.
Bit 1 : TX2INV
= 0 The SOUTB pin of UART B function or IRTX pin of IR function in normal condition.
= 1 Inverse the SOUTB pin of UART B function or IRTX pin of IR function.
Bit 0 : RX2INV.
= 0 The SINB pin of UART B function or IRRX pin of IR function in normal condition.
= 1 Inverse the SINB pin of UART B function or IRRX pin of IR function

8.3.5 Logical Device 5 (KBC)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 1 : Reserved.
Bit 0 = 1 Activates the logical device.
= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x60 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the first KBC I/O base address [0x100:0xFFF] on 1 byte boundary.

CR62, CR 63 (Default 0x00, 0x64 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the second KBC I/O base address [0x100:0xFFF] on 1 byte boundary.

CR70 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4 : Reserved.
Bit [3:0] : These bits select IRQ resource for KINT (keyboard).

CR72 (Default 0x0C if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit 7 - 4 : Reserved.
Bit [3:0] : These bits select IRQ resource for MINT (PS2 Mouse)

CRF0 (Default 0x80)

Bit 7 - 6 : KBC clock rate selection
= 00 Select 6 MHz as KBC clock input.
= 01 Select 8 MHz as KBC clock input.
= 10 Select 12 MHz as KBC clock input.
= 11 Select 16 MHz as KBC clock input.
(W83637HF-AW can support these 4 kinds of clock input)
Bit 5 - 3 : Reserved.
Bit 2 = 0 Port 92 disable.
= 1 Port 92 enable.
Bit 1 = 0 Gate20 software control.
= 1 Gate20 hardware speed up.
Bit 0 = 0 KBRST software control.
= 1 KBRST hardware speed up.

8.3.6 Logical Device 6 (CIR)

CR30 (Default 0x00)

Bit 7 - 1 : Reserved.
Bit 0 = 1 Activates the logical device.
= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select CIR I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x00)

Bit 7 - 4 : Reserved.
Bit [3:0] : These bits select IRQ resource for CIR.

8.3.7 Logical Device 7 (Game Port and MIDI Port and GPIO Port 1)

CR30 (Default 0x00)

Bit 7 - 1 : Reserved.
Bit 0 = 1 Activate Game Port and MIDI Port.
= 0 Game Port and MIDI Port is inactive.

CR60, CR 61 (Default 0x02, 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the Game Port base address [0x100:0xFFF] on 1 byte boundary.

CR62, CR 63 (Default 0x03, 0x30 if PNPCSV = 0 during POR, default 0x00 otherwise)
These two registers select the MIDI Port base address [0x100:0xFFF] on 2 byte boundary.

CR70 (Default 0x09 if PNPCSV = 0 during POR, default 0x00 otherwise)
Bit 7 - 4 : Reserved.
Bit [3:0] : These bits select IRQ resource for MIDI Port.

CRF0 (GP10-GP17 I/O selection register. Default 0xFF)
When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP10-GP17 data register. Default 0x00)
If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP10-GP17 inversion register. Default 0x00)
When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

8.3.8 Logical Device 8 (GPIO Port 2 This power of the Port is VCC source)

CR30 (GP20-GP27 Default 0x00)
Bit 7 - 1 : Reserved.
Bit 0 = 1 Activate GPIO2.
= 0 GPIO2 is inactive.

CRF0 (GP20-GP27 I/O selection register. Default 0xFF)
When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP20-GP27 data register. Default 0x00)
If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP20-GP27 inversion register. Default 0x00)
When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (Default 0x00)

Bit 7 - 4 : These bits select IRQ resource for IRQIN1.
Bit 3 - 0 : These bits select IRQ resource for IRQIN0.

CRF4 (Reserved)

CRF5 (PLED mode register. Default 0x00)

Bit 7-6 : select PLED mode
= 00 Power LED pin is tri-stated.
= 01 Power LED pin is driven low.
= 10 Power LED pin is a 1Hz toggle pulse with 50 duty cycle
= 11 Power LED pin is a 1/4Hz toggle pulse with 50 duty cycle.
Bit 5-4 : Reserved
Bit 3 : select WDTO count mode.
= 0 Second
= 1 Minute
Bit 2 : Enable the rising edge of keyboard Reset(P20) to force Time-out event.
= 0 Disable
= 1 Enable
Bit 1-0 : Reserved

CRF6 (Default 0x00)

Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. If the Bit 7 and Bit 6 are set, any Mouse Interrupt or Keyboard Interrupt event will also cause the reload of previously-loaded non-zero value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value.

Bit 7 - 0 = 0x00 Time-out Disable
= 0x01 Time-out occurs after 1 second/minute
= 0x02 Time-out occurs after 2 second/minutes
= 0x03 Time-out occurs after 3 second/minutes
.....
= 0xFF Time-out occurs after 255 second/minutes

CRF7 (Default 0x00)

Bit 7 : Mouse interrupt reset Enable or Disable
= 1 Watch Dog Timer is reset upon a Mouse interrupt
= 0 Watch Dog Timer is not affected by Mouse interrupt
Bit 6 : Keyboard interrupt reset Enable or Disable
= 1 Watch Dog Timer is reset upon a Keyboard interrupt
= 0 Watch Dog Timer is not affected by Keyboard interrupt
Bit 5 : Force Watch Dog Timer Time-out, Write only*
= 1 Force Watch Dog Timer time-out event; this bit is self-clearing.
Bit 4 : Watch Dog Timer Status, R/W
= 1 Watch Dog Timer time-out occurred
= 0 Watch Dog Timer counting
Bit 3 -0 : These bits select IRQ resource for Watch Dog. Setting of 2 selects SMI.

8.3.9 Logical Device 9 (GPIO Port 3 This power of the Port is standby source (VSB))

CR30 (Default 0x00)

Bit 7 - 1 : Reserved
Bit 0 = 1 Activate GPIO3.
= 0 GPIO3 is inactive.

CRF0 (GP30-GP35 I/O selection register. Default 0xFF Bit 7-6: Reserve)

When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP30-GP35 data register. Default 0x00 Bit 7-6: Reserve)

If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP30-GP35 inversion register. Default 0x00 Bit 7-6: Reserve)

When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (SUSLED mode register. Default 0x00)

Bit 7-6 : select Suspend LED mode
= 00 Suspend LED pin is drove low.
= 01 Suspend LED pin is tri-stated.
= 10 Suspend LED pin is a 1Hz toggle pulse with 50 duty cycle.
= 11 Suspend LED pin is a 1/4Hz toggle pulse with 50 duty cycle.
This mode selection bit 7-6 keep its settings until battery power loss.
Bit 5 - 0 : Reserved.

8.4 Logical Device A (ACPI)

(The CR30, 70, F0~F9 are VCC power source; CR E0~E7 are VRTC power source)

CR30 (Default 0x00)

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activates the logical device.

= 0 Logical device is inactive.

CR70 (Default 0x00)

Bit 7 - 4 : Reserved.

Bit 3 - 0 : These bits select IRQ resources for $\overline{\text{PME}}$.

CRE0 (Default 0x00)

Bit 7 : DIS-PANSW_IN. Disable panel switch input to turn system power supply on.

= 0 PANSW_IN is wire-ANDed and connected to PANSW_OUT.

= 1 PANSW_IN is blocked and can not affect PANSW_OUT.

Bit 6 : ENKBWAKEUP. Enable Keyboard to wake-up system via PANSW_OUT.

= 0 Disable Keyboard wake-up function.

= 1 Enable Keyboard wake-up function.

Bit 5 : ENMSWAKEUP. Enable Mouse to wake-up system via PANSW_OUT.

= 0 Disable Mouse wake-up function.

= 1 Enable Mouse wake-up function.

Bit 4 : MSRKEY. This bit combining with MSXKEY (bit 1 of CRE0 of logical device A) and ENMDAT_UP (bit 7 of CRE6 of logical device A) define what kind of mouse wake-up event can trigger an active low pulse on PSOUT#. Their combination is described in the following table.

ENMDAT_UP	MSRKEY	MSXKEY	Wake up event
1	x	1	Any button click or any movement
1	x	0	one click of left/right button
0	0	1	one click of left button
0	1	1	one click of right button
0	0	0	two times click of left button
0	1	0	two times click of right button

Bit 3 : ENCIRWAKEUP. Enable CIR to wake-up system via PSOUT#.

= 0 Disable CIR wake-up function.

= 1 Enable CIR wake-up function.

Bit 2 : KB/MS Swap. Enable Keyboard/Mouse port-swap.

= 0 Keyboard/Mouse ports are not swapped.

= 1 Keyboard/Mouse ports are swapped.

Bit 1 : MSXKEY. This bit combining with MSRKEY (bit 4 of CRE0 of logical device A) and ENMDAT_UP (bit 7 of CRE6 of logical device A) define what kind of mouse wake-up event can trigger an active low pulse on PSOUT#. Their combination is described in the following table.

ENMDAT_UP	MSRKEY	MSXKEY	Wake up event
1	x	1	Any button click or any movement
1	x	0	One click of left/right button
0	0	1	One click of left button
0	1	1	One click of right button
0	0	0	Two times click of left button
0	1	0	Two times click of right button

Bit 0 : KBXKEY. Enable any character received from Keyboard to wake-up the system

= 0 Only predetermined specific key combination can wake up the system.

= 1 Any character received from Keyboard can wake up the system.

CRE1 (Default 0x00) Keyboard Wake-Up Index Register

This register is used to indicate which Keyboard Wake-Up Shift register or Predetermined key Register is to be read/written via CRE2. The first set of wake up key combination is in the range of 0x00 - 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combination can be read through 0x10 – 0x1E. The range of CIR wake-up index register is in 0x20 - 0x2F.

CRE2 Keyboard Wake-Up Data Register

This register holds the value of wake-up key register indicated by CRE1. This register can be Read / written.

CRE3 (Read only) Keyboard/Mouse Wake-Up Status Register

Bit 7-5 : Reserved.

Bit 4 : PWRLOSS_STS: This bit is set when power loss occurs.

Bit 3 : CIR_STS. The Panel switch event is caused by CIR wake-up event. This bit is cleared by reading this register.

Bit 2 : PANSW_STS. The Panel switch event is caused by PANSW_IN. This bit is cleared by reading this register.

Bit 1 : Mouse_STS. The Panel switch event is caused by Mouse wake-up event. This bit is cleared by reading this register.

Bit 0 : Keyboard_STS. The Panel switch event is caused by Keyboard wake-up event. This bit is cleared by reading this register.

CRE4 (Default 0x00)

Bit 7 : Power loss control bit 2.
0 = Disable ACPI resume
1 = Enable ACPI resume

Bit 6-5 : Power loss control bit <1:0>
00 = System always turn off when come back from power loss state.
01 = System always turn on when come back from power loss state.
10 = System turn on/off when come back from power loss state depend on the state before power loss.
11 = Reserved.

Bit 4 : Suspend clock source select
0 = Use internal clock source.
1 = Use external suspend clock source(32.768KHz).

Bit 3 : Keyboard wake-up type select for wake-up the system from S1/S2.
0 = Password or Hot keys programmed in the registers.
1 = Any key.

Bit 2 : Enable all wake-up event set in CRE0 can wake-up the system from S1/S2 state. This bit is cleared when wake-up event occurs.
0 = Disable.
1 = Enable.

Bit 1 - 0 : Reserved.

CRE5 (Default 0x00)

Bit 7 : Reserved.

Bit 6 - 0 : Compared Code Length. When the compared codes are storied in the data register, these data length should be written to this register.

CRE6 (Default 0x00)

Bit 7 : ENMDAT_UP. This bit combining with MSRKEY (bit 4 of CRE0 of logical device A) and MSXKEY (bit 1 of CRE0 of logical device A) define what kind of mouse wake-up event can trigger an active low pulse on PSOUT#. Their combination is described in the following table.

ENMDAT_UP	MSRKEY	MSXKEY	Wake up event
1	x	1	Any button click or any movement
1	x	0	One click of left/right button
0	0	1	One click of left button
0	1	1	One click of right button
0	0	0	Two times click of left button
0	1	0	Two times click of right button

CRE6 (Default 0x00), continued

Bit6 : EN_SCUP. Enable SCPSNT# of Smart Card interface to wake up system through PSOUT#.

0 = Disable.

1 = Enable.

Bit 5 - 0 : CIR Baud Rate Divisor. The clock base of CIR is 32khz, so that the baud rate is 32khz divided by (CIR Baud Rate Divisor + 1).

CRE7 (Default 0x00)

Bit 7 : ENKD3. Enable the third set of keyboard wake-up key combinations. Its values are accessed through keyboard wake-up index register (CRE1 of logical device A) and keyboard wake-up data register (CRE2 of logical device A) at index from 40h to 4eh.

= 0 Disable wake-up function of the third set of key combinations.

= 1 Enable wake-up function of the third set of key combinations.

Bit 6 : ENKD2. Enable the second set of keyboard wake-up key combinations. Its values are accessed through keyboard wake-up index register (CRE1 of logical device A) and keyboard wake-up data register (CRE2 of logical device A) at index from 30h to 3eh.

= 0 Disable wake-up function of the second set of key combinations.

= 1 Enable wake-up function of the second set of key combinations.

Bit 5 : ENWIN98KEY. Enable WIN98 keyboard dedicated key to wake up system through PANSW_OUT if keyboard wake up function is enabled.

0 = Disable WIN98 keyboard wake up.

1 = Enable WIN98 keyboard wake up.

Bit 4 : EN_ONPSOUT. Enable to issue a 0.5 s long PSOUT# pulse when system returns from power loss state and is supposed to be on as described in CRE4 bit 6, 5 of logical device A.

0 = Disable this function.

1 = Enable this function.

Bit 3 : SELWDTORST: Select whether Watch Dog timer function is reset by LRESET_L signal or PWROK signal.

0 = Watch Dog timer function is reset by LRESET_L signal.

1 = Watch Dog timer function is reset by PWROK signal.

Bit 2 : Reset CIR Power-On function. After using CIR power-on, the software should write logical 1 to restart CIR power-on function.

Bit 1 : Invert RX Data.

= 1 Inverting RX Data.

= 0 Not inverting RX Data.

Bit 0 : Enable Demodulation.

= 1 Enable received signal to demodulate.

= 0 Disable received signal to demodulate.

CRF0 (Default 0x00)

Bit 7 : CHIPPME. Chip level auto power management enable.
= 0 Disable the auto power management functions
= 1 Enable the auto power management functions.
Bit 6 : CIRPME. Consumer IR port auto power management enable.
= 0 Disable the auto power management functions
= 1 Enable the auto power management functions.
Bit 5 : MIDIPME. MIDI port auto power management enable.
= 0 Disable the auto power management functions
= 1 Enable the auto power management functions.
Bit 4 : Reserved. Return zero when read.
Bit 3 : PRTPME. Printer port auto power management enable.
= 0 Disable the auto power management functions.
= 1 Enable the auto power management functions.
Bit 2 : FDCPME. FDC auto power management enable.
= 0 Disable the auto power management functions.
= 1 Enable the auto power management functions.
Bit 1 : URAPME. UART A auto power management enable.
= 0 Disable the auto power management functions.
= 1 enable the auto power management functions.
Bit 0 : URBPME. UART B auto power management enable.
= 0 Disable the auto power management functions.
= 1 Enable the auto power management functions.

CRF1 (Default 0x00)

Bit 7 : WAK_STS. This bit is set when the chip is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by writing a 1 to this bit position or by the sleeping/working state machine automatically when the global standby timer expires.
= 0 The chip is in the sleeping state.
= 1 The chip is in the working state.
Bit 6 - 5 : Devices' trap status.
Bit 4 : Reserved. Return zero when read.
Bit 3 - 0 : Devices' trap status.

CRF3 (Default 0x00)

Bit 7 - 0 : Device's IRQ status.

These bits indicate the IRQ status of the individual device respectively. The device's IRQ status bit is set by their source device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 7 : MSIRQSTS. MS IRQ status.

Bit 6 : Reserved

Bit 5 : MOUIRQSTS. MOUSE IRQ status.

Bit 4 : KBCIRQSTS. KBC IRQ status.

Bit 3 : PRTIRQSTS. printer port IRQ status.

Bit 2 : FDCIRQSTS. FDC IRQ status.

Bit 1 : URAIRQSTS. UART A IRQ status.

Bit 0 : URBIRQSTS. UART B IRQ status.

CRF4 (Default 0x00)

Bit 7 : Reserved. Return zero when read.

Bit 6 - 0 : These bits indicate the IRQ status of the individual GPIO function or logical device respectively. The status bit is set by their source function or device and is cleared by writing a1. Writing a 0 has no effect.

Bit 6 : SCIRQSTS. SC IRQ status.

Bit 5 : HMIRQSTS. Hardware monitor IRQ status.

Bit 4 : WDTIRQSTS. Watch dog timer IRQ status.

Bit 3 : CIRIRQSTS. Consumer IR IRQ status.

Bit 1 : IRQIN1STS. IRQIN1 status.

Bit 0 : IRQIN0STS. IRQIN0 status.

CRF6 (Default 0x00)

Bit 7 - 0 : Enable bits of the $\overline{SMI}/\overline{PME}$ generation due to the device's IRQ.

These bits enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to any IRQ of the devices. $\overline{SMI}/\overline{PME}$ logic output = (MOUIRQEN and MOUIRQSTS) or (KBCIRQEN and KBCIRQSTS) or (PRTIRQEN and PRTIRQSTS) or (FDCIRQEN and FDCIRQSTS) or (URAIRQEN and URAIRQSTS) or (URBIRQEN and URBIRQSTS) or (HMIRQEN and HMIRQSTS) or (WDTIRQEN and WDTIRQSTS) or (IRQIN3EN and IRQIN3STS) or (IRQIN2EN and IRQIN2STS) or (IRQIN1EN and IRQIN1STS) or (IRQIN0EN and IRQIN0STS)

Bit 7 : MSIRQEN.

= 0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to MS's IRQ.

= 1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to MS's IRQ.

Bit 6 Reserved

Bit 5 : MOUIRQEN.

= 0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to MOUSE's IRQ.

= 1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to MOUSE's IRQ.

Bit 4 : KBCIRQEN.

= 0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to KBC's IRQ.

= 1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to KBC's IRQ.

Bit 3 : PRTIRQEN.

= 0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to printer port's IRQ.

= 1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to printer port's IRQ.

Bit 2 : FDCIRQEN.

= 0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to FDC's IRQ.

= 1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to FDC's IRQ.

Bit 1 : URAIRQEN.

= 0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART A's IRQ.

= 1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART A's IRQ.

Bit 0 : URBIRQEN.

= 0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART B's IRQ.

= 1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART B's IRQ.

CRF7 (Default 0x00)

Bit 7 : Reserved. Return zero when read

Bit 6 - 0 : Enable bits of the $\overline{SMI}/\overline{PME}$ generation due to the GPIO IRQ function or device's IRQ.

Bit 6 : SCIRQEN.

= 0 Disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to SC's IRQ.

= 1 Enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to SC's IRQ.

Bit 5 : HMIRQEN.

= 0 Disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to hardware monitor's IRQ.

= 1 Enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to hardware monitor's IRQ.

Bit 4 : WDTIRQEN.

= 0 Disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to watch dog timer's IRQ.

= 1 Enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to watch dog timer's IRQ.

Bit 3 : CIRIRQEN.

= 0 Disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to CIR's IRQ.

= 1 Enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to CIR's IRQ

Bit 2 : MIDIIRQEN.

= 0 Disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to MIDI's IRQ.

= 1 Enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to MIDI's IRQ.

Bit 1 : IRQIN1EN.

= 0 Disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to IRQIN1's IRQ.

= 1 Enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to IRQIN1's IRQ.

Bit 0 : IRQIN0EN.

= 0 Disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to IRQIN0's IRQ.

= 1 Enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to IRQIN0's IRQ.

CRF9 (Default 0x00)

Bit 7 - 3 : Reserved. Return zero when read.

Bit 2 : PME_EN: Select the power management events to be either an $\overline{PME}$ or $\overline{SMI}$ interrupt for the IRQ events. Note that: this bit is valid only when SMIPME_OE = 1.

= 0 The power management events will generate an $\overline{SMI}$ event

= 1 The power management events will generate an $\overline{PME}$ event.

Bit 1 : FSLEEP: This bit selects the fast expiry time of individual devices.

= 0 1 second.

= 1 8 milli-seconds

Bit 0 : SMIPME_OE: This is the $\overline{SMI}$ and $\overline{PME}$ output enable bit.

= 0 Neither $\overline{SMI}$ nor $\overline{PME}$ will be generated. Only the IRQ status bit is set.

= 1 An $\overline{SMI}$ or $\overline{PME}$ event will be generated.

CRFE, FF (Default 0x00)

Reserved for Winbond test

8.5 Logical Device B (Hardware Monitor)

CR30 (Default 0x00)

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00, 0x00)

These two registers select Hardware Monitor base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit 7 - 4 : Reserved.

Bit 3 - 0 : These bits select IRQ channel for Hardware Monitor.

8.6 Logical Device C (Smart Card interface)

CR30 (Default 0x00)

Bit 7 - 1 : Reserved.

Bit 0 : Logical device active bit.

= 0 Logical device is inactive.

= 1 Activates the logical device.

CR60, CR61 (Default 0x00, 0x00)

These two registers select Smart Card interface base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit 7 - 4 : Reserved.
Bit 3 - 0 : These bits select IRQ channel for Smart Card interface.

CRF0 (Default 0x00)

Bit 7 - 1 : Reserved.
Bit 0 SCPSNT_POL (Smart Card Present Polarity). SCPSNT polarity bit.
= 0 SCPSNT is active high.
= 1 SCPSNT is active low.

8.7 Logical Device D (MS/SD Card Interface)

CR30 (Default 0x00)

Bit 7 - 3 : Reserved.
Bit 2 : SD Card Interface Active Bit
= 0 SD card interface is inactive.
= 1 SD card interface is active.
Bit 1 : MS Card Interface Active Bit
= 0 MS card interface is inactive.
= 1 MS card interface is active.
Bit 0 : MS/SD card interface active bit.
= 0 Both MS & SD card interface is inactive.
= 1 Both MS & SD card interface is active.

CR60, CR61 (Default 0x00, 0x00)

These two registers select MS/SD Card interface base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit 7 - 4 : Reserved.
Bit 3 - 0 : These bits select IRQ channel for MS/SD Card interface.

CR74 (Default 0x04)

Bit 7 - 3 : Reserved.
Bit 2 - 0 : These Bits Select DMA Channel for MS/SD Card Port.
0x00 = DMA0
0x01 = DMA1
0x02 = DMA2
0x03 = DMA3
0x04 - 0x07 = No DMA active

CRF0 (Default 0x01)

Bit 7 - 3 : Reserved.

Bit 2 : SDDET Polarity Select
= 1 Active High
= 0 Active Low

Bit 1 : External SD Card Detect Pin(SDDET; Pin 69) Enable
= 1 Enable
= 0 Disable

Bit 0 : Internal SD Card Detect Pin(DAT3; Pin 96) Enable
= 1 Enable
= 0 Disable

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage (5V)	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
RTC Battery Voltage V_{BAT}	2.2 to 4.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9.2 DC Characteristics

(T_A = 0° C to 70° C, V_{DD} = 5V ±10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	I_{BAT}			2.4	uA	V_{BAT} = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	I_{BAT}			2.0	mA	V_{SB} = 5.0 V, All ACPI pins are not connected.
I/O_{8t} - TTL level bi-directional pin with 8mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 8 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12t} - TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{24t} - TTL level bi-directional pin with 24mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12tp3} – 3.3V TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12ts} - TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24ts} - TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{24tsp3} – 3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12t} - TTL level bi-directional pin and open-drain output with 12mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24t} - TTL level bi-directional pin and open-drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD_{24ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 24mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12cs} - CMOS level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD_{16cs} - CMOS level Schmitt-trigger bi-directional pin and open drain output with 16mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD12$_{csd}$ - CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD12$_{csu}$ - CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
O4 - Output pin with 4mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -4 mA
O8 - Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
O12 - Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
O16 - Output pin with 16mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -16 mA

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
O_{24} - Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
O_{12p3} - 3.3V output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O_{24p3} - 3.3V output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12} - Open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{24} - Open drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12p3} - 3.3V open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tp3} - 3.3V TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{td} - TTL level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_{tu} - TTL level input pin with internal pull up resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tsp3} - 3.3 V TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{c} - CMOS level input pin						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{cd} - CMOS level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

DC Characteristics, continued

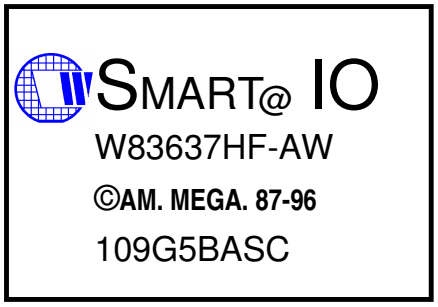
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_{cs} - CMOS level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{csu} - CMOS level Schmitt-trigger input pin with internal pull up resistor						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

10. ORDERING INSTRUCTION

PART NO.	KBC FIRMWARE	REMARKS
W83637HF-AW	AMIKEY-2™	
W83637HG-AW	AMIKEY-2™	

11. HOW TO READ THE TOP MARKING

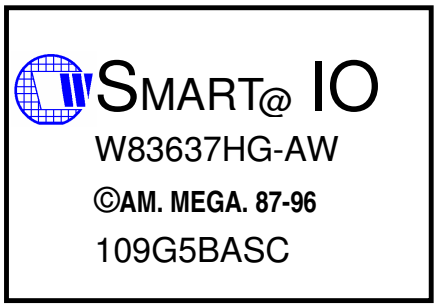
Example: The top marking of W83637HF-AW



1st line: Winbond logo and SMART@IO logo
2nd line: part number: W83637HF-AW
3rd line: the source of KBC F/W -- American Megatrends Incorporated™
4th line: the tracking code 109 G 5B A SC

109: packages made in '2001, week 09
G: assembly house ID; A means ASE, S means SPIL, G means GR, etc.
5B: Winbond internal use.
A: IC revision; A means version A, B means version B
SC: Winbond internal use.

Example: The top marking of W83637HG-AW

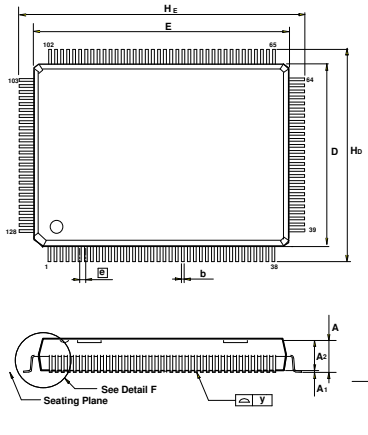


1st line: Winbond logo and SMART@IO logo
2nd line: part number: W83637HG-AW; G means Pb-free package
3rd line: the source of KBC F/W -- American Megatrends Incorporated™
4th line: the tracking code 109 G 5B A SC

109: packages made in '2001, week 09
G: assembly house ID; A means ASE, S means SPIL, G means GR, etc.
5B: Winbond internal use.
A: IC revision; A means version A, B means version B
SC: Winbond internal use.

12. PACKAGE DIMENSIONS

(128-pin QFP)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	—	0.50	—	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	—	1.60	—	—	0.063	—
y	—	—	0.08	—	—	0.003
θ	0	—	7	0	—	7

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

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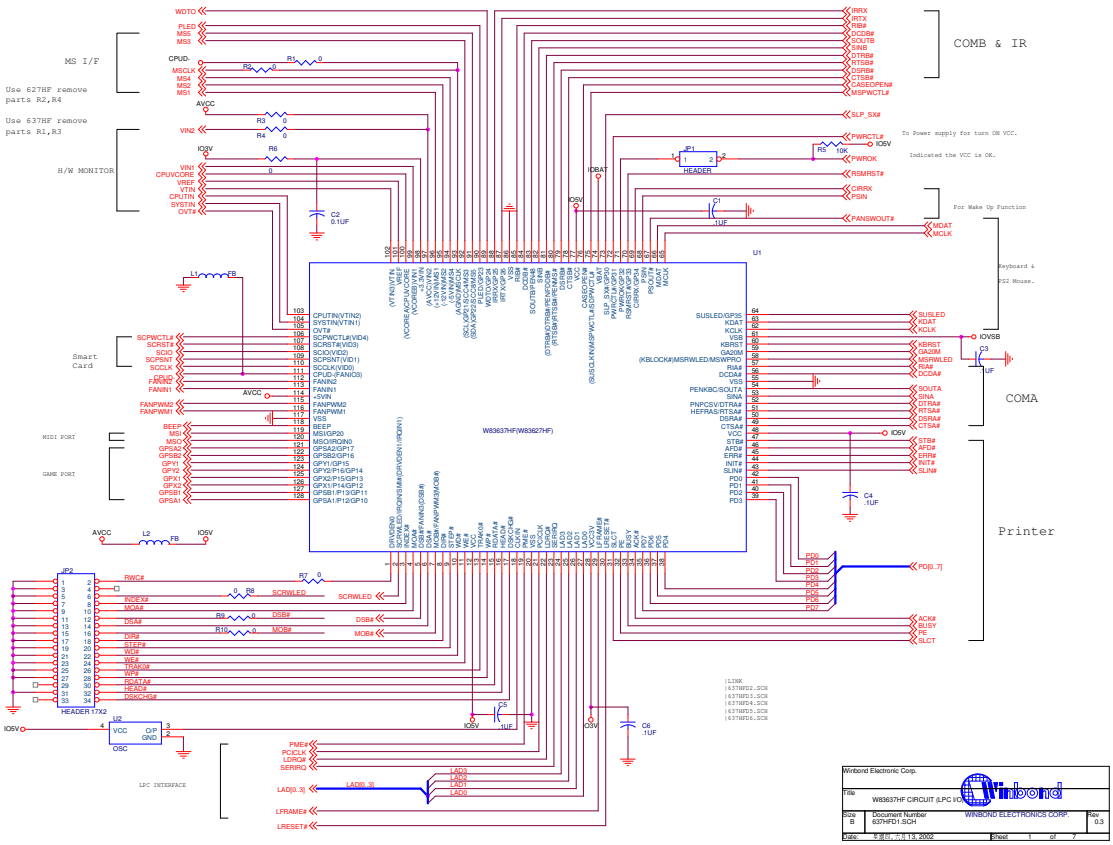
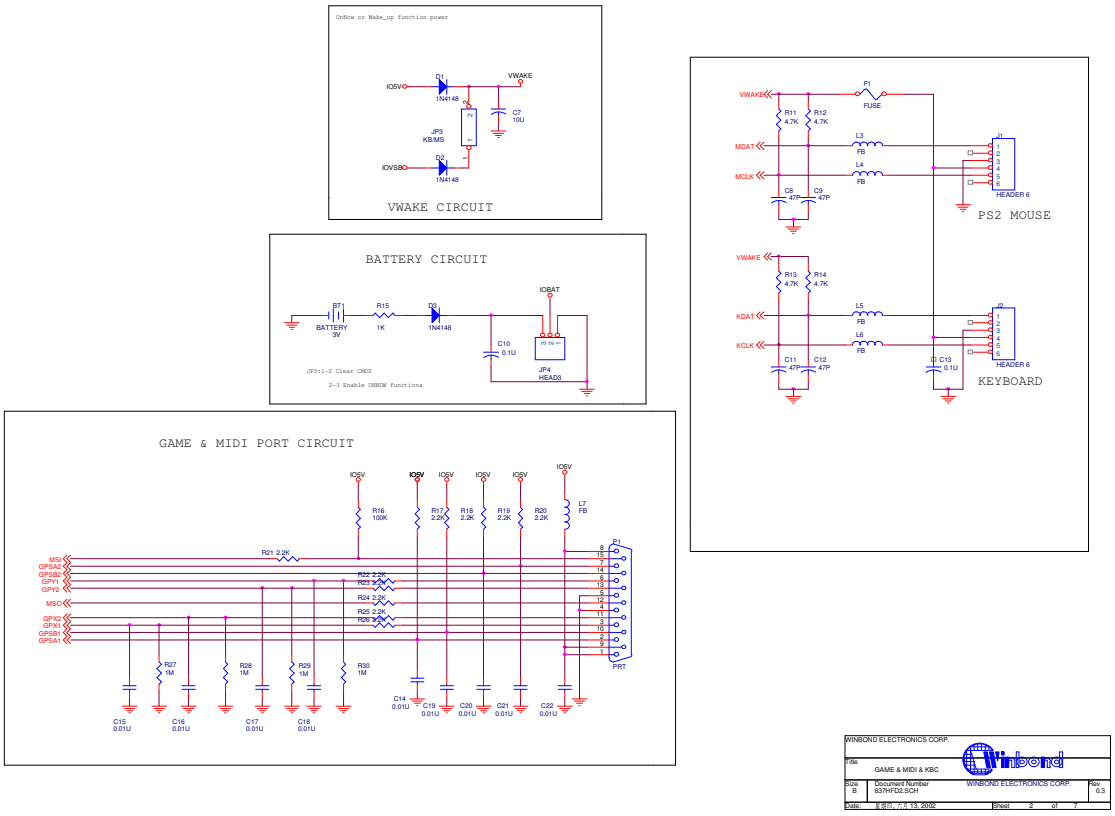
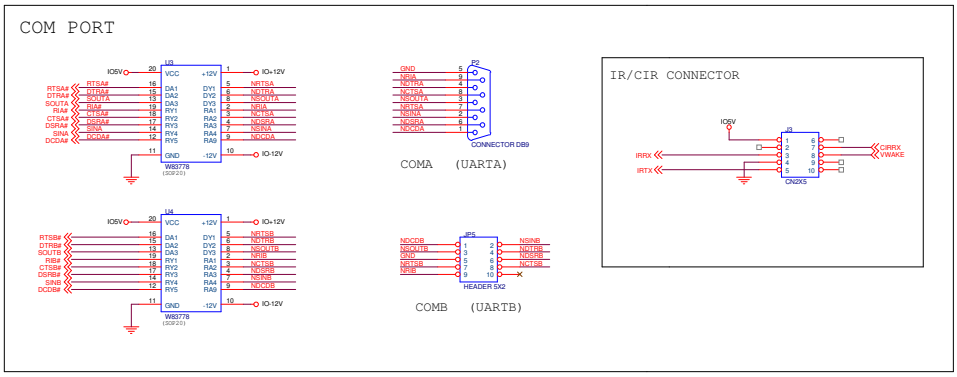
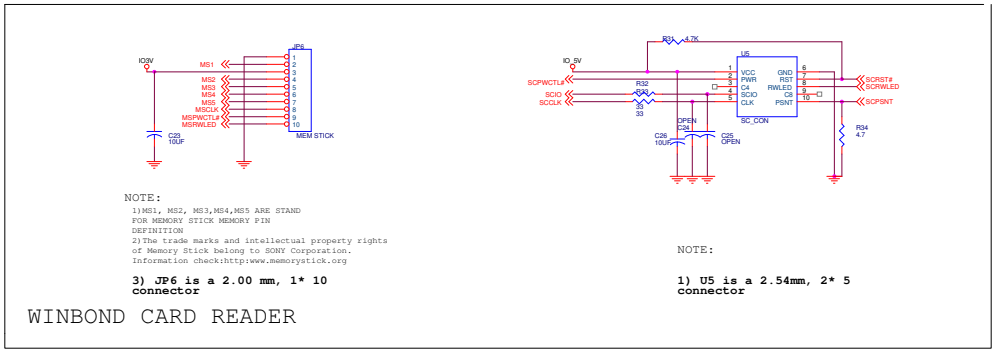
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

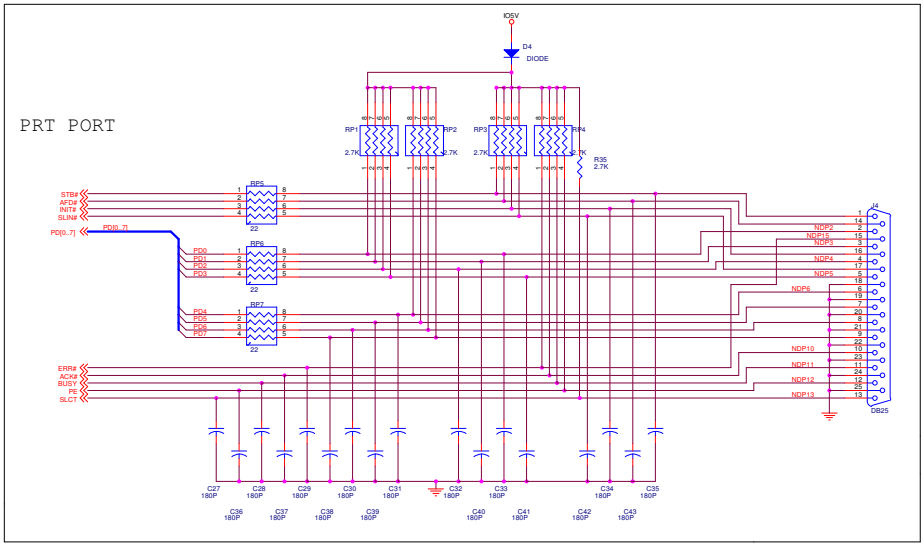
13. APPENDIX A: APPLICATION CIRCUITS



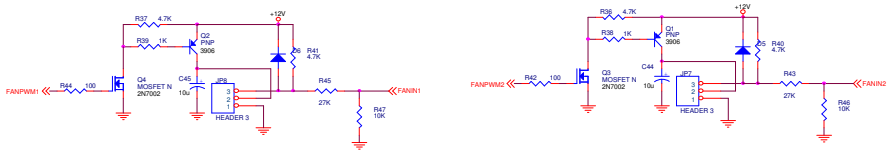




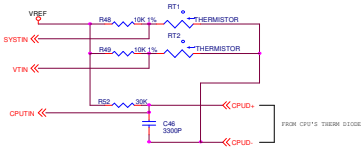


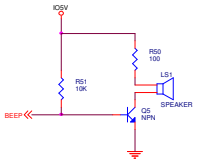


PWM Circuit for FAN speed control

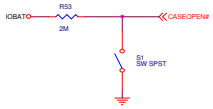


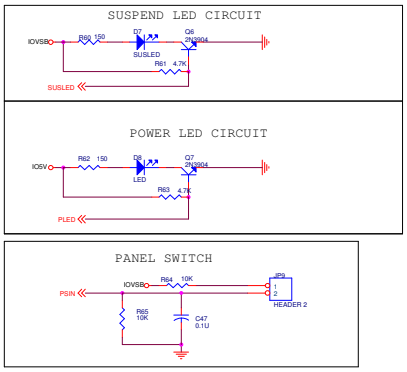
Temperature Sensing

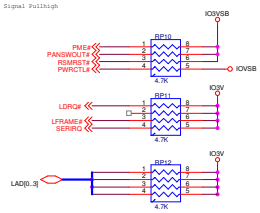




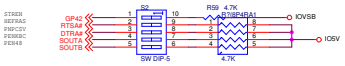
Voltage Sensing



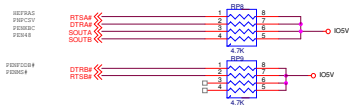




POWER ON SETTING PIN



POWER ON SETTING PIN



	0	1	
DTRB#	FDDS	FAN3	ONLY FOR 637HF
RTSA#	2E	4E	I/O CONFIGURATION ADDRESS
DTRA#	DEFAULT	ALL 0	I/O PORT BASE DEFAULT VALUE
SOUTA	KBC DISABLE	KBC ENABLE	
SOUTB	CLK 24M	CLK 48M	PIN18 INPUT CLK VALUE
RTSB#	MS	SD	ONLY FOR 637HF