

## DS50EV401

# 2.5 Gbps / 5.0 Gbps or 8.0 Gbps Quad Cable and Backplane Equalizer

## General Description

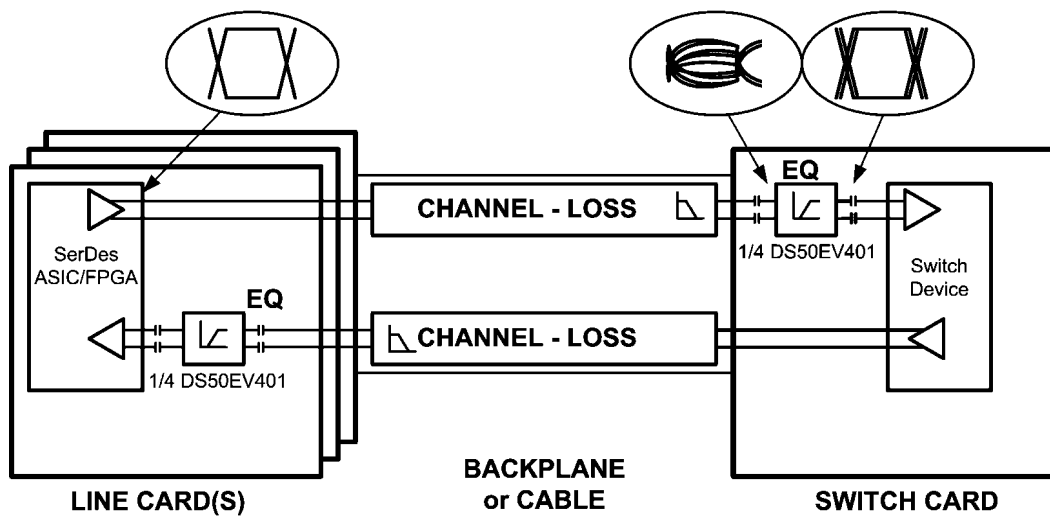
The DS50EV401 is a low power, programmable equalizer specifically designed to reduce inter-symbol interference (ISI) induced by a variety of interconnect media. In all modes, the equalizer can operate, error free, with an input eye that is completely closed by interconnect ISI. The MODE control, allows the user to select between equalization settings for 8.0 Gbps operation or 2.5 Gbps / 5.0 Gbps operation.

The DS50EV401 uses Current-mode logic (CML) on both input and output ports, which provide constant 50 ohm single-ended impedance to AC ground. Differential signaling is implemented through out the entire signal path to minimize supply induced jitter. The DS50EV401 is available in a 7mm x 7mm 48-pin leadless LLP package, and is powered from a single power supply of either 3.3 or 2.5V.

## Features

- Automatic power management on an individual lane basis
- Data rate optimized equalization
- Operates over 7 meter of 24 AWG Twin-ax Cables up to 8 Gbps
- Typical residual deterministic jitter:
  - 0.18 UI @ 8 Gbps w/ 30" of FR4
  - 0.18 UI @ 5 Gbps w/ 40" of FR4
  - 0.16 UI @ 2.5 Gbps w/ 40" of FR4
- 8 kV HBM ESD protection
- -40 to 85°C operating temperature range
- 7 mm x 7 mm 48-pin leadless LLP package
- Single power supply of either 3.3V or 2.5V
- Low power (typically 95 mW per channel at 2.5V  $V_{DD}$ )

## Application Diagram



30050550

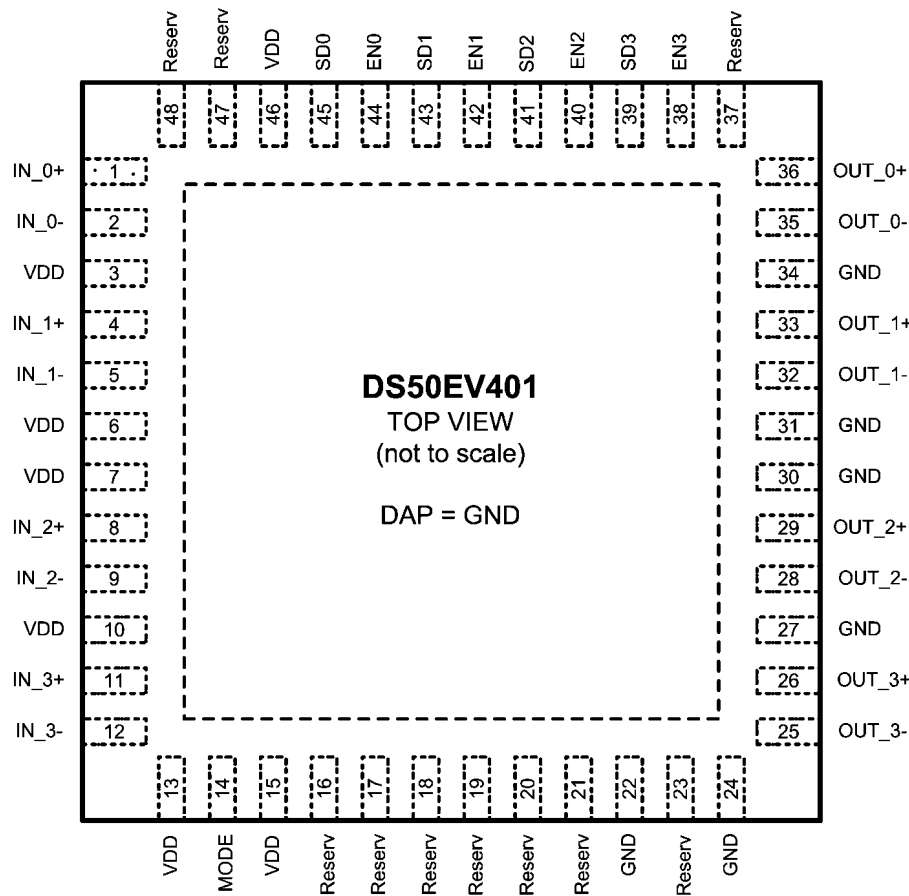
## Pin Descriptions

Pin Name	Pin Number	I/O, Type	Description
HIGH SPEED DIFFERENTIAL I/O			
IN_0+	1	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 50Ω terminating resistor connects IN_0+ to VDD and IN_0- to VDD.
IN_0-	2		
IN_1+	4	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 50Ω terminating resistor connects IN_1+ to VDD and IN_1- to VDD.
IN_1-	5		
IN_2+	8	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 50Ω terminating resistor connects IN_2+ to VDD and IN_2- to VDD.
IN_2-	9		
IN_3+	11	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 50Ω terminating resistor connects IN_3+ to VDD and IN_3- to VDD.
IN_3-	12		
OUT_0+	36	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_0+ to V <sub>DD</sub> and OUT_0- to V <sub>DD</sub> .
OUT_0-	35		
OUT_1+	33	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_1+ to V <sub>DD</sub> and OUT_1- to V <sub>DD</sub> .
OUT_1-	32		
OUT_2+	29	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_2+ to V <sub>DD</sub> and OUT_2- to V <sub>DD</sub> .
OUT_2-	28		
OUT_3+	26	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_3+ to V <sub>DD</sub> and OUT_3- to V <sub>DD</sub> .
OUT_3-	25		
EQUALIZATION CONTROL			
MODE	14	I, LVCMOS	MODE selects the equalizer frequency for EQ channels. MODE is internally pulled low. L = 6.0 - 8.0 Gbps setting H = 2.5 Gbps / 5.0 Gbps setting
DEVICE CONTROL			
EN0	44	I, LVCMOS	Channel 0 Enable Input Pin H = normal operation (enabled) L = standby mode Pin is internally pulled High.
EN1	42	I, LVCMOS	Channel 1 Enable Input Pin H = normal operation (enabled) L = standby mode Pin is internally pulled High.
EN2	40	I, LVCMOS	Channel 2 Enable Input Pin H = normal operation (enabled) L = standby mode Pin is internally pulled High.
EN3	38	I, LVCMOS	Channel 3 Enable Input Pin H = normal operation (enabled) L = standby mode Pin is internally pulled High.
SD0	45	O, LVCMOS	Channel 0 Signal Detect Output Pin H = signal detected L = no signal detected
SD1	43	O, LVCMOS	Channel 1 Signal Detect Output Pin H = signal detected L = no signal detected
SD2	41	O, LVCMOS	Channel 2 Signal Detect Output Pin H = signal detected L = no signal detected.
SD3	39	O, LVCMOS	Channel 3 Signal Detect Output Pin H = signal detected L = no signal detected

Pin Name	Pin Number	I/O, Type	Description
<b>POWER</b>			
V <sub>DD</sub>	3, 6, 7, 10, 13, 15, 46	Power	V <sub>DD</sub> = 2.5V ± 5% or 3.3V ± 10%. V <sub>DD</sub> pins should be tied to V <sub>DD</sub> plane through low inductance path. A 0.1µF bypass capacitor should be connected between each V <sub>DD</sub> pin to GND planes.
GND	22, 24, 27, 30, 31, 34	Ground	Ground reference. GND should be tied to a solid ground plane through a low impedance path.
Exposed Pad	DAP	Ground	Ground reference. The exposed pad at the center of the package must be connected to ground plane of the board.
<b>OTHER</b>			
Reserv	16, 17, 18, 19, 20, 21, 23, 37, 47, 48		Reserved. Do not connect. Leave open.

Note: I = Input O = Output

## Connection Diagram



30050526

TOP VIEW — Not to scale

## Ordering Information

NSID	Package	Tape & Reel QTY	Package Number
DS50EV401SQ	48 Lead LLP Package	1,000	SQA48D
DS50EV401SQE	48 Lead LLP Package	250	SQA48D
DS50EV401SQX	48 Lead LLP Package	2,500	SQA48D

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ( $V_{DD}$ )	-0.5V to +4.0V
LVC MOS Input Voltage	-0.5V to +4.0V
LVC MOS Output Voltage	-0.5V to +4.0V
CML Input/Output Voltage	-0.5V to +4.0V

Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C

ESD Rating

HBM, 1.5 k $\Omega$ , 100 pF  
Thermal Resistance  
 $\theta_{JA}$ , No Airflow

>8 kV

30°C/W

**Recommended Operating Conditions**

	Min	Typ	Max	Units
Supply Voltage				
$V_{DD}$ to GND, or	2.375	2.5	2.625	V
$V_{DD}$ to GND	3.0	3.3	3.6	V
Ambient Temperature	-40	25	+85	°C

**Electrical Characteristics**

Over recommended operating supply and temperature ranges with default register settings unless other specified. (Note 2, Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER						
PD	Power Dissipation 3.3V Operation	Signal active, V <sub>DD</sub> = 3.3V, 3.6V		510	700	mW
		No signal, V <sub>DD</sub> = 3.3V, 3.6V			100	mW
PD	Power Dissipation 2.5V Operation	Signal active, V <sub>DD</sub> = 2.5V, 2.625V		380	490	mW
		No signal, V <sub>DD</sub> = 2.5V, 2.625V		30		mW
N	Supply Noise Tolerance ( <i>Note 4</i> )	Up to 50 MHz		100		mV <sub>P-P</sub>
LVCMOS / LVTTL DC SPECIFICATIONS						
V <sub>IH</sub>	High Level Input Voltage	3.3V Operation	2.0		V <sub>DD</sub>	V
		2.5V Operation	1.6		V <sub>DD</sub>	V
V <sub>IL</sub>	Low Level Input Voltage		-0.3		0.8	V
V <sub>OH</sub>	High Level Output Voltage	I <sub>OH</sub> = -3mA, 3.3V Operation	2.4			V
		I <sub>OH</sub> = -3mA, 2.5V Operation	2.0			V
V <sub>OL</sub>	Low Level Output Voltage	I <sub>OL</sub> = 3mA			0.4	V
I <sub>IH</sub>	Input High Current	V <sub>IN</sub> = V <sub>DD</sub> , MODE pin (pull down)			+140	μA
		V <sub>IN</sub> = V <sub>DD</sub> , EN pins (pull up)	-15		+15	μA
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = 0V, MODE pin (pull down)	-15		+15	μA
		V <sub>IN</sub> = 0V, EN pins (pull up)	-40			μA
CML RECEIVER INPUTS (IN <sub>n+</sub> , IN <sub>n-</sub> )						
V <sub>TX</sub>	Input Voltage Swing (Launch Amplitude)	Measured at point A, AC or DC coupled, <i>Figure 1</i>	400	1000	1600	mV <sub>P-P</sub>
V <sub>IN-S</sub>	Input Voltage Sensitivity	AC-Coupled or DC-Coupled Required Differential Envelope measured at point B, <i>Figure 1</i> , ( <i>Note 5</i> ), See <i>FR4 / BACKPLANE Typical Performance Eye Diagrams</i> ,		170		mV <sub>P-P</sub>
R <sub>LI</sub>	Differential Input Return Loss	100 MHz – 4.0 GHz, with fixture's effect de-embedded		10		dB
R <sub>IN</sub>	Input Resistance	Single ended to V <sub>DD</sub>	40	50	60	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CML OUTPUTS (OUT<sub>n+</sub>, OUT<sub>n-</sub>)</b>						
V <sub>O</sub>	Output Voltage Swing	Differential measurement with OUT <sub>n+</sub> and OUT <sub>n-</sub> terminated by 50Ω to GND AC-Coupled, <a href="#">Figure 2</a>	800	1000	1200	mV <sub>P-P</sub>
V <sub>OCM</sub>	Output Common-Mode Voltage	Single-ended measurement DC-Coupled with 50Ω termination, <a href="#">(Note 6)</a>		V <sub>DD</sub> – 0.25		V
t <sub>R</sub> , t <sub>F</sub>	Transition Time	20% to 80% of differential output voltage, measured within 1" from output pins, <a href="#">Figure 2</a> , <a href="#">(Note 6)</a>		40		ps
R <sub>O</sub>	Output Resistance	Single-ended to V <sub>DD</sub>	40	50	60	Ω
R <sub>LO</sub>	Differential Output Return Loss	100 MHz – 4.0 GHz, with fixture's effect de-embedded. IN <sub>n+</sub> = static high		10		dB
t <sub>PLHD</sub>	Differential Low to High Propagation Delay	Propagation delay measurement at 50% V <sub>O</sub> between input to output, 100 Mbps, <a href="#">Figure 3</a> , <a href="#">(Note 8)</a>		240		ps
t <sub>PHLD</sub>	Differential High to Low Propagation Delay			240		ps
t <sub>ID</sub>	Idle to Valid Differential Data	V <sub>IN</sub> = 800 mVp-p, 5 Gbps, EIEOS, 40" of 6 mil microstrip FR4, <a href="#">Figure 4</a> , <a href="#">(Note 6)</a>		8		ns
t <sub>DI</sub>	Valid Differential data to idle	V <sub>IN</sub> = 800 mVp-p, 5 Gbps, EIOS, 40" of 6 mil microstrip FR4, <a href="#">Figure 4</a> , <a href="#">(Note 6)</a>		8		ns
t <sub>CCSK</sub>	Inter Pair Channel to Channel Skew	Difference in 50% crossing between channels		7		ps
<b>EQUALIZATION</b>						
DJ1	Residual Deterministic Jitter at 8 Gbps	30" of 6 mil microstrip FR4, MODE=0, PRBS-7 (2 <sup>7</sup> -1) pattern, <a href="#">(Note 6, Note 7)</a>		0.18		UI <sub>P-P</sub>
DJ2	Residual Deterministic Jitter at 5 Gbps	40" of 6 mil microstrip FR4, MODE=1, PRBS-7 (2 <sup>7</sup> -1) pattern, <a href="#">(Note 6, Note 7)</a>		0.18	0.21	UI <sub>P-P</sub>
DJ3	Residual Deterministic Jitter at 2.5 Gbps	40" of 6 mil microstrip FR4, MODE=1, PRBS-7 (2 <sup>7</sup> -1) pattern, <a href="#">(Note 6, Note 7)</a>		0.16	0.18	UI <sub>P-P</sub>
RJ	Random Jitter	<a href="#">(Note 8, Note 9)</a>		0.5		psrms

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

**Note 2:** Typical values represent most likely parametric norms at V<sub>DD</sub> = 3.3V or 2.5V, T<sub>A</sub> = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

**Note 3:** The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 4:** Allowed supply noise (mV<sub>P-P</sub> sine wave) under typical conditions.

**Note 5:** V<sub>IN-S</sub> is a measurement of the input differential envelope, see [FR4 / BACKPLANE Typical Performance Eye Diagrams](#). The device does not require an open eye.

**Note 6:** Specification is guaranteed by characterization at optimal MODE setting and is not tested in production.

**Note 7:** Deterministic jitter is measured at the differential outputs (point C of [Figure 1](#)), minus the deterministic jitter before the test channel (point A of [Figure 1](#)). Random jitter is removed through the use of averaging or similar means.

**Note 8:** Measured with clock-like {11111 00000} pattern.

**Note 9:** Random jitter contributed by the equalizer is defined as sqrt (J<sub>OUT</sub><sup>2</sup> – J<sub>IN</sub><sup>2</sup>). J<sub>OUT</sub> is the random jitter at equalizer outputs in ps-rms, see point C of [Figure 1](#); J<sub>IN</sub> is the random jitter at the input of the equalizer in ps-rms, see point B of [Figure 1](#).

## Timing Diagrams

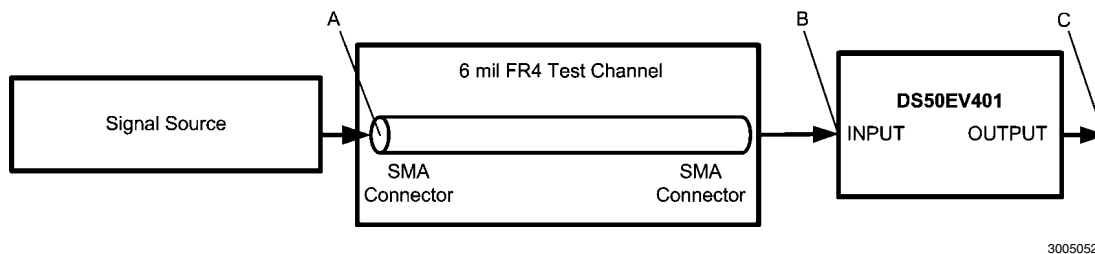


FIGURE 1. Test Setup Diagram

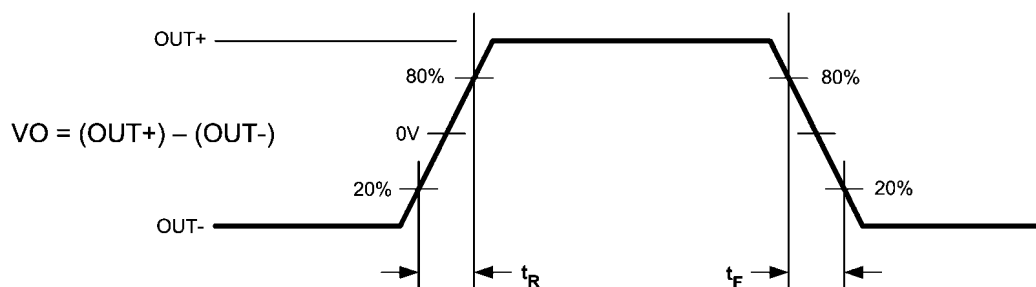


FIGURE 2. CML Output Transition Times

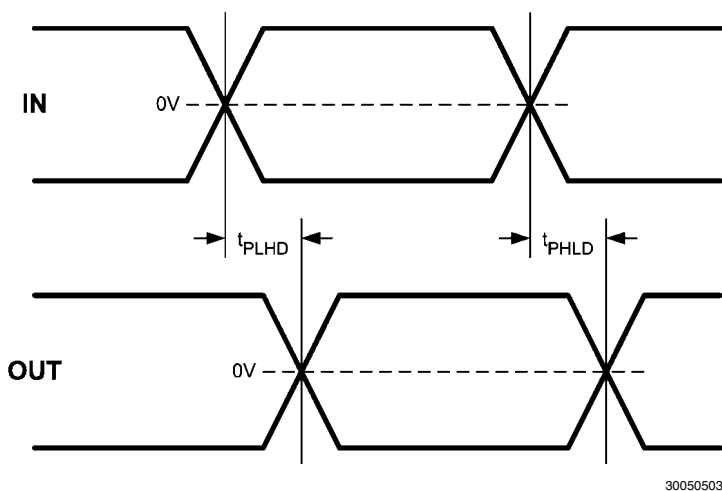


FIGURE 3. Propagation Delay Timing Diagram

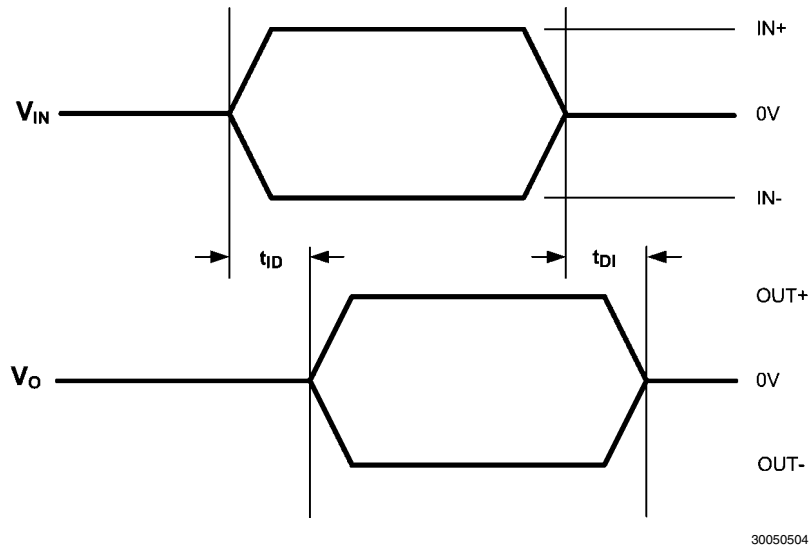


FIGURE 4. Idle Timing Diagram

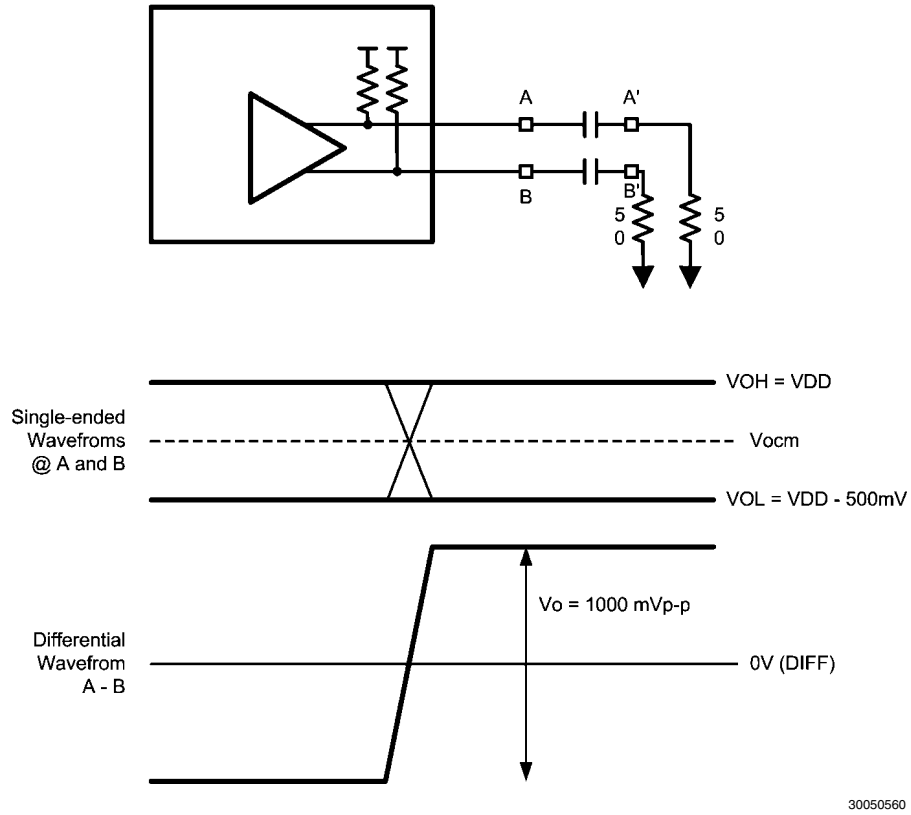


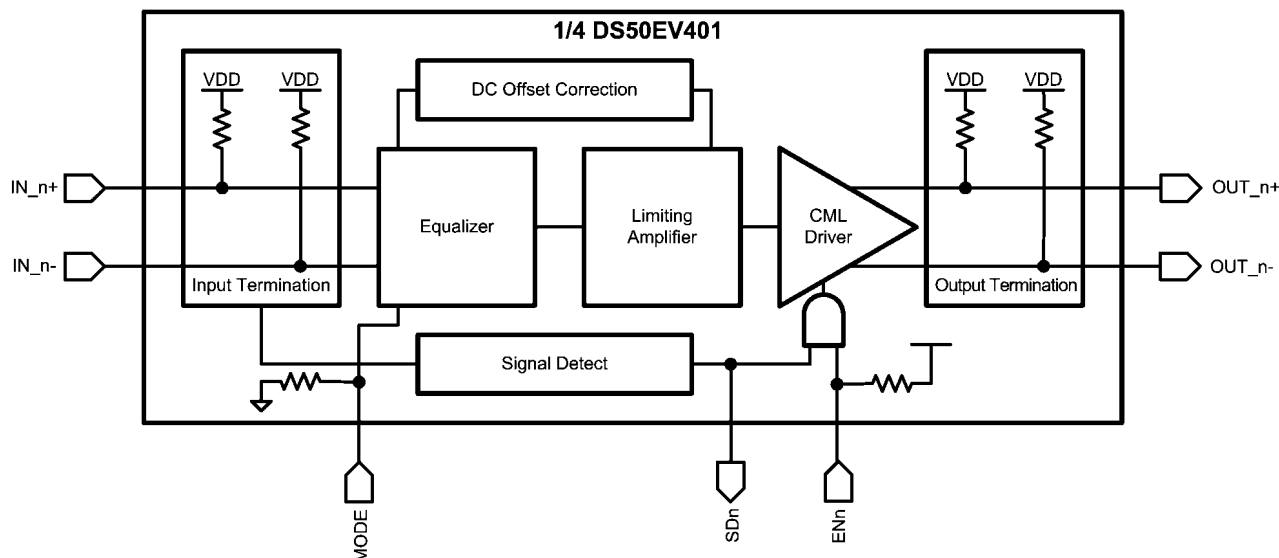
FIGURE 5. CML Output Swings at A/B

## Functional Description

### DS50EV401 APPLICATIONS INFORMATION

The DS50EV401 is a programmable quad equalizer optimized for copper backplanes and cables at transmission rates of 2.5 Gbps up to 8 Gbps. The device consists of an input receive equalizer followed by a limiting amplifier. The equalizer is designed to open an input eye that is completely closed due to inter-symbol interference (ISI) induced by the channel

interconnect. The equalization is set to keep residual deterministic jitter below 0.2 unit intervals (UI) regardless of data rate. This equalization scheme allows one equalization setting to satisfy most serial links between 2.5 and 5.0 Gbps. The DS50EV401 is intended as a unidirectional receiver that should be placed in close physical proximity to the link end point. Therefore the transmitter does not include de-emphasis as TX equalization would not be needed over the short distance between the equalizer and the end point.



30050505

FIGURE 6. General Block Diagram

### Data Channels

The DS50EV401 consists of four data channels. Each channel provides input termination, receiver equalization, signal limiting, offset cancellation, and a CML output driver, as shown in Figure 6. The data channels support two levels of equalization, controlled by the pin MODE. The equalization levels are set simultaneously on all 4 channels, as described in Table 1.

When an idle condition is sensed on a channel's input, the transmit driver is automatically placed into electrical idle

mode. The common mode voltage is set, and the differential output is forced to zero. To save power, the output driver current is powered off when the device is in electrical idle mode. All other circuits maintain their bias currents allowing a fast recovery from idle to the active state. Electric idle is performed on a per channel basis, and several channels can be in idle while others are actively passing data.

TABLE 1. MODE Control Table

6 mil microstrip FR4 trace length (in)	24 AWG Twin-AX cable length (m)	Frequency	Channel Loss	MODE
0–30	0–7	8 Gbps	16 dB	0
0–40	0–10	2.5 Gbps 5.0 Gbps	14 dB 20 dB	1

## Applications Information

### GENERAL RECOMMENDATIONS

The DS50EV401 is a high performance device capable of delivering excellent performance. As with most CML devices, it is recommended that AC coupling capacitors be used to ensure I/O compatibility with other devices. In order to extract full performance from the device in a particular application, good high-speed design practices must be followed. National Semiconductor's LVDS Owner's Manual, provides detailed information about managing signal integrity and power delivery to get the most from your design.

### PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and outputs must have a controlled differential impedance of  $100\Omega$ . It is preferable to route CML lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the CML signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on LLP packages.

### PACKAGE FOOTPRINT / SOLDERING

See National's Application Note number 1187, "Leadless Leadframe Package" for information on PCB footprint and soldering recommendations.

### POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS50EV401 is provided with an adequate power supply. First, the supply ( $V_{DD}$ ) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the  $V_{DD}$  and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A  $0.1\mu\text{F}$  bypass capacitor should be connected to each  $V_{DD}$  pin such that the capacitor is placed as close as possible to the DS50EV401. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of  $2.2\mu\text{F}$  to  $10\mu\text{F}$  should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic and should be placed as close as possible to the DS50EV401.

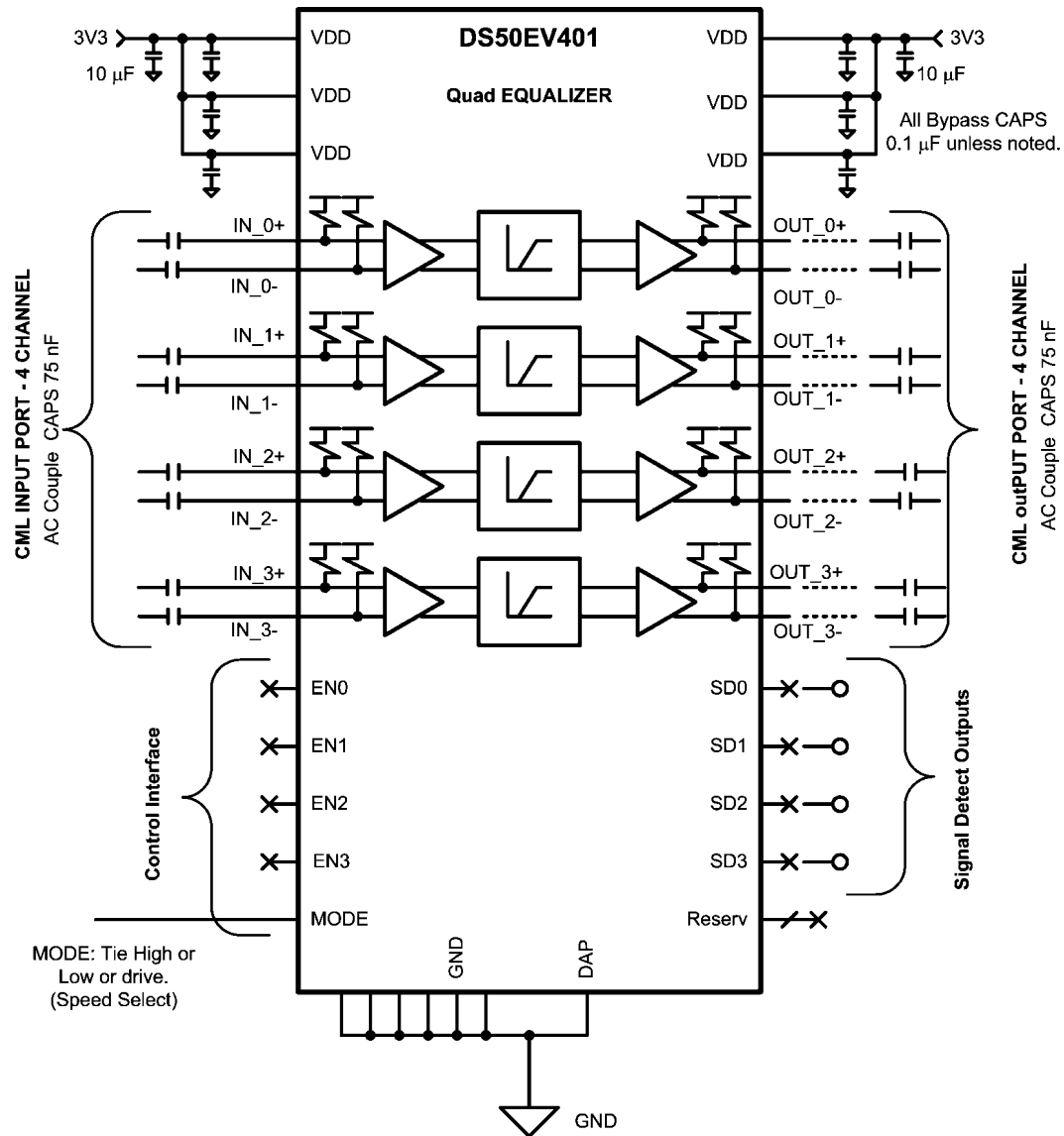


FIGURE 7. Typical Interface Circuit

The CML inputs are AC coupled to the device as shown in [Figure 7](#). Internal to the device are  $50\Omega$  terminations to  $V_{DD}$ . The CML outputs drive  $100\Omega$  transmission lines and are AC coupled and terminated at their load.

The ENABLE inputs and SIGNAL DETECT outputs are optional. Internal to the device the signal detect circuitry is connected to the enable circuit providing the automatic power management feature. When the No-signal condition is detected, the respective channel is placed in standby mode. The

MODE pin is used to select between low and high data rate equalization settings. Depending upon the application it may be tied High, tied Low, or driven. There are several reserved pins on the device, these are NC pins and should be left open. Power is supplied through six  $V_{DD}$  pins to the device. A  $0.1\mu F$  capacitor is recommended per pin as close to the device as possible. A larger bulk capacitor is also recommended to be placed near by the device. Ground is supplied to the device via the ground pins and also the DAP.

## FR4 / BACKPLANE Typical Performance Eye Diagrams

The plots show the unequalized and equalized eye patterns for various interconnects as noted. Unequalized is shown in

the left column and the corresponding equalized eye pattern in shown in the right column.

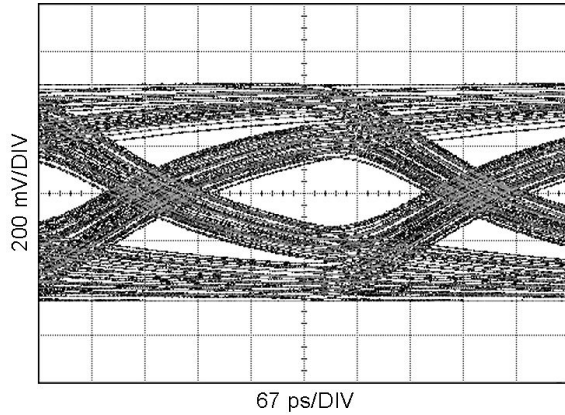


Figure 8. Unequalized Signal (40 in FR4, 2.5 Gbps, PRBS7) <sup>30050508</sup>

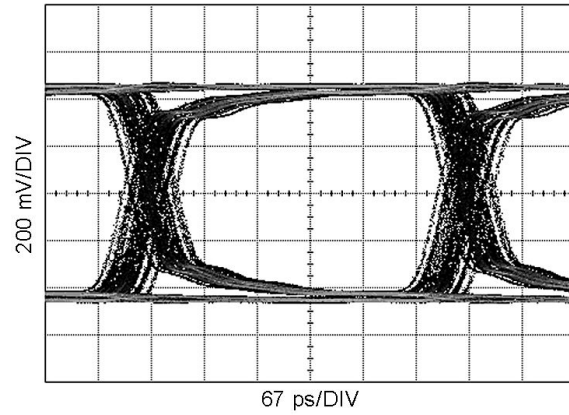


Figure 9. Equalized Signal (40 in FR4, 2.5 Gbps, PRBS7, MODE=1) <sup>30050509</sup>

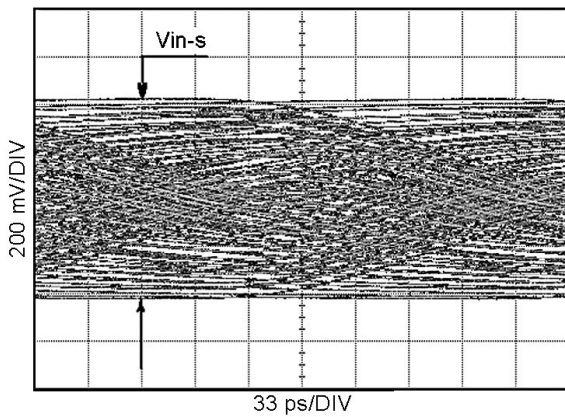


Figure 10. Unequalized Signal (40 in FR4, 5 Gbps, PRBS7) <sup>30050510</sup>

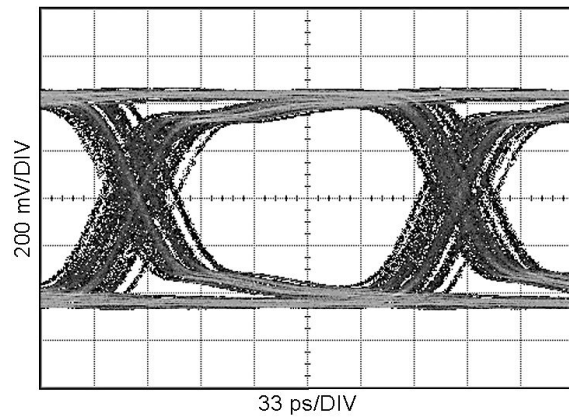


Figure 11. Equalized Signal (40 in FR4, 5 Gbps, PRBS7, MODE=1) <sup>30050511</sup>

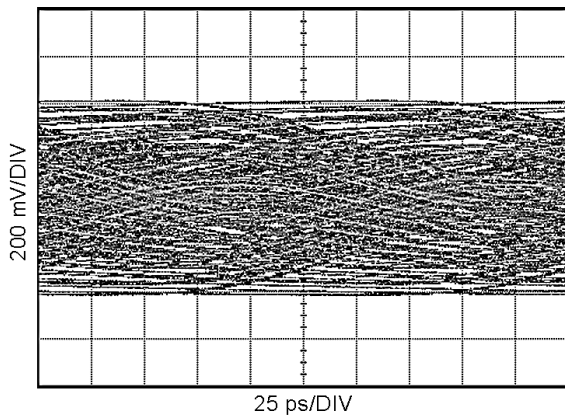


Figure 12. Unequalized Signal (30 in FR4, 8 Gbps, PRBS7) <sup>30050512</sup>

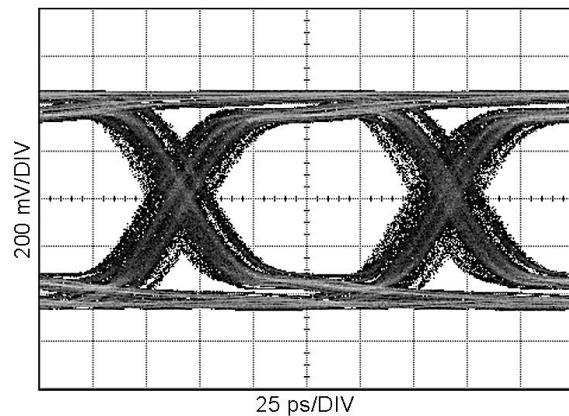


Figure 13. Equalized Signal (30 in FR4, 8 Gbps, PRBS7, MODE=0) <sup>30050513</sup>

## Twin-AX CABLES Typical Performance Eye Diagrams

The plots show the unequalized and equalized eye patterns for various interconnects as noted. Unequalized is shown in

the left column and the corresponding equalized eye pattern in shown in the right column.

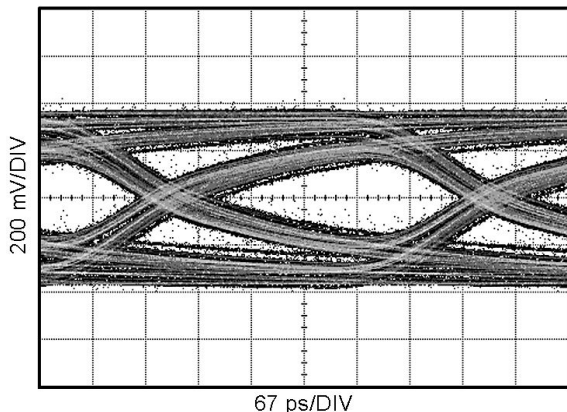


Figure 14. Unequalized Signal (10 m 24 AWG Twin-AX Cable, 2.5 Gbps, PRBS7)

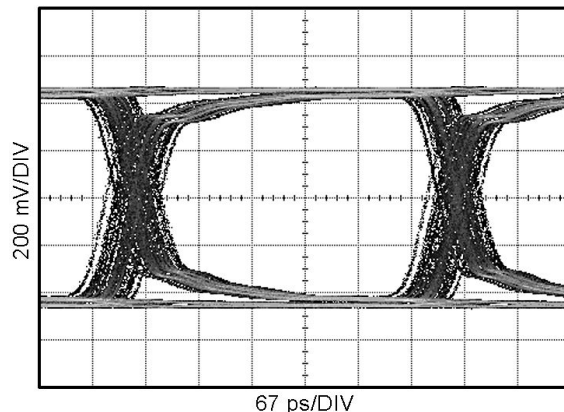


Figure 15. Equalized Signal (10 m 24 AWG Twin-AX Cable, 2.5 Gbps, PRBS7, MODE=1)

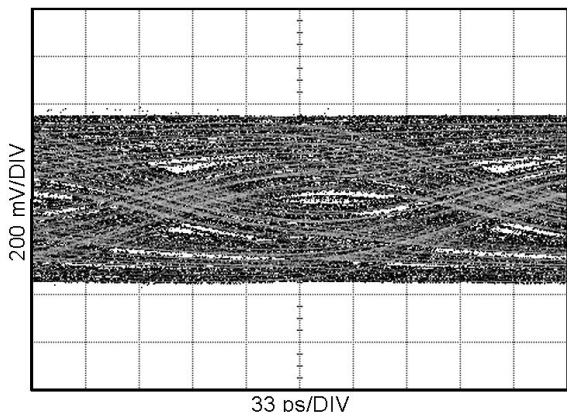


Figure 16. Unequalized Signal (10 m 24 AWG Twin-AX Cable, 5 Gbps, PRBS7)

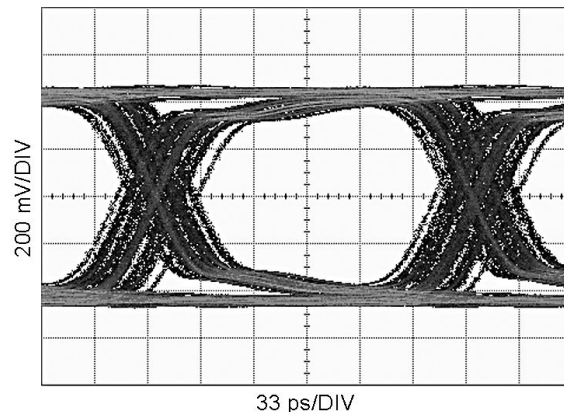


Figure 17. Equalized Signal (10 m 24 AWG Twin-AX Cable, 5 Gbps, PRBS7, MODE=1)

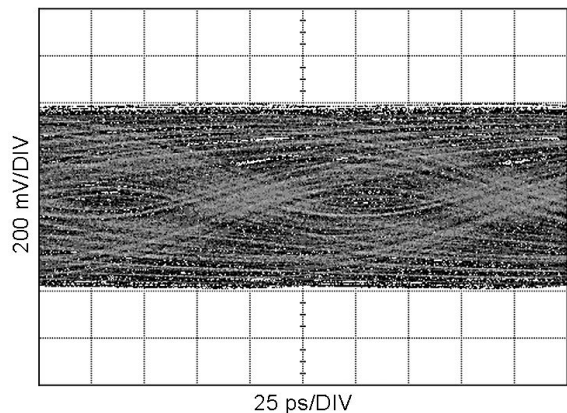


Figure 18. Unequalized Signal (7 m 24 AWG Twin-AX Cable, 8 Gbps, PRBS7)

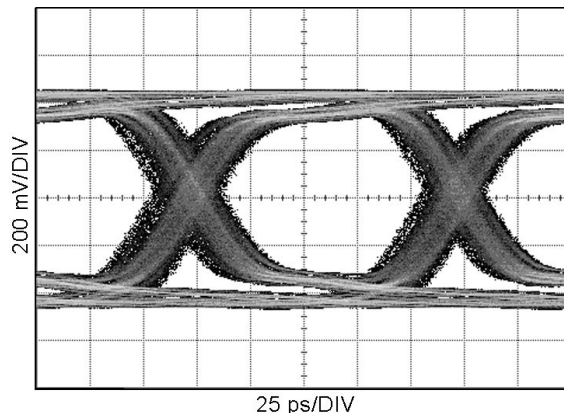
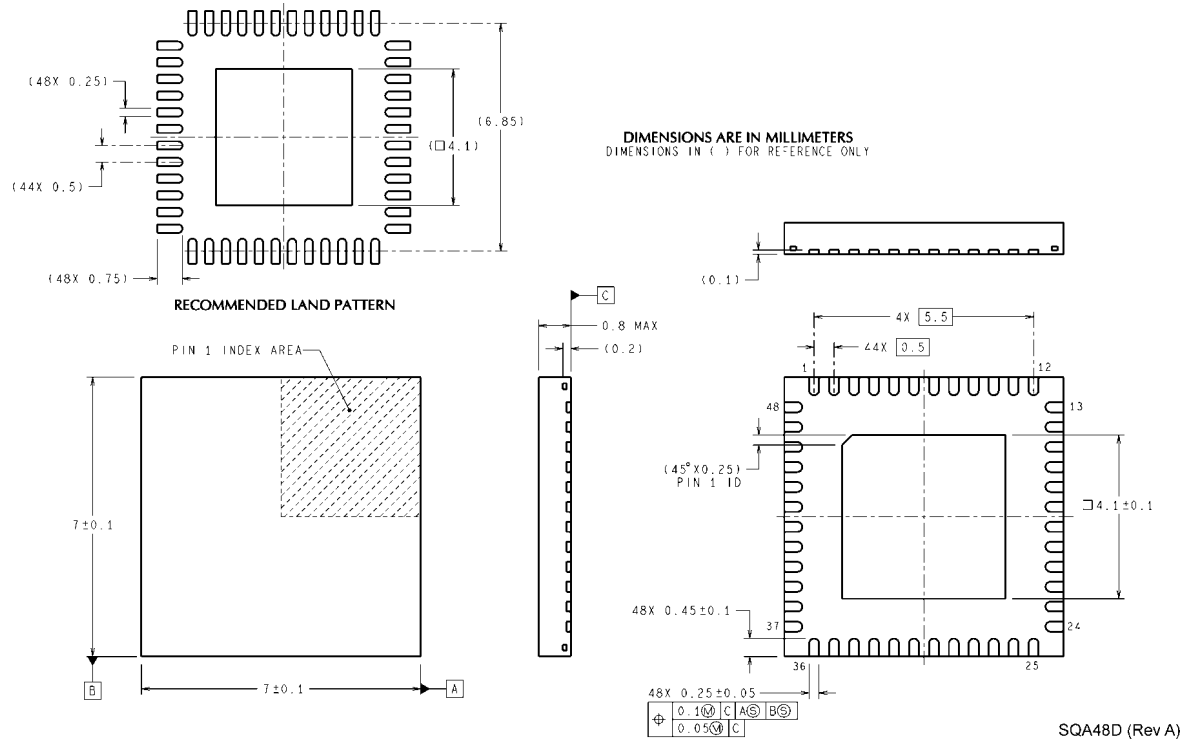


Figure 19. Equalized Signal (7 m 24 AWG Twin-AX Cable, 8 Gbps, PRBS7, MODE=0)

# Physical Dimensions inches (millimeters) unless otherwise noted



## Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:  
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