NCN6000

Compact Smart Card Interface IC

The NCN6000 is an integrated circuit dedicated to the smart card interface applications. The device handles any type of smart card through a simple and flexible microcontroller interface. On top of that, due to the built−in chip select pin, several couplers can be connected in parallel. The device is particularly suited for low cost, low power applications, with high extended battery life coming from extremely low quiescent current.

Features

- 100% Compatible with ISO7816−3 and EMV Standard
- Wide Battery Supply Voltage Range: 2.7 ≤ Vbat ≤ 6.0 V
- Programmable CRD_VCC Supply to Cope with either 3.0 V or 5.0 V Card Operation
- Built−in DC−DC Converter Generates the CRD_VCC Supply with a Single External Low Cost Inductor only, providing a High Efficiency Power Conversion
- Full Control of the Power Up/Down Sequence Yields High Signal Integrity on both the Card I/O and the Signal Lines
- Programmable Card Clock Generator
- Built−in Chip Select Logic allows Parallel Coupling Operation
- ESD Protection on Card Pins (8.0 kV, Human Body Model)
- Fault Monitoring includes $Vbat_{low}$ and Vcc_{low}, providing Logic Feedback to External CPU
- Card Detection Programmable to Handle Positive or Negative Going Input
- Built−in Programmable CRD_CLK Stop Function Handles both High or Low State
- These are Pb−Free Devices**

Typical Application

- E−Commerce Interface
- ATM Smart Card
- Pay TV System

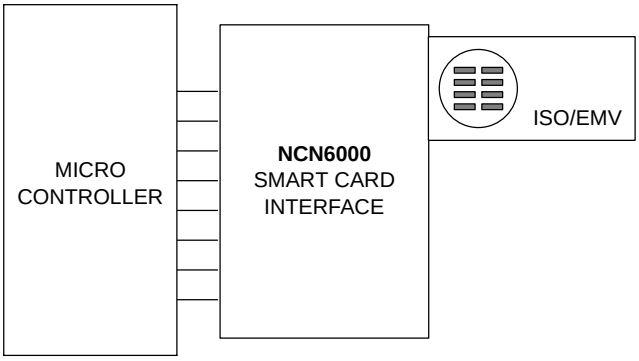

Figure 1. Simplified Application

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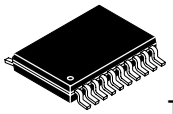
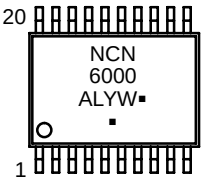
MARKING DIAGRAM

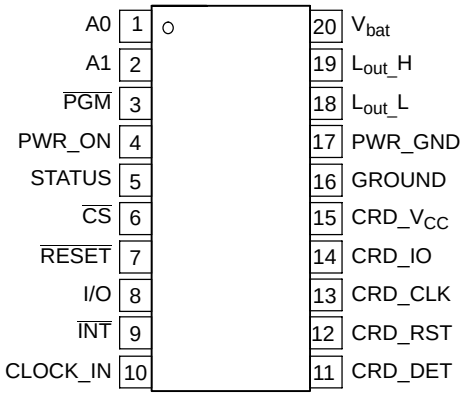


TSSOP−20
DTB SUFFIX
CASE 948E



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCN6000DTB	TSSOP−20*	75 Units / Rail
NCN6000DTBG	TSSOP−20*	75 Units / Rail
NCN6000DTBR2	TSSOP−20*	2500/Tape & Reel
NCN6000DTBR2G	TSSOP−20*	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb−Free.

**For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

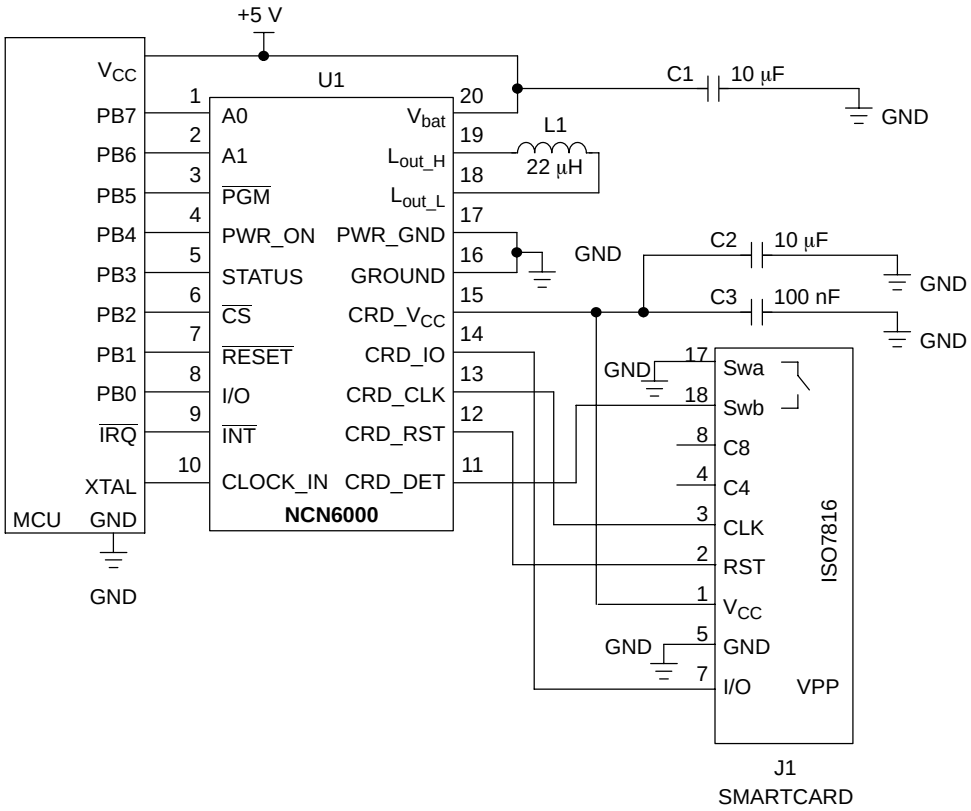


Figure 2. Typical Application

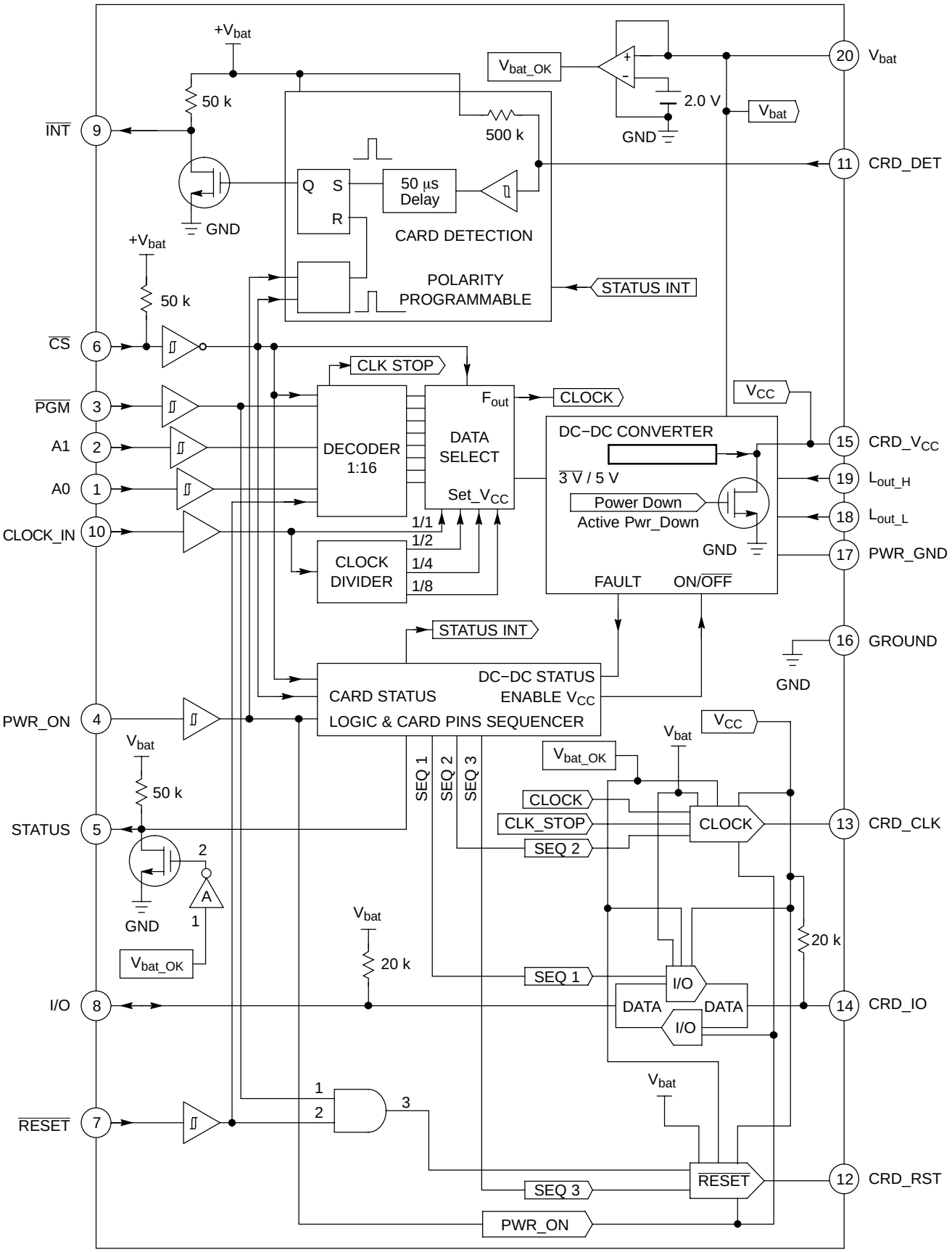
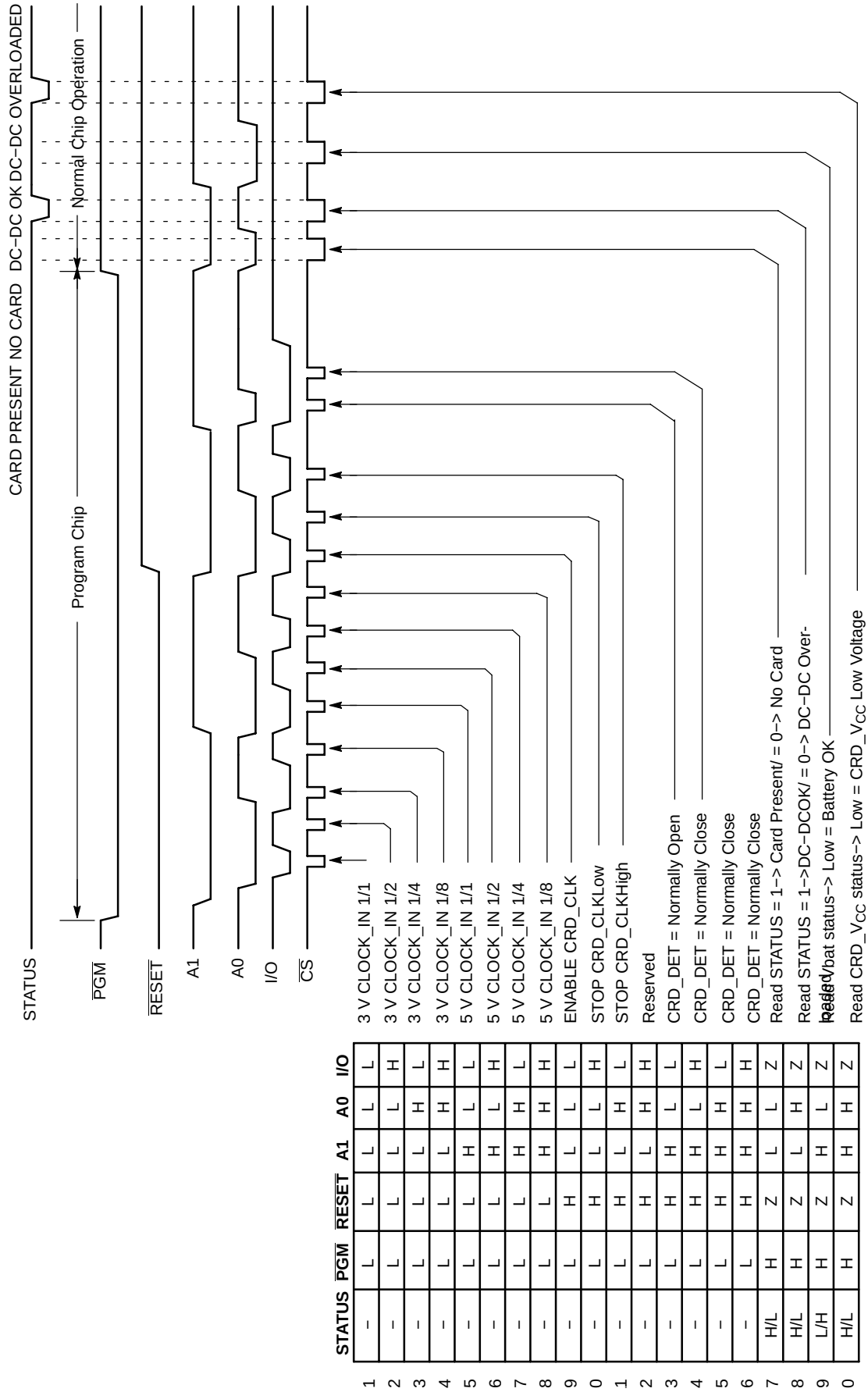


Figure 3. Block Diagram



	STATUS	PGM	RESET	A1	A0	I/O	
1	–	L	L	L	L	L	3 V CLOCK_IN 1/1
2	–	L	L	L	L	H	3 V CLOCK_IN 1/2
3	–	L	L	L	H	L	3 V CLOCK_IN 1/4
4	–	L	L	L	H	H	3 V CLOCK_IN 1/8
5	–	L	L	H	L	L	5 V CLOCK_IN 1/1
6	–	L	L	H	L	H	5 V CLOCK_IN 1/2
7	–	L	L	H	H	L	5 V CLOCK_IN 1/4
8	–	L	L	H	H	H	5 V CLOCK_IN 1/8
9	–	L	H	L	L	L	ENABLE CRD_CLK
0	–	L	H	L	L	H	STOP CRD_CLKLow
1	–	L	H	L	H	L	STOP CRD_CLKHigh
2	–	L	H	L	H	H	Reserved
3	–	L	H	H	L	L	CRD_DET = Normally Open
4	–	L	H	H	L	H	CRD_DET = Normally Close
5	–	L	H	H	H	L	CRD_DET = Normally Close
6	–	L	H	H	H	H	CRD_DET = Normally Close
7	H/L	H	Z	L	L	Z	Read STATUS = 1−> Card Present/ = 0−> No Card
8	H/L	H	Z	L	H	Z	Read STATUS = 1−>DC−DCOK/ = 0−> DC−DC Over-loaded
9	L/H	H	Z	H	L	Z	Read bat status−> Low = Battery OK
0	H/L	H	Z	H	H	Z	Read CRD_V_{CC} status−> Low = CRD_V_{CC} Low Voltage

Figure 4. Programming and Normal Operation Basic Timing

The programming can be achieved with the card powered ON or OFF. The identification of the interrupt is carried out by polling the STATUS pin, the Vbat voltage and the DC−DC results being provided on the same pin as depicted by the table in Figure 4. During the programming mode, the $\overline{PGM}$ pin can be released to High since the mode is internally latched by the Negative going transition presents on the Chip Select pin.

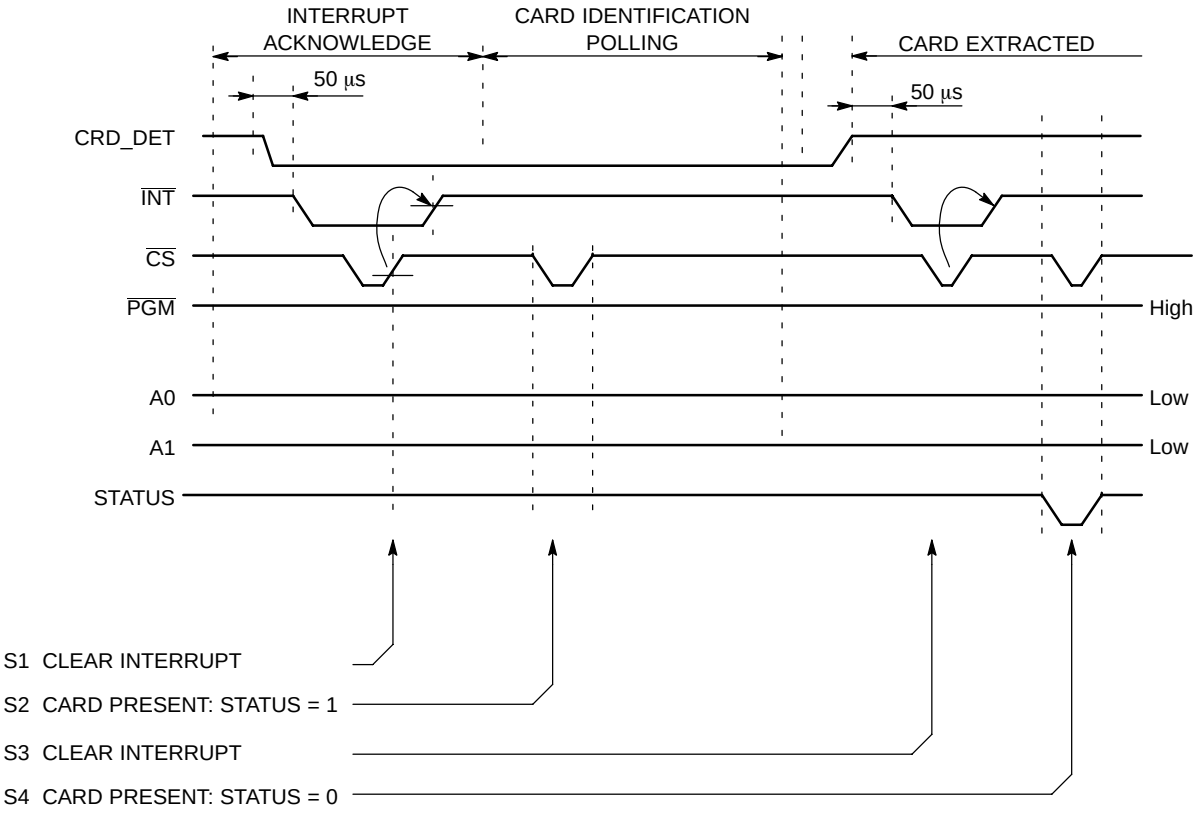


Figure 5. Interrupt Servicing and Card Polling

When a card is either inserted or extracted, the CRD_DET pin signal is debounced internally prior to pull the $\overline{INT}$ pin to Low. The built−in logic circuit automatically accommodates positive or negative input signal slope, on both insertion and extraction state, depending upon the polarity defined during the initialization sequence. The default condition is Normally Open switch, negative going card detection. The external CPU shall acknowledge the request by forcing $\overline{CS}$ = L which, in turn, releases the $\overline{INT}$ pin to High upon positive going of Chip Select (Table 4). Polling the STATUS pin as depicted in Table 3 identifies the active card. If a card is present, the STATUS returns High, otherwise a Low is presented pin 5. The 50 μs digital filter is activated during both Insertion and Extraction of the card. The MPU shall clear the $\overline{INT}$ line when the card has been extracted, making the interrupt function available for other purposes. However, neither the NCN6000 operation nor the smart card I/O line or commands are affected by the state of the $\overline{INT}$ pin.

On the other hand, clearing the $\overline{INT}$ and reading the STATUS register can be performed by a single read by the MPU: states S1 and S2 can be combined in a single instruction, the same for S3 and S4.

ABBREVIATIONS

Lout_H	DC−DC External Inductor
Lout_L	DC−DC External Inductor
Cout	Output Capacitor
VCC	Card Power Supply Input
Icc	Current at CRD_VCC Pin
Class A	5.0 V Smart Card
Class B	3.0 V Smart Card
$\overline{CS}$	Chip Select (from MPU)
Z	High Impedance Logic State (according to ISO7816)
CRD_VCC	Interface IC Card Power Supply Output
CRD_CLK	Interface IC Card Clock Output
CRD_RST	Interface IC Card Reset Output
CRD_IO	Interface IC Card I/O Signal Line
CRD_DET	Interface IC Card Detection
ATR	Answer to Reset
$\overline{PGM}$	Select Programming or Normal Operation
$\overline{INT}$	Interrupt (to MPU)
tr	Rise Time
tf	Fall Time
td	Delay Time
ts	Storage Time

PIN FUNCTIONS AND DESCRIPTION

Pin	Name	Type	Description
1	A0	INPUT	This pin is combined with A1, $\overline{PGM}$, $\overline{RESET}$ and I/O to program the chip mode of operation and to read the data provided by STATUS. (Figures 4 and 5 and Tables 2 and 3)
2	A1	INPUT	This pin is combined with A0, $\overline{PGM}$, $\overline{RESET}$ and I/O to program the chip mode of operation and to read the data provided by STATUS. (Figures 4 and 5 and Tables 2 and 3)
3	$\overline{PGM}$	INPUT	This pin is combined with A0, A1, $\overline{RESET}$ and I/O to program the chip mode of operation and to read the data provided by STATUS. (Figures 4 and 5 and Tables 2 and 3)
4	PWR_ON	INPUT Pull Down	This pin validates the operation of the internal DC−DC converter: $\overline{CS}$ = L + PWR_ON = Negative going: DC−DC is OFF $\overline{CS}$ = L + PWR_ON = Positive going: DC−DC is ON Note: The PWR_ON bit must be combined with a Low state $\overline{CS}$ signal to activate the function. (Table 2)
5	STATUS	OUTPUT	This pin provides logic state related to the card and NCN6000 status. According to the A0, A1 and $\overline{PGM}$ logic state, this pin carries either the Card present status or the Vbat or the DC−DC operation state. When $\overline{PGM}$ = L, STATUS is not affected, see Table 2.
6	$\overline{CS}$	INPUT Pull Up	This pin provides the NCN6000 chip select function. The PWR_ON, $\overline{RESET}$, I/O, A0, A1 and $\overline{PGM}$ signals are disabled when $\overline{CS}$ = H. When $\overline{PGM}$ = L and $\overline{CS}$ = L, the device jumps to the programming mode (Figure 4 and Tables 1, 2 and 3). The Chip Select pin must be a unique physical address when more than one card are controlled by a single MPU. The data presented by the MPU are latched upon positive going edge of the Chip Select pin.
7	$\overline{RESET}$	INPUT Pull Down	This pin provides two modes of operation depending upon the logic state of $\overline{PGM}$ pin 3: **$\overline{PGM}$ = 1**: The signal present at this pin is translated to pin 12 (card reset signal) when $\overline{CS}$ = L and PWR_ON = H. It is latched when $\overline{CS}$ = H. **$\overline{PGM}$ = 0**: The signal present on this pin is used as a logic input to program the internal functions (Figure 5 and Tables 2 and 3).

PIN FUNCTIONS AND DESCRIPTION (continued)

Pin	Name	Type	Description
8	I/O	Input/Output Pull Up	This pin is connected to an external microcontroller interface. A bidirectional level translator adapts the serial I/O signal between the smart card and the microcontroller. The level translator is enabled when $\overline{CS}$ = L. The signal present on this pin is latched when $\overline{CS}$ = H. This pin is also used in programming mode (Tables 1, 2 and 3, Figures 4 and 5).
9	$\overline{INT}$	OUTPUT Pull Down	This pin is activated LOW when a card has been inserted and detected by the interface or when the NCN6000 reports Vbat or CRD_VCC status (See Table 6). The signal is reset to a logic 1 on the rising edge of either $\overline{CS}$ or PWR_ON. The Collector open mode makes possible the wired AND/OR external logic. When two or more interfaces share the $\overline{INT}$ function with a single microcontroller, the software must poll the STATUS pin to identify the origin of the interrupt (Figure 5).
10	CLOCK_IN	CLOCK INPUT High Impedance	This pin can be connected to either the microcontroller master clock, or to any clock signal, to drive the external smart cards. The signal is fed to internal clock selector circuit and translated to the CRD_CLK pin at either the same frequency, or divided by 2 or 4 or 8, depending upon the programming mode (Tables 1, 2 and 3). Care must be observed, at PCB level, to minimize the pick−up noise coming from the CLOCK_IN line. It is recommended to put a shield, built with a 10 mil copper track, around this line and terminated to the GND.
11	CRD_DET	INPUT	The signal coming from the external card connector is used to detect the presence of the card. A built−in pull up low current source makes this pin active LOW or HIGH, assuming one side of the external switch is connected to ground. At Vbat start up, the default condition is Normally Open switch, negative going insertion detection. The Normally Closed switch, positive going insertion detection, can be defined by programming the NCN6000 accordingly. In this case, the polarity must be set up during the first cycles of the system initialization, otherwise an already inserted card will not be detected by the chip.
12	CRD_RST	OUTPUT	This pin is connected to the $\overline{RESET}$ pin of the card connector. A level translator adapts the $\overline{RESET}$ signal from the microcontroller to the external card. The output current is internally limited to 15 mA. The CRD_RST is validated when PWR_ON = H and $\overline{PGM}$ = H and hard wired to Ground when the card is deactivated.
13	CRD_CLK	OUTPUT	This pin is connected to the CLK pin of the card connector. The CRD_CLK signal comes from the clock selector circuit output. Combining A0, A1, $\overline{PGM}$ and I/O, as depicted in Table 3 and Figure 3, programs the clock selection. This signal can be forced into a standby mode with CRD_CLK either High or Low, depending upon the mode defined by the programming sequence (Tables 1, 2 and 3 and Figure 4). Care must be observed, at PCB level, to minimize the pick−up noise coming from the CRD_CLK line. It is recommended to put a shield, built with a 10mil copper track, around this line and terminated to the GND.
14	CRD_IO	I/O	This pin handles the connection to the serial I/O pin of the card connector. A bidirectional level translator adapts the serial I/O signal between the card and the microcontroller. The CRD_IO pin current is internally limited to 15 mA. A built−in register holds the previous state presents on the I/O input pin.
15	CRD_VCC	POWER	This pin provides the power to the external card. It is the logic level “1” for CRD_IO, CRD_RST and CRD_CLK signals. The energy stored by the DC−DC external inductor Lout must be smoothed by a 10 μF capacitor, associated with a 100 nF ceramic in parallel, connected across CRD_VCC and GND. In the event of a CRD_VCC U_{VLOW} voltage, the NCN6000 detects the situation and feedback the information in the STATUS bit. The device does not take any further action, particularly the DC−DC converter is neither stopped nor reprogrammed by the NCN6000. It is up to the external MPU to handle the situation. However, when the CRD_VCC is overloaded, the NCN6000 shut off the DC−DC converter, pulls the $\overline{INT}$ pin Low and reports the fault in the STATUS register.
16	GROUND	SIGNAL	The logic and low level analog signals shall be connected to this ground pin. This pin must be externally connected to the PWR_GND pin 17. The designer must make sure no high current transients are shared with the low signal currents flowing into this pin.
17	PWR_GND	POWER	This pin is the Power Ground associated with the built−in DC−DC converter and must be connected to the system ground together with GROUND pin 11. Using good quality ground plane is recommended to avoid spikes on the logic signal lines.
18	Lout_L	POWER	The High Side of the external inductor is connected between this pin and Lout_H to provide the DC−DC function. The built−in MOS devices provide the switching function together with the CRD_VCC voltage rectification.

PIN FUNCTIONS AND DESCRIPTION (continued)

Pin	Name	Type	Description
19	Lout_H	POWER	The High Side of the external inductor is connected between this pin and Lout_L to provide the DC−DC function. The current flowing into this inductor is limited by a sense resistor internally connected from Vbat/pin 20 and pin 19. Typically, Lout = 22 μH, with ESR < 2.0 Ω, for a nominal 55 mA output load.
20	Vbat	POWER	This pin is connected to the supply voltage and monitored by the NCN6000. The operation is inhibited when Vbat is below the minimum 2.70 V value, followed by a PWR_DOWN sequence and a Low STATUS state.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Battery Supply Voltage	Vbat	7.0	V
Battery Supply Current (Note 2)	Ibat	300	mA
Power Supply Voltage	Vcc	6.0	V
Power Supply Current	Icc	±100	mA
Digital Input Pins	Vin	$-0.5\ V < V_{in} < V_{bat} + 0.5\ V$, but < 7.0 V	V
Digital Input Pins	Iin	±5.0	mA
Digital Output Pins	Vout	$-0.5\ V < V_{in} < V_{bat} + 0.5\ V$, but < 7.0 V	V
Digital Output Pins	Iout	±10	mA
Card Interface Pins	Vcard	$-0.5\ V < V_{card} <$ CRD_VCC +0.5 V	V
Card Interface Pins, except CRD_CLK	Icard	±15	mA
Inductor Current	ILout	300	mA
ESD Capability (Note 3) Standard Pins Card Interface Pins and CRD_DET	VESD	 2.0 8.0	kV
TSSOP−20 Package Power Dissipation @ Tamb = +85°C Thermal Resistance Junction to Air ($R_{\theta ja}$)	 P_{DS} $R_{\theta ja}$	 320 125	 mW °C/W
Operating Ambient Temperature Range	TA	−25 to +85	°C
Operating Junction Temperature Range	TJ	−25 to +125	°C
Maximum Junction Temperature (Note 4)	TJmax	+150	°C
Storage Temperature Range	Tsg	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.
2. This current represents the maximum peak current the pin can sustain, not the NCN6000 consumption (see $Ibat_{op}$).
3. Human Body Model, R = 1500 Ω, C = 100 pF.
4. Absolute Maximum Rating beyond which damage to the device may occur.

POWER SUPPLY SECTION (−25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Symbol	Pin	Min	Typ	Max	Unit
Power Supply	Vbat	20	2.7	−	6.0	V
Standby Supply Current Conditions: PWR_ON = L, STATUS = H, CLOCK_IN = H, $\overline{CS}$ = H. All other logic inputs and outputs are open: Vbat = 3.0 V Vbat = 5.0 V	$Ibat_{sb}$	20	 − −	 3.0 −	 8.0 15	μA
DC Operating Current (Figure 19) PWR_ON = H, CLOCK_IN = 0, $\overline{CS}$ = H, all CRD pins unloaded @ Vbat = 6.0 V, CRD_VCC = 5.0 V @ Vbat = 3.6 V, CRD_VCC = 5.0 V	$Ibat_{op}$	20	 − −	 7.0 2.0	 − 5.0	mA
Vbat Undervoltage $Detection_{High}$ Vbat Undervoltage $Detection_{Low}$ Vbat Undervoltage $Detection_{Hysteresis}$	$Vbat_{LH}$ $Vbat_{LL}$ $Vbat_{HY}$	20	2.1 2.0 −	− − 100	2.7 2.6 −	V V mV
Output Card Supply Voltage @ Icc = 55 mA @ 2.70 V ≤ Vbat ≤ 6.0 V CRD_VCC = 3.0 V CRD_VCC = 5.0 V @ $Vbat_{LL}$ < Vbat < 2.70 V CRD_VCC = 5.0 V	Vcc V_{C3H} V_{C5H} V_{C5H}	15	 2.75 4.75 4.50	 − − −	 3.25 5.25 −	V
Output Card Supply Peak Current @ Vcc = 5.0 V @ CRD_VCC = 5.0 V @ CRD_VCC = 3.0 V @ Vbat = 3.6 V, CRD_VCC = 5.0 V, Tamb < 65°C	Iccp	15	 55 55 65	 − − −	 − − −	mA
Output Current Limit Time Out	tdoff	15	−	4.0	−	ms
Output Over Current Limit	Iccov	15	−	−	100	mA
Output Dynamic Peak Current @ CRD_VCC = 3.0 V or 5.0 V, Cout = 10 μF Ceramic XR7, Pulse Width 400 ns (Notes 5 and 6)	Iccd	15	100	−	−	mA
Battery Start−Up Current @ CRD_VCC = 3.0 V, −25°C ≤ TA ≤ + 85°C @ CRD_VCC = 5.0 V, −25°C ≤ TA ≤ + 85°C	Icc_{st}	20	 − −	 140 300	 − −	mA
Output Card Supply Voltage Ripple @ Lout = 22 μH, Cout 1 = 10 μF, Cout 2 = 100 nF, Vbat = 3.6 V Iout = 55 mA CRD_VCC = 5.0 V (Note 5) CRD_VCC = 3.0V	Vcc_{rip}	15	 − −	 − −	 50 50	mV
Output Card Supply Turn On Time @ Lout = 22 μF, Cout1 = 10 μF, Cout2 = 100 nF, Vbat = 2.7 V, CRD_VCC = 5.0 V	Vcc_{TON}	15	−	−	2.0	ms
Output Card Supply Shut Off Time @ Cout1 = 10 μF, Ceramic, Vbat = 2.7 V, CRD_VCC = 5.0 V, Vcc_{OFF} < 0.4 V	Vcc_{TOFF}	15	−	−	250	μs
DC−DC Converter Operating Frequency	Fsw	18	−	600	−	kHz
Power Switch Drain/Source Resistor	R_{ONS}	18	−	1.9	2.2	Ω
Output Rectifier ON Resistor	R_{OND}	15	−	2.8	3.4	Ω

5. Ceramic X7R, SMD types capacitors are mandatory to achieve the CRD_VCC specifications. When electrolytic capacitor is used, the external filter must include a 100 nF, max 50 mΩ ESR capacitor in parallel, to reduce both the high frequency noise and ripple to a minimum. Depending upon the PCB layout, it might be necessary is to use two 6.8 μF/10 V/ceramic/X7R//SMD1206 in parallel, yielding an improved CRD_VCC ripple over the temperature range.
6. According to ISO7816−3, paragraph 4.3.2.

DIGITAL PARAMETERS SECTION @ 2.70 V ≤ Vbat ≤ 6.0 V, NORMAL OPERATING MODE (−25°C to +85°C ambient temperature, unless otherwise noted.) Note: Digital inputs undershoot < −0.30 V to ground, Digital inputs overshoot <0.30 V to Vbat

Rating	Symbol	Pin	Min	Typ	Max	Unit
Input Asynchronous Clock Duty Cycle = 50% @ Vbat = 3.0V over the temperature range	F_{CLKIN}	10	−	−	40	MHz
Clock Rise Time Clock Fall Time	F_{tr} F_{tf}	10	− −	− −	5.0 5.0	ns
I/O Data Transfer Switching Time, Both Directions (I/O and CRD_IO), @ Cout = 30 pF I/O Rise Time* (Note 7) I/O Fall Time	 T_{RIO} T_{FIO}	8, 14	−	−	 0.8 0.8	µs
Input/Output Data Transfer Time, Both Directions @ 50% CRD_VCC, L to H and H to L	T_{TIO}	8, 14	−	−	150	ns
Minimum PWR_ON Low Level Logic State Time to Power Down the DC−DC Converter	T_{WON}	4	2.0	−	−	µs
CRD_VCC Power Up/Down Sequence Interval	T_{DSEQ}		−	0.5	2.0	µs
STATUS Pull Up Resistance	R_{STA}	5	20	50	80	kΩ
Chip Select $\overline{CS}$ Pull Up Resistance	R_{CSPU}	6	20	50	80	kΩ
Interrupt $\overline{INT}$ Pull Up Resistance	R_{INTPU}	9	20	50	80	kΩ
Positive Going Input High Voltage Threshold (A0, A1, $\overline{PGM}$, PWR_ON, $\overline{CS}$, $\overline{RESET}$, CRD_DET)	V_{IH}	1, 2, 3, 4, 6, 7, 11	0.70 * Vbat	−	Vbat	V
Negative Going Input High Voltage Threshold (A0, A1, $\overline{PGM}$, PWR_ON, $\overline{CS}$, $\overline{RESET}$, CRD_DET)	V_{IL}	1, 2, 3, 4, 6, 7, 11	0	−	0.30 * Vbat	V
Output High Voltage STATUS, $\overline{INT}$ @ I_{OH} = −10 µA	V_{OH}	5, 9	Vbat − 1.0 V	−	−	V
Output High Voltage STATUS, $\overline{INT}$ @ I_{OH} = 200 µA	V_{OL}	5, 9	−	−	0.40	V

7. Since a 20 kΩ pull up resistor is provided by the NCN6000, the external MPU can use an Open Drain connection.

DIGITAL PARAMETERS SECTION @ 2.70 V ≤ Vbat ≤ 6.0 V, CHIP PROGRAMMING MODE (−25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Symbol	Pin	Min	Typ	Max	Unit
A0, A1, $\overline{PGM}$, PWR_ON, $\overline{RESET}$ and I/O Data Set Up Time	T_{SMOD}	1, 2, 3, 4, 7, 8	2.0	−	−	µs
A0, A1, $\overline{PGM}$, PWR_ON, $\overline{RESET}$ and I/O Data Set Up Time	T_{HMOD}	1, 2, 3, 4, 7, 8	2.0	−	−	µs
Chip Select $\overline{CS}$ Low State Pulse Width	T_{WCS}	6	2.0	−	−	µs

SMART CARD SECTION (−25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Symbol	Pin	Min	Typ	Max	Unit
CRD_RST @ CRD_VCC = +5.0 V		12		−		
Output $\overline{\text{RESET}}$ V_{OH} @ Icrd_rst = −20 μA	V_{OH}		CRD_VCC − 0.9		CRD_VCC	V
Output $\overline{\text{RESET}}$ V_{OL} @ Icrd_rst = 200 μA	V_{OL}		0		0.4	V
Output $\overline{\text{RESET}}$ Rise Time @ Cout = 30 pF	t_R				100	ns
Output $\overline{\text{RESET}}$ Fall Time @ Cout = 30 pF	t_F				100	ns
CRD_RST @ Vcc = +3.0 V						
Output $\overline{\text{RESET}}$ V_{OH} @ Icrd_rst = −20 μA	V_{OH}		CRD_VCC − 0.9		CRD_VCC	V
Output $\overline{\text{RESET}}$ V_{OL} @ Icrd_rst = 200 μA	V_{OL}		0		0.4	V
Output $\overline{\text{RESET}}$ Rise Time @ Cout = 30 pF	t_R				100	ns
Output $\overline{\text{RESET}}$ Fall Time @ Cout = 30 pF	t_F				100	ns
CRD_CLK @ CRD_VCC = +3.0 V or +5.0 V		13		−		
CRD_VCC = +5.0 V						
Output Frequency (See Note 8)	F_{CRDCLK}				5.0	MHz
Output Duty Cycle @ DC Fin = 50% ±1%	F_{CRDDC}		45		55	%
Output CRD_CLK Rise Time @ Cout = 30 pF	t_R				18	ns
Output CRD_CLK Fall Time @ Cout = 30 pF	t_F				18	ns
Output V_{OH} @ Icrd_clk = −20 μA	V_{OH}		3.15		CRD_VCC	V
Output V_{OL} @ Icrd_clk = 100 μA	V_{OL}		0		+0.5	V
CRD_VCC = +3.0 V						
Output Frequency (See Note 8)	F_{CRDCLK}				5.0	MHz
Output Duty Cycle @ DC Fin = 50% ±1%	F_{CRDDC}		40		60	%
Output CRD_CLK Rise Time @ Cout = 30 pF	t_R				18	ns
Output CRD_CLK Fall Time @ Cout = 30 pF	t_F				18	ns
Output V_{OH} @ Icrd_clk = −20 μA @ Cout = 30 pF	V_{OH}		1.85		CRD_VCC	V
Output V_{OL} @ Icrd_clk = 100 μA @ Cout = 30 pF	V_{OL}		0		0.7	V
CRD_I/O @ CRD_VCC = +5.0 V		14				
CRD_I/O Data Transfer Frequency	F_{IO}			315		kHz
CRD_I/O Rise Time @ Cout = 30 pF	T_{RIO}				0.8	μs
CRD_I/O Fall Time @ Cout = 30 pF	T_{FIO}				0.8	μs
Output V_{OH} @ Icrd_i/o = −20 μA	V_{OH}		CRD_VCC − 0.9		CRD_VCC	V
Output V_{OL} @ Icrd_i/o = 500 μA, V_{IL} = 0 V	V_{OL}		0		0.4	V
CRD_I/O @ CRD_VCC = +3.0 V						
CRD_I/O Data Transfer Frequency	F_{IO}			315		kHz
CRD_I/O Rise Time @ Cout = 30 pF	T_{RIO}				0.8	μs
CRD_I/O Fall Time @ Cout = 30 pF	T_{FIO}				0.8	μs
Output V_{OH} @ Icrd_i/o = −20 μA	V_{OH}		CRD_VCC − 0.9		CRD_VCC	V
Output V_{OL} @ Icrd_i/o = 500 μA, V_{IL} = 0 V	V_{OL}		0		0.4	V
CRD_IO Pull Up Resistor @ PWR_ON = H	R_{CRDPU}	14	14	20	26	kΩ
Card Detection Debouncing Delay:		11		−		
Card Insertion	T_{CRDIN}		50		150	μs
Card Extraction	T_{CRDOFF}		50		150	μs
Card Insertion or Extraction Positive Going Input High Voltage	V_{IHDET}	11	0.70 * Vbat	−	Vbat	V
Card Insertion or Extraction Negative Going Input Low Voltage	V_{ILDET}	11	0	−	0.30 * Vbat	V
Card Detection Bias Pull Up Current @ Vbat = 5.0 V	I_{DET}	11	−	10	−	μA
Output Peak Max Current Under Card Static Operation Mode @ Vcc = 3.0 V or Vcc = 5.0 V	Icrd_iorst	12, 14	−	−	15	mA
Output Peak Max Current Under Card Static Operation Mode @ Vcc = 3.0 V or Vcc = 5.0 V	Icrd_clk	13	−	−	70	mA

8. The CRD_CLK clock can operate up to 20 MHz, but the rise and fall time are not guaranteed to be fully within the ISO7816 specification over the temperature range. Typically, tr and tf are 12 ns @ CRD_CLK = 10 MHz.

Programming and Status Functions

The NCN6000 features a programming interface and a status interface. Figure 4 illustrates the programming mode.

Table 1. Programming and Status Functions Pinout Logic

Pins	Name	CRD_VCC Prg. 3.0 V/5.0 V	CLOCK_IN Divide Ratio	CRD_DET	CLOCK STOP AND START	Poll Card Status	DC−DC Status	Vbat Status	CRD_VCC Status
5	STATUS	Not Affected	Not Affected	Not Affected	Not Affected	READ	READ	READ	READ
6	$\overline{CS}$	Latch On Rising Edge	Latch On Rising Edge	Latch On Rising Edge	Latch On Rising Edge	0	0	0	0
3	$\overline{PGM}$	0	0	0	0	1	1	1	1
1	A0	0/1	0/1	0/1	0/1	0	1	0	1
2	A1	0/1	0/1	1	0	0	0	1	1
7	$\overline{RESET}$	0	0	1	1	Z	Z	Z	Z
8	I/O (in)	0/1	0/1	0/1	0/1	Z	Z	Z	Z

The $\overline{PGM}$ signal, pin 3, controls the mode of operation (chip programming or smart card transaction) and must be set up accordingly prior to pull Chip Select (pin 6) Low.

Table 2. Status Pin Logic Output

Name	$\overline{CS}$	$\overline{PGM}$	A1	A0	Status Logic Level
None	H	X	X	X	No Chip Access
None	L	L	X	X	Programming Mode, No Read Available
CARD PRESENT	L	H	L	L	Low: No Card Inserted High: Card inserted
DC−DC	L	H	L	H	Low: DC−DC Over Range High: DC−DC Operates Normally
Vbat	L	H	H	L	Low: Vbat Within Range High: Vbat Below Minimum range
CRD_VCC Overload	L	H	H	H	Low: CRD_VCC Voltage Below Minimum Range High: CRD_VCC in Range

Card VCC, Card CLOCK and Card Detection Polarity Programming

The CRD_VCC and CLOCK_IN programming options allows matching the system frequency with the card clock frequency, and to select 3.0 V or 5.0 V CRD_VCC supply. The CRD_DET programming option allows the usage of either Normally Open or Normally Close detection switch. Table 3 highlights the A0, A1, $\overline{PGM}$ and I/O logic states for the possible options. **The default power up reset condition is state 1: asynchronous clock, ratio 1/1, CRD_CLK active, CRD_DET = Normally Open, CRD_VCC = 3.0 V.** All states are latched for each output variable in programming mode at the positive going slope of Chip Select [$\overline{CS}$] signal. It is the system designer's responsibility to set up the options needed to match the chip with the peripherals. In particular, when using Normally Close switch, the CRD_DET polarity must be defined during the first cycles of the initialization.

Table 3. Card VCC, Card Clock and Card Detection Polarity Truth Table

HEXA	$\overline{CS}$	PWR_ON	$\overline{PGM}$	$\overline{RESET}$	A1	A0	I/O	CRD_VCC	CRD_CLK	CRD_DET	STATUS
$00	**L**	**−**	**L**	**L**	**L**	**L**	**L**	**3.0 V**	**CLOCK_IN 1/1**	**−**	H (Note 13)
$01	L	−	L	L	L	L	H	3.0 V	CLOCK_IN 1/2	−	H (Note 13)
$02	L	−	L	L	L	H	L	3.0 V	CLOCK_IN 1/4	−	H (Note 13)
$03	L	−	L	L	L	H	H	3.0 V	CLOCK_IN 1/8	−	H (Note 13)
$04	L	−	L	L	H	L	L	5.0 V	CLOCK_IN 1/1	−	H (Note 13)
$05	L	−	L	L	H	L	H	5.0 V	CLOCK_IN 1/2	−	H (Note 13)
$06	L	−	L	L	H	H	L	5.0 V	CLOCK_IN 1/4	−	H (Note 13)
$07	L	−	L	L	H	H	H	5.0 V	CLOCK_IN 1/8	−	H (Note 13)
$08	L	−	L	H	L	L	L	−	**START**	−	H (Note 13)
$09	L	−	L	H	L	L	H	−	STOP Low	−	H (Note 13)
$0A	L	−	L	H	L	H	L	−	STOP High	−	H (Note 13)
$0B	L	−	L	H	L	H	H	−	Reserve	−	H (Note 13)
$0C	L	−	L	H	H	L	L	−	−	Normally Open (Note 12)	H (Note 13)
$0D	L	−	L	H	H	L	H	−	−	Normally Close (Note 12)	H (Note 13)
$0E	L	−	L	H	H	H	L	−	−	Normally Close (Note 12)	H (Note 13)
$0F	L	−	L	H	H	H	H	−	−	Normally Close Note 12)	H (Note 13)
$10	L	−	H	Z	L	L	Z	−	−	−	Card Present
$12	L	1	H	Z	L	H	Z	−	−	−	DC−DC status
$14	L	−	H	Z	H	L	Z	−	−	−	Vbat
$16	L	1	H	Z	H	H	Z	−	−	−	CRD_VCC

9. The programmed conditions are latched upon the Chip Select ($\overline{CS}$, pin 6) positive going transient.
10. Card clock integrity is guaranteed no spikes whatever be the frequency switching.
11. The STATUS register is not affected when the NCN6000 operates in any of the programming functions.
12. The CRD_VCC and CRD_CLK are not affected when the NCN6000 operates outside their respective decoded logic address.
13. The High Level on STATUS in registers $00 to $0F, inclusive, having being implemented to reduce current consumption but have no other meanings.
14. At turn on, the NCN6000 is initialized with CRD_VCC = 3.0V, CLOCK_IN Ratio = 1/1, CRD_CLK = START, CRD_DET = Normally Open.

DC−DC Converter and Card Detector Status

The NCN6000 status can be polled when $\overline{CS}$ = L. Please consult Figures 4 and 5 for a description of input and output signals. The status message is described in Table 4.

Note: in order to cope with a start up under low battery condition, the Vbat OK message uses a negative logic as depicted here below.

Table 4. Card and DC−DC Status Output

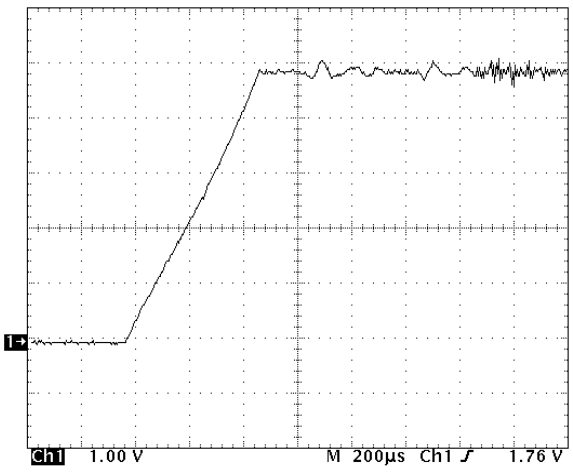
$\overline{PGM}$	A1	A0	STATUS	Message
HIGH	L	L	LOW	No Card
HIGH	L	L	HIGH	Card Present
HIGH	L	H	LOW	DC−DC Converter Overloaded
HIGH	L	H	HIGH	DC−DC Converter OK
HIGH	H	L	LOW	Vbat OK
HIGH	H	L	HIGH	Vbat Undervoltage
HIGH	H	H	HIGH	CRD_VCC OK
HIGH	H	H	LOW	CRD_VCC Undervoltage

The STATUS pin provides a feedback related to the detection of the card, the state of the DC−DC converter, the Vbat undervoltage and CRD_VCC undervoltage situations. When $\overline{PGM}$ = H, the STATUS pin returns a High if a card is detected present, a Low being asserted if there is no card inserted. In any case, the external card is not automatically powered up. When the external MPU asserts PWR_ON = H, together with $\overline{CS}$ = L, the CRD_VCC supply is provided to the card and the state of the DC−DC converter, the Vbat and the CRD_VCC can be polled through the STATUS pin.

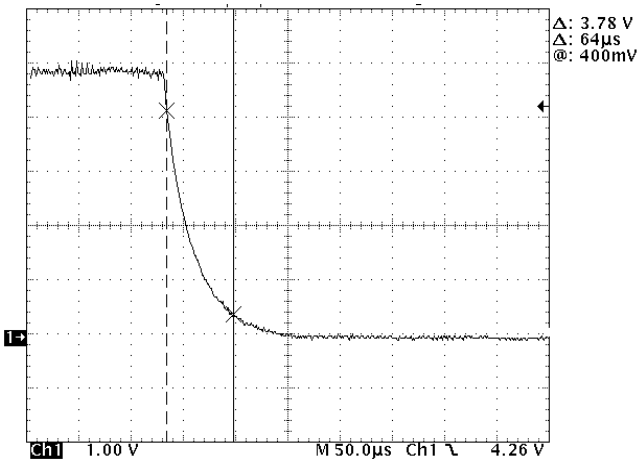
Card Power Supply Timing

At power up, the CRD_VCC power supply rise time depends upon the current capability of the DC−DC converter associated with the external inductor L1 and the reservoir capacitor connected across CRD_VCC and GROUND.

On the other hand, at turn off, the CRD_VCC fall time depends upon the external reservoir capacitor and the peak current absorbed by the internal CMOS transistor built across CRD_VCC and GROUND. These behaviors are depicted in Figure 6. Since these parameters have finite values, depending upon the external constraints, the designer must take care of these limits if the t_{ON} or the t_{OFF} provided by the data sheets does not meet his requirements.



Typical CRD_VCC Rise Time @ Cout = 10 µF, V = 5.0 V



Typical CRD_VCC Fall Time @ Cout = 10 µF, V = 5.0 V

Figure 6. Card Power Supply Turn ON and OFF Timing

Basic Operating Modes Flow Chart

The NCN6000 brings all the functions necessary to handle data communication between a host computer and the smart card. The built−in Chip Select pin provides a simple way to share the same MPU bus with several card interface. On top of that, the logic control are derived from specific pins, avoiding the risk of mixing up the operation when the interface is controlled by a low end microcontroller.

During the transaction operation, the external MPU takes care of whatever is necessary to he data on the single bidirectional I/O line. Leaving aside the DC−DC control and associated failures, the NCN6000 does not take any further responsibility in the data transaction.

When the chip operates in the programming mode, the NCN6000 provide a flexible access to set up the CRD_VCC voltage, the CRD_CLK and the CRD_DET smart card signals.

The external microcontroller takes care of the smart card transaction and shall handle the interface accordingly.

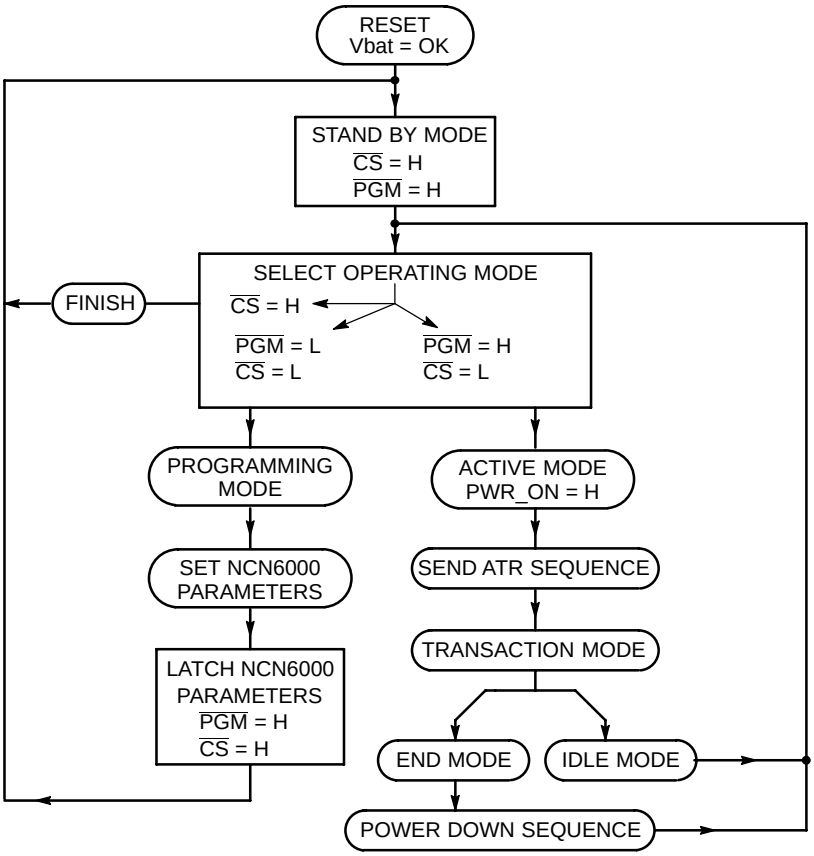


Figure 7. Operating Modes Flow Chart

Standby Mode

The Standby Mode allows the NCN6000 to detect a card insertion, keeping the power consumption at a minimum. The power supply CRD_VCC is not applied to the card, until the external controllers set PWR_ON = H with $\overline{CS}$ = L.

Standby Mode Logic Conditions:		**Card Output:**	
$\overline{CS}$	= H	CRD_VCC	= 0 V
PWR_ON	= H	CRD_CLK	= L
A0	= Z	CRD_RST	= L
A1	= Z	CRD_IO	= L
$\overline{PGM}$	= Z		
I/O	= Z		
$\overline{RESET}$	= Z		

When a card is inserted, the internal logic filters the signal present pin 11, then asserts the $\overline{INT}$ pin to Low if the pulse applied to CRD_DET is longer than 150 μs. The external MPU shall run whatever is necessary to handle the card.

The $\overline{INT}$ is cleared (return to High) when a positive going transition is asserted to either the $\overline{CS}$ or to the PWR_ON signal logically combined with Chip Select = Low.

Programming Mode

The programming mode allows the configuration of the card power supply, card clock and Card Detection input logic polarity. These signals (CRD_VCC, CRD_CLK and CRD_DET) are described in the pin description paragraph associated with Tables 1 and 3 and Figures 4 and 8.

Programming Mode Logic Conditions:		**Card Output:**	
$\overline{CS}$	= L	CRD_VCC	= 0 V
PWR_ON	= L	CRD_CLK	= L
A0	= H/L	CRD_RST	= L
A1	= H/L	CRD_IO	= H/L depending upon the previous I/O pin logic state
$\overline{PGM}$	= L		
I/O	= L/H		
$\overline{RESET}$	= L/H		

The I/O and $\overline{RESET}$ pins are not connected to the smart card and become logic inputs to control the NCN6000 programming sequence. The programmed values are latched upon transition of $\overline{CS}$ from Low to High, $\overline{PGM}$ being Low during the transition.

When a programming mode is validated by a Chip Select negative going transient, the mode is latched and $\overline{PGM}$ can be released to High. This latch is automatically reset when $\overline{CS}$ returns to High.

The logic input signals can be set simultaneously, or one bit a time (using either a STAA or a BSET function), the key point being the minimum delay between the shorter bit and the Chip Select pulse. The programmed value is latched into the NCN6000 register on the $\overline{CS}$ positive going edge.

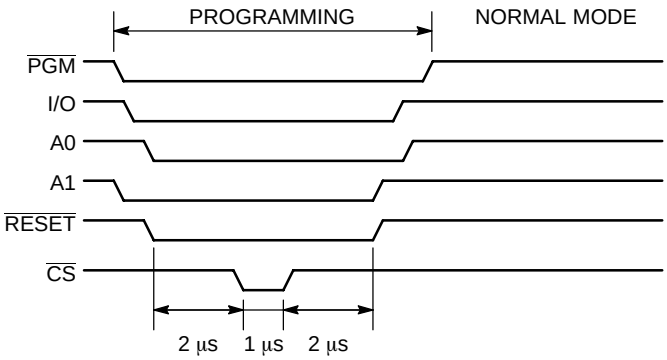


Figure 8. Minimum Programming Timings

Active Mode

In the active mode, the NCN6000 is selected by the external MPU and the STATUS pin can be polled to get the status of either the DC−DC converter or the presence of the card (inserted or not valid). The power is not connected to the card: CRD_VCC = 0 V.

Active Mode Logic Conditions:		**Card Output:**	
$\overline{CS}$	= L	CRD_VCC	= 0 V
PWR_ON	= L	CRD_CLK	= L
A0	= L	CRD_RST	= L
A1	= L	CRD_IO	= H/L depending upon the previous I/O pin logic state
$\overline{PGM}$	= H		
I/O	= Z		
$\overline{RESET}$	= Z		
STATUS	= L/H is Card Inserted?		

The Chip Select pulse [$\overline{CS}$] will automatically clear the previously asserted $\overline{INT}$ signal upon the positive going transition.

If a card is present, the MPU shall activate the DC−DC converter by asserting PWR_ON = H. The NCN6000 will automatically run a power up sequence when the CRD_VCC reaches the undervoltage level (either V_{C5H} or V_{C3H}, depending upon the CRD_VCC voltage supply programmed). The CRD_IO, CRD_RST and CRD_CLK pins are validated, according to the ISO7816−3 sequence. The interface is now in transaction mode and the system is ready for data exchange through the I/O and $\overline{RESET}$ lines. At any time, the microcontroller can change the CRD_CLK frequency and mode, or the CRD_VCC value as determined by the card being in use.

Transaction Mode

During the transaction mode, the NCN6000 maintains power supply and clock signal to the card. All the signal levels related with the card are translated as necessary to cope with the MPU and the card.

The DC−DC converter status and the Vbat state can be monitored on the STATUS by using the A0 and A1 logic inputs as depicted in Tables 3 and 4.

Transaction Mode Logic Conditions:		**Card Output:**	
$\overline{CS}$	= L	CRD_VCC	= 3.0 or 5.0 V
PWR_ON	= H	CRD_CLK	= CLOCK
A0	= H	CRD_RST	= H/L
A1	= H	CRD_IO	= DATA TRANSFER
$\overline{PGM}$	= H		
I/O	= DATA TRANSFER		
$\overline{RESET}$	= H/L		
STATUS	= L/H DC−DC status: Fail/Pass?		

To make sure the data are not polluted by power losses, it is recommended to check the state of CRD_VCC before launching a new data transaction. Since $\overline{CS}$ = L, this is achieved by forcing bits A0 and A1 according to Table 4, and reading the STATUS pin 5.

Idle Mode

The idle mode is used when a card is powered up (CRD_VCC = Vcc), without communication on going.

Idle Mode Logic Conditions:		**Card Output:**	
$\overline{CS}$	= L	CRD_VCC	= 3.0 or 5.0 V
PWR_ON	= H	CRD_CLK	= CLOCK active or L or H
A0	= H	CRD_RST	= H
A1	= H	CRD_IO	= Z
$\overline{PGM}$	= H		
I/O	= Z		
$\overline{RESET}$	= H		
STATUS	= L/H according to the internal register results		

In addition, the CRD_CLK signal can be stopped, as depicted in Tables 3 and 4, to minimize the current consumption of the external smart card, leaving CRD_VCC active.

Power Down Operation

The power down mode can be initiated by either the external MPU (pulling PWR_ON = L) or by one of the internal error condition (CRD_VCC overload or Vbat Low). The communication session is terminated immediately, according to the ISO7816−3 sequence. On the other hand, the MPU can run the Standby mode by forced $\overline{CS}$ = H.

When the card is extracted, the interface shall detect the operation and run the Power Shut Off of the card as described by the ISO/CEI 7816−3 sequence depicted here after:

ISO7816−3 sequence:

⇒ Force RST to Low

⇒ Force CLK to Low, unless it is already in this state

⇒ Force CRD_IO to Low

⇒ Shut Off the CRD_VCC supply

Since the internal digital filter is activated for any card insertion or extraction, the physical power sequence will be activated 150 μs maximum after the card has been extracted. Of course, such a delay does not exist when the MPU launch the power down intentionally.

The time delay between each negative going signal is 500 ns typical (Figure 10).

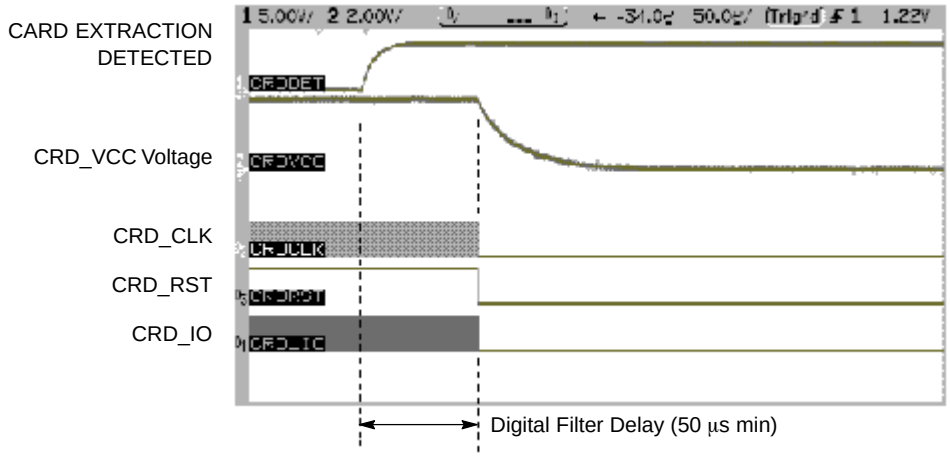


Figure 9. Typical Power Down Sequence in the NCN6000 Interface

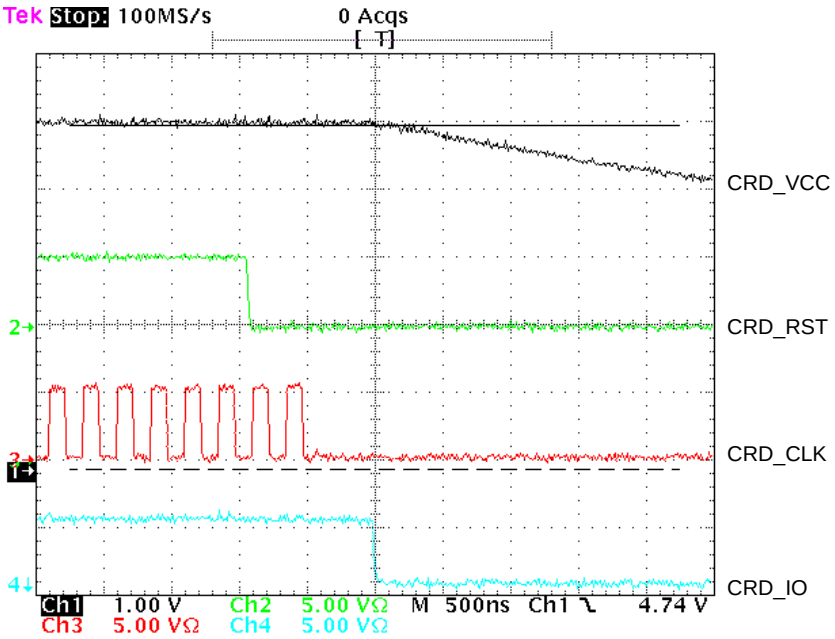


Figure 10. Power Down Sequence Details

Card Detection

The card detector circuit provides a 500 kΩ pull up resistor to bias the CRD_DET pin, yielding a logic High when the pin is left open (assuming a NO switch). The internal logic associated with pin 11 provides an automatic selection of the slope card detection, depending upon the polarity set by the external MPU. At start up, the CRD_DET is preset to cope with Normally Open switch. When a Normally Close switch is used in the card socket, it is mandatory to program the NCN6000 chip during the initialization sequence, otherwise the system will not start if a card was previously inserted. Table 3 gives the programming code for such a function. The next lines provide a typical assembler source to handle this CRD_DET Normally Close polarity:

```
Smart  EQU  $20        ; NCN6000 Physical CS Address
       LDX  #$1000     ; Offset
       LDAA #$09       ; I/O = H, A0 = A1 = L, RESET = H
       STAA smart, X   ; Set CRD_DET = Normally Closed
                         Switch
```

The CRD_DET polarity can be updated at any time, during the Program Mode sequence ($\overline{PGM}$ = L), but, generally speaking, is useless since the switch does not change during the usage of the considered module. On the other hand, the card detection switch shall be connected across pin 11 and ground, for any polarity selected.

The transition presents pin 11, whatever be the polarity, is filtered out by the internal digital filter circuit, avoiding false interrupt. In addition to the minimum internal 50 μs timing, the MPU shall provide an additional delay to cope with the mechanical stabilization of the card interface (typically 3 ms), prior to valid the CRD_VCC supply.

When a card is inserted, the detector circuit asserts $\overline{INT}$ = Low as depicted before. When the NCN6000 detects a card extraction, the power down sequence is activated, regardless of the PWR_ON state, and the $\overline{INT}$ pin is asserted Low. It is up to the external MPU to clear this interrupt by forcing a chip select pulse as depicted in Figure 5.

The 75 μs delay represent the digital filter built−in the NCN6000 chip being used for the characterization. Any pulse shorter than this delay does not generate an interrupt. However, to guarantee an interrupt will be generated, the CRD_DET signal must be longer than 150 μs as defined by the specification.

The Chip Select pulse is generated by the external microcontroller, the minimum pulse width being 2 μs to make sure the card is detected.

The oscillogram, Figure 11, depicts the behavior for a Normally Open switch, the delay existing between the interrupt negative going state and the $\overline{CS}$ being Low comes from the particular software latency existing in this particular MPU.

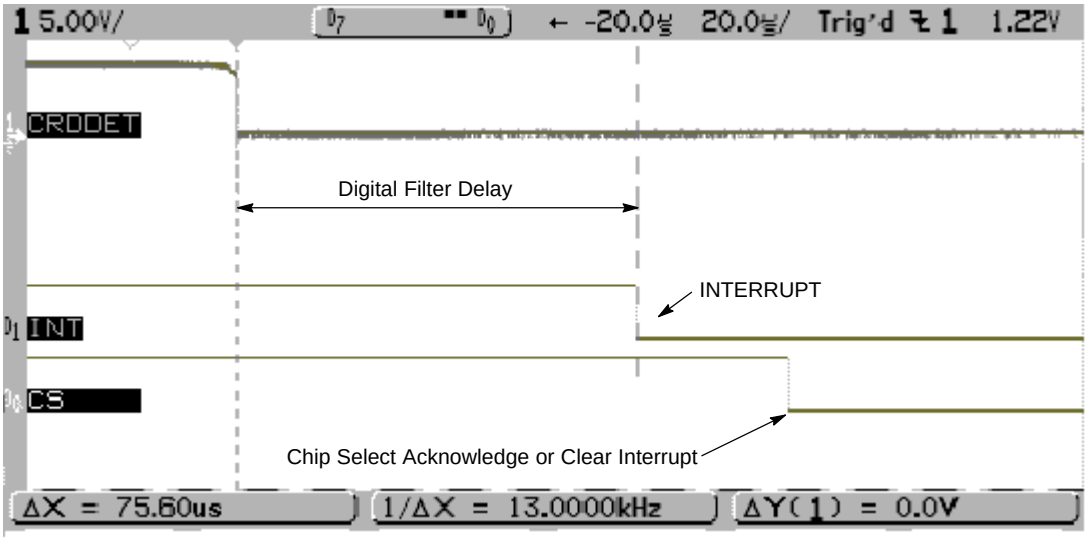


Figure 11. Card Insertion Detection and Interrupt Signals

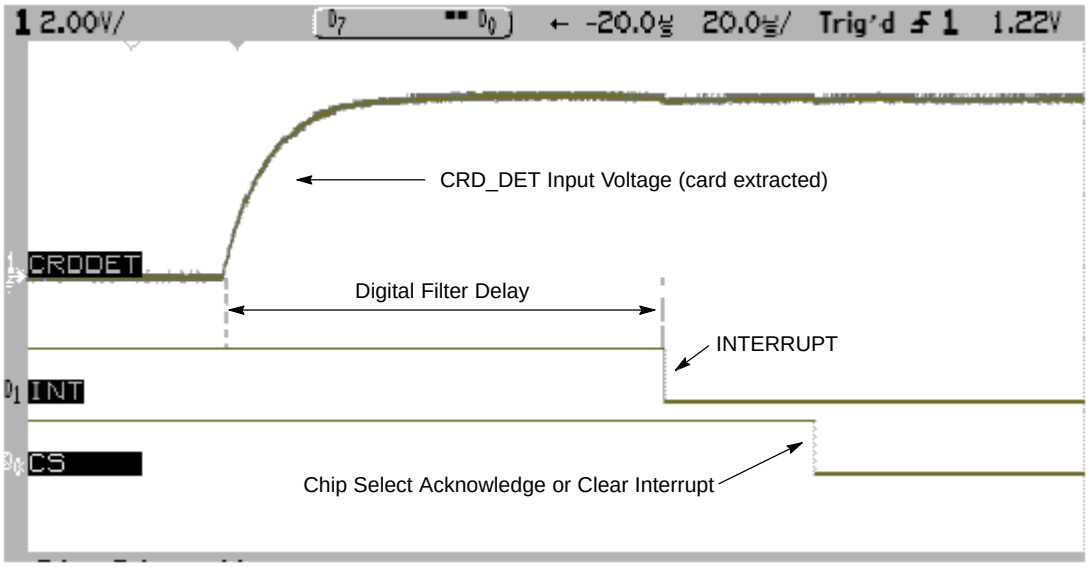


Figure 12. Card Extraction Detection and Interrupt Signals

When the card is extracted, the CRD_DET signal generates an interrupt, assuming the positive pulse width is longer than the digital filter. The oscillogram, Figure 12, depicts the behavior for a Normally Open switch.

Note: since the internal pull up resistor is relatively high (500 kΩ typical), one must use a 10 MΩ input impedance probe to read this signal.

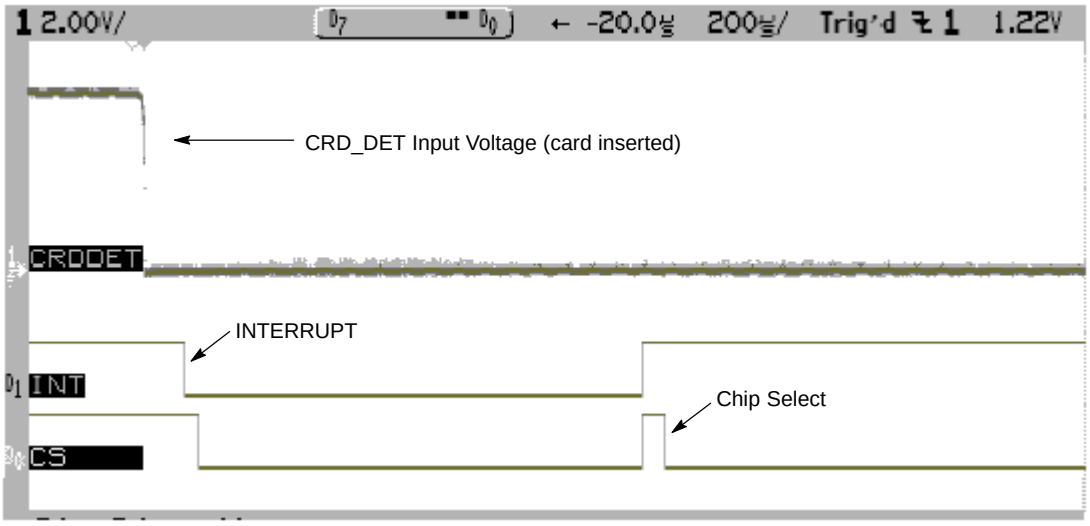


Figure 13. Interrupt Acknowledgement During a Card Insertion Detection Sequence

The interrupt signal, provided pin 9, is cleared by a positive going Chip Select signal as depicted by the oscillogram, Figure 13. The $\overline{CS}$ pulse width is irrelevant, as long as it is larger than 2.0 µs, to activate a different sequence. Leaving the interrupt signal Low has no influence on the internal behavior of the NCN6000, but will be automatically cleared when the DC−DC will be activated by the MPU ($\overline{CS}$=L, PWR_ON = Positive High transition)

Power Management

The purpose of the power management is to activate the circuit functions needed to run a given mode of operation, yielding a minimum current consumption on the Vbat supply. In the Standby mode (PWR_ON = L), the power management provides energy to the card detection circuit only. All the card interface pins are forced to ground potential.

In the event of a power up request coming from the external MPU (PWR_ON = H, $\overline{CS}$ = L), the power manager starts the DC−DC converter.

When the CRD_VCC voltage reaches the programmed value (3.0 V or 5.0 V), the circuit activates the card signals according to the following sequence:

CRD_VCC
⇒CRD_IO
⇒CRD_CLK
⇒CRD_RST

The logic level of the data lines are asserted High or Low, depending upon the state forced by the external MPU, when the start up sequence is completed. Under no situation the NCN6000 shall launch automatically a smart card ATR sequence. Assuming PWR_ON = H, the CRD_VCC voltage is maintained whatever be the logic level presents on Chip Select, pin 6.

At the end of the transaction, asserted by the MPU (PWR_ON = L, $\overline{CS}$ = L), or under a card extraction, the ISO7816−3 power down sequence takes place:

CRD_RST
⇒CRD_CLK
⇒CRD_IO
⇒CRD_VCC

When $\overline{CS}$ = H, the bi−directional I/O line (pins 8 and 15) is forced into the High impedance mode to avoid signal collision with any data coming from the external MPU.

The CRD_VCC voltage is controlled by means of $\overline{CS}$ and PWR_ON logic signal as depicted in Figure 14. The PWR_ON logic level define the CRD_VCC voltage status, the amplitude being the one pre programmed into the chip.

In order to avoid uncontrolled command applied to the smart card, the NCN6000 internal logic circuit, together with the Vbat monitoring, clamps the card outputs until the CRD_VCC voltage reaches the minimum value. During the CRD_VCC slope, all the card outputs are kept Low and no spikes can be write to the smart card. The oscillogram on the right hand side is a magnification of the curves given on the opposite side.

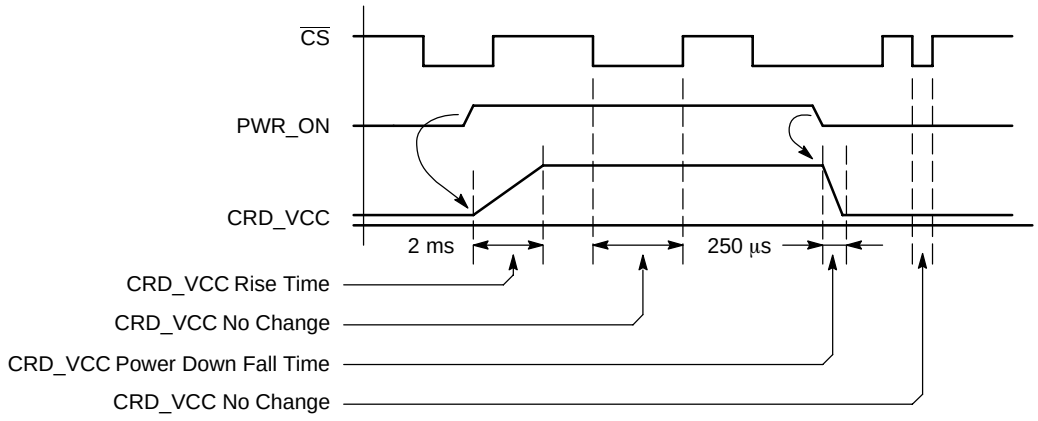


Figure 14. Card Power Supply Control

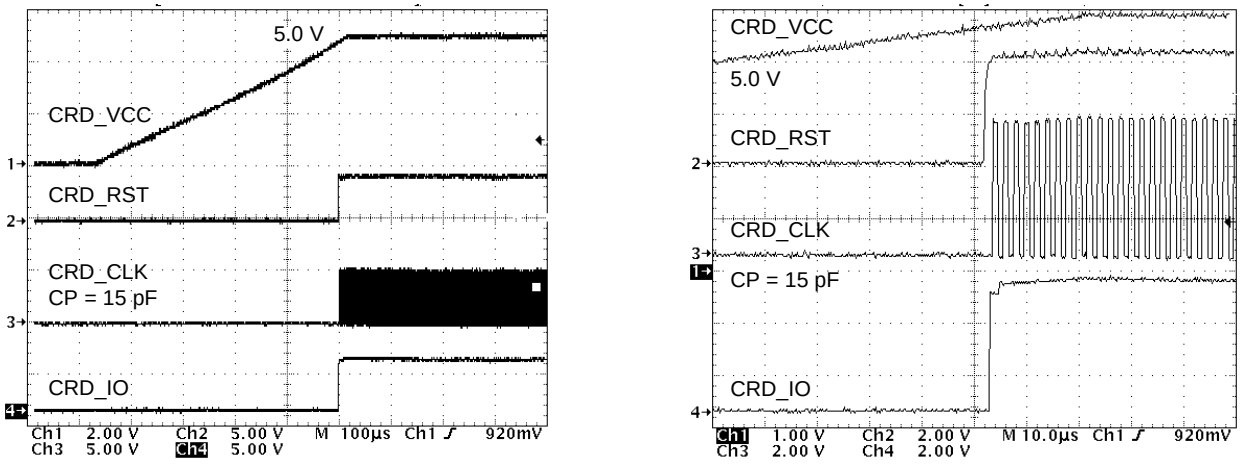


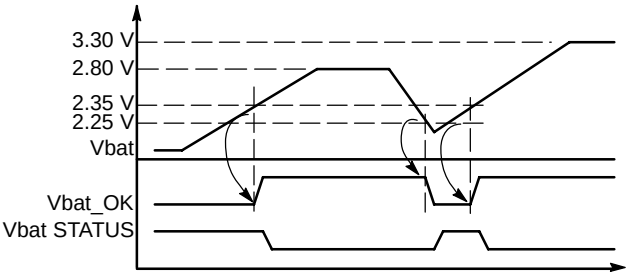
Figure 15. Smart Card Signals Sequence at Power On

Vbat Supply Voltage Monitoring

The built−in comparator, associated with the band gap reference, continuously monitors the +Vbat input. During the start up, all the NCN6000 functions are deactivated and no data transfer can take place. When the +Vbat voltage rises above 2.35 V (typical), the chip is activated and all the functions becomes available. The typical behavior is provided here after Figure 16. At this point, the internal Power On Reset signal is activated (not accessible externally) and all the logic signals are forced into the states as defined by Table 3.

If the +Vbat voltage drops below 2.25 V (typical) during the operation, the NCN6000 generate a Power Down sequence and is forced in a no operation mode. The built−in 100 mV (typical) hysteresis avoids unstable operation when the battery voltage slowly varies around the 2.30 V.

On the other hand, the microcontroller can read the STATUS signal, pin 5, to control the state of the battery prior to launch either a NCN6000 programming or an ATR sequence (Table 4).



Note: Drawing is not to scale and voltages are typical.
See specifications data for details.

Figure 16. Typical Vbat Monitoring

DC−DC Converter Operation

The built−in DC−DC converter is based on a modified boost structure to cover the full battery and card operating voltage range. The built−in battery voltage monitor provides an automatic system to accommodate the mode of operation whatever be the Vbat and CRD_VCC voltages. Comparator U3/Figure 17 tracks the two voltages and set up the operating mode accordingly.

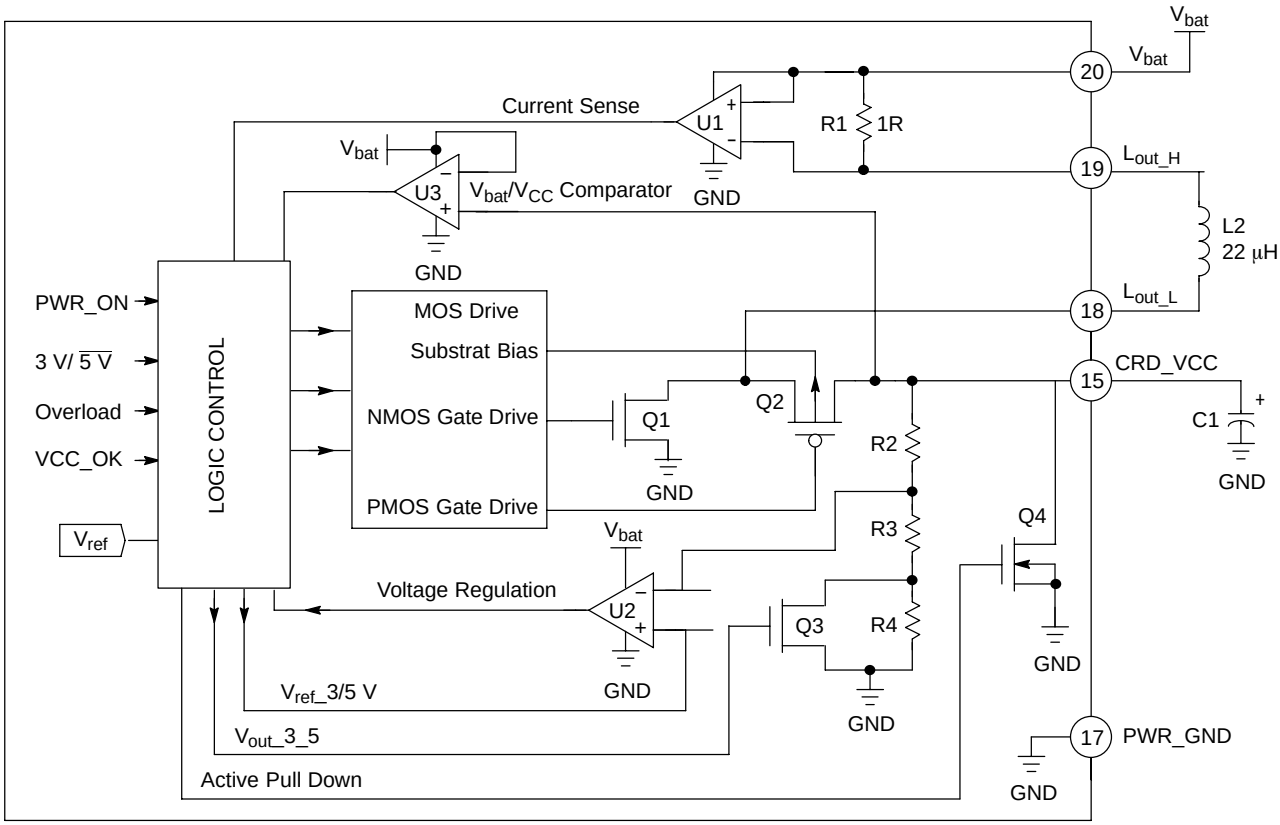


Figure 17. Basic DC−DC Structure

When the input voltage Vbat is lower than the programmed CRD_VCC, the system operates under the boost mode, providing the voltage regulation and current limit to the smart card. In this mode, the external inductor, typically 22 μH, stores the energy to drive the +5.0 V card supply from the external low voltage battery. The oscillogram, Figure 18, depicts the DC−DC behavior under these two modes of operation.

Beside the DC−DC converter, NMOS Q4 provides a low impedance to ground during the Power Down sequence, yielding the 250 μs maximum switch time depicted in the data sheet.

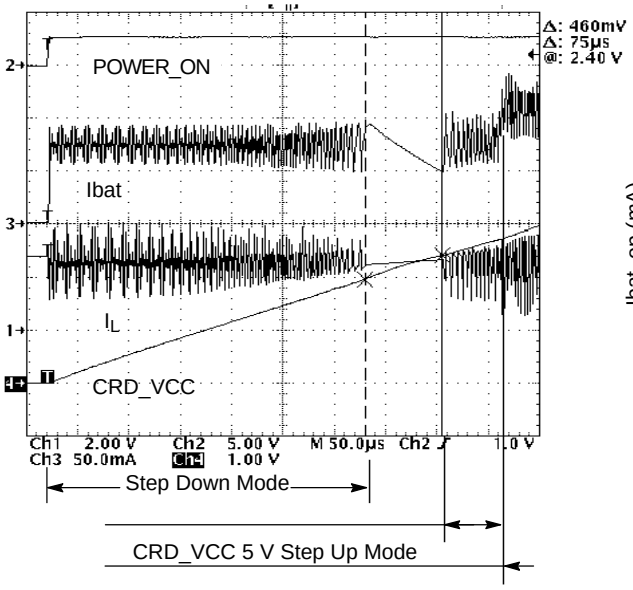


Figure 18. DC−DC Operating Modes

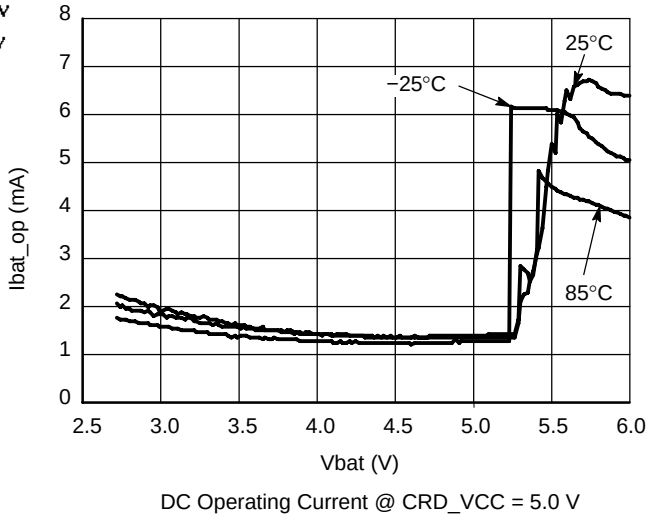


Figure 19. Typical DC Operating Current

When the input voltage Vbat is higher than the programmed CRD_VCC, the system operates under a step down mode, yielding the voltage regulation and current limit identical to the boost mode. In this case, the built−in structure turns Off Q1 and inverts the Q2 substrate bias to control the current flowing to the load.These operations are fully automatic and transparent for the end user.

The High and Low limits of the current flowing into the external inductor L1 are sensed by the operational amplifier U1 associated with the internal shunt R1. Since this shunt resistor is located on the hot side of the inductor, the device reads both the charge and discharge of the inductor, providing a clean operation of the converter.

In order to optimize the DC−DC power conversion efficiency, it is recommended to use external inductor with R < 2.0 Ω.

The output capacitor C1 stores the energy coming from the converter and smooths the CRD_VCC voltage applied to the external card. At this point, care must be observed, beside the micro farad value, to select the right type of capacitor. According to the capacitor's manufacturers, the internal ESR can range from a low 10 mΩ to more than 3.0 Ω, thus yielding high losses during the DC−DC operation, depending upon the technology used to build the capacitor.

The standard electrolytic capacitors have the low cost advantage for a relative high micro farad value, but have poor tolerance, high leakage current and high ESR.

The tantalum type brings much lower leakage current together with high capacity value per volume, but cost can be an issue and ESR is rarely better than 500 mΩ.

The new ceramic type have a very low leakage together with ESR in the 50 mΩ range, but value above 10 μF are relatively rare. Moreover, depending upon the low cost ceramic material used to build these capacitors, the thermal coefficient can be very bad, as depicted in Figure 20. The X7R type is highly recommended to achieve low voltage ripple.

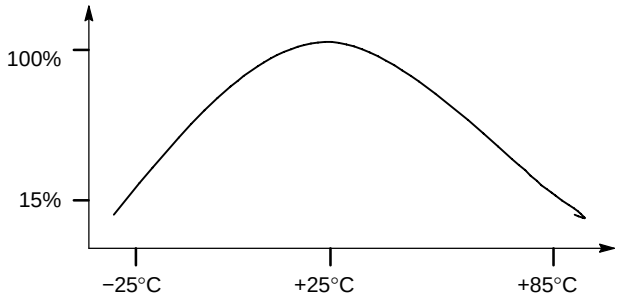
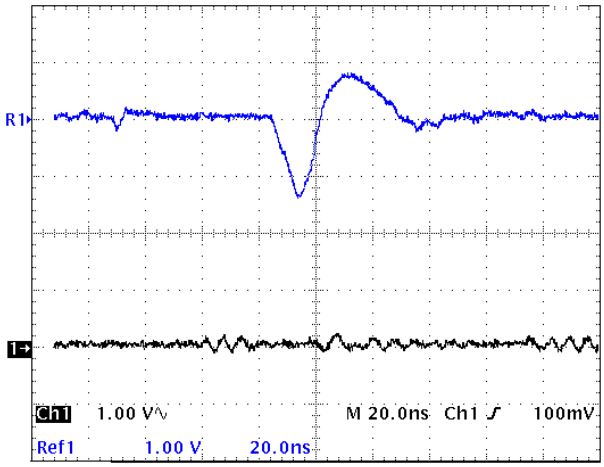


Figure 20. Typical Y7R Ceramic Type Value as a Function of the Temperature.

Based on the experiments carried out during the NCN6000 characterization, the best comprise, at time of printing this document, is to use two 6.8 μF/10 V/Ceramic/X7R capacitor in parallel to achieve the CRD_VCC filtering. The ESR will not extend 50 mΩ over the temperature range and the combination of standard parts provide an acceptable –20% to +20% tolerance, together with a low cost. Obviously, the capacitor must be SMD type to achieve the extremely low ESR and ESL necessary for this application. Figure 21 illustrates the CRD_VCC ripple observed in the NCN6000 demo board depending upon the type of capacitor used to filter the output voltage.

Table 5. Ceramic/Electrolytic Capacitors Comparison

Manufacturers	Type/Series	Format	Max Value	Tolerance	Typ. Z @ 500 kHz
MURATA	CERAMIC/GRM225	0805	10 μF/6.3 V	+80%/−20%	30 mΩ
VISHAY	Tantalum/594C/593C		10 μF/16 V		450 mΩ
VISHAY	Electrolytic/94SV		10 μF/10 V	−20%/+20%	400 mΩ
	Electrolytic Low Cost		10 μF/10 V	−35%/+50%	2.0 Ω



Top Trace = Electrolytic or Tantalum 10 μF
Bottom Trace = X7R 10 μF ceramic
The high ripple pulse across CRD_VCC is the consequence of the large ESR of the electrolytic capacitor.

Figure 21. CRD_VCC Ripple as a Function of the Capacitor Technology

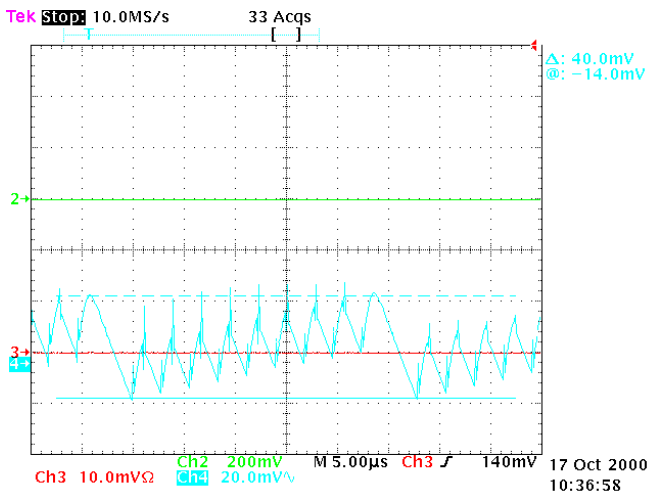
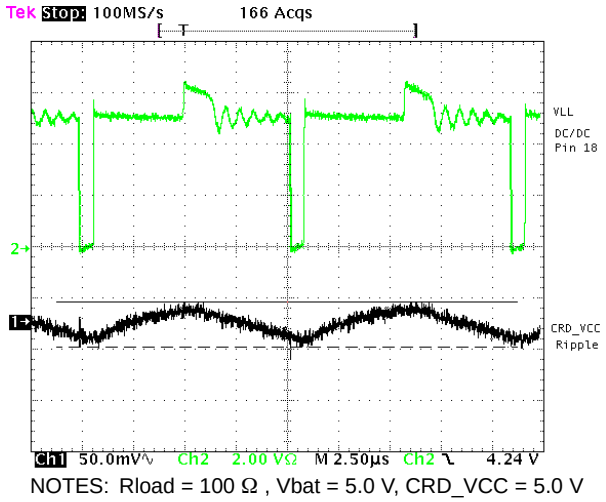


Figure 22. External Capacitor Current Charge and CRD_VCC Voltage Ripple.



NOTES: Rload = 100 Ω , Vbat = 5.0 V, CRD_VCC = 5.0 V
Cout = 10 μF/X7R, CRD_CLK = Stop High

Figure 23. CRD_VCC Voltage Ripple

Clock Divider

The main purpose of the built−in clock generator is threefold:

1. Adapts the voltage level shifter to cope with the different voltages that might exist between the MPU and the Smart Card.
2. Provides a frequency division to adapt the Smart Card operating frequency from the external clock source.
3. Controls the clock state according to the smart card specification.

In addition, the NCN6000 adjusts the signal coming from the microprocessor to get the Duty Cycle window as defined by the ISO7816−3 specification.

The logic input pins A0, A1, $\overline{\text{PGM}}$, I/O and $\overline{\text{RESET}}$ fulfill the programming functions when both $\overline{\text{PGM}}$ and $\overline{\text{CS}}$ are Low. The clock input stage (CLOCK_IN) can handle a 40 MHz frequency maximum, the divider being capable to provide a 1:8 ratio. Of course, the ratio must be defined by the engineer to cope with the Smart Card considered in a given application and, in any case, the output clock [CRD_CLK] shall be limited to 20 MHz maximum signal. In order to maximize the CLOCK_IN bandwidth, this pin has no Schmitt trigger input. The simple associated CMOS has a Vbat/2 threshold level. In order to minimize the dI/dt and dV/dV developed in the CRD_CLK line, the peak current as been internally limited to 30 mA peak (typical @ CRD_VCC = 5.0 V), hence limited the rise and fall time to 10 ns typical. Consequently, the NCN6000 fulfills the ISO7816 specification up to 10 MHz maximum, but can be used up to 20 MHz when the final application operates in a limited ambient temperature range.

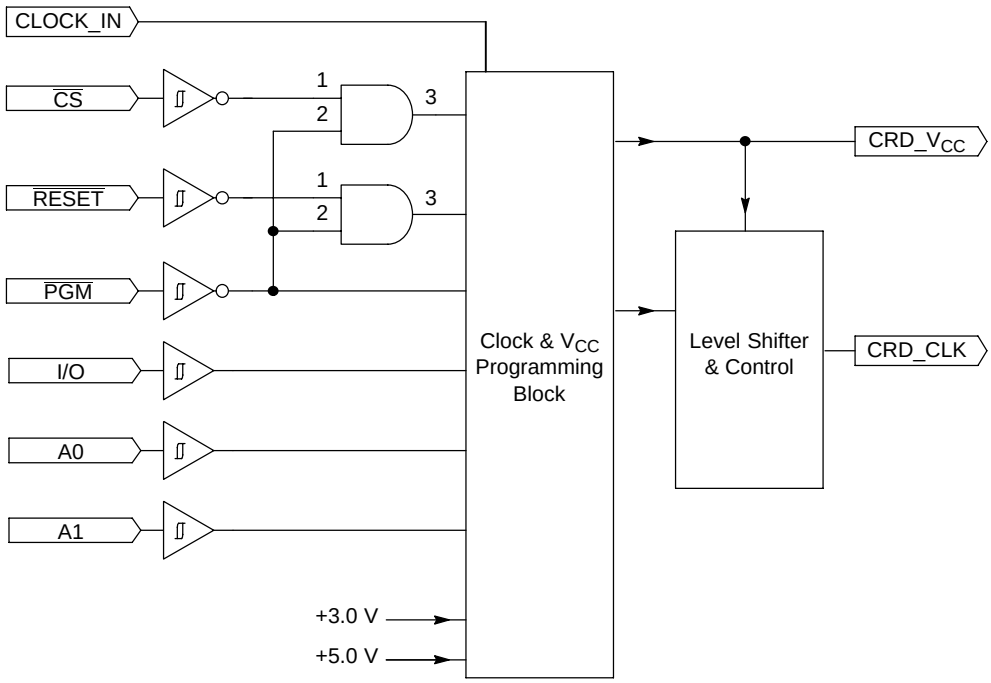
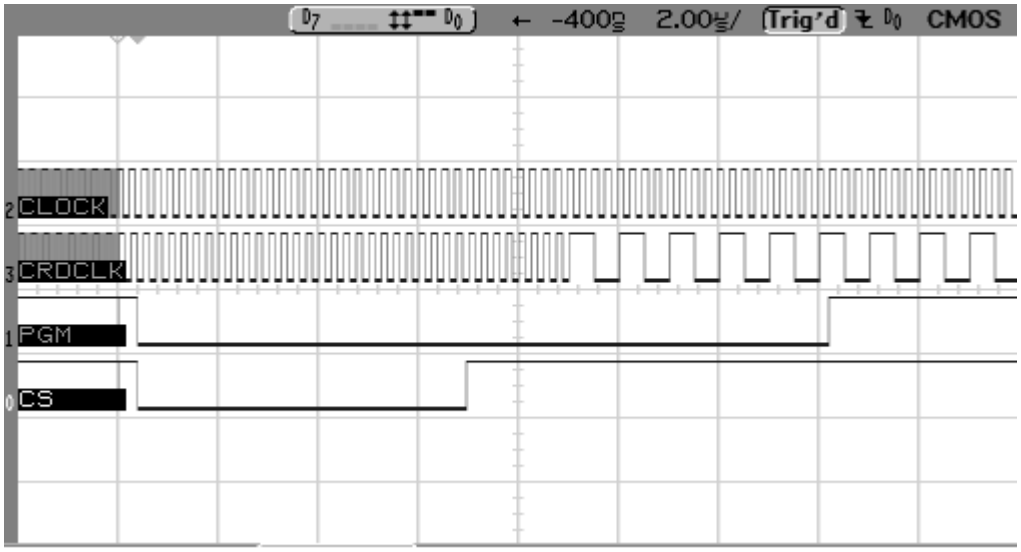


Figure 24. Simplified Frequency Divider and Programming Functions

In order to avoid any duty cycle out of the frequency smart card ISO7816−3 specification, the divider is synchronized by the last flip flop, thus yielding a constant 50% duty cycle, whatever be the divider ratio. Consequently, the output CRD_CLK frequency division can be delayed by eight CLOCK_IN pulses and the microcontroller software must take this delay into account prior to launch a new data transaction.



The example given by the oscillogram here above highlights the delay coming from the internal clock duty cycle resynchronization. In this example, the clock is internally divided by 2 prior to be applied to the CRD_CLK pin. Since the clock signal is asynchronous, it is up to the programmer to make sure the next card transaction is not activated before the CRD_CLK signal has been updated. Generally speaking, such a delay can be derived from the maximum clock frequency provided to the interface, keeping in mind the maximum delay is eight incoming clock pulses.

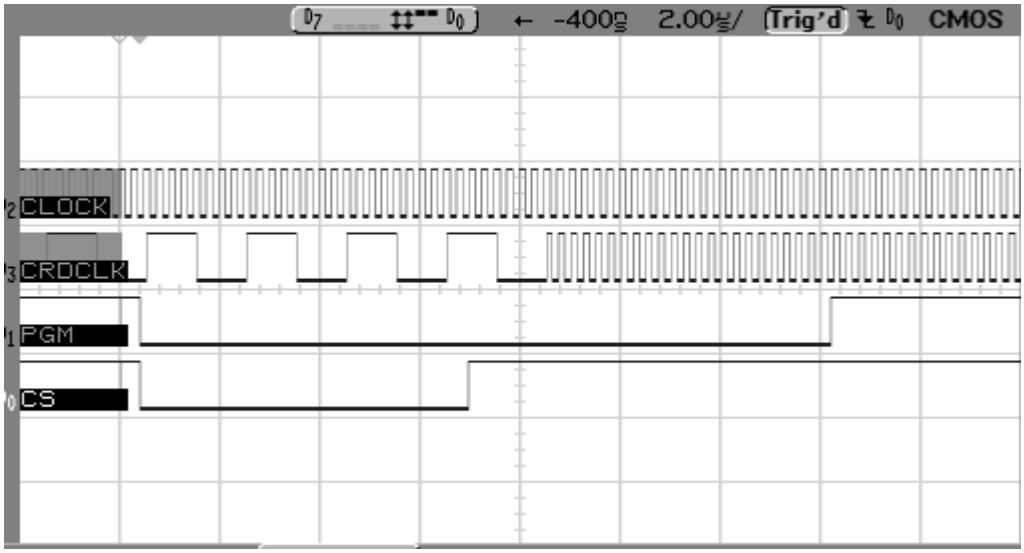


Figure 25. Clock Programming Examples

The clock can be re−programmed without halting the rest of the circuit, whatever be the new clock divider ratio. In particular, the CRD_VCC can be applied to the card while the clock is re−programmed.

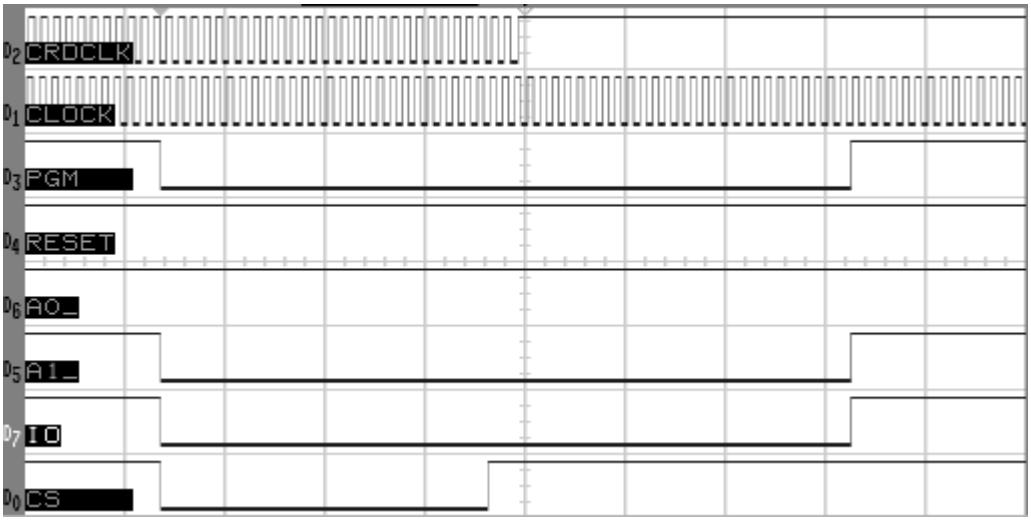


Figure 26. Command Stop Clock HIGH

The CRD_CLK signal is halted in the High logic state, following the Chip Select positive going transition. Logic Input conditions:

$\overline{\text{PGM}}$	= Low	A0	= Low
$\overline{\text{RESET}}$	= Low	A1	= Low
I/O	= Low	$\overline{\text{CS}}$	= Low pulsed

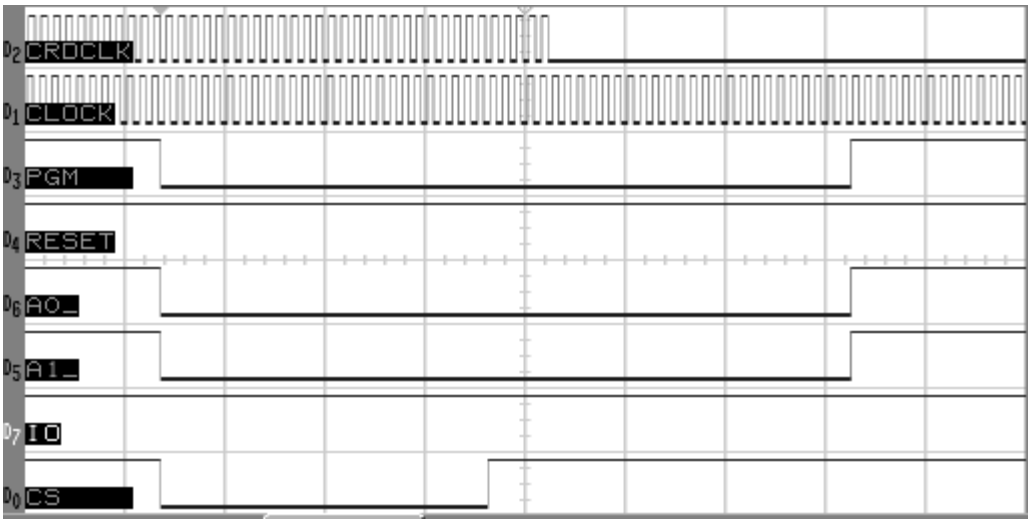


Figure 27. Command Stop Clock LOW

The CRD_CLK signal is halted in the Low logic state, following the Chip Select positive going transition. Logic Input conditions:

$\overline{\text{PGM}}$	= Low	A0	= Low
$\overline{\text{RESET}}$	= Low	A1	= Low
I/O	= High	$\overline{\text{CS}}$	= Low, pulsed

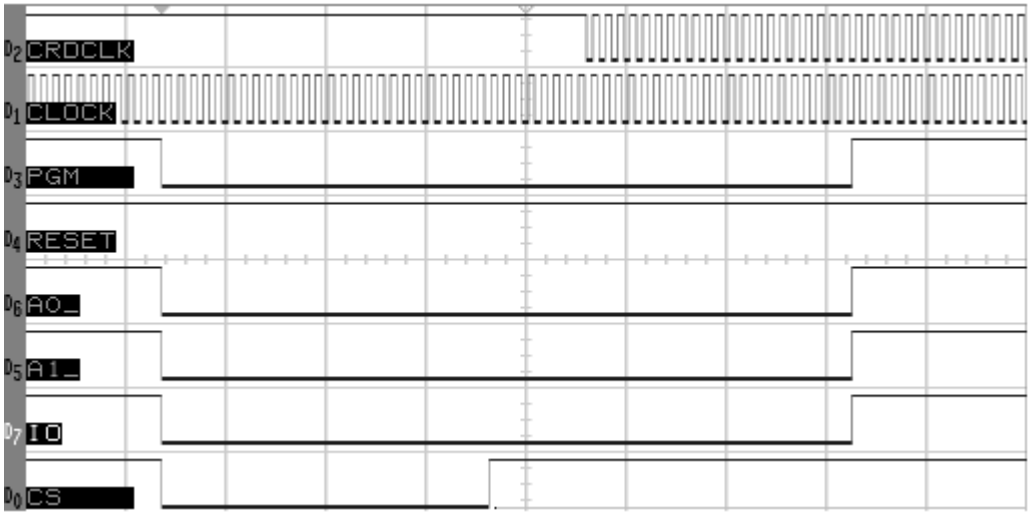


Figure 28. Command Resume Clock Normal Operation

The CRD_CLK signal is resumed in the normal operation, following the Chip Select positive going transition. The previous halted state is irrelevant and the clock signal is synchronized with the internal clock divider to avoid non CRD_CLK 50% duty cycle.

$\overline{PGM}$	= Low	A0	= Low
$\overline{RESET}$	= High	A1	= Low
I/O	= Low	$\overline{CS}$	= Low, pulsed

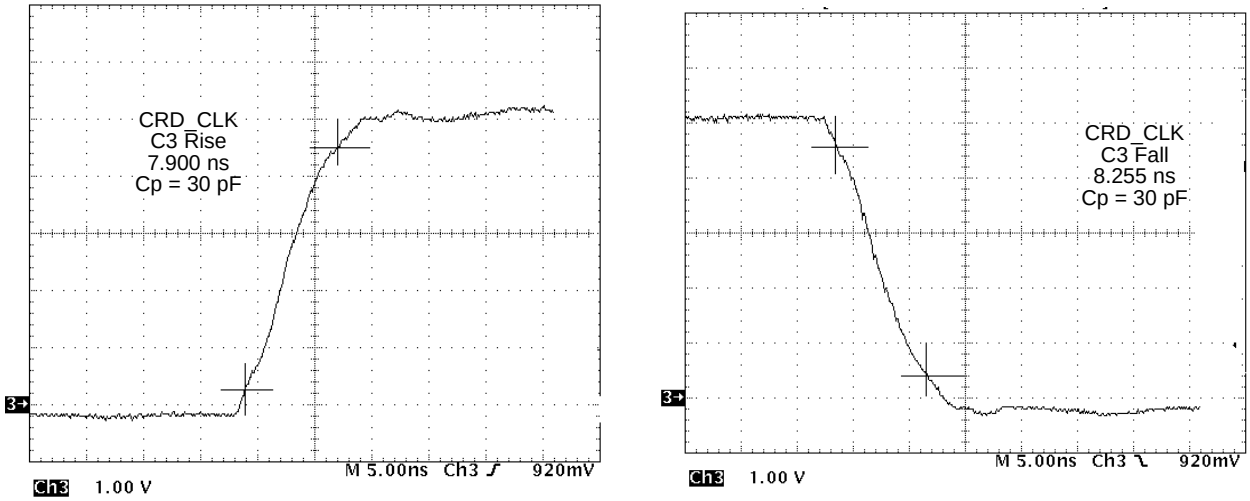


Figure 29. Card Clock Rise and Fall Time

Since the CRD_CLK signal can generate very fast transient (i.e. tr = 2.5 ns @ Cp = 10 pF), adapting the design to cope with the EMV noise specification might be necessary at final check out. Using an external RC network is a way to reduce the dv/dt, hence the EMI noise.

Typically, the external series resistor is 10 Ω, the total capacitance being 30 pF to 50 pF

Bidirectional Level Shifter

The NCN6000 carries out the voltage difference between the MPU and the Smart Card I/O signals. When the start sequence is completed, and if no failures have been detected, the device becomes essentially transparent for the data transferred on the I/O line. To fulfill the ISO7816−3 specification, both sides of the I/O line have built in pulsed circuitry to accelerate the signal rise transient. The I/O line is connected on both side of the interface by a NMOS switch which provide the level shifter and, due to its relative high internal impedance, protects the Smart Card in the event of data collision. Such a situation could occurs if either the MPU of the smart card forces a signal in the opposite logic level direction.

When the $\overline{CS}$ signal goes High, or if the MPU is running any of the programming functions, the built in register holds the previous state presents on the input I/O pin. This mechanism is useful to force the CRD_IO card pin in either a High or a Low pre−defined logic state. It is the responsibility of the programmer to set up the I/O line according to the system's activity

Device Q4 provides a low impedance to ground when the CRD_IO line is deactivated. This mechanism avoids noise presence on this line during any of the power operation.

When either side of this level shifter is forced to Low, the externally connected device will be forward biased by the DC current flowing through the pull up resistors as depicted in Figure 30. Since these two resistors will carry 350 μA max each under the worst case conditions, care must be observed to make sure the external device will be capable to handle this level of current. Note: the typical series impedance of the internal MOS device (Q3, Figure 30) is 400 Ω.

The oscillograms in Figure 31 give the worst case operation when the stray capacitance is 15 pF.

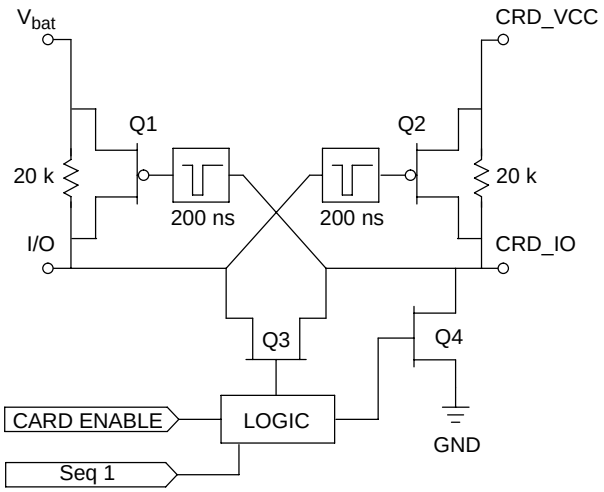


Figure 30. Basic Internal I/O Level Shifter

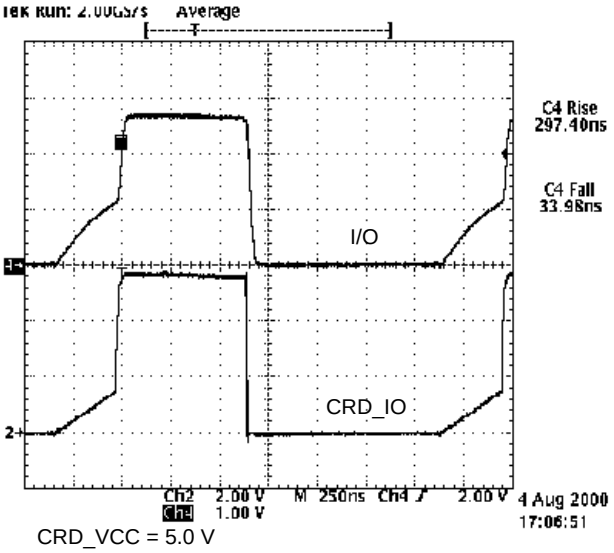
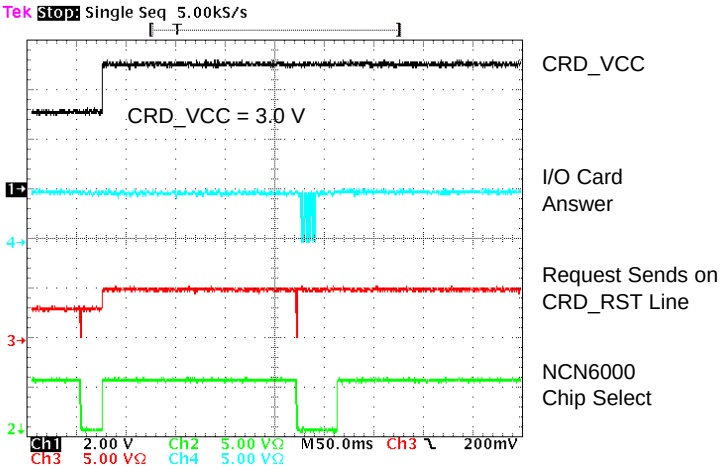


Figure 31. Typical CRD_IO Rise Time



Note: The I/O data depends solely upon the smart card ATR content, the NCN6000 being not involved in these data.

Figure 32. Typical I/O and RST Signals During an ATR Sequence.

Input Schmitt Triggers

All the Logic Input pins have built−in Schmitt trigger circuits to prevent the NCN6000 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 33.

The output signal is guaranteed to go High when the input voltage is above 0.70*Vbat, and will go Low when the input voltage is below 0.30*Vbat.

The CLOCK_IN pin has been design to provide a 40 MHz bandwidth clock receiver input, capable to drive the internal clock divider. This front end circuit yields a constant Duty Cycle signal, according to the ISO specification, to the external smart card, even when the NCN6000 division ratio is 1:1.

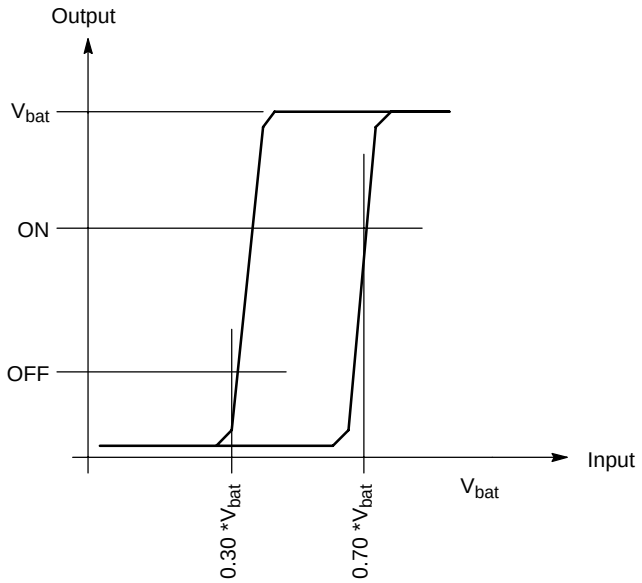


Figure 33. Typical Schmitt Trigger Characteristic

Interrupt Function

The NCN6000 flags the external microprocessor by pulling down the $\overline{INT}$ signal provided in pin 9. This signal is activated by one of the here below referenced operations.

Table 6. Interrupt Functions

	Pin Related	Clear Function	STATUS Pin 5
Card Insertion and Extraction	11	Positive Going Chip Select, or logical combination of Chip Select Low and PWR_ON Positive Going	High = Card Presents Low = No Card Inserted
DC−DC Converter Overloaded	15	Positive Going Chip Select, or logical combination of Chip Select Low and PWR_ON Positive Going	High = DC−DC Operates Normally Low = Output CRD_VCC Overloaded

Leaving the $\overline{INT}$ pin Low has no influence on the NCN6000 internal behavior. It is up to the engineering to decide when and how the interrupt will be cleared from this pin. As described before, this can be achieved by either providing a Chip Select positive transient, or by starting the DC−DC converter with the standard command PWR_ON = H and $\overline{CS}$ =L.

Security Features

In order to protect both the interface and the external smart card, the NCN6000 provides security features to prevent catastrophic failures as depicted here after.

Pin Current Limitation: In the case of a short circuit to ground, the current forced by the device is limited to 15 mA for any pins, except CRD_CLK pin. No feedback is provided to the external MPU.

DC−DC Operation: The internal circuit continuously senses the CRD_VCC voltage and, in the case of either over or undervoltage situation, update the STATUS register accordingly. This register can be read out by the MPU.

Battery Voltage: Both the Over and Undervoltage are detected by the NCN6000, a POWER_DOWN sequence and the STATUS register being updated accordingly. The external MPU can read the STATUS pin to take whatever is appropriate to cope with the situation.

ESD Protection

The NCN6000 includes silicon devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed across these pins, the built−in structures have been designed to handle either 2.0 kV, when related to the microcontroller side, or 8.0 kV when connected with the external contacts. Practically, the CRD_RST, CRD_CLK, CRD_IO and CRD_DET pins can sustain 8 kV, the digital pins being capable to sustain 2 kV. The CRD_VCC pin has the same 8 kV ESD protection, but can source up to 55 mA continuously, the absolute maximum current being 100 mA.

To save as much battery current as possible when no card is inserted, one should use a Normally Open Card Detection switch connected pin 11. Since the internal card detection circuit source 10 μA (typical) to bias the switch, using a Normally Open avoid this direct sink to ground from the battery.

Parallel Operation

When two or more NCN6000 operate in parallel on a common digital bus, the Chip Select pin allows the selection of one chip from the bank of the paralleled devices. Of course, the external MPU shall provide one unique $\overline{CS}$ line for each of the NCN6000 considered interfaces. When a given interface is selected by $\overline{CS}$ = L, all the logic inputs becomes active, the chip can be programmed or/and the external card can be accessed. When $\overline{CS}$ = H, all the input logic pins are in the high impedance state, thus leaving the bus available for other purpose. On the other hand, when $\overline{CS}$ = H, the CRD_IO and CRD_RST hold the previous I/O and $\overline{RESET}$ logic state, the CRD_CLK being either active or stopped, according to the programmed state forced by the MPU.

Since there is one single I/O line to communicate with the external microcontroller, one should provide a software routine to save the code when data exchanged are performed between the two cards. Generally speaking, the internal microcontroller RAM can be used to support such a transaction.

The CRD_VCC voltage and CRD_CLK signal of each NCN6000 can be operated simultaneously, these two pins being activated even when the related chip select is High. As depicted in Figure 14, the DC−DC converter is not deactivated when PWR_ON goes to Low when $\overline{CS}$ = High.

Minimum Power Consumption

To achieve a minimum current consumption, the interface shall be programmed as follow:

1. Turn off the DC−DC converter : this will disconnect the smart card if still inserted in the socket), reducing the power supply to the minimum needed to control the interface.
2. Force the input signals to a logic High to avoid current flowing through the pull up resistors. This applies to the here below table:

$\overline{INT}$	Pin 9
$\overline{CS}$	Pin 6
STATUS	Pin 5
I/O	Pin 8
CRD_IO	Pin 14

To save as much battery current as possible when no card is inserted, one should use a Normally Open Card Detection switch connected pin 11 to ground. Since the internal card detection circuit source is 10 μA (typical), using such a NO switch saves the direct sink to ground current from the battery to ground.

During this mode of operation, the only active sub functions are the card detection and the battery monitoring. The activity resume immediately after either a card insertion, or a $\overline{CS}$ = Low signal applied to pin 6.

Printed Circuit Board Layout

Since the NCN6000 carries high speed currents together with high frequency clock, the printed circuit board must be carefully designed to avoid the risk of uncontrolled operation of the interface.

A typical single−sided PCB layout is provided in Figure 34 highlighting the ground technique.

The card socket uses a low cost ISO only version, all the parts being located on the Component side. Connector J3 makes reference to the microcontroller used by the final application. Of course, the connector is not necessary and standard copper tracks might be used to connect the MPU to the NCN6000 interface chip.

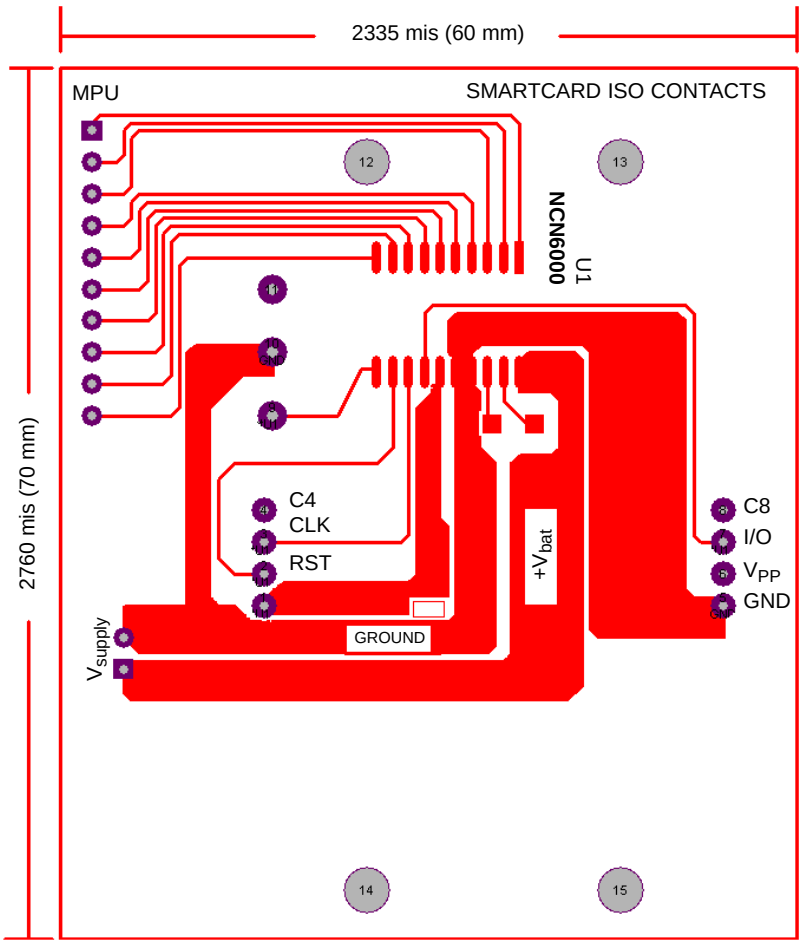


Figure 34. Typical Single Sided Printed Circuit Board Layout

Application Note

A partial schematic diagram of the demo board designed to support the NCN6000 applications is depicted in Figure 35. This schematic diagram highlights the interface between the microcontroller and the Smart Card, leaving aside the peripherals used to control the MPU.

Conclusion

From a practical stand point, the CRD_VCC output capacitor has been split into two 6.8 μF/10 V/X7R, one being located as close as possible across pins 13 and 17 of the NCN6000, the second one being located close by the smart card physical connector. On the other hand, care has been observed to minimize the cross coupling between the clock signals (both Input and CRD_CLK) and the other signals presents on the board.

The microcontroller holds the software necessary to program the NCN6000, together with the code handling the T0 operation. Provisions are made to provide a communication link with an external computer by using the RS232 standard port.

Due to the Chip Select signal, several NCN6000 can share a common data bus as depicted in Figure 36. In this example, two interfaces are connected to a single MPU, the $\overline{CS}$ pins being controlled by two different signals.

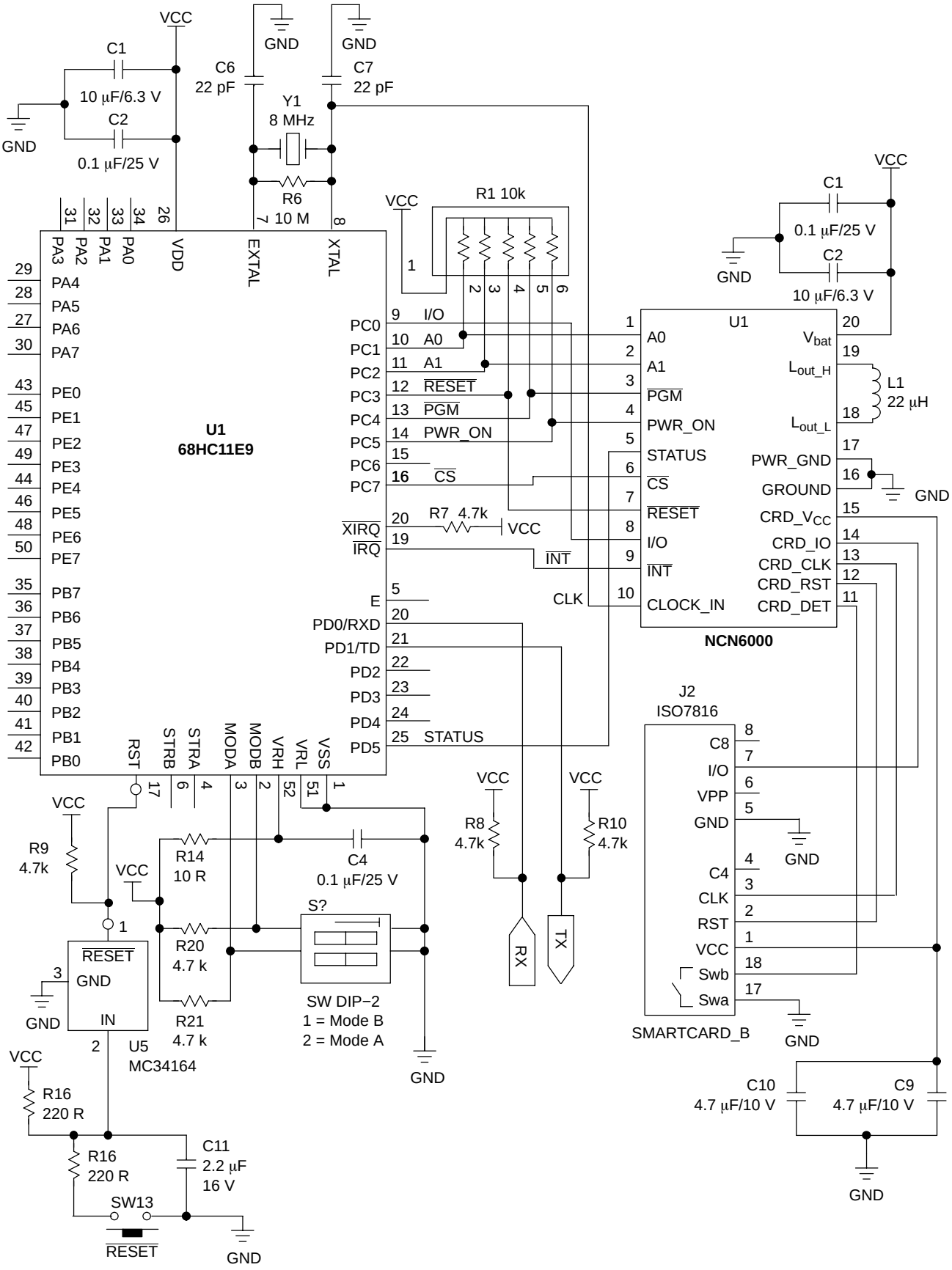


Figure 35. NCN6000 Single Interface Demo Board

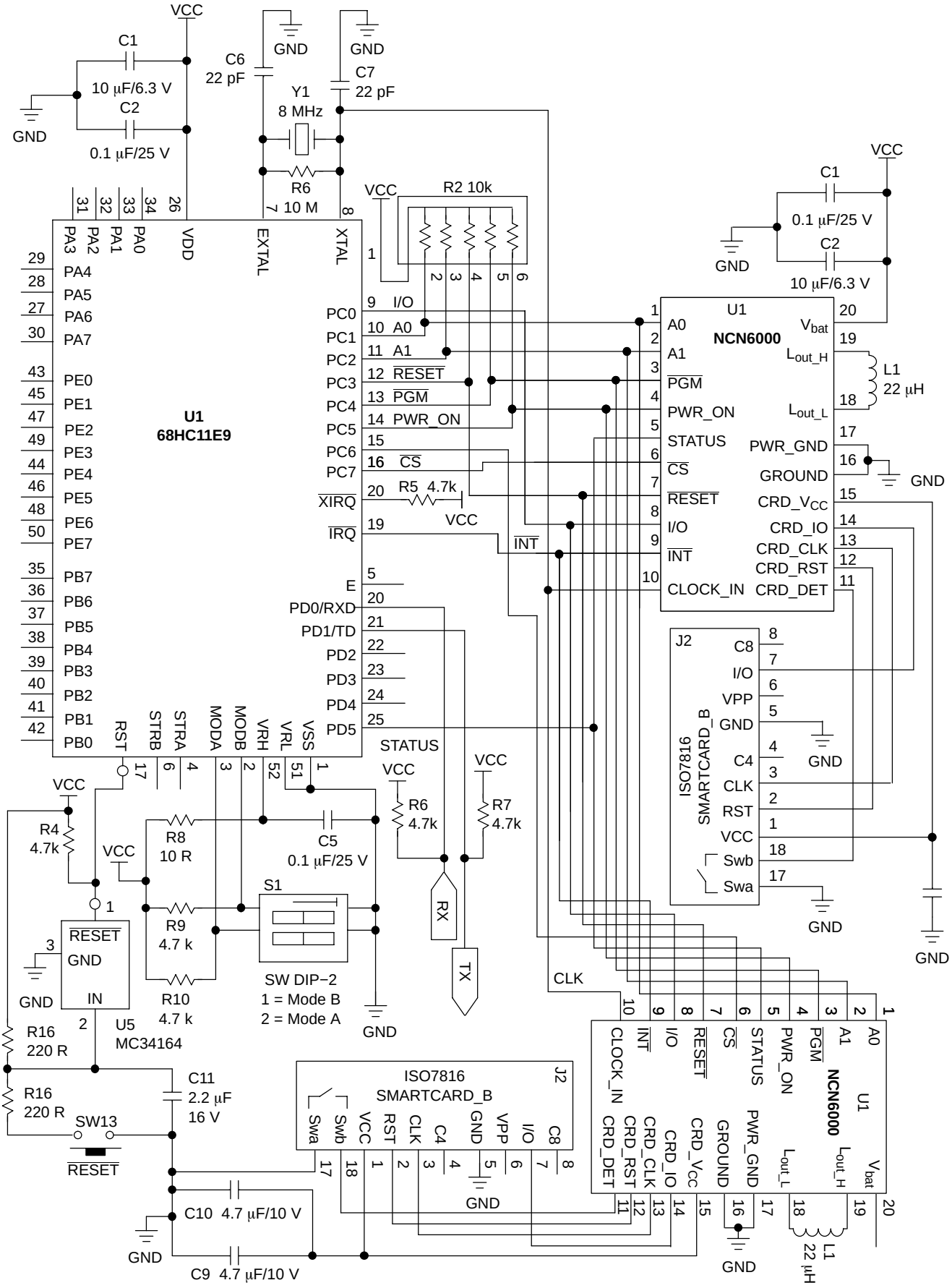


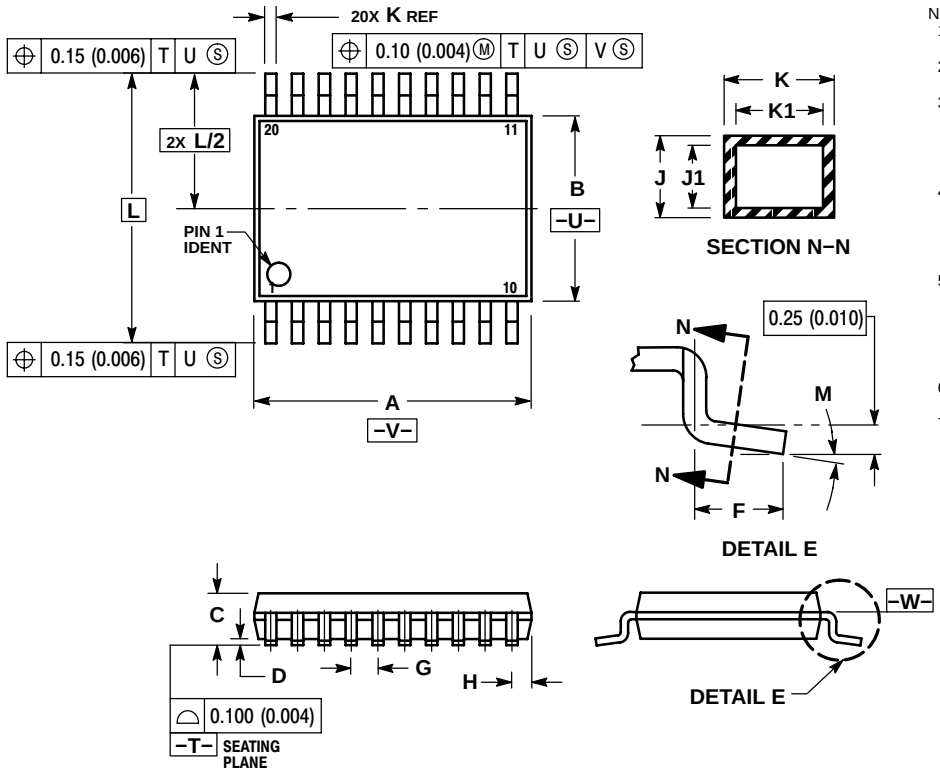
Figure 36. NCN6000 Single Interface Demo Board

Summary

Figure Index

PACKAGE DIMENSIONS

TSSOP−20
DTB SUFFIX
CASE 948E−02
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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