19-4770; Rev 3; 8/10

±15kV ESD-Protected, Single/Dual/Octal, CMOS Switch Debouncers

General Description

The MAX6816/MAX6817/MAX6818 are single, dual, and octal switch debouncers that provide clean interfacing of mechanical switches to digital systems. They accept one or more bouncing inputs from a mechanical switch and produce a clean digital output after a short, preset qualification delay. Both the switch opening bounce and the switch closing bounce are removed. Robust switch inputs handle ±25V levels and are ±15kV ESD-protected for use in harsh industrial environments. They feature single-supply operation from +2.7V to +5.5V. Undervoltage lockout circuitry ensures the output is in the correct state upon power-up.

The single MAX6816 and dual MAX6817 are offered in SOT packages and require no external components. Their low supply current makes them ideal for use in portable equipment.

The MAX6818 octal switch debouncer is designed for data-bus interfacing. The MAX6818 monitors switches and provides a switch change-of-state output ($\overline{CH}$), simplifying microprocessor (µP) polling and interrupts. Additionally, the MAX6818 has three-state outputs controlled by an enable ($\overline{EN}$) pin, and is pin-compatible with the LS573 octal latch (except for the $\overline{CH}$ pin), allowing easy interfacing to a digital data bus.

Applications

µP Switch Interfacing

Industrial Instruments

PC-Based Instruments

Portable Instruments

Automotive Applications

Membrane Keypads

Features

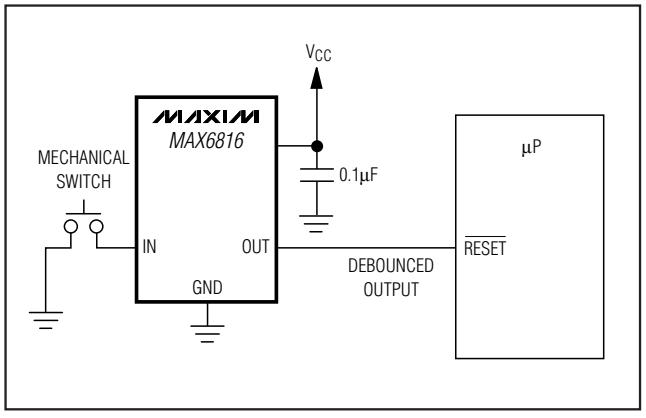
- **Robust Inputs can Exceed Power Supplies up to ±25V**
- **ESD Protection for Input Pins**
  ±15kV—Human Body Model
  ±8kV—IEC 1000-4-2, Contact Discharge
  ±15kV—IEC 1000-4-2, Air-Gap Discharge
- **Small SOT Packages (4 and 6 pins)**
- **Single-Supply Operation from +2.7V to +5.5V**
- **Single (MAX6816), Dual (MAX6817), and Octal (MAX6818) Versions Available**
- **No External Components Required**
- **6µA Supply Current**
- **Three-State Outputs for Directly Interfacing Switches to µP Data Bus (MAX6818)**
- **Switch Change-of-State Output Simplifies Polling and Interrupts (MAX6818)**
- **Pin-Compatible with 'LS573 (MAX6818)**

Ordering Information

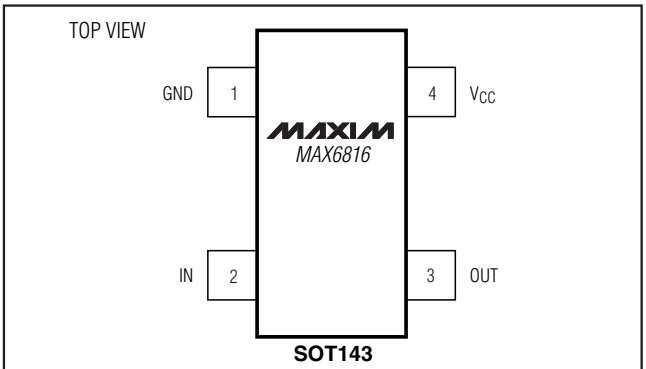
PART	TEMP RANGE	PIN-PACKAGE	SOT TOP MARK
MAX6816EUS-T	-40°C to +125°C	4 SOT143	KABA
MAX6817EUT-T	-40°C to +125°C	6 SOT23-6	AAAU
MAX6818EAP	-40°C to +125°C	20 SSOP	—

Note: *There is a minimum order increment of 2500 pieces for SOT packages.*
Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

Typical Operating Circuit



Pin Configurations



SOT143

Pin Configurations continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

±15kV ESD-Protected, Single/Dual/Octal, CMOS Switch Debouncers

ABSOLUTE MAXIMUM RATINGS

Voltage (with respect to GND)
- V_{CC} .....-0.3V to +6V
- IN_ (Switch Inputs) .....-30V to +30V
- $\overline{EN}$.....-0.3V to +6V
- OUT_, $\overline{CH}$ .....-0.3V to (V_{CC} + 0.3V)

OUT Short-Circuit Duration
(One or Two Outputs to GND).....Continuous
Continuous Power Dissipation (T_A = +70°C)
- 4-Pin SOT143 (derate 4.0mW/°C above +70°C).....320mW
- 6-Pin SOT23 (derate 8.7mW/°C above +70°C).....691mW
- 20-Pin SSOP (derate 8.0mW/°C above +70°C) 640mW

Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
- Lead(Pb)-free.....+260°C
- Containing lead.....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 1)

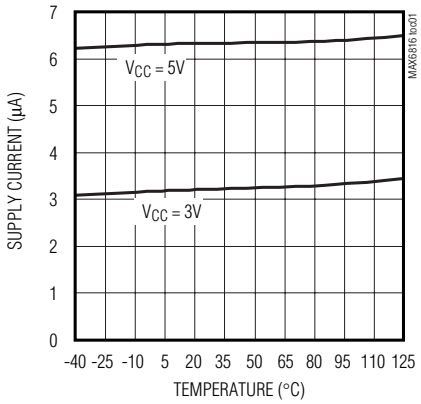
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		2.7		5.5	V
Supply Current	I_{CC}	V_{CC} = 5V, I_{OUT} = 0A, IN_ = V_{CC}		6	20	µA
Debounce Duration	t_{DP}	MAX6818	20	40	60	ms
		MAX6816/MAX6817	20	50	80	
Input Threshold	V_{IL}				0.8	V
	V_{IH}	V_{CC} = 5V	2.4			V
		V_{CC} = 2.7V	2.0			
Input Hysteresis				300		mV
Input Pullup Resistance			32	63	100	kΩ
IN Input Current	I_{IN}	V_{IN} = ±15V			±1	mA
Input Voltage Range	V_{IN}		-25		+25	V
Undervoltage-Lockout Threshold				1.9	2.6	V
OUT_, $\overline{CH}$ Output Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
	V_{OH}	I_{SOURCE} = 0.4mA	V_{CC} - 1.0			
$\overline{EN}$ Pulse Width	t_{EN}		200			ns
$\overline{EN}$ Threshold		V_{CC} = 5V	0.8	1.7	2.4	V
		V_{CC} = 2.7V	0.8	1.1	2.0	
$\overline{EN}$ Input Current	I_{IL}				±1	µA
$\overline{EN}$ Low to Out Active Propagation Delay	t_{PE}	R_L = 10kΩ, C_L = 100pF			100	ns
$\overline{EN}$ High to Out Three-State Propagation Delay	t_{PD}	R_L = 1kΩ, C_L = 15pF			100	ns
$\overline{EN}$ Low to $\overline{CH}$ Out High Propagation Delay	t_{PC}	R_L = 10kΩ, C_L = 50pF			100	ns
OUT_ Three-State Leakage Current		V_{OUT} = 0V or V_{CC}			±10	µA
ESD CHARACTERISTICS						
ESD Protection		IN_ — IEC 1000-4-2 Air Discharge		±15		kV
		IN_ — IEC 1000-4-2 Contact Discharge		±8		
		IN_ — Human Body Model		±15		

Note 1: MAX6816 and MAX6817 production testing is done at T_A = +25°C; overtemperature limits are guaranteed by design.

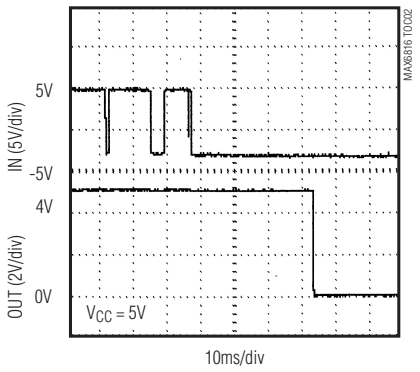
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

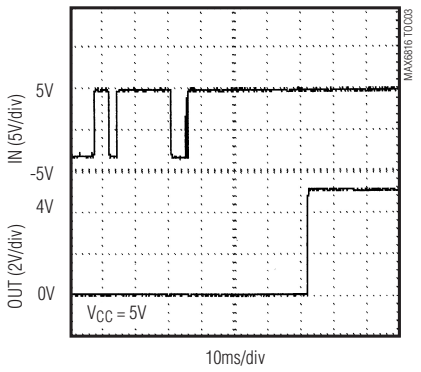
SUPPLY CURRENT vs. TEMPERATURE



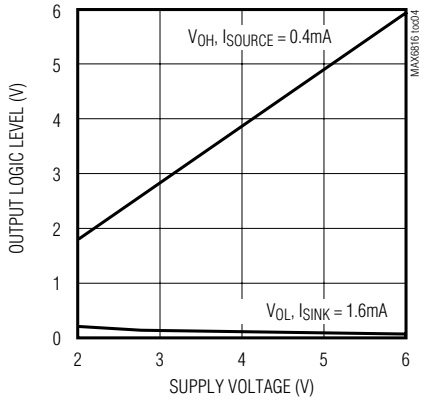
DEBOUNCE OF CLOSING SWITCH



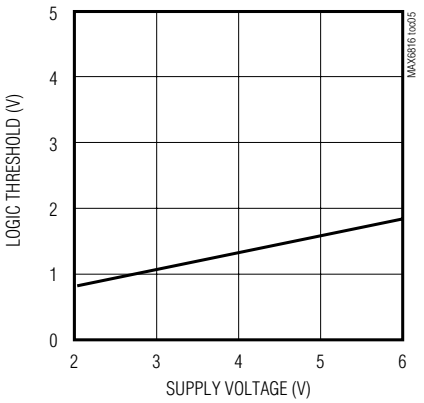
DEBOUNCE OF OPENING SWITCH



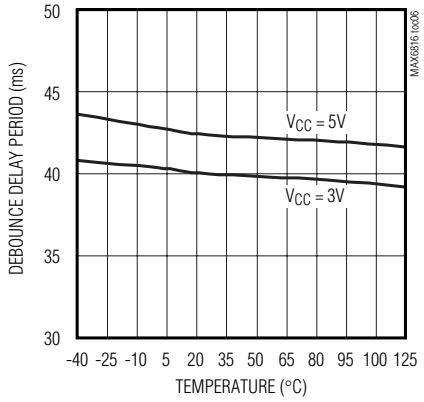
OUTPUT LOGIC LEVEL vs. SUPPLY VOLTAGE



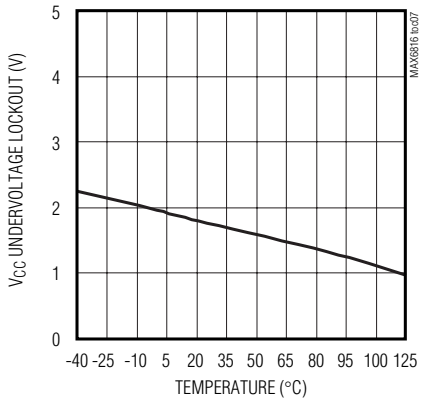
MAX6818 $\overline{EN}$ INPUT LOGIC THRESHOLD vs. SUPPLY VOLTAGE



DEBOUNCE DELAY PERIOD vs. TEMPERATURE



V_{CC} UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



±15kV ESD-Protected, Single/Dual/Octal, CMOS Switch Debouncers

Pin Description

PIN			NAME	FUNCTION
MAX6816	MAX6817	MAX6818		
1	2	10	GND	Ground
2	—	—	IN	Switch Input
—	1, 3	—	IN1, IN2	Switch Inputs
—	—	2–9	IN1–IN8	Switch Inputs
3	—	—	OUT	CMOS Debounced Output
—	4, 6	—	OUT2, OUT1	CMOS Debounced Outputs
—	—	12–19	OUT8–OUT1	CMOS Debounced Outputs
4	5	20	V_{CC}	+2.7V to +5.5V Supply Voltage
—	—	1	$\overline{EN}$	Active-Low, Three-State Enable Input for outputs. Resets $\overline{CH}$. Tie to GND to “always enable” outputs.
—	—	11	$\overline{CH}$	Change-of-State Output. Goes low on switch input change of state. Resets on $\overline{EN}$. Leave unconnected if not used.

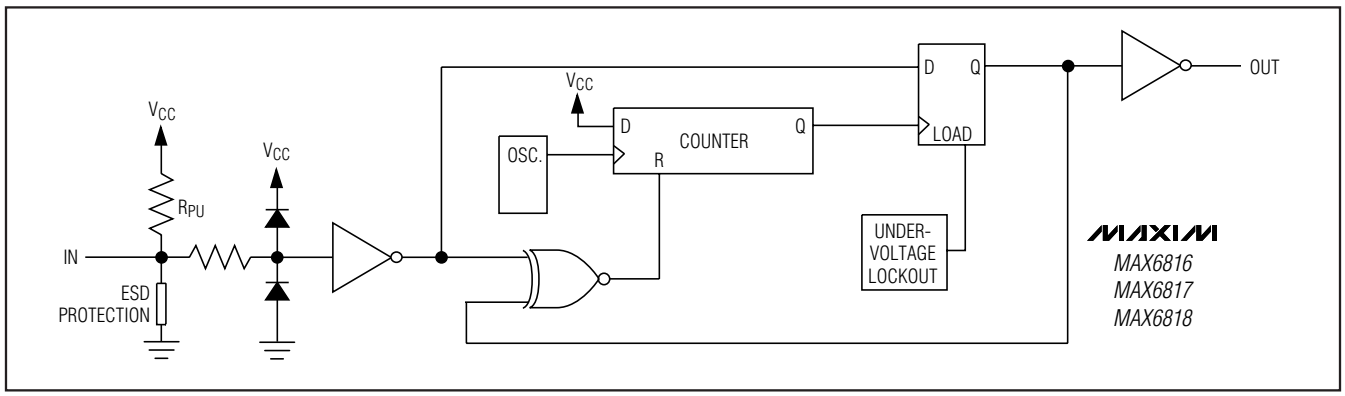


Figure 1. Block Diagram

Detailed Description

Theory of Operation

The MAX6816/MAX6817/MAX6818 are designed to eliminate the extraneous level changes that result from interfacing with mechanical switches (switch bounce). Virtually all mechanical switches bounce upon opening or closing. These switch debouncers remove bounce when a switch opens or closes by requiring that sequentially clocked inputs remain in the same state for a number of sampling periods. The output does not change until the input is stable for a duration of 40ms.

The circuit block diagram (Figure 1) shows the functional blocks consisting of an on-chip oscillator, counter, exclusive-NOR gate, and D flip-flop. When the input does not equal the output, the XNOR gate issues a counter reset. When the switch input state is stable for the full qualification period, the counter clocks the flip-flop, updating the output. Figure 2 shows the typical opening and closing switch debounce operation. On the MAX6818, the change output ($\overline{CH}$) is updated simultaneously with the switch outputs.

Undervoltage Lockout

The undervoltage lockout circuitry ensures that the outputs are at the correct state on power-up. While the supply voltage is below the undervoltage threshold (typically 1.9V), the debounce circuitry remains transparent. Switch states are present at the logic outputs with no debouce delay.

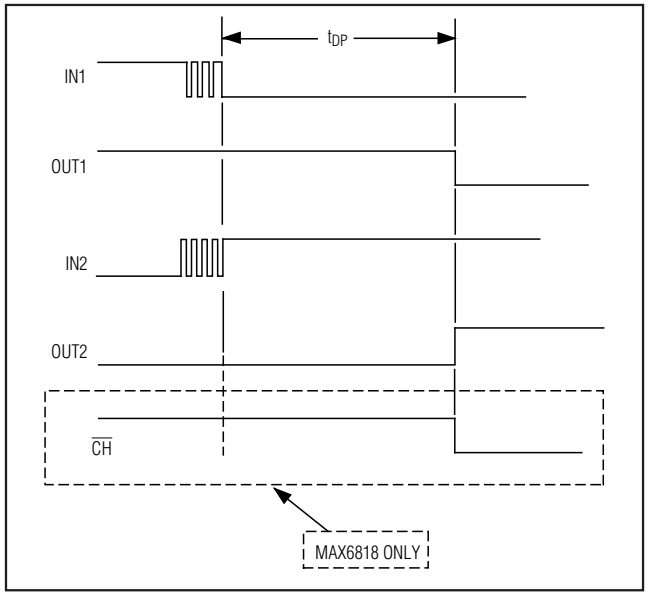


Figure 2. Input Characteristics

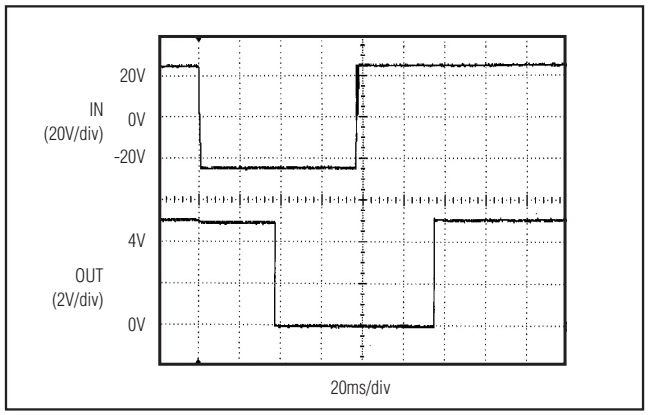


Figure 3. Switch Input ±25V Fault Tolerance

Robust Switch Inputs

The switch inputs on the MAX6816/MAX6817/MAX6818 have overvoltage clamping diodes to protect against damaging fault conditions. Switch input voltages can safely swing ±25V to ground (Figure 3). Proprietary ESD-protection structures protect against high ESD encountered in harsh industrial environments, membrane keypads, and portable applications. They are designed to withstand ±15kV per the IEC 1000-4-2 Air Gap Discharge Test and ±8kV per the IEC 1000-4-2 Contact Discharge Test.

Since there are 63kΩ (typical) pullup resistors connected to each input, driving an input to -25V will draw approximately 0.5mA (up to 4mA for eight inputs) from the V_{CC} supply. Driving an input to +25V will cause approximately 0.32mA of current (up to 2.6mA for eight inputs) to flow back into the V_{CC} supply. If the total system V_{CC} supply current is less than the current flowing back into the V_{CC} supply, V_{CC} will rise above normal levels. In some low-current systems, a zener diode on V_{CC} may be required.

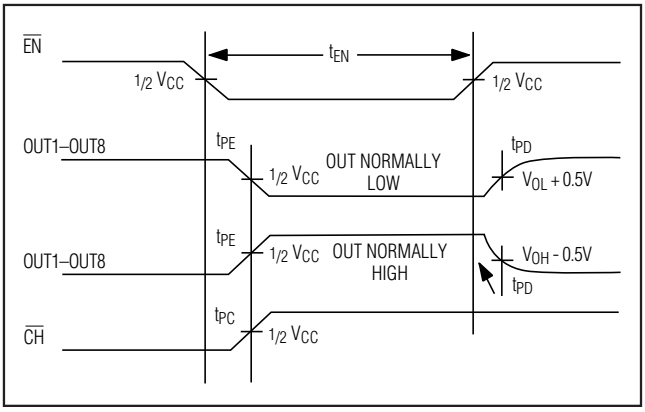


Figure 4. MAX6818 µP-Interface Timing Diagram

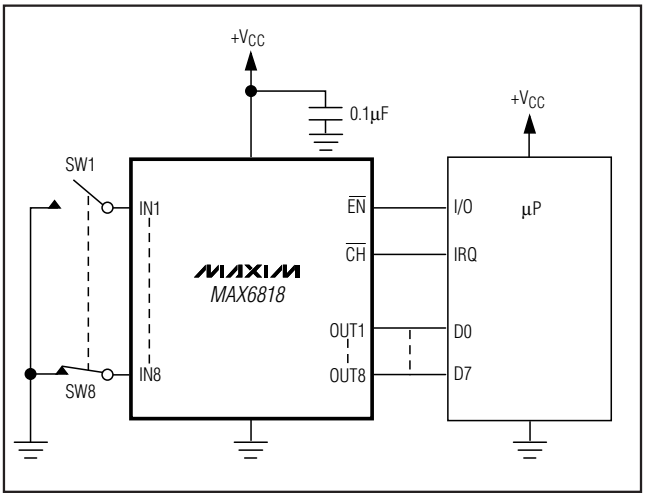


Figure 5. MAX6818 Typical µP Interfacing Circuit

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX6816/MAX6817/MAX6818 have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect against ESD of ±15kV at the switch inputs without

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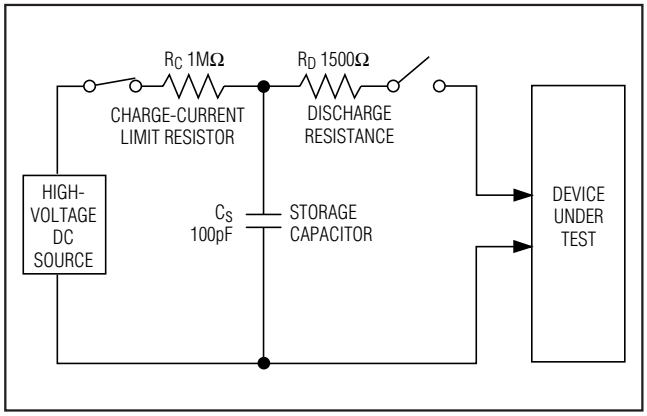


Figure 6a. Human Body ESD Test Model

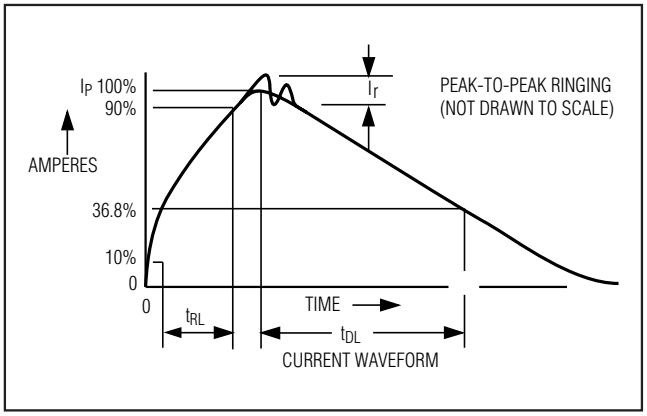


Figure 6b. Human Body Current Waveform

damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX6816/MAX6817/MAX6818 keep working without latchup, whereas other solutions can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways; these products are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±8kV using the Contact-Discharge method specified in IEC 1000-4-2
3) ±15kV using IEC 1000-4-2's Air-Gap method.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

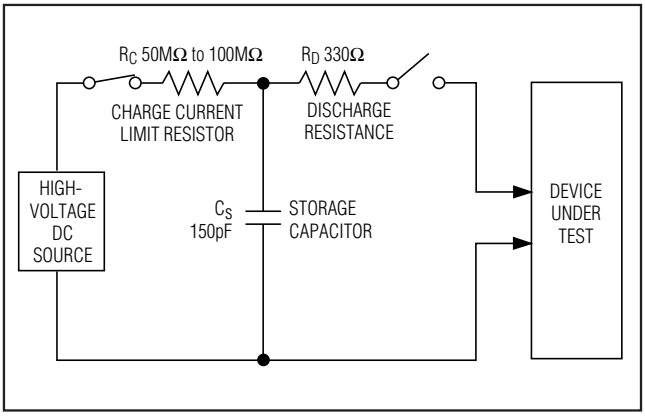


Figure 7a. IEC 1000-4-2 ESD Test Model

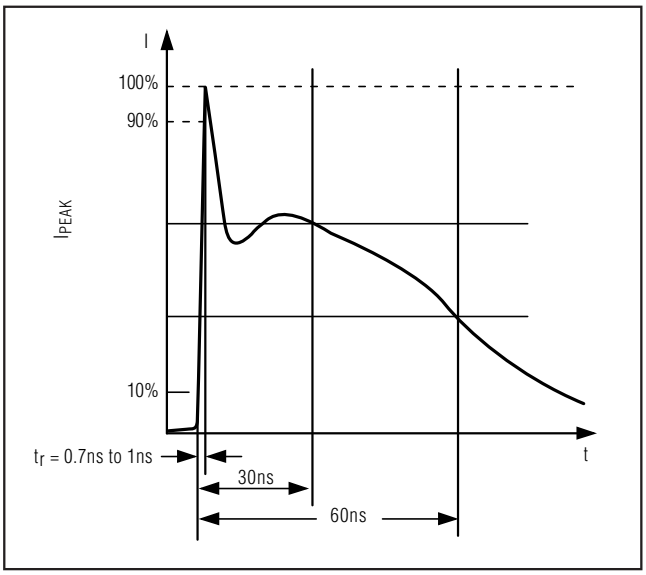


Figure 7b. IEC 1000-4-2 ESD Generator Current Waveform

Human Body Model

Figure 6a shows the Human Body Model and Figure 6b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX6816/MAX6817/MAX6818 help you design equipment that

meets Level 4 (the highest level) of IEC 1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7a shows the IEC 1000-4-2 model and Figure 7b shows the current waveform for the 8kV, IEC 1000-4-2, Level 4, ESD Contact-Discharge test.

The Air-Gap test involves approaching the device with a charged probe. The Contact-Discharge method connects the probe to the device before the probe is energized.

Machine Model

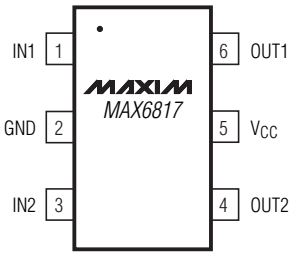
The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing.

MAX6818 µP Interfacing

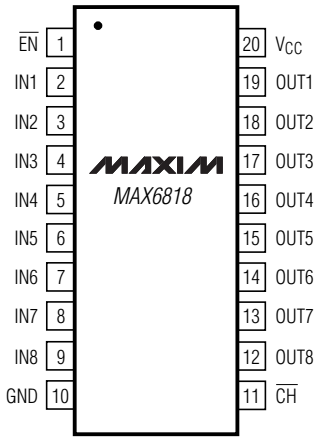
The MAX6818 has an output enable ($\overline{EN}$) input that allows switch outputs to be three-stated on the µP data bus until polled by the µP. Also, state changes at the switch inputs are detected, and an output ($\overline{CH}$) goes low after the debounce period to signal the µP. Figure 4 shows the timing diagram for enabling outputs and reading data. If the output enable is not used, tie $\overline{EN}$ to GND to "always enable" the switch outputs. If $\overline{EN}$ is low, $\overline{CH}$ is always high. If a change of state is not required, leave $\overline{CH}$ unconnected.

Pin Configurations (continued)

TOP VIEW



SOT23-6



SSOP

Chip Information

SUBSTRATE CONNECTED TO GND
PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
4 SOT143	U4-1	21-0052	90-0183
6 SOT23	U6-4	21-0058	90-0175
20 SSOP	A20-1	21-0056	90-0094

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/98	Initial release	—
3	8/10	Updated *Ordering Information*, *Electrical Characteristics*, *Typical Operating Characteristics*, and the *Undervoltage Lockout* section.	1–4, 7