Tsi310™ 133-MHz PCI-X Bridge Product Brief

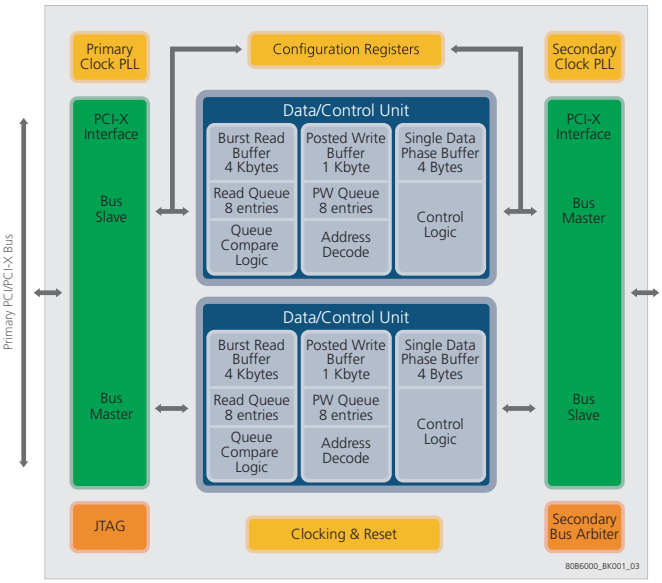
Device Overview

The IDT Tsi310 is a 64-bit PCI-X bus bridge that operates at speeds up to 133 MHz, and supports transfer rates up to 1 GBps. The PCI-X protocol is backward compatible with the PCI 2.2 bus standard ensuring that legacy PCI-based systems are portable to the faster PCI-X environment.

The Tsi310 connects two electrically separate PCI-X bus domains, allowing concurrent operations on both buses. This results in optimal use of the buses in various system configurations, and enables hierarchical expansion of I/O bus structures. The device also supports configurations of PCI or PCI-X mode on either bus, and in any combination.

In addition, the Tsi310 provides extensive buffering and prefetching mechanisms for efficient data transfer between two buses, facilitating multi-threaded operation and high system throughput.

Block Diagram



PCI-X Interfaces

The Tsi310 has two identical PCI-X Interfaces that each handle PCI and PCI-X transactions for its respective bus, and, depending on the type of transaction, can act as either a bus master or a bus slave. These interfaces transfer data and control information flowing to and from the blocks shown in the figure.

The Tsi310 uses the 3.3V signaling environment. It employs two phase-locked loops (PLLs), one for the primary clock domain and one for the secondary clock domain. The PLL for each domain is used when the bus is operating in PCI-X mode. In PCI mode, the PLL is bypassed to allow full frequency range as required by the bus architecture. The two bus clocks may be run synchronously or asynchronously, and a spread-spectrum clock input is supported for either or both interfaces.

Memory Buffer Architecture

The Tsi310 memory buffer architecture has the following features (see Data/Control unit in the Block Diagram):

- Two 4-Kbyte burst read buffers that support up to eight concurrent, upstream and downstream transactions
- Two 1-Kbyte posted write buffers that support up to eight concurrent, upstream and downstream transactions
- Two 4-Byte single data phase buffers that support transaction forwarding in either direction

Transaction Forwarding

The Tsi310 includes one data/control unit for downstream transactions and one for upstream transactions. Each of these identical units contains separate buffers for burst read, posted write, and single data phase operations. Also included in these blocks are write queues, queue compare logic, address decoding upstream for forwarding, control logic, and other control functions. The clocking and reset control unit manages these common device functions.

The device has I/O and Memory Base Address registers and Prefetchable Memory Base Address registers for downstream forwarding, as well as inverse decoding for upstream forwarding, VGA-compatible addressing, and palette snooping for upstream transactions. The Tsi310 uses a flat addressing model and supports 64-bit addressing and dual address cycles.

The Tsi310 responds as a medium-speed device on both PCI-X Interfaces, and supports fast, back-to-back transactions as a bus slave.

PCI Bus Arbitration

The Tsi310 uses an arbiter for the secondary bus, which can be disabled if an external arbiter is employed. When enabled, bus arbitration is provided for the Tsi310 and up to six external masters. Each bus master can be assigned high or low priority, or be masked off.

Opaque Addressing (Optional)

The Tsi310 has an optional feature that can define an opaque (undecoded) memory address region to facilitate applications with embedded processors.

Features

- Industry-standard 64-bit, 133-MHz PCI-X bridge chip
- Full PCI 2.2 backward compatibility
- Allows concurrent primary and secondary bus operation
- Supports configuration of PCI or PCI-X mode on either bus in any combination
- Extensive built-in buffering and prefetching mechanisms to enable efficient data transfer between buses
- Complies with the *PCI-X Addendum (Rev. 2.0a) and the PCI Local Bus Specification (Rev. 2.2)*
- 304-pin, 31-mm HPBGA package
- 3.3V I/Os

Optional Features

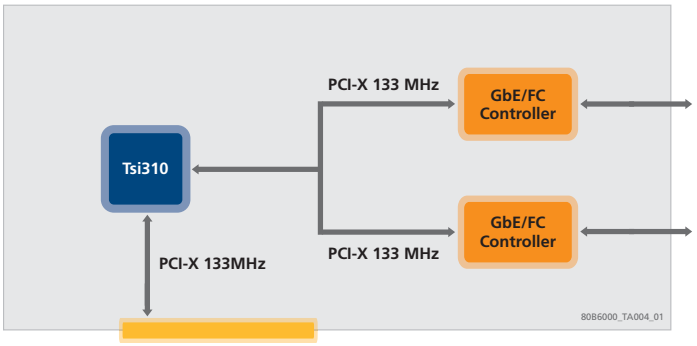
- Support for secondary side PCI-X device privatization
- Ability to define an opaque (undecoded) memory address region to facilitate applications with embedded processors
- Definable base address register for use by embedded subsystems on the secondary bus
- Access to configuration register space from the secondary bus

Benefits

- Eases the migration of system designs from PCI to the faster, more robust, PCI-X protocol
- Simplifies system design by offering a multitude of highly configurable features
- Increases system performance by supporting concurrent, upstream and downstream transactions

Typical Applications

- Server RAID controllers
- External RAID systems
- Fibre Channel host bus adapters
- Network interface cards
- Embedded computing



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