CYV15G0101EQ

Multi Rate Video Cable Equalizer

Features

- Multi rate adaptive equalization
- Operates from 143 to 1485 Mbps serial data rate
- SMPTE 292M, SMPTE 344M, and SMPTE 259M compliant
- Supports DVB-ASI at 270 Mbps
- Cable length indicator for HD-SDI and SD-SDI data rates
- Maximum cable length adjustment for HD-SDI and SD-SDI data rates
- Carrier detect and mute functionality for HD-SDI and SD-SDI data rates
- Equalizer bypass mode
- Seamless connection with HOTLink II™ family
- Equalizes up to 350m of Canare L-5CFB and Belden 1694A coaxial cable at 270 Mbps
- Typically equalizes up to 200m of Canare L-5CFB and Belden 1694A coaxial cable at 1.485 Gbps
- Low power: 160 mW at 3.3V
- Single 3.3V supply
- 16-pin SOIC
- 0.18 μm CMOS technology
- Pb-free and RoHS compliant
- Uses Cypress CLEANLink™ technology
- Pin compatible to existing equalizer devices

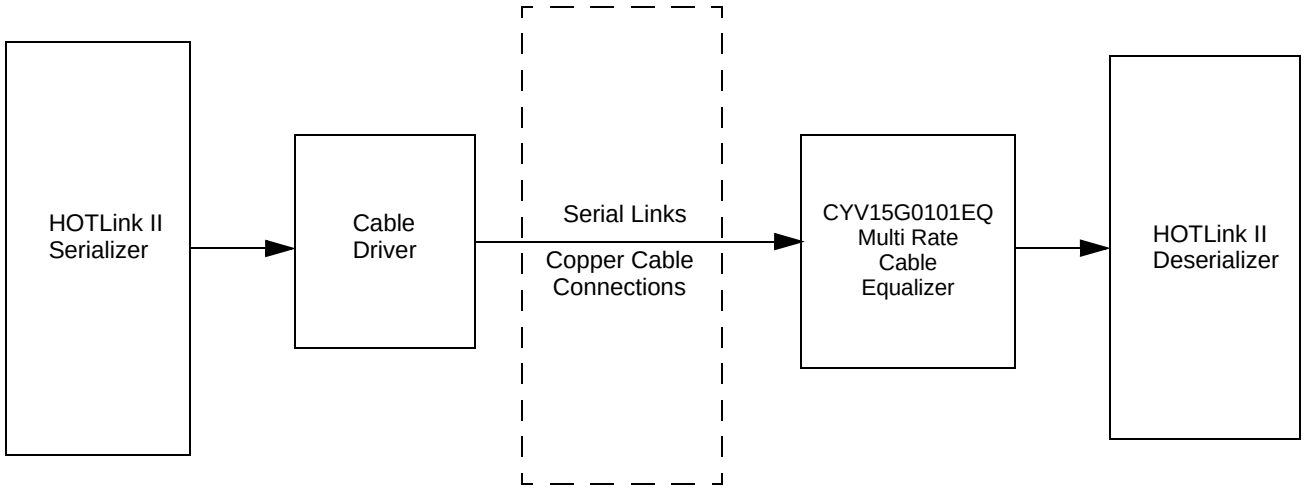
Functional Description

The CYV15G0101EQ is a multi rate adaptive equalizer designed to equalize and restore signals received over 75Ω coaxial cable. The equalizer meets SMPTE 292M, SMPTE 344M, and SMPTE 259M data rates. The CYV15G0101EQ is optimized to equalize up to 350m of Belden 1694A coaxial cable at 270 Mbps and typically up to 200m of Belden 1694A coaxial cable at 1.485 Gbps. The CYV15G0101EQ connects seamlessly to the HOTLink II family of transceivers.

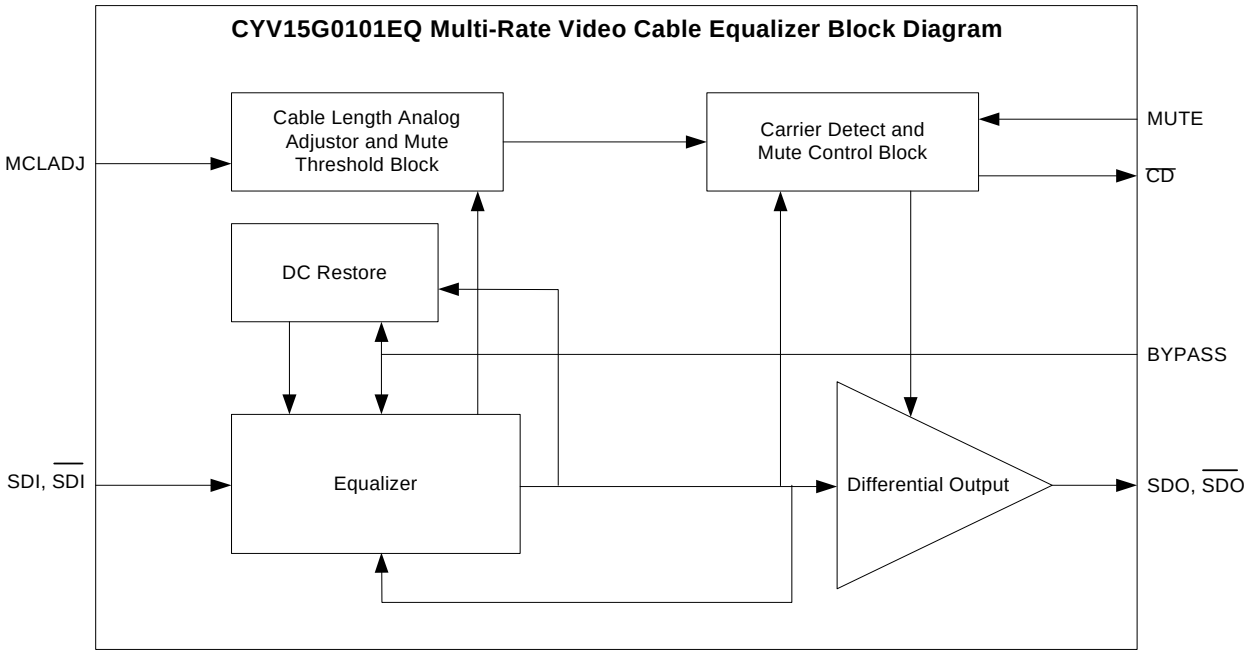
The CYV15G0101EQ has DC restoration to compensate for the DC content of the SMPTE pathological patterns. A cable length indicator (CLI) provides an indication of the cable length being equalized at HD-SDI and SD-SDI data rates. The maximum cable length adjust (MCLADJ) sets the approximate maximum cable length to equalize at SD and HD data rates. The CYV15G0101EQ's differential serial outputs (SDO, $\overline{SDO}$) mute when the approximate cable length set by MCLADJ is reached. $\overline{CD}$/MUTE is a bidirectional pin that provides an indication of the signal present at the equalizer inputs. It also controls muting the outputs of the equalizer at HD and SD data rates.

Power consumption is typically 160 mW at 3.3V.

Equalizer System Connection Diagram



Equalizer Block Diagram



Pinouts

Figure 1. Pin Diagram - 16 Pin SOIC (Top View)

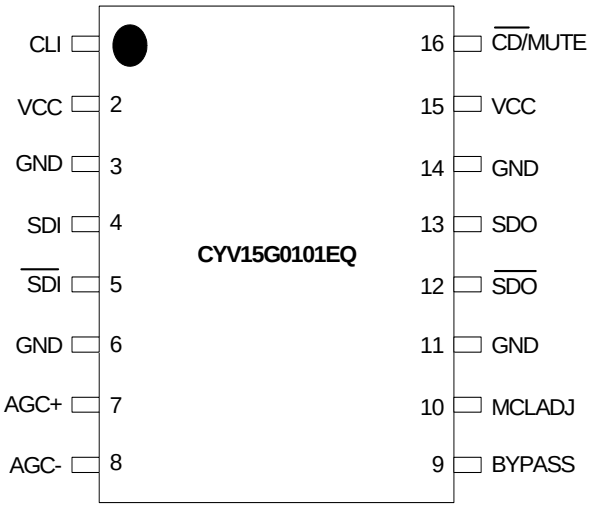


Table 1. Pin Descriptions - CYV15G0101EQ Single Channel Cable Equalizer

Name	IO Characteristics	Signal Description
Control Signals		
CLI	Analog Output	**Cable Length Indicator.** CLI provides an analog voltage proportional to the equalized cable length. CLI works at both SD-SDI and HD-SDI data rates.
$\overline{CD}$/MUTE	LVTTL IO	**Carrier Detect or Mute Indicator.** **Output:** When the incoming data stream is present and the cable length does not exceed that set by MCLADJ, the $\overline{CD}$/MUTE outputs a voltage less than 0.8V. When the incoming data stream is not present or the cable length exceeds that set by MCLADJ, the $\overline{CD}$/MUTE outputs a voltage greater than 2.8V. **Input:** When the $\overline{CD}$/MUTE pin is set LOW, the equalizer's differential serial outputs are not muted. When the $\overline{CD}$/MUTE pin is set HIGH, the equalizer's differential serial outputs are muted.
MCLADJ	Analog Input	**Maximum Cable Length Adjust.** The maximum equalized cable length is set by the voltage applied to the MCLADJ input. When the maximum cable length set by MCLADJ is reached, CD is driven high and the differential output is muted. If MCLADJ functionality is not needed, this pin should be left floating or tied to ground to allow maximum equalized cable length. MCLADJ works at both SD and HD data rates.
BYPASS	LVTTL Input	**Equalizer Bypass.** When BYPASS is set HIGH, the signal presented at the equalizer's differential serial inputs (SDI, $\overline{SDI}$) is routed to the equalizer's differential serial outputs (SDO, $\overline{SDO}$) without performing equalization. When BYPASS is set LOW, the incoming video data stream is equalized and presented at the equalizer's serial differential outputs (SDO, $\overline{SDO}$). In equalizer bypass mode, $\overline{CD}$/MUTE is not functional.
AGC±	Analog	**Automatic Gain Control.** Place a capacitor of 1 μF between the AGC± pins.
SDO, $\overline{SDO}$	Differential Output	**Differential Serial Outputs.** The equalized serial video data stream is presented at the SDO/$\overline{SDO}$ differential serial CML output.
SDI, $\overline{SDI}$	Differential Input	**Differential Serial Inputs.** SDI/$\overline{SDI}$ accepts either a single-ended or differential serial video data stream over 75Ω coaxial cable.
Power		
VCC	Power	**+3.3V Power.**
GND	Gnd	**Connect to Ground.**

Equalizer Operation

The CYV15G0101EQ is a high speed adaptive cable equalizer designed to equalize standard definition (SD) and high definition (HD) serial digital interface (SDI) video data streams. CYV15G0101EQ equalizer is optimized to equalize up to 350m of Canare L-5CFB and Belden 1694A cable at 270 Mbps and typically up to 200m of Canare L-5CFB and Belden 1694A cable at 1.485 Gbps. The CYV15G0101EQ equalizer contains one power supply and typically consumes 160 mW power at 3.3V. The multi rate equalizer meets the SMPTE 259M, SMPTE 292M, SMPTE 344M, and DVB-ASI video standards. It meets all patho-logical requirements for SMPTE 292M as defined by RP198, and for SMPTE 259M as defined by RP178. The CYV15G0101EQ multi rate cable equalizer is auto adaptive from 143 Mbps to 1.485 Gbps.

The CYV15G0101EQ equalizer has variable gain and multiple equalization stages that reverse the effects of the cable. This equalization is achieved by separate regulation of the lower and higher frequency components in the signal to give a clean output eye diagram. The CYV15G0101EQ has DC restoration to compensate for the DC content of the SMPTE pathological patterns.

SDI, $\overline{\text{SDI}}$

The CYV15G0101EQ accepts single-ended or differential serial video data streams over 75Ω coaxial cable. It is recommended to AC couple the SDI and $\overline{\text{SDI}}$ inputs as they are internally biased to 1.2V.

SDO, $\overline{\text{SDO}}$

The CYV15G0101EQ has differential serial output interface drivers that use current mode logic (CML) drivers to provide source matching for the transmission line. These outputs are either AC coupled or DC coupled to the HOTLink II SerDes device.

CLI

Cable Length Indicator (CLI) is an analog output that gives an output voltage proportional to the equalized cable length. CLI gives an approximation of the length of cable at the differential serial inputs (SDI, $\overline{\text{SDI}}$). CLI works at high definition (HD) data rates and standard definition (SD) data rates. The graph in Figure 3 on page 7 illustrates the CLI output voltage at various Belden 1694A cable lengths. With an increase in cable length, CLI output voltage decreases.

MCLADJ

Maximum Cable Length Adjust (MCLADJ) sets the approximate maximum amount of cable to be equalized. When the maximum cable length set by MCLADJ is reached, CD is driven high and the outputs are muted. MCLADJ works at SD and HD data rates.

The graph in Figure 2 on page 7 illustrates the voltage required at MCLADJ input to equalize various Belden 1694A cable lengths for SD and HD data rates. If MCLADJ functionality is not needed, this pin should be left floating or tied to ground to allow maximum equalized cable length.

$\overline{\text{CD}}$/MUTE

Carrier Detect/MUTE ($\overline{\text{CD}}$/MUTE) is a bidirectional pin that provides an indication of the signal present at the equalizer's input, or it controls the muting of the equalizer's output. The ($\overline{\text{CD}}$/MUTE) operates for both HD and SD data rates.

If $\overline{\text{CD}}$/MUTE is used as an output and the incoming data stream is not present or the cable length exceeds that set by MCLADJ, the voltage at the $\overline{\text{CD}}$/MUTE output is greater than 2.8V. If $\overline{\text{CD}}$/MUTE is used as an output, the incoming data stream is present and the cable length does not exceed that set by MCLADJ, then the voltage at the $\overline{\text{CD}}$/MUTE output is less than 0.8V.

If $\overline{\text{CD}}$/MUTE is used as an input and is set LOW, the equalizer serial outputs are not muted. If the $\overline{\text{CD}}$/MUTE is used as an input and is set HIGH, then the equalizer serial outputs are muted.

When an invalid signal or a signal transmitted with a launch amplitude of less than 500 mV at HD data rates is received, the equalizer's serial outputs are muted.

BYPASS

The CYV15G0101EQ has a bypass mode that allows the user to bypass the equalizer's equalization and DC restoration functions. When the bypass mode is set HIGH, the signal presented at the equalizer's differential serial inputs (SDI, $\overline{\text{SDI}}$) is routed to the equalizer's differential serial outputs (SDO, $\overline{\text{SDO}}$) without equalizing.

When BYPASS is set LOW, the incoming video data stream is equalized and presented at the equalizer's differential serial outputs (SDO, $\overline{\text{SDO}}$).

In equalizer bypass mode, $\overline{\text{CD}}$/MUTE is not functional.

AGC

Place a capacitor of 1 µF between the AGC± pins of the CYV15G0101EQ equalizer.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential.....–0.5V to +3.8V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage ..... –0.5V to V_{CC}+0.5V

Electro Static Discharge (ESD) HBM.....> 2000 V (JEDEC EIA/JESD-A114A)

Latch Up Current ..... > 200 mA

Power Up Requirements

The CYV15G0101EQ contains one power supply. The voltage on any input or IO pin must not exceed the power pin during power up.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+3.3V ±5%

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage[1]	–	3.135	3.3	3.465	V
P_D	Power Consumption[2]	–	125	160	190	mW
I_S	Supply Current[1]	–	38	48	60	mA
V_{CMOUT}	Output Common Mode Voltage[1]	Load = 50Ω	–	VCC – ΔVSDO/2 = 2.9	–	V
V_{CMIN}	Input Common Mode Voltage[1] (Bypass = High)	–	1		1.4	V
	Input Common Mode Voltage[1] (Bypass = Low)	–	0		2.9	V
–	CLI DC Voltage (0m)[1]	–	2.2	2.65	2.95	V
–	CLI DC Voltage (No Signal)[1]	–	1.5	1.9	2.3	V
–	Floating MCLADJ DC Voltage[1]	–		1.3		V
–	MCLADJ Range[3]	–	0.4	0.72	1.02	V
$V_{\overline{CD}/MUTE(OH)}$	$\overline{CD}$/MUTE Output Voltage[1]	Carrier Not Present	2.8	–	–	V
$V_{\overline{CD}/MUTE(OL)}$		Carrier Present	–	–	0.8	V
$V_{\overline{CD}/MUTE}$	$\overline{CD}$/MUTE Input Voltage Required to Force Outputs to Mute[1]	Min to Mute	2.5	–	–	V
$V_{\overline{CD}/MUTE}$	$\overline{CD}$/MUTE Input Voltage Required to Force Active[1]	Max to Activate	–	–	1	V

Notes
1. Production test.
2. Calculated results from production test.
3. Not tested. Based on characterization.

AC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
–	Serial Input Data Rate[1]	–	143	–	1485	Mbps
V_{SDI}	Input Voltage Swing	Single-ended, at the transmitter, HD data rate	500[5]		1200	mV
V_{SDI}	Input Voltage Swing	Single-ended, at the transmitter, SD data rate	500[6]		1200	mV
ΔV_{SDO}	Output Voltage Swing[1]	Differential$_{p-p}$, 50Ω load	450	700	950	mV
–	Output Jitter for Various Cable Lengths and Data Rates	270 Mbps Belden 1694A: 0-350m Canare L-5CFB: 0-350m 800 mV transmit amplitude Equalizer pathological pattern	–	0.2[1]	–	UI
		1.485 Gbps Belden 1694A: 0-140m Canare L-5CFB: 0-140m 800 mV transmit amplitude Equalizer pathological pattern	–	0.25[1]	–	UI
		1.485 Gbps Belden 1694A: 140-200m Canare L-5CFB: 140-200m 800 mV transmit amplitude Equalizer pathological pattern	–	0.3[7]	–	UI
–	Output Rise/Fall Time[3, 4]	20% - 80%, HD data rate	80	120	220	ps
–	Output Rise/Fall Time[3, 4]	20% - 80%, SD data rate	80	120	350	ps
–	Mismatch in Rise/Fall Time[3, 4]	–	–	–	30	ps
–	Duty Cycle Distortion[3, 4]	HD color bar pattern	–	20	–	ps
–	Overshoot[3, 4]	–	–	–	10	%
–	Input Return Loss[3]	–	-15	–	–	dB
–	Input Resistance[3, 4]	Single-ended	–	2.5	–	kΩ
–	Input Capacitance[3, 4]	Single-ended	–	1	–	pF
–	Output Resistance[3, 4]	Single-ended	–	50	–	Ω

Notes
4. Not tested. Guaranteed by design simulations.
5. Based on characterization across temperature and voltage with 140m of Belden 1694A cable, transmitting SMPTE Equalizer Pathological Test Pattern.
6. Based on characterization across temperature and voltage with 350m of Belden 1694A cable, transmitting SMPTE Equalizer Pathological Test Pattern.
7. Based on characterization at T_A = 25°C, V_{CC} = 3.3V

Typical Performance Graphs

(Unless otherwise stated, V_{CC} = 3.3V, T_A = 25°C)

Figure 2. MCLADJ Input Voltage vs. Belden 1694A Cable Length at SD-SDI and HD-SDI Data Rates

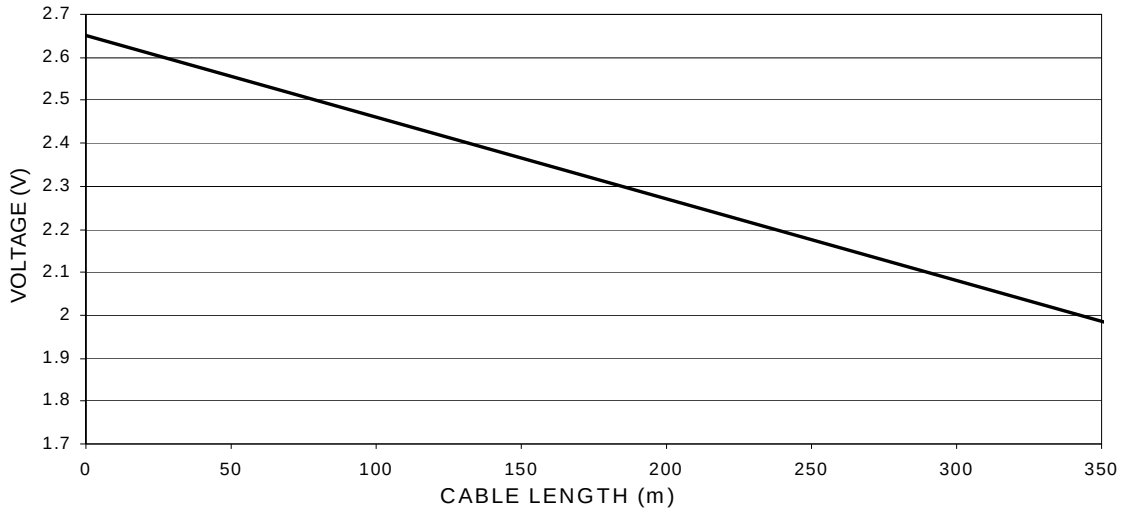
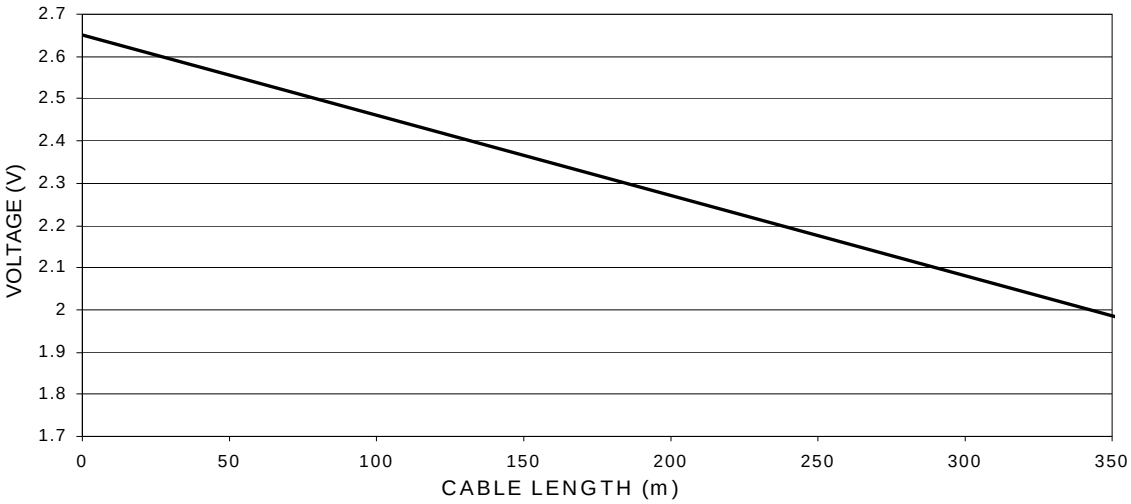
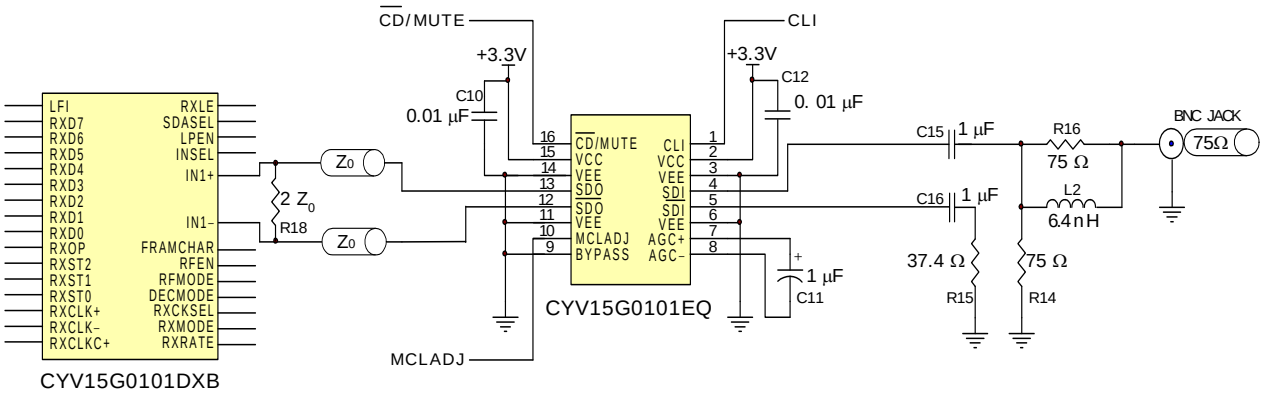


Figure 3. CLI Output Voltage vs. Belden 1694A Cable Length at SD-SDI and HD-SDI Data Rates



Typical Application Circuit

Figure 4. Interfacing CYV15G0101EQ to the HOTLink II SerDes

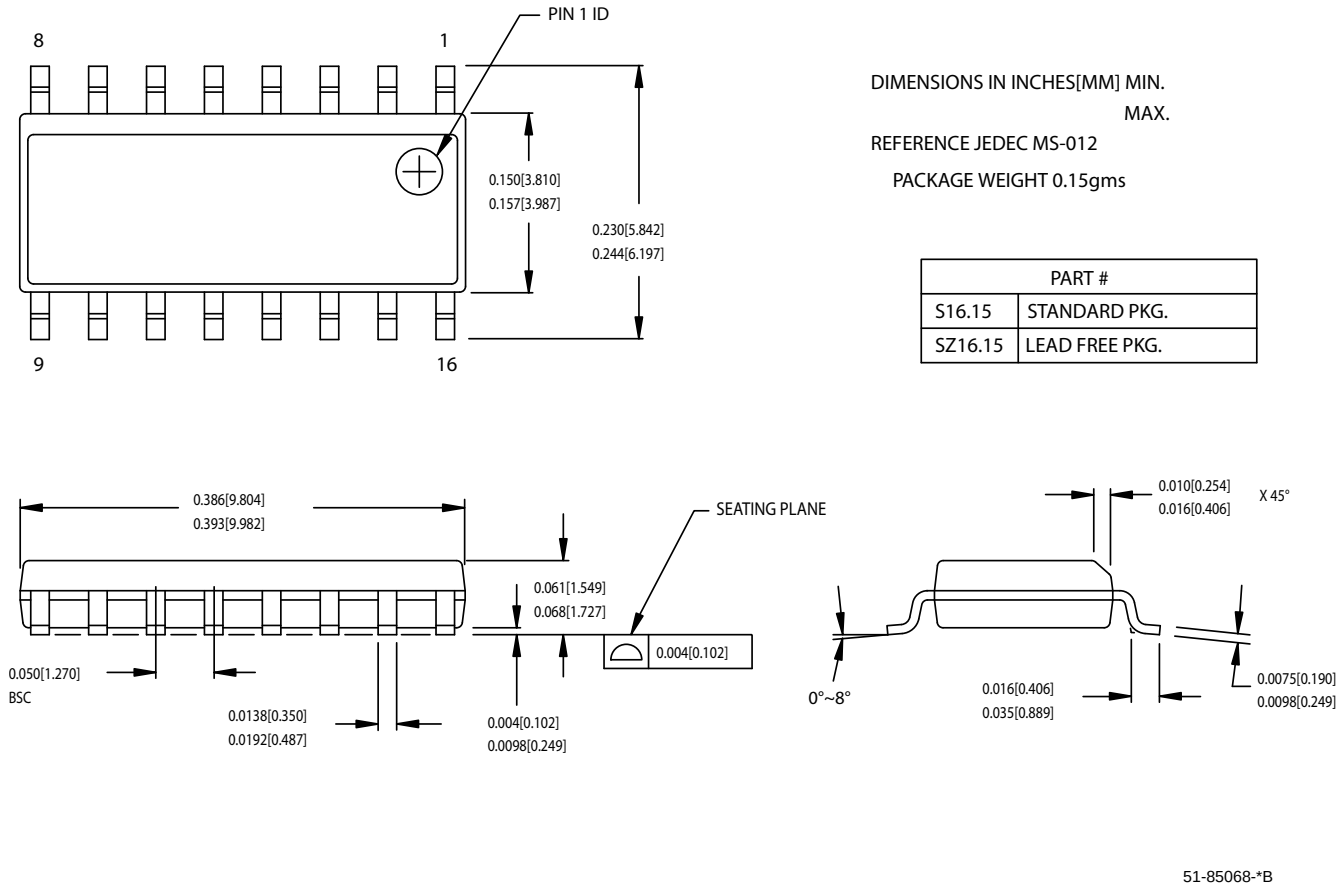


Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CYV15G0101EQ-SXC	SZ16.15	Pb-free 16-Pin 150 Mil SOIC	0 to 70°C

Package Dimension

Figure 5. 16-Pin (150 Mil) SOIC S16.15



Document History Page

Document Title: CYV15G0101EQ Multi Rate Video Cable Equalizer Document Number: 001-04184				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	389196	SEE ECN	BCD	New preliminary datasheet
*A	394763	SEE ECN	BCD	Updated preliminary datasheet for release to the internet
*B	431556	SEE ECN	BCD	Changed AC and DC parameters
*C	504487	SEE ECN	FRE	Updated AC and DC parameters. Changed datasheet status from preliminary to final
*D	514998	SEE ECN	FRE	Fixed typo in diagrams on page 2
*E	1396423	SEE ECN	UKK/AESA	Updated AC and DC electrical characteristics and pin description of MCLADJ and CD.