DATA SHEET

PCA9559

5-bit multiplexed/1-bit latched 6-bit I^2C EEPROM DIP switch

Product data
Supersedes data of 2002 May 24

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Philips Semiconductors

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5-bit multiplexed/1-bit latched 6-bit I²C EEPROM DIP switch

PCA9559

FEATURES

- 5-bit 2-to-1 multiplexer, 1-bit latch DIP switch
- 6-bit internal non-volatile register
- Internal non-volatile register programmable and readable via I²C-bus
- Override input forces all outputs to logic 0
- 5 open drain multiplexed outputs
- 1 open drain non-multiplexed (latched) output
- 5 V and 2.5 V tolerant inputs
- Useful for 'jumperless' configuration of PC motherboards
- 2 address pins, allowing up to 4 devices on the I²C-bus
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

DESCRIPTION

The PCA9559 is a 20-pin CMOS device consisting of one 6-bit non-volatile EEPROM registers, 5 hardware pin inputs and a 5-bit multiplexed output with one latched EEPROM bit. It is used for DIP switch-free or jumper-less system configuration and supports Mobile and Desktop VID Configuration, where 2 preset values (1 set of internal non-volatile registers and 1 set of external hardware pins) set processor voltage for operation in either performance or deep sleep modes. The PCA9559 is also useful in server and telecom/networking applications when used to replace DIP switches or jumpers, since the settings can be easily changed via I²C/SMBus without having to power down the equipment to open the cabinet. The non-volatile memory retains the most current setting selected before the power is turned off.

The PCA9559 typically resides between the CPU and Voltage Regulator Module (VRM) when used for CPU VID (Voltage IDentification code) configuration. It is used to bypass the CPU-defined VID values and provide a different set of VID values to the VRM, if an increase in the CPU voltage is desired. An increase in CPU voltage combined with an increase in CPU frequency leads to a performance boost of up to 7.5%. Lower CPU voltage reduces power consumption.

The PCA9559 has 2 address pins allowing up to 4 devices to be placed on the same I²C-bus or SMBus.

PIN CONFIGURATION

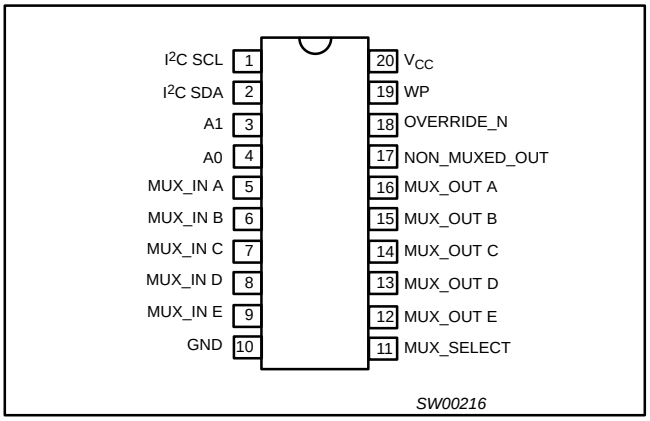


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	I²C SCL	Serial I²C-bus clock
2	I²C SDA	Serial bi-directional I²C-bus data
3	A1 Address	A1
4	A0 Address	A0
5-9	MUX_IN A-E	External inputs to multiplexer
10	GND	Ground
11	MUX_SELECT	Selects MUX_IN inputs or register contents for MUX_OUT outputs
12-16	MUX_OUT E-A	Open drain multiplexed outputs
17	NON_MUXED_OUT	Open drain outputs from non-volatile memory
18	OVERRIDE_N	Forces all outputs to logic 0
19	WP	Non-volatile register write-protect
20	V_{CC}	Power supply: +3.0 to +3.6 V

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
20-Pin Plastic TSSOP	0 to +70 °C	PCA9559PW	PCA9559	SOT360-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

FUNCTIONAL DESCRIPTION

When the MUX_SELECT signal is logic 0, the multiplexer will select the data from the non-volatile register to drive on the MUX_OUT pins. When the MUX_SELECT signal is logic 1, the multiplexer will select the MUX_IN lines to drive on the MUX_OUT pins. The MUX_SELECT signal is also used to latch the NON_MUXED_OUT signal which outputs data from the non-volatile register. The NON_MUXED_OUT signal latch is transparent when MUX_SELECT is in a logic 0 state, and will latch data when MUX_SELECT is in a logic 1 state. When the active-LOW OVERRIDE_N signal is set to logic 0 and the MUX_SELECT signal is at a logic 0, all outputs will be driven to logic 0. This information is summarized in Table 1.

The Write Protect (WP) input is used to control the ability to write the contents of the 6-bit non-volatile register. If the WP signal is logic 0, the I²C-bus will be able to write the contents of the non-volatile register. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile register.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I²C-bus (described in the next section).

The OVERRIDE_N, WP, MUX_IN, and MUX_SELECT signals have internal pull-up resistors. See the DC and AC Characteristics for hysteresis and signal spike suppression figures.

FUNCTION TABLE

OVERRIDE_N	MUX_SELECT	MUX_OUT OUTPUTS	NON_MUXED_OUT OUTPUT
0	0	All 0's	All 0's
0	1	MUX_IN inputs	Latched NON_MUXED_OUT [1]
1	0	From non-volatile register	From non-volatile register
1	1	MUX_IN inputs	From non-volatile register

NOTE:
1. NON_MUXED_OUT state will be the value present on the output at the time of the MUX_SELECT input transitioned from a logic 0 to a logic 1 state.

I²C INTERFACE

Communicating with this device is initiated by sending a valid address on the I²C-bus. The address format (see FIgure 1) has 5 fixed bits and two user-programmable bits followed by a 1-bit read/write value which determines the direction of the data transfer.

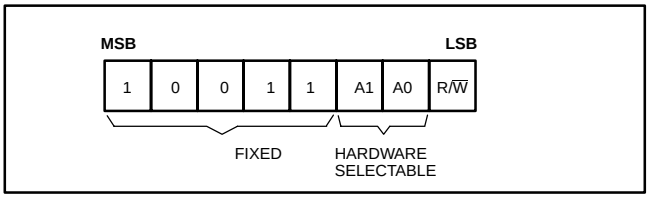


Figure 2. I²C Address Byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the non-volatile register. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The four high-order bits are latched outputs, while the four low order bits are multiplexed outputs (Figure 3).

NOTE:
1. To ensure data integrity, the non-volatile register must be internally write protected when V_{CC} to the I²C-bus is powered down or V_{CC} to the component is dropped below normal operating levels.

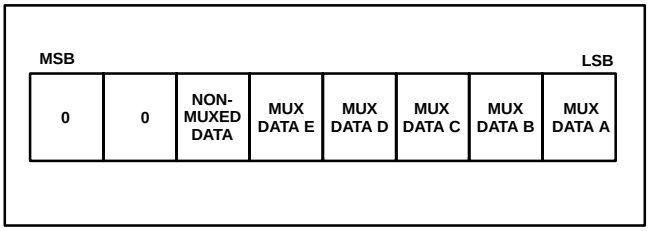


Figure 3. I²C Data Byte

POWER-ON RESET (POR)

When power is applied to V_{CC}, an internal power-on reset holds the PCA9559 in a reset state until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9559 volatile registers and I²C/SMBus state machine will initialize to their default states.

The MUX_OUT and NON_MUXED_OUT pin values depend on:
- the OVERRIDE # and MUX_SELECT logic levels
- the previously stored values in the EEPROM register/current MUX_IN pin values as shown in the Function Table.

BLOCK DIAGRAM

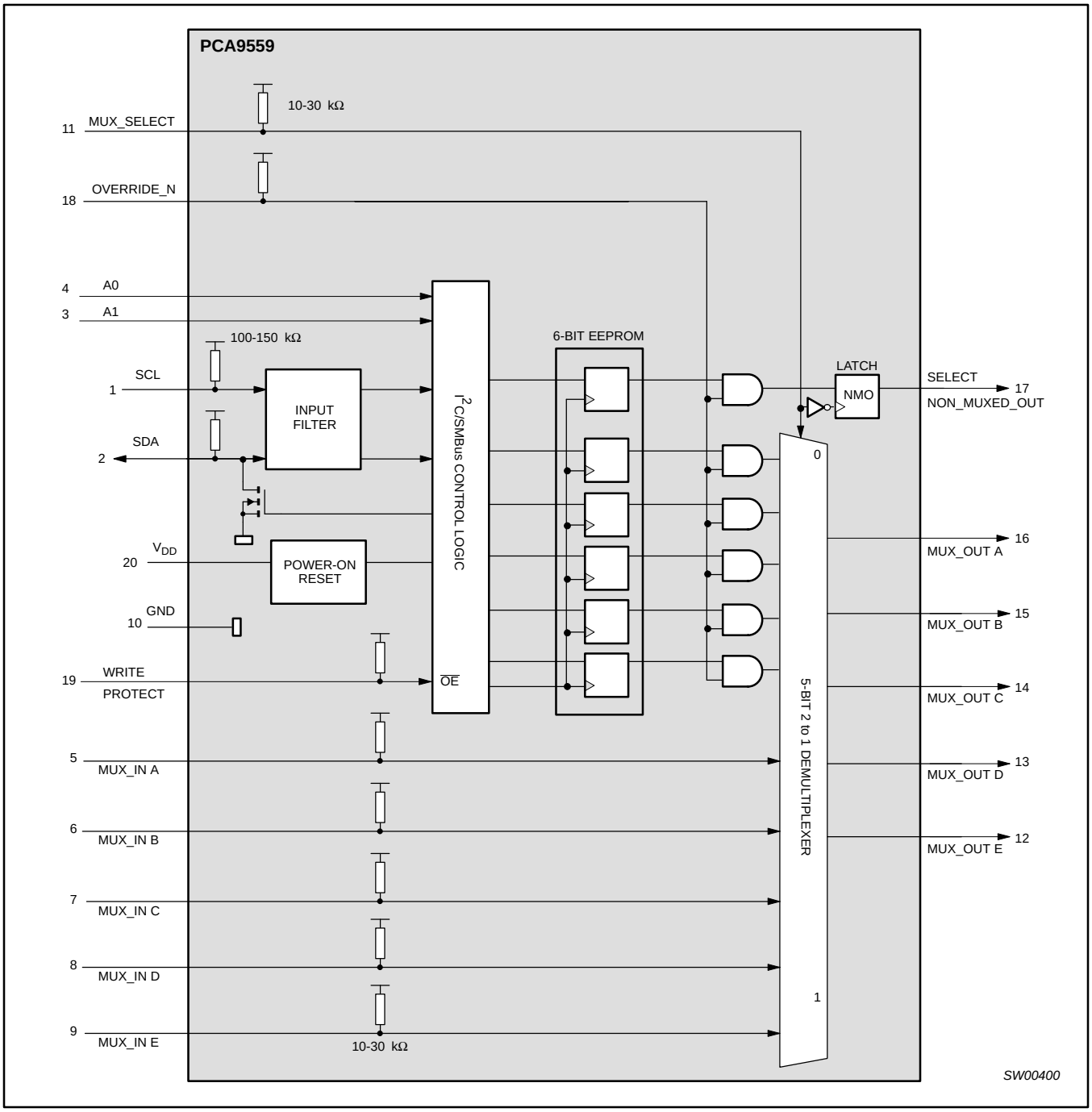


Figure 4. Block diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
V_I	DC input voltage	Note 3	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC output voltage	Note 3	-0.5 to V_{CC} +0.5	V
T_{stg}	Storage temperature range		-60 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		CONDITIONS	LIMITS		UNIT
				MIN	MAX	
V_{CC}	DC supply voltage			3.0	3.6	V
V_{IL}	LOW-level input voltage	SCL, SDA	I_{OL}= 3 mA	-0.5	0.9	V
V_{IH}	HIGH-level input voltage	SCL, SDA	I_{OL}= 3 mA	2.7	4.0	V
V_{OL}	LOW-level output voltage	SCL, SDA	I_{OL}= 3 mA	—	0.4	V
			I_{OL}= 6 mA	—	0.6	
V_{IL}	LOW-level input voltage	OVERRIDE_N, MUX_IN, MUX_SELECT		-0.5	0.8	V
V_{IH}	HIGH-level input voltage	OVERRIDE_N, MUX_IN, MUX_SELECT		2.0	4.0	V
I_{OL}	LOW-level output current	MUX_OUT, NON_MUXED_OUT		—	8	mA
I_{OH}	HIGH-level output current	MUX_OUT, NON_MUXED_OUT		—	100	µA
dt/dv	Input transition rise or fall time			0	10	ns/V
T_{amb}	Operating temperature			0	70	°C

DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Supply						
V_{CC}	Supply voltage		3	—	3.8	V
I_{CCL}	Supply current	Operating mode ALL inputs = 0 V	—	—	10	mA
I_{CCH}	Supply current	Operating mode ALL inputs = V_{CC}	—	—	600	µA
V_{POR}	Power-on reset voltage	no load; $V_I = V_{CC}$ or GND	—	1.9	2.6	V
Input SCL: Input/Output SDA						
V_{IL}	LOW-level input voltage		-0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2	—	V_{CC} + 0.5	V
I_{OL}	LOW-level output curret	V_{OL} = 0.4 V	3	—	—	mA
I_{OL}	LOW-level output curret	V_{OL} = 0.6 V	6	—	—	mA
I_{IH}	Leakage current HIGH	$V_I = V_{CC}$	-1.5	—	-12	µA
I_{IL}	Leakage current LOW	V_I = GND	-7	—	-32	µA
C_I	Input capacitance		—	—	10	pF
OVERRIDE_N, WP, MUX_SELECT						
I_{IH}	Leakage current HIGH	$V_I = V_{CC}$	-20	—	-100	µA
I_{IL}	Leakage current LOW	V_I = GND	-86	—	-267	µA
C_I	Input capacitance		—	—	10	pF
MUX_IN A ⇒ E						
I_{IH}	Leakage current HIGH	$V_I = V_{CC}$	-0.166	—	-0.75	mA
I_{IL}	Leakage current LOW	V_I = GND	-0.72	—	-2	mA
C_I	Input capacitance		—	—	10	pF
A0, A1 Inputs						
I_{IH}	Leakage current HIGH	$V_I = V_{CC}$	-1	—	1	µA
I_{IL}	Leakage current LOW	V_I = GND	-1	—	1	µA
C_I	Input capacitance		—	—	10	pF
MUX_OUT E ⇒ A						
V_{OL}	LOW-level output curret	I_{OL} = 100 µA	—	—	0.4	V
V_{OL}	LOW-level output curret	I_{OL} = 2 mA	—	—	0.7	V
NON_MUXED_OUT						
V_{OL}	LOW-level output curret	I_{OL} = 100 µA	—	—	0.4	V
V_{OL}	LOW-level output curret	I_{OL} = 2 mA	—	—	0.7	V

NOTES:
1. V_{HYS} is the hysteresis of Schmitt-Trigger inputs

NON-VOLATILE STORAGE SPECIFICATIONS

PARAMETER	SPECIFICATION
Memory cell data retention	10 years min
Number of memory cell write cycles	100,00 cycles min

Application Note *AN250 I²C DIP Switch* provides additional information on memory cell data retention and the minimum number of write cycles.

AC CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
MUX_IN ⇒ MUX_OUT					
t_{PLH}	LOW-to-HIGH transition time	—	28	37	ns
t_{PHL}	HIGH-to-LOW transition time	—	16	21	ns
Select ⇒ MUX_OUT					
tPLH	LOW-to-HIGH transition time	—	30	39	ns
tPHL	HIGH-to-LOW transition time	—	17	22	ns
OVERRIDE_N ⇒ NON-MUXED_OUT					
t_{PLH}	LOW-to-HIGH transition time	—	34	43	ns
t_{PHL}	HIGH-to-LOW transition time	—	19	25	ns
OVERRIDE_N ⇒ MUX_OUT					
t_{PLH}	LOW-to-HIGH transition time	—	31	41	ns
t_{PHL}	HIGH-to-LOW transition time	—	21	27	ns
t_R	Output rise time	1.0	—	3	ns/V
t_F	Output fall time	1.0	—	3	ns/V
P_F	Pull-up resistor for outputs	1.0	—	—	ns/V
C_L	Test load capacitance on outputs	—	—	—	pF
I²C-bus					
t_{SCL}	SCL clock frequency	10	—	400	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3	—	—	µs
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	600	—	—	ns
t_{LOW}	LOW period of SCL clock	1.3	—	—	µs
t_{HIGH}	HIGH period of SCL clock	600	—	-12	ns
$t_{SU:STA}$	Set-up time for a repeated START condition	600	—	-32	ns
$t_{HD:DAT}$	Data hold time	0	—	10	ns
$t_{SU:DAT}$	Data set-up time	100	—	-100	ns
t_{SP}	Data spike time	0	—	50	ns
$t_{SU:STO}$	Set-up time for STOP condition	600	—	10	ns
t_R	Rise time for both SDA and SCL signals (10 - 400 pF bus)	20	—	300	ns
t_I	Fall time for both SDA and SCL signals (10 - 400 pF bus)	20	—	300	ns
C_L	Capacitive load for each bus line	—	—	400	pF
T_W	Write cycle time[1]	—	15	—	ms

NOTE:
1. WRITE CYCLE time can only be measured indirectly during the write cycle. During this time, the device will not acknowledge its I²C Address.

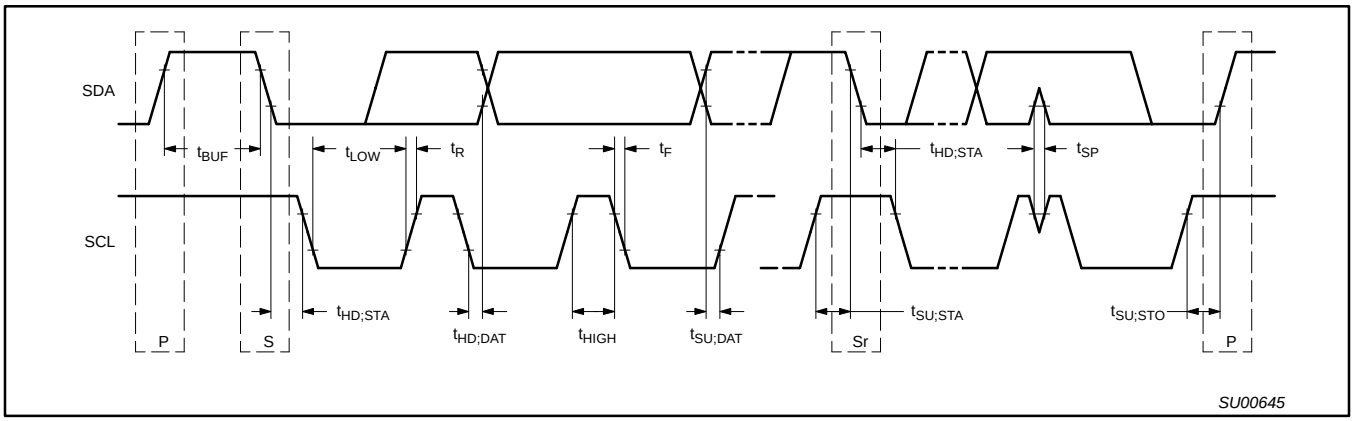


Figure 5. Definition of timing

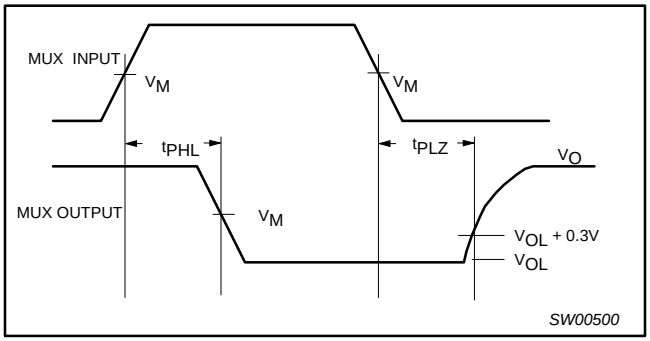


Figure 6. Open drain output enable and disable times

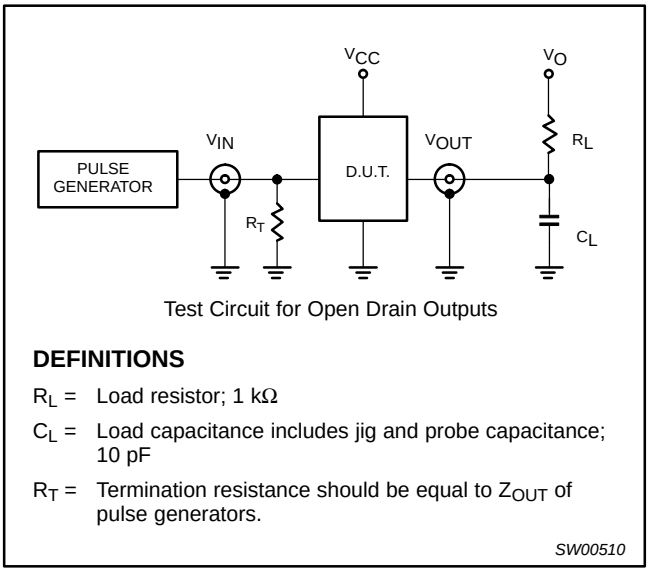
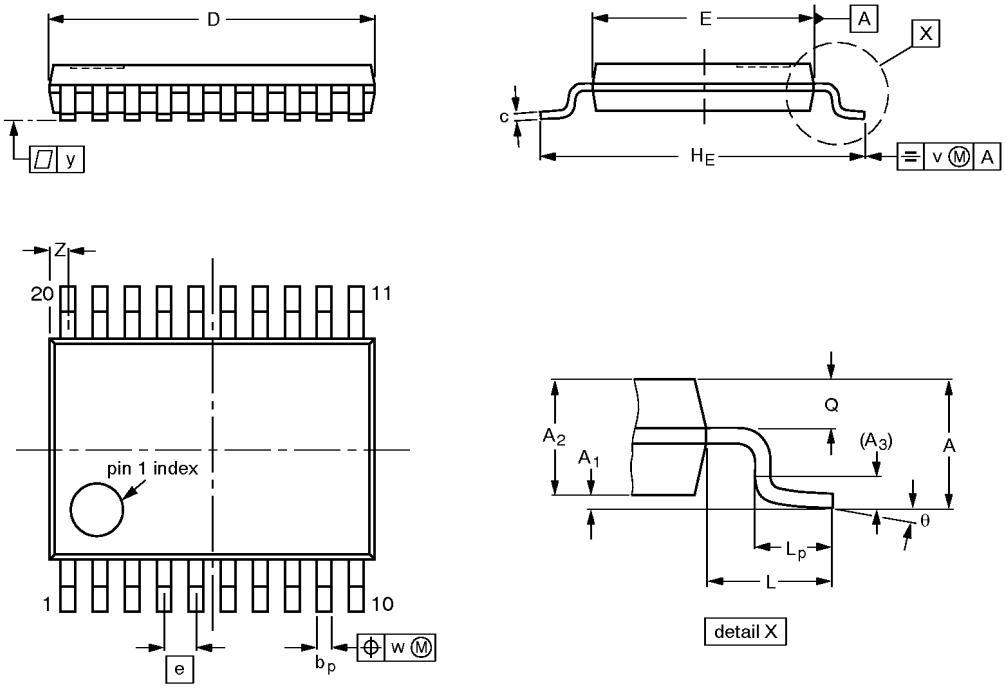
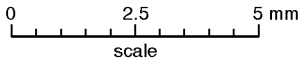


Figure 7. Test circuit

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

REVISION HISTORY

Rev	Date	Description
_4	20030627	**Product data (9397 750 11675); ECN 853-2181 29936 dated 19 May 2003. Supersedes data of 2002 May 24 (9397 750 09891).** Modifications: • Update marketing information. • Increase number of write cycles from 3K to 100K.
_3	20020524	Product data (9397 750 09891); ECN 853-2181 28310 of 24 May 2002.

5-bit multiplexed/1-bit latched 6-bit I²C EEPROM DIP switch

PCA9559

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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