

## DDC Accelerator (DDCA)

The ISL54103 DDC Accelerator (DDCA) is a dual active pull-up bus terminator designed to improve data transmission speed on the DDC 2-wire serial bus interfaces.

The DDCA detects rising input transitions with two internal voltage references and two comparators per channel. After the voltage on a data line crosses the first threshold ( $V_{TRIPL}$ ), the boost pull-up current source is activated to speed transition. After the voltage crosses the second threshold ( $V_{TRIPH}$ ), the boost pull-up current source is de-activated, leaving an active pull-up current of 275 $\mu$ A on the line. When both channels are HIGH, the pull-up current for both lines is reduced to 100 $\mu$ A to save power. Internal logic ensures that the active and boost pull-up current sources are not activated during downward transitions.

The level for  $V_{TRIPH}$  is controlled by a bandgap voltage referred to  $V_{DD}$ . This feature makes the switching behavior invariant for all power supply voltages between 2.7V and 5.5V.

A noise filter on each channel prevents the circuit from responding to input transitions that do not exceed a voltage-time threshold. To activate the boost circuit, the input must exceed  $V_{TRIPL}$  by 100Vns (typical) (See Figure 10).

The DDCA permits operation of the bus at frequencies up to 100kHz, despite the capacitive loads of multiple devices and/or long PC board traces. Enhanced ESD protection on the accelerator pins are guaranteed to withstand 8kV ESD (HBM) events.

The DDC Accelerator provides an essential function in DDC applications because of distributed capacitance of the DDC wires in long video cables. By incorporating DDCA, systems using DDC can reliably increase their bus load, allowing longer cables, without the risk of data corruption.

## Ordering Information

PART NUMBER	TAPE & REEL	TEMP RANGE (°C)	PACKAGE
ISL54103IHZ-T7 (Note)	7"	-40 to 85	5 Ld SOT-23 (Pb-free)

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

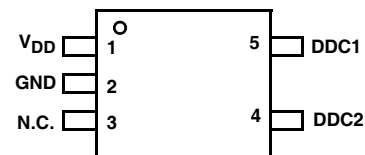
- Active Termination for DDC Lines
- Enhances System Bus Signal Rise Time
- More Reliable HDCP Performance In Video Multiplexers and Cable Extenders
- Increases Maximum Cable Length While Guaranteeing Data Integrity
- 2.2mA Current Boost on Low to High Transitions
- 8kV ESD Protection on SDA and SCL Pins
- Wide Operating Voltage Range: 2.7V to 5.5V
- Small Package - 5 Ld SOT-23
- Pb-free Plus Anneal Available (RoHS Compliant)

## Target Applications

- Video Multiplexers
- Video Cable Extenders
- Video Distribution Amplifiers
- Televisions
- Computer Monitors
- Projectors

## Pinout

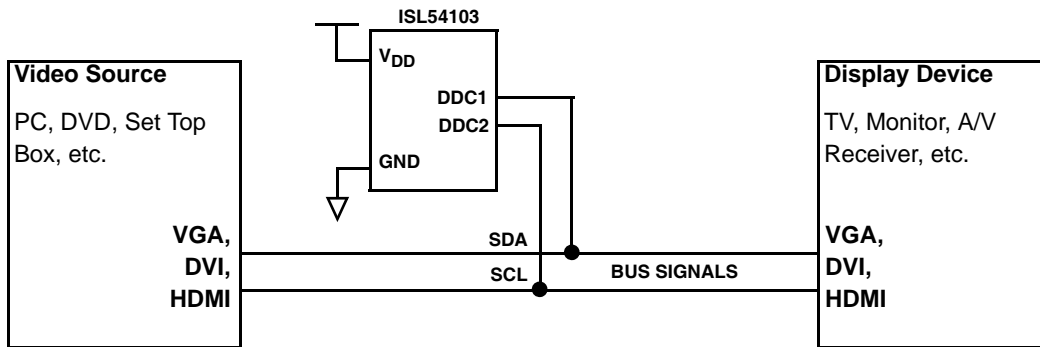
**ISL54103**  
**(5 LD SOT-23)**  
TOP VIEW



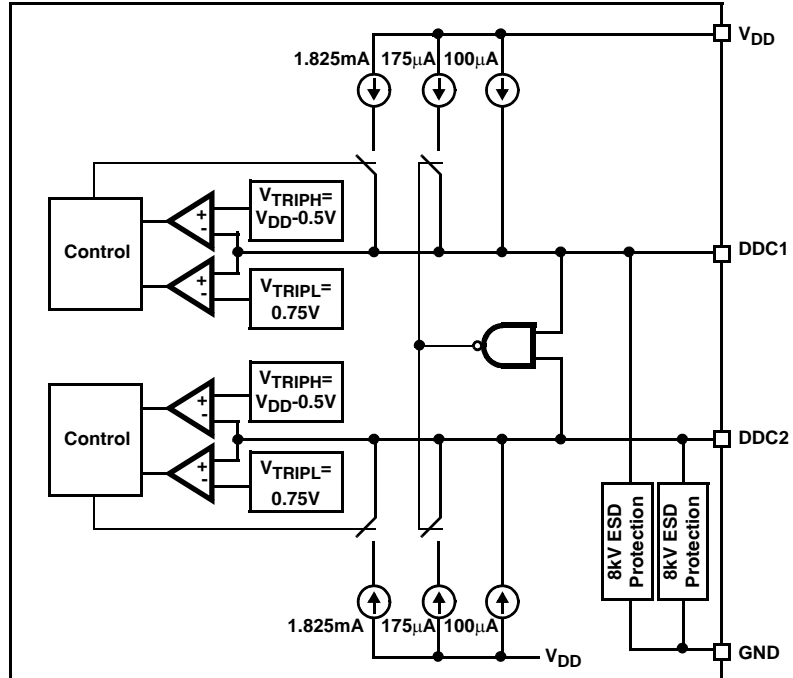
**Pin Descriptions**

SOT-23	SYMBOL	DESCRIPTION
1	V <sub>DD</sub>	Supply Voltage
2	GND	Ground
3	N.C.	No Connect
4	DDC1	Active Pull-Up for DDC Signal
5	DDC2	Active Pull-Up for DDC Signal

**System Diagram**



**IC Block Diagram**



**Absolute Maximum Ratings**

Supply Voltage Range . . . . . -1V to 6.5V  
 Operating Junction Temperature . . . . . +135°C  
 Storage Temperature Range . . . . . -65°C to +150°C  
 Voltage on Pins . . . . . -0.3V to  $V_{DD}+0.3V$   
 Lead Temperature (soldering, 10s) . . . . . 300°C  
 ESD Min Other Pins (HBM) . . . . . >2kV  
 ESD DDC1 and DDC2 Pins (HBM) . . . . . >8kV

**Recommended Operating Conditions**

Temperature . . . . . -40°C to +85°C  
 Supply Voltage . . . . . 2.7V to 5.5V

*CAUTION: Absolute Maximum Ratings indicate limits beyond which permanent damage to the device and impaired reliability may occur. These are stress ratings provided for information only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied.*

*For guaranteed specifications and test conditions, see Electrical Specifications. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.*

**Electrical Specifications** Over all operating conditions unless otherwise specified, Typical values are measured at  $V_{DD} = 3.3V$  and  $T_A = +25^\circ C$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG PARAMETERS</b>						
$V_{DD}$	Supply Voltage Range		2.7		5.5	V
$V_{DD\ RAMP}$	$V_{DD}$ Ramp Rate		0.05		50	V/ms
$I_{DD}$	Supply Current	DDC1 = DDC2 = Open		80	100	$\mu A$
$I_{OUT\_SB}$	Standby Pull-Up Current	DDC1 = DDC2 = $V_{DD} - 1.0V$		80	125	$\mu A$
$I_{OUT\_A1}$	Active Pull-Up Current	DDC1 = GND; DDC2 = Open	125	275	350	$\mu A$
$I_{OUT\_A2}$		DDC1 = Open; DDC2 = GND	125	275	350	$\mu A$
$I_{OUT\_B1}$	Boost Pull-Up Current (Figure 2)	$V_{TRIPL} < DDC1 < V_{TRIPH}$ , DDC2 = Open	1.6	2.2		mA
$I_{OUT\_B2}$		$V_{TRIPL} < DDC2 < V_{TRIPH}$ , DDC1 = Open	1.6	2.2		mA
$V_{TRIPL}$	Input Voltage Threshold Low		0.65	0.75	0.85	V
$V_{TRIPH}$	Input Voltage Threshold High		$V_{DD} - 0.60$	$V_{DD} - 0.50$	$V_{DD} - 0.40$	V
$f_{MAX}$	DDC Max Frequency				100	kHz
NSS	Noise Spike Suppression (Note Figure 1) (Figure 10)			20		V-ns

NOTES:

1. Measured as area under triangular waveform above  $V_{TRIPL}$ , with time as base and  $V_{IN}$  as height (See Figure 10).

Typical Performance Curves

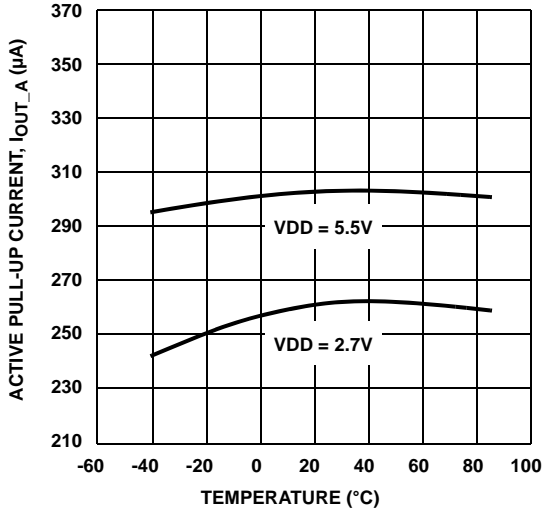


FIGURE 1. ACTIVE PULL-UP CURRENT, DDC PIN = 0V

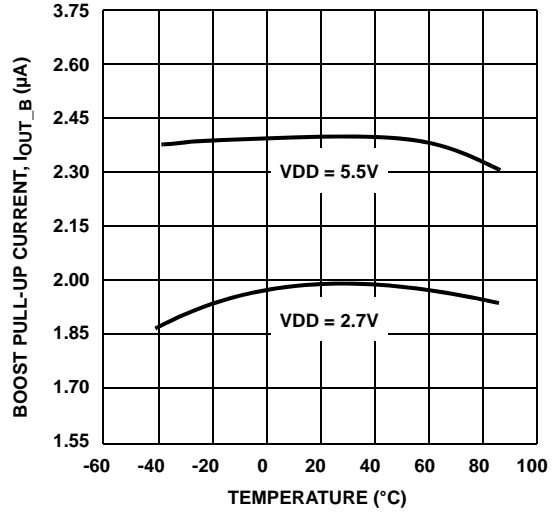


FIGURE 2. BOOST PULL-UP CURRENT, DDC PIN = VDD/2

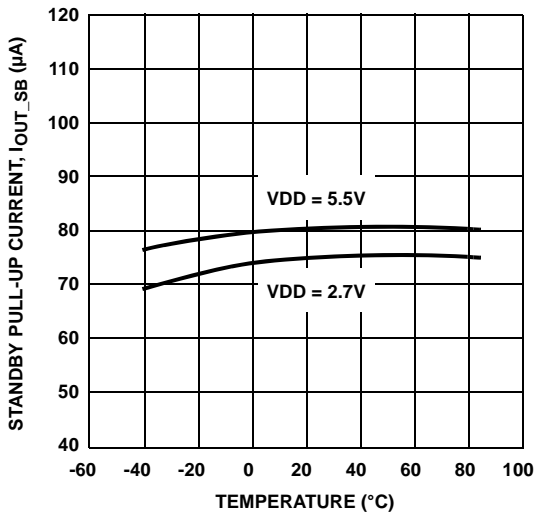


FIGURE 3. STANDBY PULL-UP CURRENT, DDC1, 2 = VDD - 0.5V

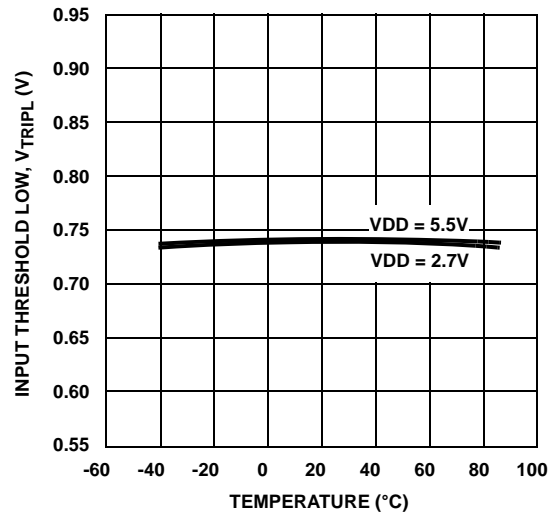


FIGURE 4. VTRIPL VOLTAGE

## Typical Performance Curves (Continued)

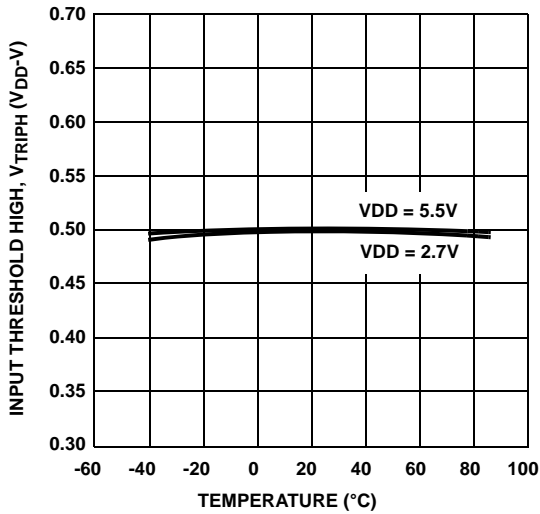


FIGURE 5. V<sub>TRIPHI</sub> VOLTAGE

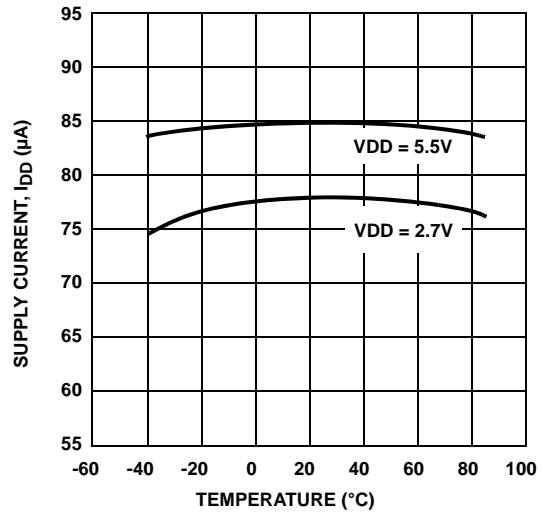


FIGURE 6. I<sub>DD</sub> CURRENT, DDC1 = DDC2 = OPEN

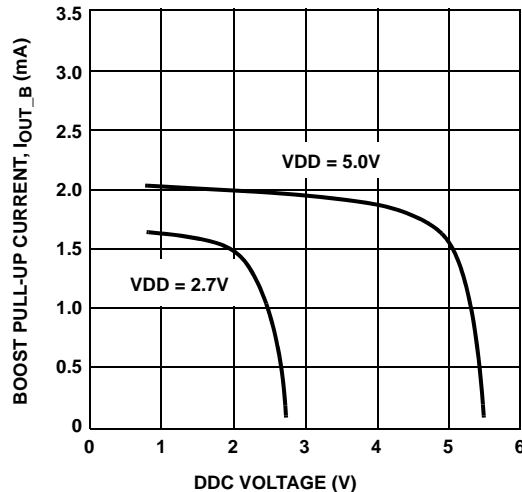


FIGURE 7. BOOST PULL-UP CURRENT vs DDC VOLTAGE

## Functional Description

### DDC Overview

DDC is a 2-wire serial communication standard based on the I<sup>2</sup>C standard. Devices communicate to each other using one clock (SCL) and one data (SDA) line. These are both bidirectional.

Each signal is connected to a positive supply voltage via a current-source or pull-up resistor (see "System Diagram" on page 2). When the bus is free, both lines are HIGH. The output stages of all devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function.

Simple pull-up resistors on the clock and data lines work well unless there are long signal lines. The combined capacitance of long cables increases the rise time on the signal to such an extent that the communication becomes unreliable or fails to meet the bus timing specifications. Smaller value resistors can sometimes compensate for the extra capacitance, but this increases the current consumption when the signal lines are pulled LOW.

### ISL54103 Operation

To improve the operation of the DDC where larger bus capacitance exists, the ISL54103 provides active pull-up using switched current sources. When the bus is idle and both lines are HIGH, a standby pull-up current of 100µA is used to maintain the signal level while minimizing power

consumption. When either of the two signals is pulled LOW, an active pull-up current of 275 $\mu$ A maintains a good  $V_{OL}$  noise margin.

When the bus line is released, it is pulled high by the ISL54103 active current until the voltage exceeds the  $V_{TRIPH}$  level for a period of time. This voltage-time combination filters out noise on the signal line. Once the ISL54103 detects a valid rising edge, a 2.2mA boost current pulls the bus line high very quickly (see Figure 8). This boost current turns off when the input level reaches the  $V_{TRIPH}$  threshold and the pull-up current returns to the active level. If both inputs are HIGH, the pull-up current drops to the standby level of 100 $\mu$ A.

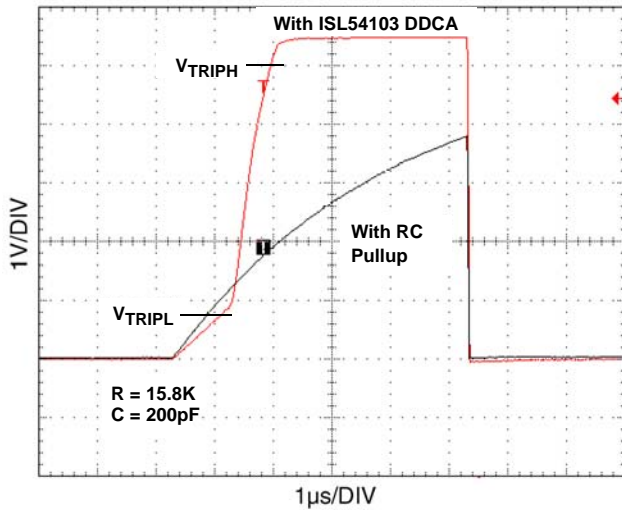


FIGURE 8. ISL54103 DDC SYSTEM BOOST PULL-UP COMPARED TO RESISTOR PULL-UP ( $V_{DD} = 5.5V$ )

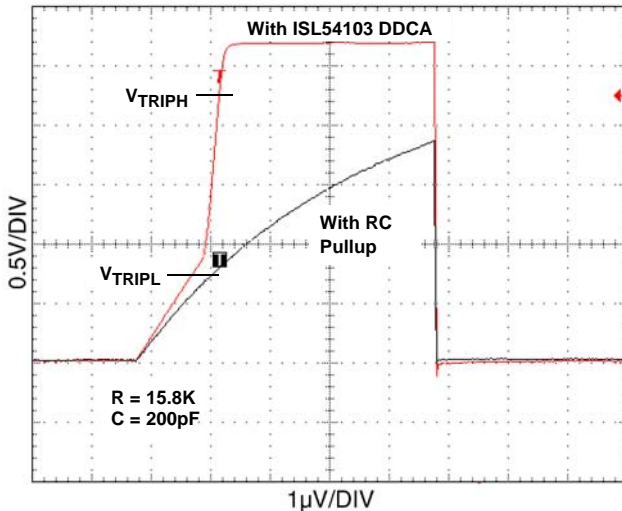


FIGURE 9. ISL54103 DDC SYSTEM BOOST PULL-UP COMPARED TO RESISTOR PULL-UP ( $V_{DD} = 2.7V$ )

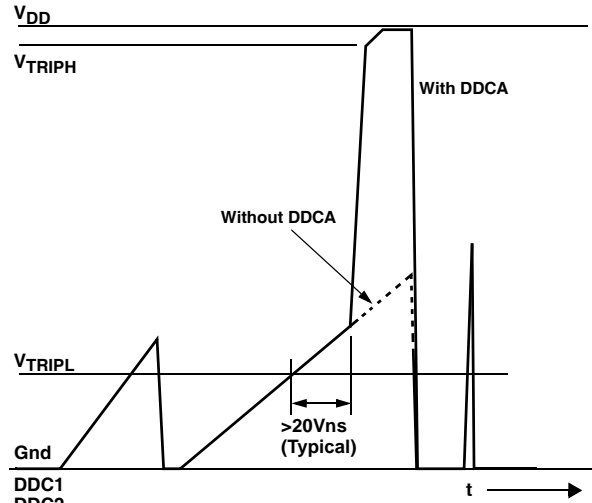
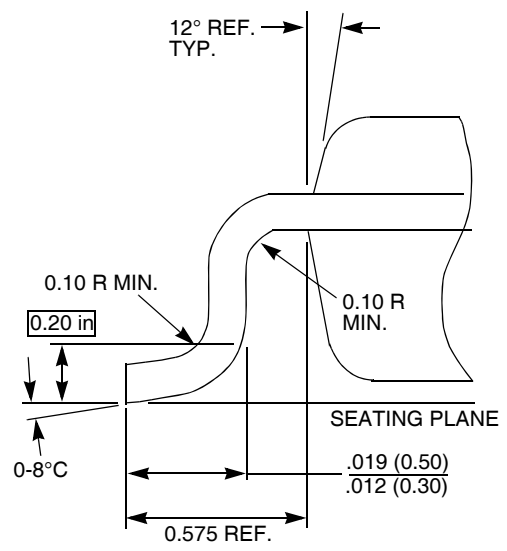
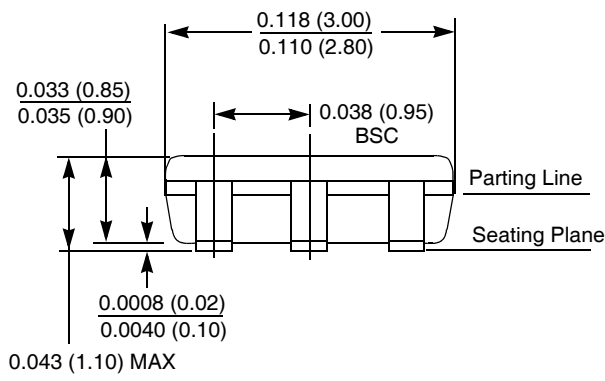
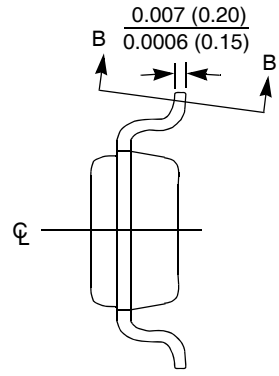
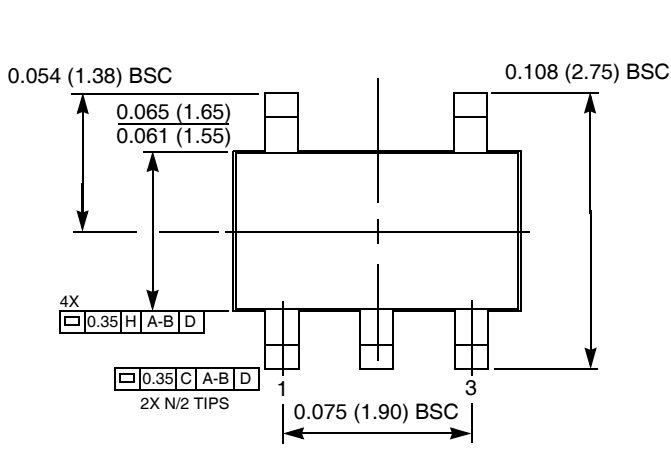


FIGURE 10. NOISE SUPPRESSION. BOOST CURRENT APPLIED WHEN INPUT SIGNAL EXCEEDS 20Vns (TYPICAL)

Package Outline Drawing

5-Lead, SOT23, Package Code H5



- NOTES:**
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
  2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH
  3. DIMENSIONING AND TOLERANCES PER ASME, Y14.5-1994
  4. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193.
  5. THIS PART IS FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74

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