



# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

## General Description

The MAX9174/MAX9175 are 670MHz, low-jitter, low-skew 1:2 splitters ideal for protection switching, loopback, and clock and signal distribution. The devices feature ultra-low 1.0ps(RMS) random jitter (max) that ensures reliable operation in high-speed links that are highly sensitive to timing errors.

The MAX9174 has a fail-safe LVDS input and LVDS outputs. The MAX9175 has an anything differential input (CML/LVDS/LVPECL) and LVDS outputs. The outputs can be put into high impedance using the power-down inputs. The MAX9174 features a fail-safe circuit that drives the outputs high when the input is open, undriven and shorted, or undriven and terminated. The MAX9175 has a bias circuit that forces the outputs high when the input is open. The power-down inputs are compatible with standard LVTTL/LVCMOS logic. The power-down inputs tolerate undershoot of -1V and overshoot of  $V_{CC} + 1V$ . The MAX9174/MAX9175 are available in 10-pin  $\mu$ MAX and 10-lead thin QFN with exposed pad packages, and operate from a single +3.3V supply over the -40°C to +85°C temperature range.

## Applications

Protection Switching  
Loopback  
Clock Distribution

**Functional Diagram and Pin Configurations appear at end of data sheet.**

## Features

- ◆ 1.0ps(RMS) Jitter (max) at 670MHz
- ◆ 80ps(p-p) Jitter (max) at 800Mbps Data Rate
- ◆ +3.3V Supply
- ◆ LVDS Fail-Safe Inputs (MAX9174)
- ◆ Anything Input (MAX9175) Accepts Differential CML/LVDS/LVPECL
- ◆ Power-Down Inputs Tolerate -1.0V and  $V_{CC} + 1.0V$
- ◆ Low-Power CMOS Design
- ◆ 10-Lead  $\mu$ MAX and Thin QFN Packages
- ◆ -40°C to +85°C Operating Temperature Range
- ◆ Conform to ANSI TIA/EIA-644 LVDS Standard
- ◆ IEC 61000-4-2 Level 4 ESD Rating

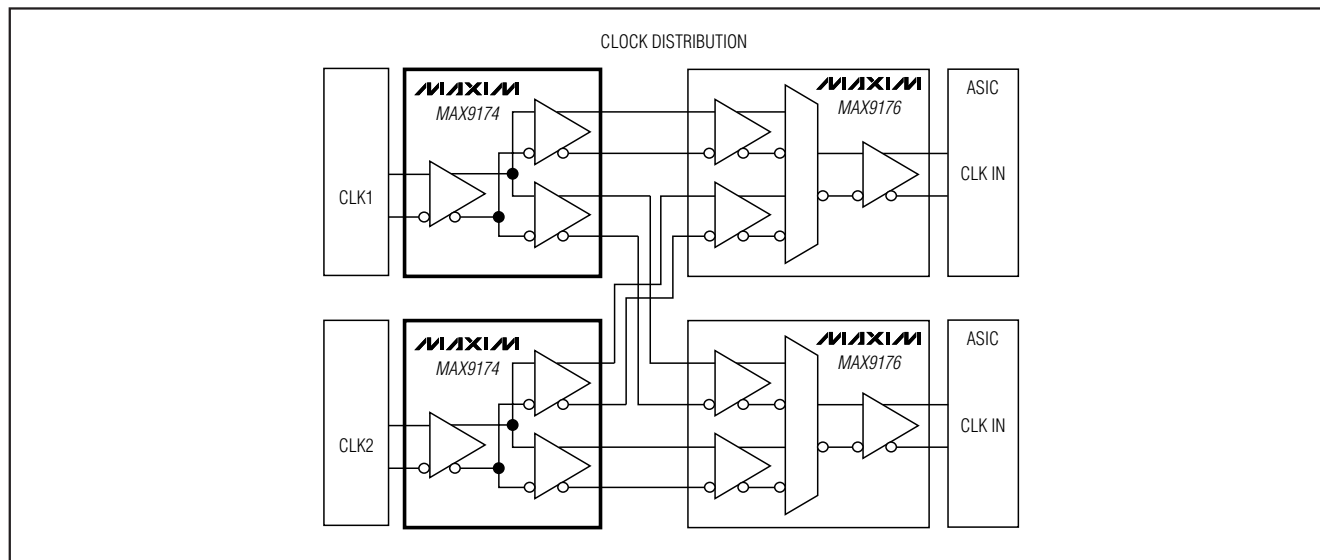
## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9174EUB	-40°C to +85°C	10 $\mu$ MAX
MAX9174ETB*	-40°C to +85°C	10 Thin QFN-EP**
MAX9175EUB	-40°C to +85°C	10 $\mu$ MAX
MAX9175ETB*	-40°C to +85°C	10 Thin QFN-EP**

\*Future product—contact factory for availability.

\*\*EP = Exposed paddle.

## Typical Application Circuit



Maxim Integrated Products 1

**For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).**

MAX9174/MAX9175

# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$  to GND ..... -0.3V to +4.0V  
 $IN+$ ,  $IN-$  to GND ..... -0.3V to +4.0V  
 $OUT_+$ ,  $OUT_-$  to GND ..... -0.3V to +4.0V  
 $PD0$ ,  $PD1$  to GND ..... -1.4V to  $(V_{CC} + 1.4V)$   
 Single-Ended and Differential Output  
 Short-Circuit Duration ( $OUT_+$ ,  $OUT_-$ ) ..... Continuous  
 Continuous Power Dissipation ( $T_A = +70^\circ C$ )  
     10-Pin  $\mu MAX$  (derate 5.6mW/ $^\circ C$  above  $+70^\circ C$ ) ..... 444mW  
     10-Lead QFN (derate 24.4mW/ $^\circ C$  above  $+70^\circ C$ ) ..... 1951mW  
 Maximum Junction Temperature .....  $+150^\circ C$

Storage Temperature Range .....  $-65^\circ C$  to  $+150^\circ C$   
 ESD Protection  
     Human Body Model ( $R_D = 1.5k\Omega$ ,  $C_S = 100pF$ )  
      $IN+$ ,  $IN-$ ,  $OUT_+$ ,  $OUT_-$  .....  $\pm 2kV$   
     Other Pins ( $V_{CC}$ ,  $PD0$ ,  $PD1$ ) .....  $\pm 2kV$   
     IEC 61000-4-2 Level 4 ( $R_D = 330\Omega$ ,  $C_S = 150pF$ )  
     Contact Discharge  $IN+$ ,  $IN-$ ,  $OUT_+$ ,  $OUT_-$  .....  $\pm 8kV$   
     Air-Gap Discharge  $IN+$ ,  $IN-$ ,  $OUT_+$ ,  $OUT_-$  .....  $\pm 15kV$   
     Lead Temperature (soldering, 10s) .....  $+300^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $\overline{PD_-}$  = high, differential input voltage  $|V_{ID}| = 0.05V$  to  $1.2V$ , MAX9174 input common-mode voltage  $V_{CM} = |V_{ID}|/2$  to  $(2.4V - |V_{ID}|/2)$ , MAX9175 input common-mode voltage  $V_{CM} = |V_{ID}|/2$  to  $(V_{CC} - |V_{ID}|/2)$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = +1.25V$ ,  $T_A = +25^\circ C$ .) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIFFERENTIAL INPUT (IN+, IN-)							
Differential Input High Threshold	VTH					+50	mV
Differential Input Low Threshold	VTL			-50			mV
Input Current	IIN+, IIN-	Figure 1		-20		+20	μA
Power-Off Input Current	IIN+, IIN-	MAX9174	VCC = 0V or open, Figure 1	-20		+20	μA
		MAX9175	VIN+ = 3.6V or 0V, VIN- = 3.6V or 0V, VCC = 0V or open, Figure 1				
Fail-Safe Input Resistors (MAX9174)	RIN1	VCC = 3.6V, 0V or open, Figure 1		60		108	kΩ
	RIN2			200		394	
Input Resistors (MAX9175)	RIN3	VCC = 3.6V, 0V or open, Figure 1		212		450	kΩ
Input Capacitance	CIN	IN+ or IN- to GND (Note 4)				4.5	pF
LVTTTL/LVCMOS INPUTS (PD0, PD1)							
Input High Voltage	VIH			2.0		VCC + 1	V
Input Low Voltage	VIL			-1.0		+0.8	V
Input Current	IIN	-1.0V ≤ PD <sub>−</sub> ≤ 0V		-1.5			mA
		0V ≤ PD <sub>−</sub> ≤ VCC		-20		+20	μA
		VCC ≤ PD <sub>−</sub> ≤ VCC + 1.0V				+1.5	mA
LVDS OUTPUTS (OUT_+, OUT_-)							
Differential Output Voltage	VOD	Figure 2		250	393	475	mV
Change in Differential Output Voltage Between Logic States	ΔVOD	Figure 2			1.0	15	mV
Offset Voltage	VOS	Figure 3		1.125	1.29	1.375	V

# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

MAX9174/MAX9175

## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $\overline{PD}_-$  = high, differential input voltage  $|V_{ID}| = 0.05V$  to  $1.2V$ , MAX9174 input common-mode voltage  $V_{CM} = |V_{ID}|/2$  to  $(2.4V - |V_{ID}|/2)$ , MAX9175 input common-mode voltage  $V_{CM} = |V_{ID}|/2$  to  $(V_{CC} - |V_{ID}|/2)$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = +1.25V$ ,  $T_A = +25^\circ C$ .) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Change in Offset Voltage Between Logic States	$\Delta V_{OS}$	Figure 3		1.0	15	mV
Fail-Safe Differential Output Voltage (MAX9174)	$V_{OD}$	Figure 2	250	393	475	mV
Differential Output Resistance	$R_{DIFF}$	$V_{CC} = 3.6V$ or $0V$	86	119	160	$\Omega$
Power-Down Single-Ended Output Current	$I_{PD}$	$\overline{PD}_- = \text{low}$ $V_{OUT\_+} = \text{open}, V_{OUT\_+} = 3.6V$ or $0V$ $V_{OUT\_+} = \text{open}, V_{OUT\_+} = 3.6V$ or $0V$	-1.0	$\pm 0.03$	+1.0	$\mu A$
Power-Off Single-Ended Output Current	$I_{OFF}$	$\overline{PD0}, \overline{PD1} = \text{low}, V_{CC} = 0V$ or open $V_{OUT\_+} = \text{open}, V_{OUT\_+} = 3.6V$ or $0V$ $V_{OUT\_+} = \text{open}, V_{OUT\_+} = 3.6V$ or $0V$	-1.0	$\pm 0.03$	+1.0	$\mu A$
Output Short-Circuit Current	$I_{OS}$	$V_{ID} = +50mV$ or $-50mV$ , $V_{OUT\_+} = 0V$ or $V_{CC}$ $V_{ID} = +50mV$ or $-50mV$ , $V_{OUT\_+} = 0V$ or $V_{CC}$	-15		+15	mA
Differential Output Short-Circuit Current Magnitude	$ I_{OSD} $	$V_{ID} = +50mV$ or $-50mV$ , $V_{OD} = 0V$ (Note 4)			15	mA
Supply Current	$I_{CC}$	$\overline{PD0} = V_{CC}, \overline{PD1} = 0V$ or $\overline{PD0} = 0V, \overline{PD1} = V_{CC}$ $\overline{PD0} = V_{CC}, \overline{PD1} = V_{CC}$		17 25	26 35	mA
Power-Down Supply Current	$I_{CCPD}$	$\overline{PD1}, \overline{PD0} = 0V$		0.5	20	$\mu A$
Output Capacitance	$C_O$	$OUT\_+$ or $OUT_-$ to GND (Note 4)			5.2	pF

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## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $C_L = 5pF$ , differential input voltage  $|V_{ID}| = 0.15V$  to  $1.2V$ , MAX9174 input common-mode voltage,  $V_{CM} = |V_{ID}|/2$  to  $(2.4V - |V_{ID}|/2)$ , MAX9175 input common-mode voltage  $V_{CM} = |V_{ID}|/2$  to  $(V_{CC} - |V_{ID}|/2)$ ,  $\overline{PD}_- = \text{high}$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = +1.25V$ ,  $T_A = +25^\circ C$ .) (Notes 5, 6, 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-to-Low Propagation Delay	$t_{PHL}$	Figures 4, 5	1.33	2.38	3.23	ns
Low-to-High Propagation Delay	$t_{PLH}$	Figures 4, 5	1.33	2.39	3.23	ns
Added Deterministic Jitter	$t_{DJ}$	Figures 4, 5 (Note 8)			80	ps(P-P)
Added Random Jitter	$t_{RJ}$	Figures 4, 5			1.0	ps(RMS)
Pulse Skew $ t_{PLH} - t_{PHL} $	$t_{SKP}$	Figures 4, 5		10	141	ps
Output-to-Output Skew	$t_{SKOO}$	Figure 6		14	45	ps
Part-to-Part Skew	$t_{SKPP1}$	Figures 4, 5 (Note 9)		0.4	1.3	ns
	$t_{SKPP2}$	Figures 4, 5 (Note 10)			1.9	
Rise Time	$t_R$	Figures 4, 5	110	257	365	ps
Fall Time	$t_F$	Figures 4, 5	110	252	365	ps
Power-Down Time	$t_{PD}$	Figures 7, 8		10	13	ns
Power-Up Time	$t_{PU}$	$\overline{PD0}, \overline{PD1} = L \rightarrow H$ , Figures 7, 8		18	35	$\mu s$
		$\overline{PD0} = H, \overline{PD1} = L \rightarrow H$ , Figures 7, 8		92	103	ns
		$\overline{PD1} = H, \overline{PD0} L \rightarrow H$ , Figures 7, 8		92	103	
Maximum Data Rate	$D_{RMAX}$	Figures 4, 5, $ V_{OD}  \geq 250mV$ (Note 11)	800			Mbps
Maximum Switching Frequency	$f_{MAX}$	Figures 4, 5, $ V_{OD}  \geq 250mV$ (Note 11)	670			MHz
Switching Supply Current	$I_{CCSW}$	$f_{IN} = 670MHz$		55	65	mA
		$f_{IN} = 155MHz$		35	44	
PRBS Supply Current	$I_{CCPR}$	$D_R = 800Mbps$ , $2^{23} - 1$ PRBS input		37	46	mA

**Note 1:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except  $V_{TH}$ ,  $V_{TL}$ ,  $V_{ID}$ ,  $V_{OD}$ , and  $\Delta V_{OD}$ .

**Note 2:** Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at  $T_A = +25^\circ C$ .

**Note 3:** Tolerance on all external resistors (including figures) is  $\pm 1\%$ .

**Note 4:** Guaranteed by design.

**Note 5:** AC parameters are guaranteed by design and characterization and are not production tested. Limits are set at  $\pm 6$  sigma.

**Note 6:**  $C_L$  includes scope probe and test jig capacitance.

**Note 7:** Pulse-generator output for differential inputs  $IN+$ ,  $IN-$  (unless otherwise noted):  $f = 670MHz$ , 50% duty cycle,  $R_O = 50\Omega$ ,  $t_R = 700ps$ , and  $t_F = 700ps$  (0% to 100%). Pulse-generator output for single-ended inputs  $\overline{PD0}$ ,  $\overline{PD1}$ :  $t_R = t_F = 1.5ns$  ( $0.2V_{CC}$  to  $0.8V_{CC}$ ), 50% duty cycle,  $V_{OH} = V_{CC} + 1.0V$  settling to  $V_{CC}$ ,  $V_{OL} = -1.0V$  settling to zero,  $f = 10kHz$ .

**Note 8:** Pulse-generator output for  $t_{DJ}$ :  $|V_{OD}| = 0.15V$ ,  $V_{OS} = 1.25V$ , data rate 800Mbps,  $2^{23} - 1$  PRBS,  $R_O = 50\Omega$ ,  $t_R = 700ps$ , and  $t_F = 700ps$  (0% to 100%).

**Note 9:**  $t_{SKPP1}$  is the magnitude of the difference of any differential propagation delays between devices operating under identical conditions.

**Note 10:**  $t_{SKPP2}$  is the magnitude of the difference of any differential propagation delays between devices operating over rated conditions.

**Note 11:** Meets all AC specifications.

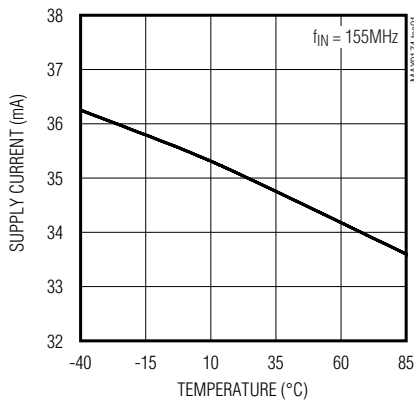
# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

## Typical Operating Characteristics

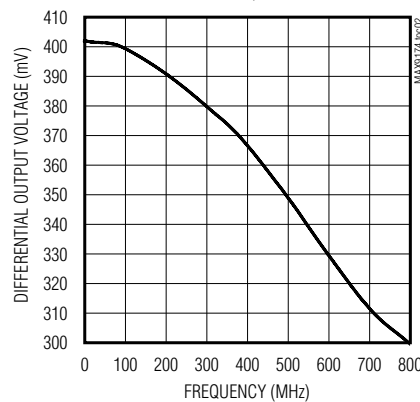
((MAX9174)  $V_{CC} = +3.3V$ ,  $|V_{ID}| = 0.15V$ ,  $V_{CM} = 1.25V$ ,  $T_A = +25^\circ C$ ,  $R_L = 100\Omega \pm 1\%$ ,  $C_L = 5pF$ ,  $\overline{PD}_- = V_{CC}$ , unless otherwise noted.)

MAX9174/MAX9175

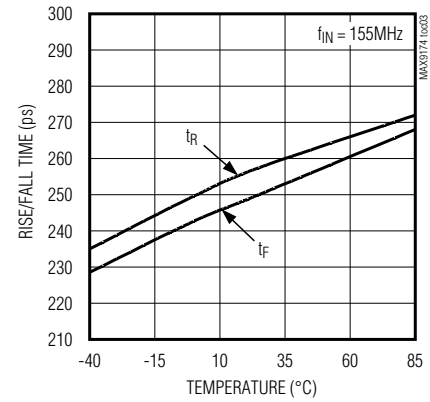
**SUPPLY CURRENT vs. TEMPERATURE**



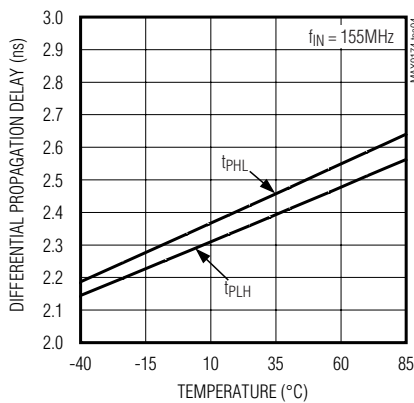
**DIFFERENTIAL OUTPUT VOLTAGE vs. FREQUENCY**



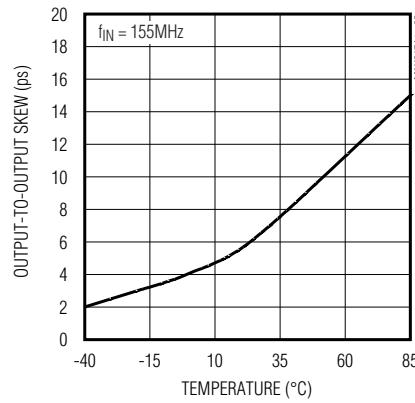
**OUTPUT RISE/FALL TIME vs. TEMPERATURE**



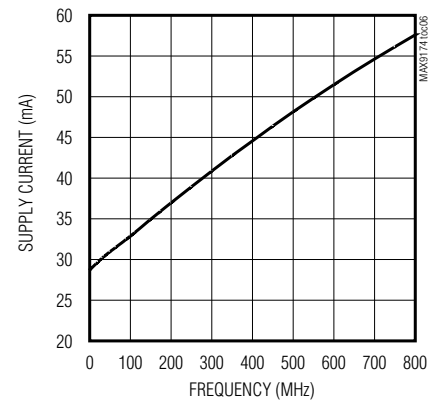
**DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE**



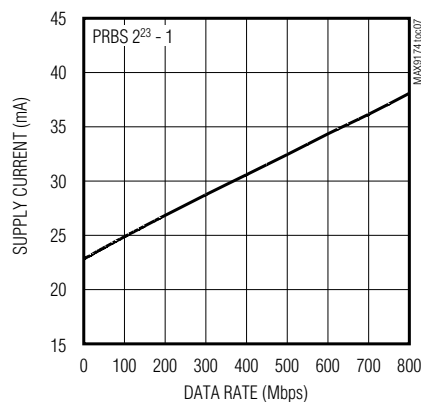
**OUTPUT-TO-OUTPUT SKEW vs. TEMPERATURE**



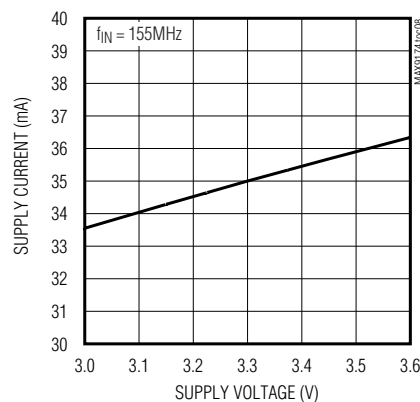
**SUPPLY CURRENT vs. FREQUENCY**



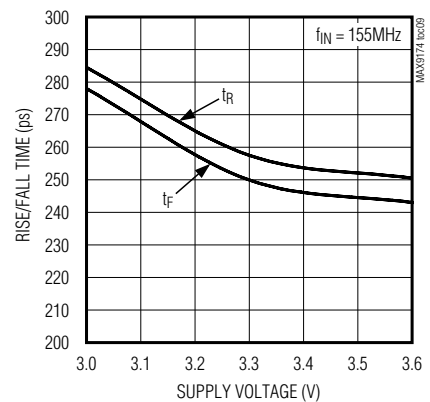
**SUPPLY CURRENT vs. DATA RATE**



**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



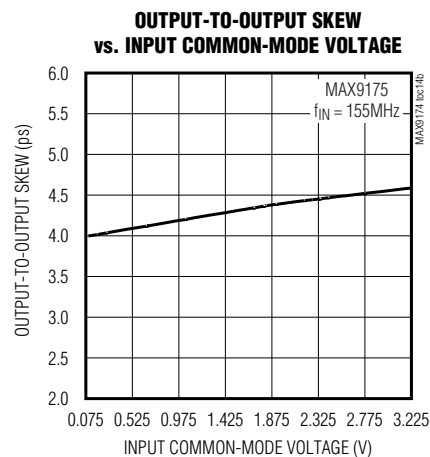
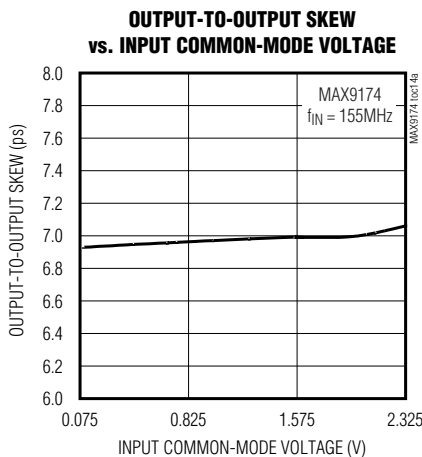
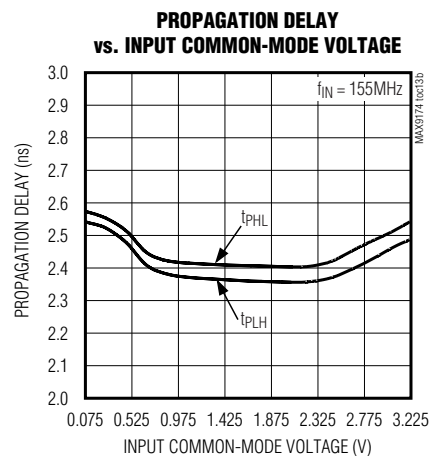
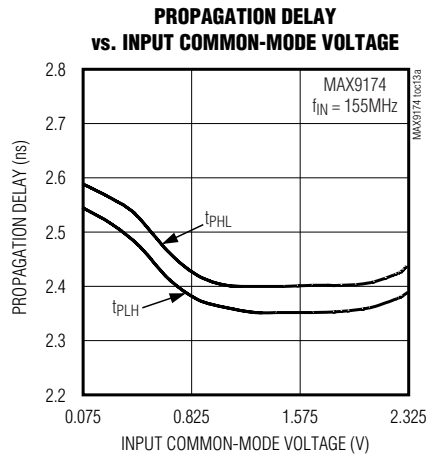
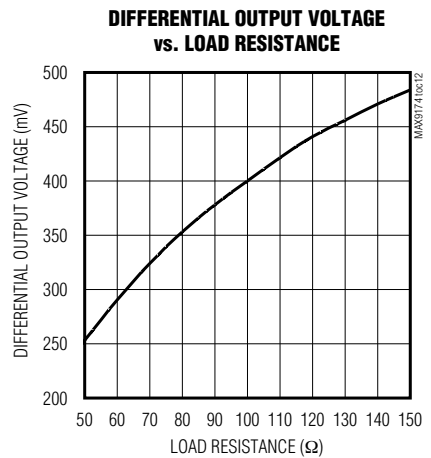
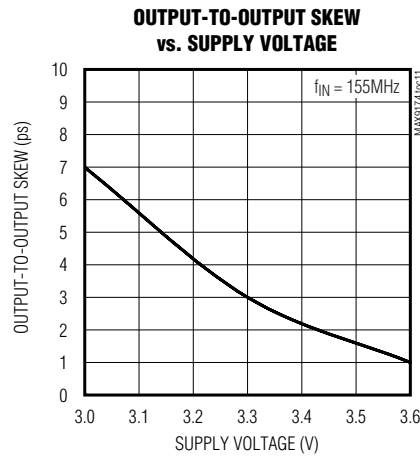
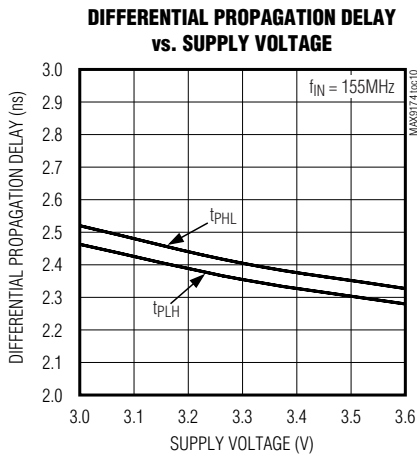
**OUTPUT RISE/FALL TIME vs. SUPPLY VOLTAGE**



# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

## Typical Operating Characteristics (continued)

((MAX9174)  $V_{CC} = +3.3V$ ,  $|V_{ID}| = 0.15V$ ,  $V_{CM} = 1.25V$ ,  $T_A = +25^\circ C$ ,  $R_L = 100\Omega \pm 1\%$ ,  $C_L = 5pF$ ,  $\overline{PD}_- = V_{CC}$ , unless otherwise noted.)



# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

## Pin Description

PIN		NAME	FUNCTION
μMAX	QFN		
1	1	IN+	Noninverting Differential Input
2	2	IN-	Inverting Differential Input
3	3	GND	Ground
4	4	$\overline{\text{PD1}}$	LVTTL/LVCMOS Input. OUT1+, OUT1- are high impedance to ground when $\overline{\text{PD1}}$ is low. Internal pulldown resistor to GND.
5	5	$\overline{\text{PD0}}$	LVTTL/LVCMOS Input. OUT0+, OUT0- are high impedance to ground when $\overline{\text{PD0}}$ is low. Internal pulldown resistor to GND.
6	6	OUT0-	Inverting LVDS Output 0
7	7	OUT0+	Noninverting LVDS Output 0
8	8	VCC	Power Supply
9	9	OUT1-	Inverting LVDS Output 1
10	10	OUT1+	Noninverting LVDS Output 1
—	EP	Exposed Pad	Exposed Pad. Solder to ground.

MAX9174/MAX9175

## Detailed Description

The MAX9174/MAX9175 are 670MHz, low-jitter, low-skew 1:2 splitters ideal for protection switching, loop-back, and clock and signal distribution. The devices feature ultra-low 80ps<sub>p-p</sub> deterministic jitter (max) that ensures reliable operation in high-speed links that are highly sensitive to timing error.

The MAX9174 has a fail-safe LVDS input and LVDS outputs. The MAX9175 has an anything differential input (CML/LVDS/LVPECL) and LVDS outputs. The outputs can be put into high impedance using the power-down inputs. The MAX9174 features a fail-safe circuit that drives the outputs high when the input is open, undriven and shorted, or undriven and terminated. The MAX9175 has a bias circuit that forces the outputs high when the input is open. The power-down inputs are compatible with standard LVTTL/LVCMOS logic.

The power-down inputs tolerate undershoot of -1V and overshoot of VCC + 1V. The MAX9174/MAX9175 are available in 10-pin μMAX and 10-lead thin QFN packages, and operate from a single +3.3V supply over the -40°C to +85°C temperature range.

### Current-Mode LVDS Outputs

The LVDS outputs use a current-steering configuration. This approach results in less ground bounce and less output ringing, enhancing noise margin and system speed performance.

A differential output voltage is produced by steering current through the parallel combination of the integrated differential output resistor and transmission line impedance/termination resistor. When driving a 100Ω termination resistor, a differential voltage of 250mV to 475mV is produced. For loads greater than 100Ω, the output voltage is larger, and for loads less than 100Ω, the output voltage is smaller. See the Differential Output Voltage vs. Load Resistance curve in *Typical Operating Characteristics* for more information. The outputs are short-circuit current limited for single-ended and differential shorts.

### MAX9174 Input Fail-Safe

The fail-safe feature of the MAX9174 sets the outputs high when the differential input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without a fail-safe circuit, when the input is undriven, noise at the input may switch the outputs and it may appear to the system that data is being sent. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when a driver output is in high impedance. A shorted input can occur because of a cable failure.

# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

When the input is driven with a differential signal of  $|V_{ID}| = 50\text{mV}$  to  $1.2\text{V}$  within a voltage range of  $0$  to  $2.4\text{V}$ , the fail-safe circuit is not activated. If the input is open, undriven and shorted, or undriven and terminated, an internal resistor in the fail-safe circuit pulls the input above  $V_{CC} - 0.3\text{V}$ , activating the fail-safe circuit and forcing the outputs high (Figure 1).

## Overshoot and Undershoot Voltage Protection

The MAX9174/MAX9175 are designed to protect the power-down inputs (PD0 and PD1) against latchup due to transient overshoot and undershoot voltage. If the input voltage goes above  $V_{CC}$  or below  $GND$  by up to  $1\text{V}$ , an internal circuit limits input current to  $1.5\text{mA}$ .

## Applications Information

### Power-Supply Bypassing

Bypass the  $V_{CC}$  pin with high-frequency surface-mount ceramic  $0.1\mu\text{F}$  and  $0.001\mu\text{F}$  capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to  $V_{CC}$ .

### Differential Traces

Input and output trace characteristics affect the performance of the MAX9174/MAX9175. Use controlled-impedance differential traces ( $100\Omega$  typ). To reduce radiated noise and ensure that noise couples as common mode, route the differential input and output signals within a pair close together. Reduce skew by matching the electrical length of the two signal paths that make up the differential pair. Excessive skew can result in a degradation of magnetic field cancellation. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

### Cables and Connectors

Interconnect for LVDS typically has a controlled differential impedance of  $100\Omega$ . Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

### Termination

The MAX9174/MAX9175 require external input and output termination resistors. For LVDS, connect an input

Table 1. Input Function Table

INPUT		OUTPUTS
(IN+) - (IN-)		(OUT+) - (OUT-)
$\geq +50\text{mV}$		H
$\leq -50\text{mV}$		L
$-50\text{mV} < V_{ID} < +50\text{mV}$		Indeterminate
MAX9175	Open	H
MAX9174	Open, undriven short, or undriven parallel termination	

Table 2. Power-Down Function Table

PD1	PD0	OUT+, OUT-
H	H	Both outputs enabled
L or open	L or open	Shutdown to minimum power, outputs high impedance to ground
L or open	High	OUT0 enabled, OUT1 high impedance to ground
High	L or open	OUT1 enabled, OUT0 high impedance to ground

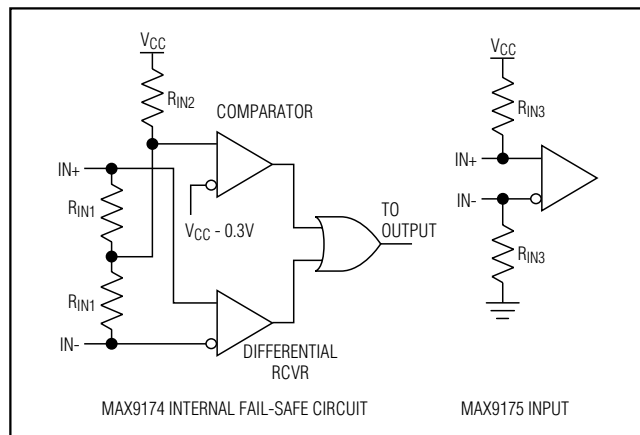


Figure 1. Input Structure

termination resistor across the differential input and at the far end of the interconnect driven by the LVDS outputs. Place the input termination resistor as close to the receiver input as possible. Termination resistors should match the differential impedance of the transmission line. Use 1% surface-mount resistors.



# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

MAX9174/MAX9175

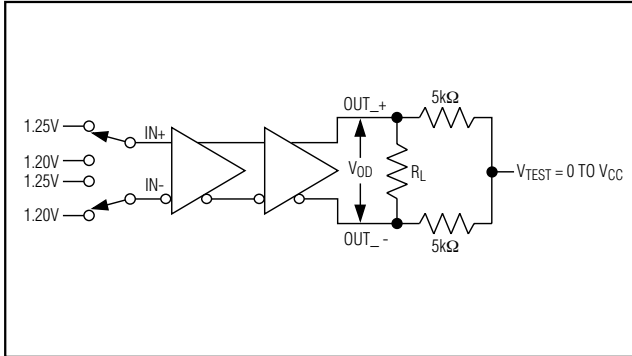


Figure 2.  $V_{OD}$  Test Circuit

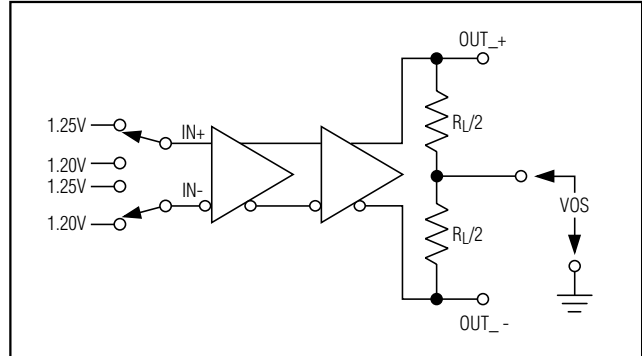


Figure 3.  $V_{OS}$  Test Circuit

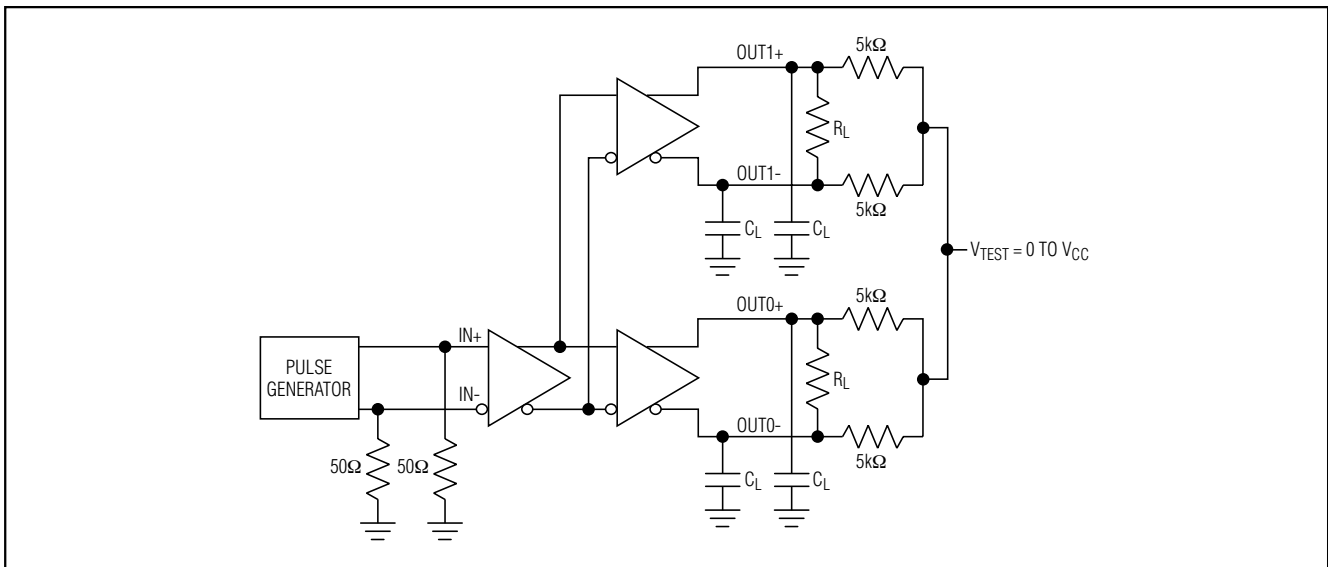


Figure 4. Transition Time, Propagation Delay, and Output-to-Output Skew Test Circuit

The MAX9174/MAX9175 feature an integrated differential output resistor. This resistor reduces jitter by damping reflections produced by a mismatch between the transmission line and termination resistor at the far end of the interconnect.

## Board Layout

Separate the differential and single-ended signals to reduce crosstalk. A four-layer printed circuit board with separate layers for power, ground, differential signals, and single-ended logic signals is recommended. Separate the differential signals from the logic signals with power and ground planes for best results.

## IEC 61000-4-2 Level 4 ESD Protection

The IEC 61000-4-2 standard (Figure 9) specifies ESD tolerance for electronic systems. The IEC 61000-4-2 model specifies a 150pF capacitor that is discharged into the device through a 330Ω resistor. The MAX9174/MAX9175 differential inputs and outputs are rated for IEC 61000-4-2 level 4 ( $\pm 8$ kV Contact Discharge and  $\pm 15$ kV Air-Gap Discharge). The Human Body Model (HBM, Figure 10) specifies a 100pF capacitor that is discharged into the device through a 1.5kΩ resistor. IEC 61000-4-2 level 4 discharges higher peak current and more energy than the HBM due to the lower series resistance and larger capacitor.

# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

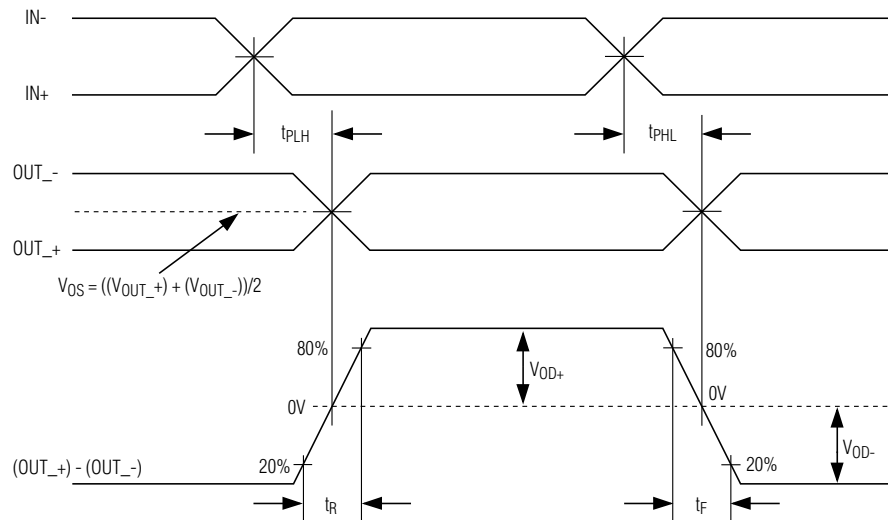


Figure 5. Transition Time and Propagation Delay Timing

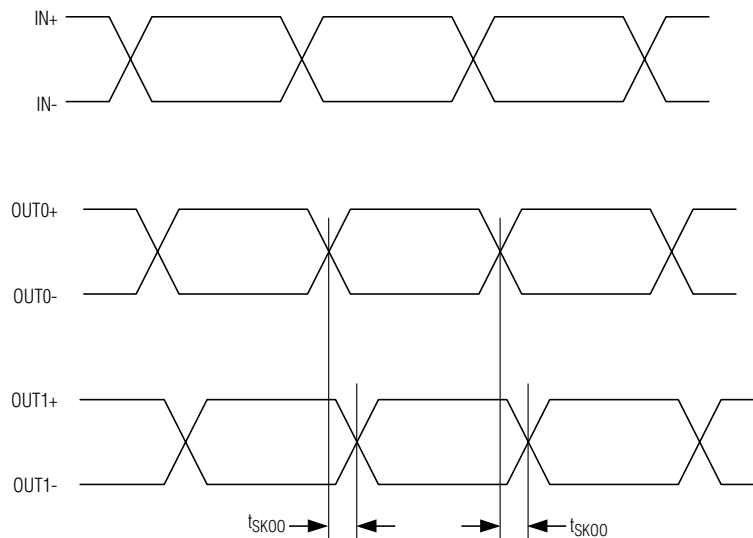


Figure 6. Output-to-Output Skew

# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

**MAX9174/MAX9175**

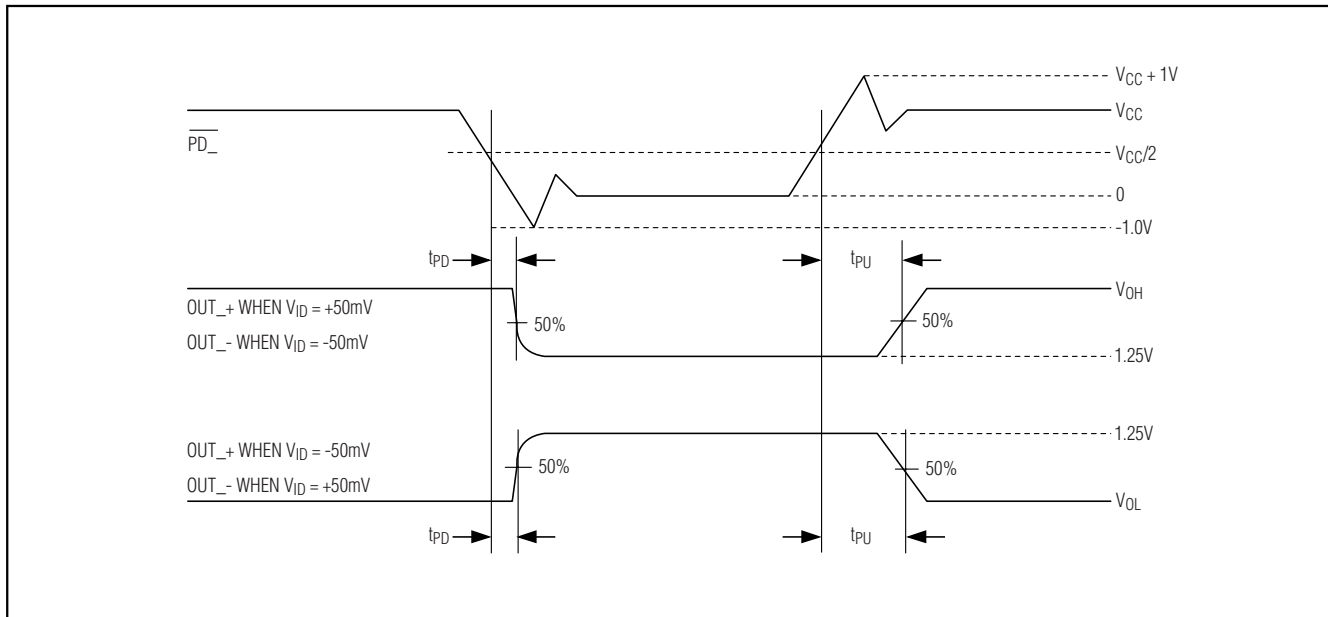


Figure 7. Power-Up/Down Delay Waveform

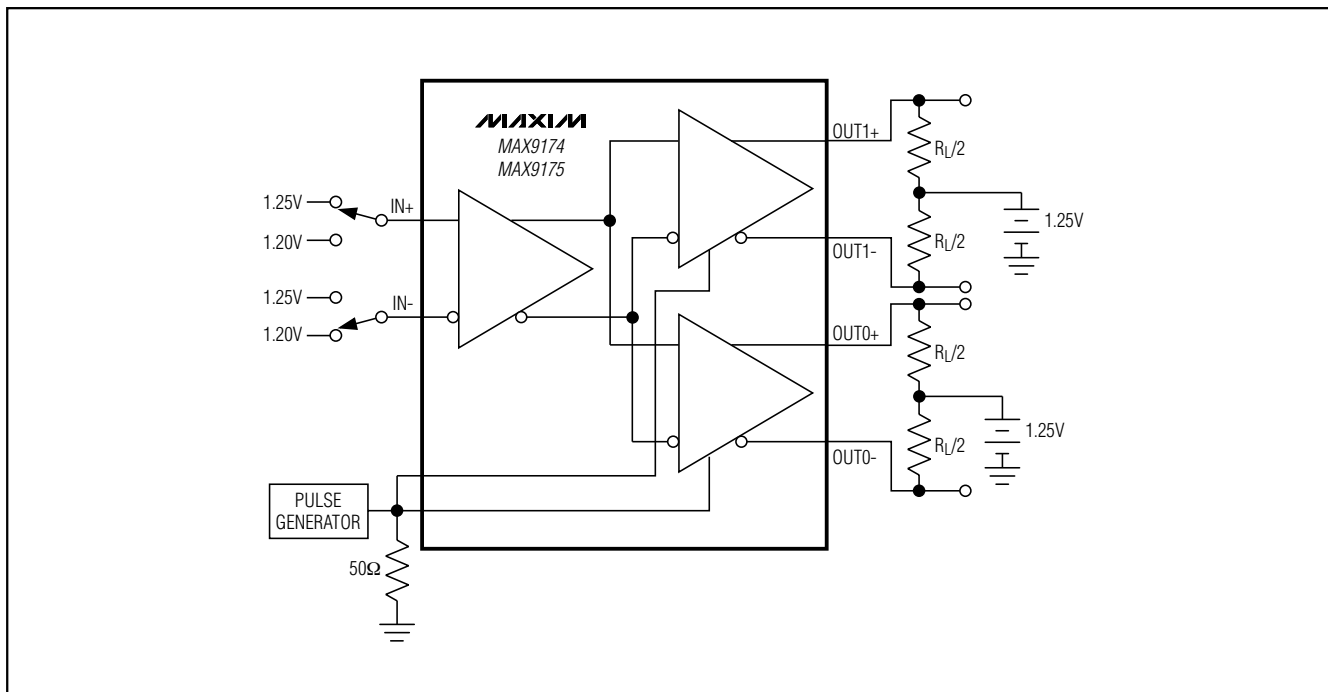


Figure 8. Power-Up/Down Delay Test Circuit

# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

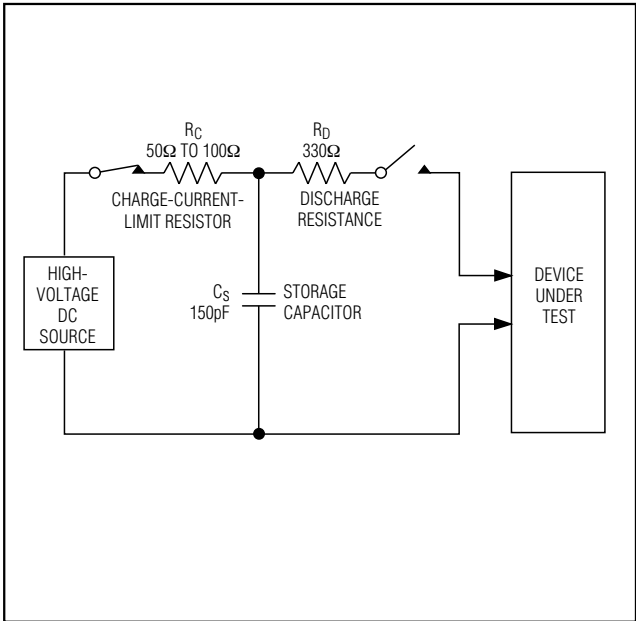


Figure 9. IEC 61000-4-2 Contact Discharge ESD Test Model

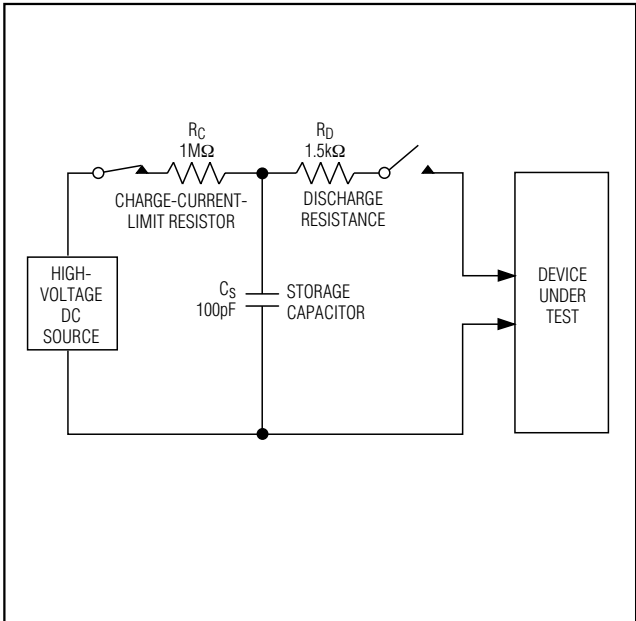
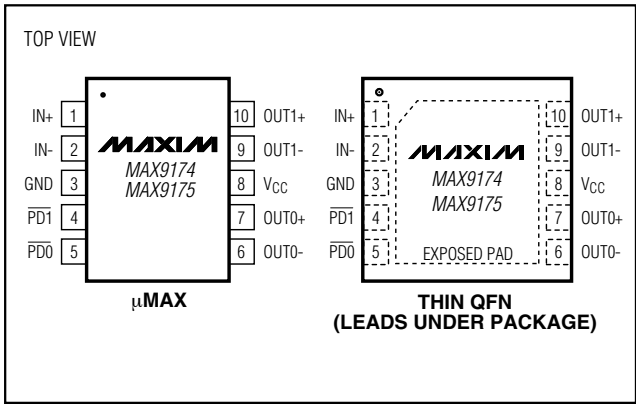
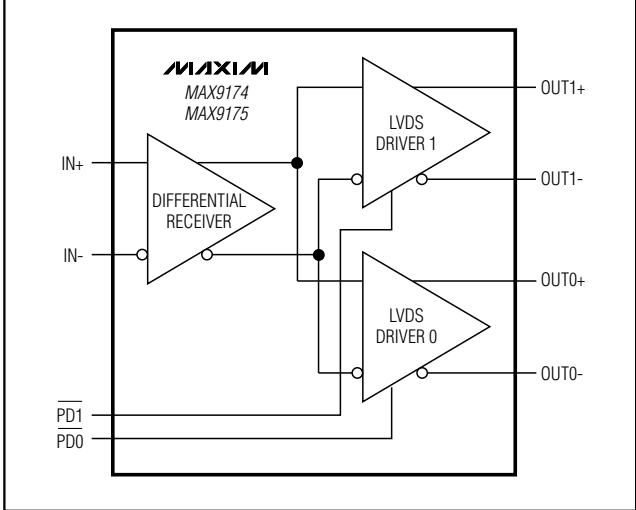


Figure 10. Human Body ESD Test Model

## Pin Configurations



## Functional Diagram



## Chip Information

TRANSISTOR COUNT: 693  
PROCESS: CMOS

**MAX9174/MAX9175**

## 10LUMAX.EPS

The drawing illustrates the mechanical specifications of a 10L uMAX/uSOP package. It includes four views: TOP VIEW, BOTTOM VIEW, FRONT VIEW, and SIDE VIEW. The TOP VIEW shows a rectangular body with 10 pins on each long side, a central square pad with a diameter of  $\varnothing 0.50 \pm 0.1$ , and dimensions for pin pitch (e), pin width (1), and body width (4X S). The FRONT VIEW shows the package height (H), pin height (A), and body width (D1, D2). The SIDE VIEW shows the package profile with dimensions for pin height (A), body height (A1), body width (D1, D2), and pin pitch (e). A table of values provides the minimum and maximum dimensions in inches and millimeters for various parameters.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
$\alpha$	0°	6°	0°	6°

**NOTES:**

- D&E DO NOT INCLUDE MOLD FLASH.
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
- CONTROLLING DIMENSION: MILLIMETERS.
- MEETS JEDEC MO-187C-BA.

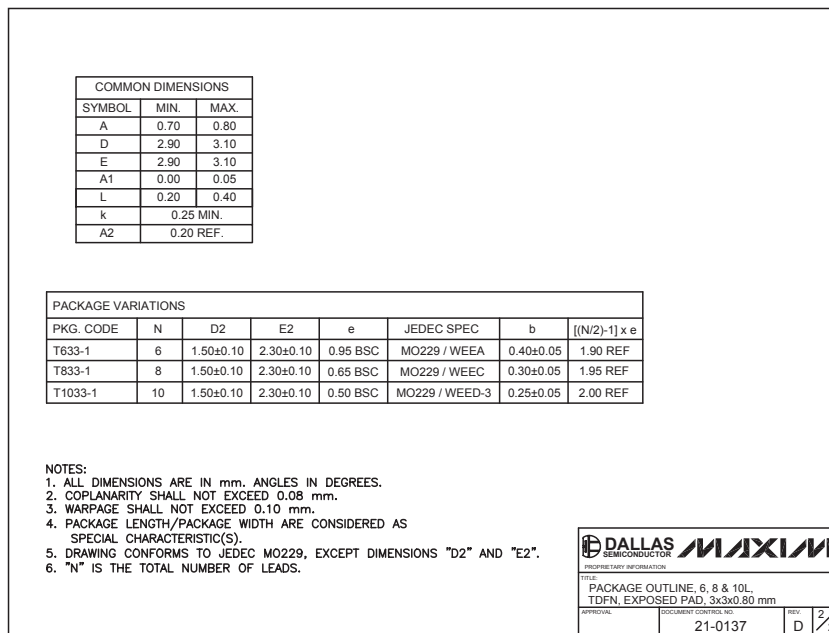
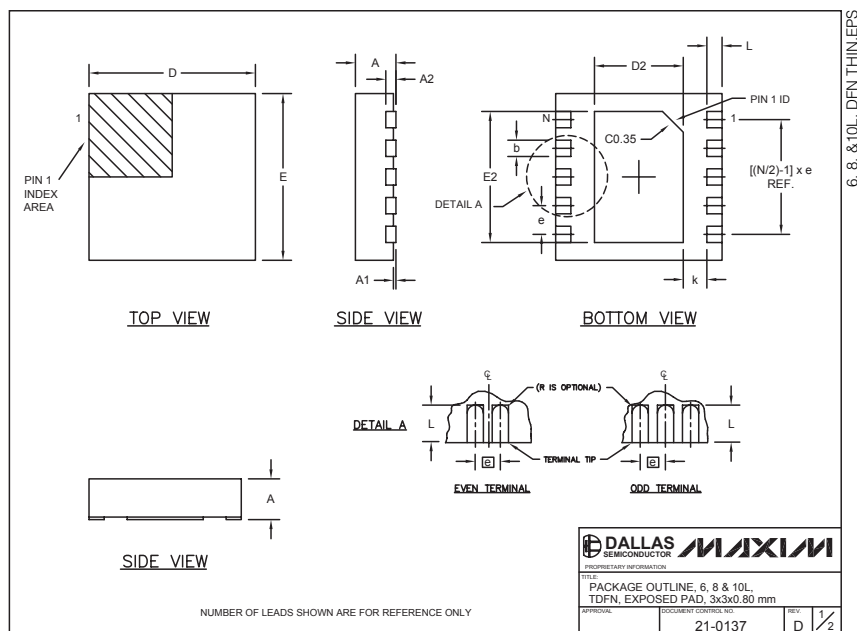
**PACKAGE OUTLINE, 10L uMAX/uSOP**

APPROVAL: \_\_\_\_\_ DOCUMENT CONTROL NO. 21-0061 REV. I 1/

# 670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



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