

DS32EL0421, DS32ELX0421

125 – 312.5 MHz FPGA-Link Serializer with DDR LVDS Parallel Interface

General Description

The DS32EL0421/DS32ELX0421 is a 125 MHz to 312.5 MHz (DDR) serializer for high-speed serial transmission over FR-4 printed circuit board backplanes, balanced cables, and optical fiber. This easy-to-use chipset integrates advanced signal and clock conditioning functions, with an FPGA friendly interface.

The DS32EL0421/DS32ELX0421 serializes up to 5 parallel input LVDS channels to create a maximum data payload of 3.125 Gbps. If the integrated DC-balance encoding is enabled, the maximum data payload achievable is 2.5 Gbps.

The DS32EL0421/DS32ELX0421 serializers feature remote sense capability to automatically detect and negotiate link status with its companion DS32EL0124/DS32ELX0124 deserializers without requiring an additional feedback path.

The parallel LVDS interface reduces FPGA I/O pins, board trace count and alleviates EMI issues, when compared to traditional single-ended wide bus interfaces.

The DS32EL0421/DS32ELX0421 is programmable through a SMBus interface as well as through control pins.

Target Applications

- Imaging: Industrial, Medical Security, Printers
- Displays: LED walls, Commercial
- Video Transport
- Communication Systems
- Test and Measurement
- Industrial Bus

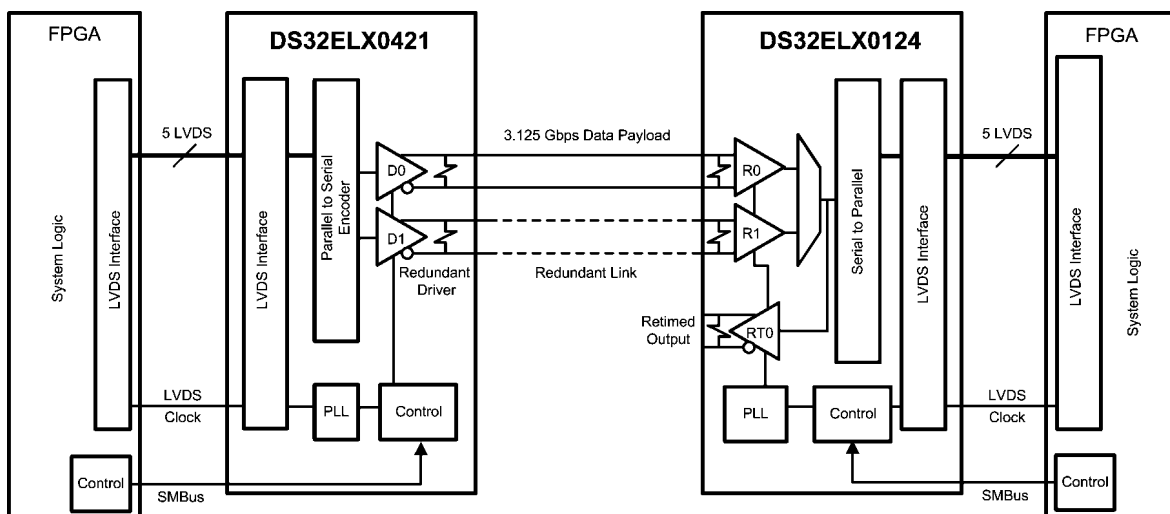
Features

- 5-bit DDR LVDS parallel data interface
- Programmable transmit de-emphasis
- Configurable output levels (V_{OD})
- Selectable DC-balanced encoder
- Selectable data scrambler
- Remote Sense for automatic detection and negotiation of link status
- On chip LC VCOs
- Redundant serial output (ELX device only)
- Data valid signaling to assist with synchronization of multiple receivers
- Supports AC- and DC-coupled signaling
- Integrated CML and LVDS terminations
- Configurable PLL loop bandwidth
- Programmable output termination (50Ω or 75Ω).
- Built-in test pattern generator
- Loss of lock and error reporting
- Configurable via SMBus
- 48-pin LLP package with exposed DAP

Key Specifications

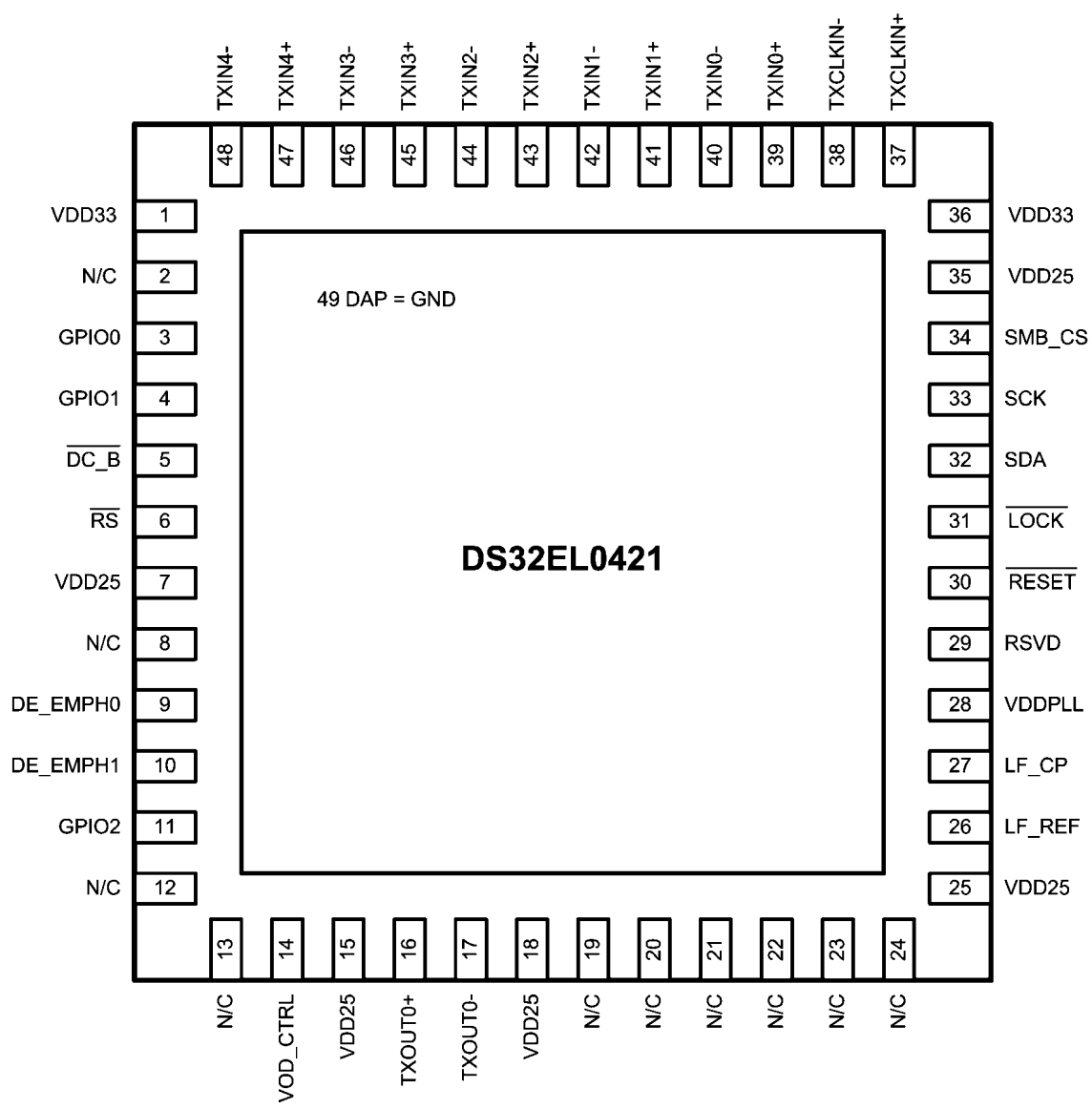
- 1.25 to 3.125 Gbps serial data rate
- 125 to 312.5 MHz DDR parallel clock
- -40° to $+85^{\circ}\text{C}$ temperature range
- >8 kV ESD (HBM) protection
- Low Intrinsic Jitter — 35ps at 3.125 Gbps

Typical Application

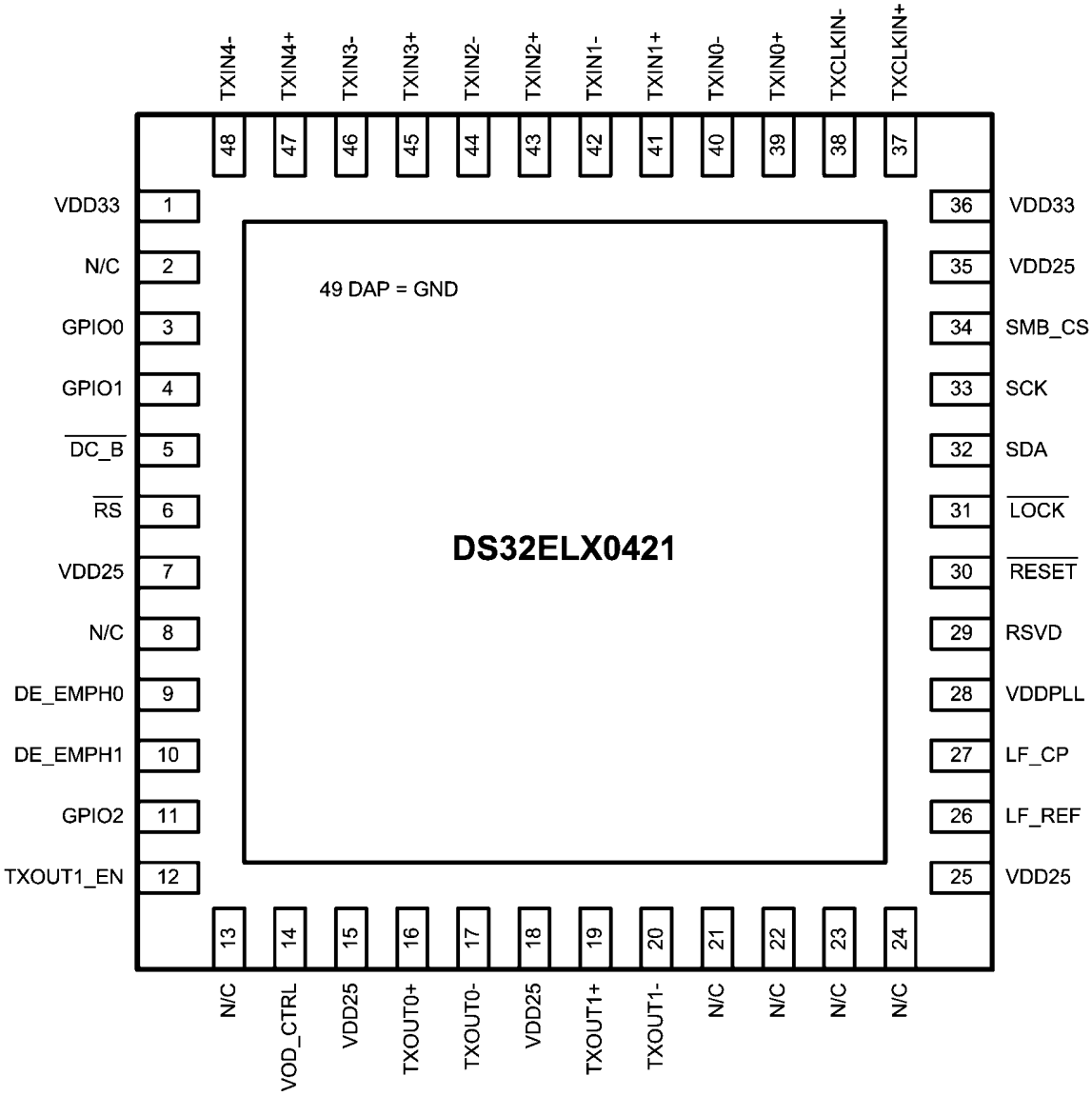


30032101

Connection Diagrams



30032102



30032103

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Description
Power, Ground and Analog Reference			
VDD33	1, 36	I, VDD	3.3V supply
VDD25	7, 15, 18, 25, 35	I, VDD	2.5V supply
VDDPLL	28	I, VDD	3.3V supply
VOD_CTRL	14	Analog	V _{OD} control. The serializer output amplitude can be adjusted by connecting this pin to a pull-down resistor. The value of the resistor determines the VOD. See CML LAUNCH AMPLITUDE for more details.
LF_CP	27	Analog	Loop filter connection for PLL
LF_REF	26	Analog	Loop filter ground reference
Exposed Pad	49	GND	Exposed Pad must be connected to GND by 9 vias
CML I/O			
TxOUT0+	16	O, CML	Inverting and non-inverting high speed CML differential outputs of the serializer. These outputs are internally terminated.
TxOUT0-	17		
TxOUT1+	19	O, CML	DS32ELX0421 ONLY. Redundancy output. Inverting and non-inverting high speed CML differential outputs of the serializer. These outputs are internally terminated
TxOUT1-	20		
LVDS Parallel Data Bus			
TxCLKIN+	37	I, LVDS	Serializer input clock. TxCLKIN+/- are the inverting and non-inverting LVDS transmit clock input pins.
TxCLKIN-	38		
TxIN[4:0]+/-	39, 40, 41, 42, 43, 44, 45, 46, 47, 48	I, LVDS	Serializer input data. TxIN[4:0]+/- are the inverting and non-inverting LVDS serializer input data pins.
LVCMOS Control Pins			
DC_B	5	I,	DC-balance and Remote Sense pins. See Device Configuration section for device behavior.
RS	6	LVC MOS	
DE_EMPH0	9	I,	DE_EMPH0, DE_EMPH1 select the output de-emphasis level. These pins are internally pull-down. 00: Off 01: Low 10: Medium 11: Maximum
DE_EMPH1	10	LVC MOS	
TXOUT1_EN	12	I, LVC MOS	DS32ELX0421 ONLY. When held high, redundant output TxOUT1+/- is enabled. This pin must be tied high when using TxOUT1+/-.
RESET	30	I, LVC MOS	When held low, reset the device. 0 = Device Reset 1 = Normal operation
LOCK	31	O, LVC MOS	Lock indication output. The input data on TxIN[0:4]+/- pins is ignored when LOCK pin is high.
SMBus Interface			
SCK	33	I/O, SMBus	SMBus compatible clock.
SDA	32	I/O, SMBus	SMBus compatible data line.
SMB_CS	34	I, SMBus	SMBus chip select. When held high, SMBus management control is enabled.

Pin Name	Pin Number	I/O, Type	Description
Other			
GPIO0	3	I/O, LVCMOS	Software configurable I/O pin.
GPIO1	4	I/O, LVCMOS	Software configurable I/O pin.
GPIO2	11	I/O, LVCMOS	Software configurable I/O pin.
NC	2, 8, 12, 13, 19, 20, 21, 22, 23, 24, 29	Misc.	No Connect, for DS32EL0421
	2, 8, 13, 21, 22, 23, 24, 29	Misc.	No Connect, for DS32ELX0421

Absolute Maximum Ratings *(Note 1)*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (3.3V V_{DD33})	-0.3V to +4V
Supply Voltage (2.5V V_{DD25})	-0.3V to +3V
LVC MOS Input Voltage	-0.3V to ($V_{DD} + 0.3V$)
LVC MOS Output Voltage	-0.3V to ($V_{DD} + 0.3V$)
LVDS Input Voltage (IN+, IN-)	-0.3V to +3.6V
CML Output Voltage	-0.3V to +3.6V
Junction Temperature	+125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Thermal Resistance, θ_{JA}	25°C/W
ESD Susceptibility	
HBM <i>(Note 2)</i>	>8 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ($V_{DD33} - GND$)	3.135	3.3	3.465	V
Supply Voltage ($V_{DD25} - GND$)	2.375	2.5	2.625	V
Supply Noise Amplitude from 10 Hz to 50 MHz			100	mV _{P-P}
Ambient Temperature (T_A)	-40	+25	+85	°C

Power Supply Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. *(Note 3, Note 5)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD25}	2.5V supply current 1 Output Enabled	1.25 Gbps		87	94	mA
		2.5 Gbps		95	105	
		3.125 Gbps		101	112	
	2.5V supply current 2 Outputs Enabled	1.25 Gbps		126	135	
		2.5 Gbps		136	145	
		3.125 Gbps		142	152	
I_{DD33}	3.3V supply current 1 Output Enabled	1.25 Gbps		74	85	mA
		2.5 Gbps		74	85	
		3.125 Gbps		74	85	
	3.3V supply current 2 Outputs Enabled	1.25 Gbps		80	92	
		2.5 Gbps		80	92	
		3.125 Gbps		80	92	
P_D	Power Consumption 1 Output Enabled	1.25 Gbps		460	540	mW
		2.5 Gbps		485	560	
		3.125 Gbps		500	575	
	Power Consumption 2 Output Enabled	1.25 Gbps		580	670	
		2.5 Gbps		605	695	
		3.125 Gbps		620	710	

LVC MOS Electrical Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. Applies to GPIO0, GPIO1, GPIO2, RESET, LOCK, RS, and DC_BAL. ([Note 3](#), [Note 4](#), [Note 5](#))

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		0		0.8	V
V_{OH}	High Level Output Voltage	$I_{OH} = -2\text{mA}$	2.7	3.3		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2\text{mA}$			0.3	V
V_{CL}	Input Clamp Voltage	$I_{CL} = -18\text{mA}$		-0.79	-1.5	V
I_{IN}	Input Current	$V_{IN} = 0.4\text{V}, 2.5\text{V}, \text{ or } V_{DD}$	-35		35	μA
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0\text{V}$ (Note 6)		42		mA

SMBus Electrical Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. ([Note 3](#), [Note 4](#), [Note 5](#))

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SIL}	Data, Clock Input Low Voltage				0.8	V
V_{SIH}	Data, Clock Input High Voltage		2		V_{SDD}	V
V_{SDD}	Nominal Bus Voltage		2.375		3.6	V
i_{SLEAKB}	Input Leakage Per Bus Segment			± 200		μA
C_{SI}	Capacitance for SDA and SCLK	(Note 9 , Note 10)		10		pF

SMBus Timing Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. ([Note 3](#), [Note 5](#))

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{SMB}	Bus Operating Frequency		10		100	kHz
t_{BUF}	Bus Free Time between Stop and Start Condition		4.7			μs
$t_{HD:STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		4.0			μs
$t_{SU:STA}$	Repeated Start Condition Setup Time		4.7			μs
$t_{SU:STO}$	Stop Condition Setup Time		4.0			μs
$t_{HD:DAT}$	Data Hold Time		300			ns
$t_{SU:DAT}$	Data Setup Time		250			ns
t_{LOW}	Clock Low Time		4.7			μs
t_{HIGH}	Clock High Time		4.0		50	μs
t_F	Clock/Data Fall Time	20% to 80%			300	ns
t_R	Clock/Data Rise Time				1000	ns
$t_{SU:CS}$	SMB_CS Setup Time			30		ns
t_{POR}	Time in which the device must be operation after power on	(Note 8)			500	ms

LVDS Electrical Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. ([Note 3](#), [Note 4](#), [Note 5](#))

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	$0.05V < V_{LVCM} < V_{DD25} - 0.05V$			+100	mV
V_{TL}	Differential Input Low Threshold		-100			mV
V_{LVCM}	LVDS Input Common Mode Voltage		0.05		$V_{DD25} - 0.05$	V
V_{LVOS}	LVDS Input Loss of Signal	LVDS input loss of signal level. (Note 7)		20		mV _{P-P}
R_{LVIN}	Input Impedance	Internal LVDS input termination between differential pairs.	85	100	115	Ω

LVDS Timing Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. ([Note 3](#), [Note 5](#))

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f	Input DDR Clock (TxCLKIN) Frequency Range		125		312.5	MHz
t_{CIP}	TxCLKIN Period	See Figure 3	3.2	2T	8	ns
t_{CIT}	TxCLKIN Transition Time	See Figure 2 (Note 8)	0.5	1.0	3.0	ns
t_{XIT}	TxIN Transition Time		0.15		3	ns
t_{CIH}	TxCLKIN High Time	See Figure 3	0.7T	T	1.3T	ns
t_{CIL}	TxCLKIN Low Time		0.7T	T	1.3T	ns
t_{STC}	TxIN Setup to TxCLKIN		-550			ps
t_{HTC}	TxIN Hold to TxCLKIN		900			ps
t_{LVDS}	LVDS Input Clock Delay Step Size	Programmable through the SMBus, register 30'h Default setting = 011'b [7:5] See		100		ps

CML Electrical Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. ([Note 3](#), [Note 4](#), [Note 5](#))

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{OT}	Output Terminations	On chip termination from TxOUT0/1 + and TxOUT0/1 - to V_{DD25} 50 Ω mode	40	50	60	Ω
		75 Ω mode	60	75	90	Ω
ΔR_{OT}	Mismatch in Output Termination Resistors				5	%
V_{OD}	Output Differential Voltage Swing	Based on VOD_CTRL = 9.1 k Ω	1175	1350	1450	mV _{P-P}

CML Timing Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. ([Note 3](#), [Note 5](#))

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LR	Line Rate	Tested with alternating 1-0 pattern.	1.25		3.125	Gbps
t_{OS}	Output Overshoot	(Note 8)			10	%
t_R	Differential Low to High Transition Time	(Note 8)		60	90	ps
t_F	Differential High to Low Transition Time			60	90	ps
t_{RFMM}	Mismatch in Rise/Fall Time	(Note 8)			15	ps
t_{DE}	De-emphasis width	Measured from zero-crossing at rising edge to 80% of VOD from zero-crossing at falling edge. TDE is measured at the High setting during test.		1		UI

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{BIT}	Serializer Bit Width			$0.2 \times t_{CIP}$		ns
t_{SD}	Serializer Propagation Delay – Latency			$t_{CIP} + 5.5$		ns
t_{JIND}	Serializer Output Deterministic Jitter	Serializer output intrinsic deterministic jitter. Measure with PRBS-7 test pattern De-emphasis disabled. (Note 8) 1.25 Gbps		10		ps
		2.5 Gbps		24		ps
		3.125 Gbps		21		ps
t_{JINR}	Serializer Output Random Jitter	Serializer output intrinsic random jitter. Bit error rate $\geq 10^{-15}$. Alternating-10 pattern. De-emphasis disabled. (Note 8) 1.25 Gbps		1.3		ps _{RMS}
		2.5 Gbps		1.15		ps _{RMS}
		3.125 Gbps		1.14		ps _{RMS}
t_{JINT}	Peak-to-peak Serializer Output Jitter	Serializer output peak-to-peak jitter includes deterministic jitter, random jitter, and jitter transfer from serializer input. Measure with PRBS-7 test pattern. Bit error rate $\geq 10^{-15}$. De-emphasis disabled. (Note 8) 1.25 Gbps		28		ps
		2.5 Gbps		38		ps
		3.125 Gbps		35		ps
λ_{TXBW}	Jitter Transfer Function -3 dB Bandwidth (Note 8)	1.25 Gbps		100		kHz
		3.125 Gbps		300		kHz
δ_{TX}	Jitter Transfer Function Peaking (Note 8)			0.5		dB

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: Human Body Model, applicable std. JESD22-A114C

Note 3: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 4: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD} .

Note 5: Typical values represent most likely parametric norms for $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 6: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

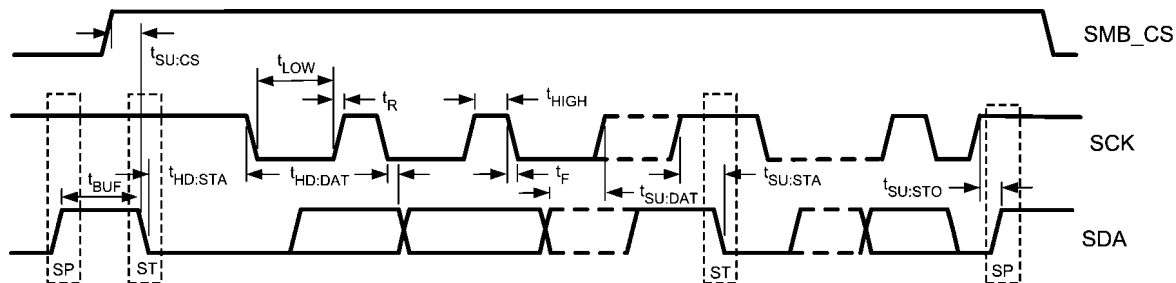
Note 7: If input LVDS signal is below $20mV_{P,P}$, loss of signal (LOS) is detected. The device will flag a valid input signal if the signal level is above $100mV_{P,P}$.

Note 8: Parameter is guaranteed by characterization and is not tested at production.

Note 9: Recommended value, parameter is not tested.

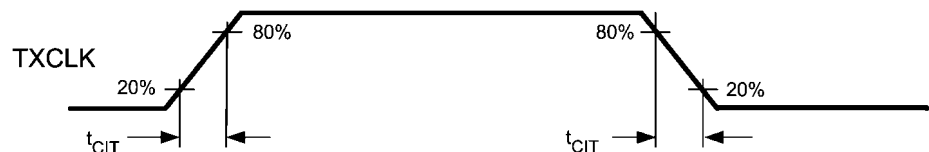
Note 10: Recommended maximum capacitance load per bus segment is 400 pF.

Timing Diagrams



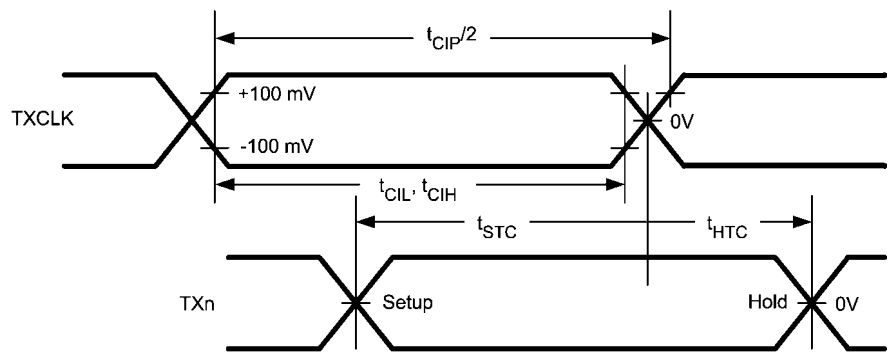
30032106

FIGURE 1. SMBus timing parameters



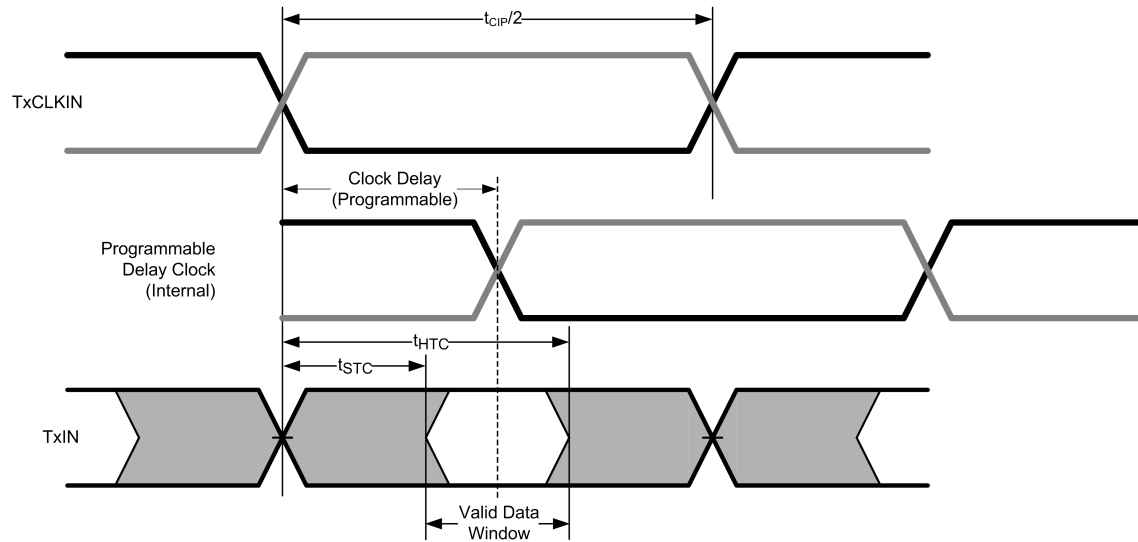
30032111

FIGURE 2. Serializer Input Clock Transition Time



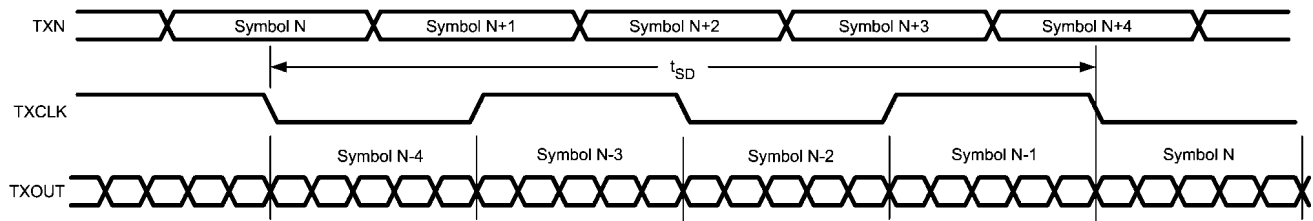
30032110

FIGURE 3. Serializer (LVDS Interface) Setup/Hold and High/Low Times



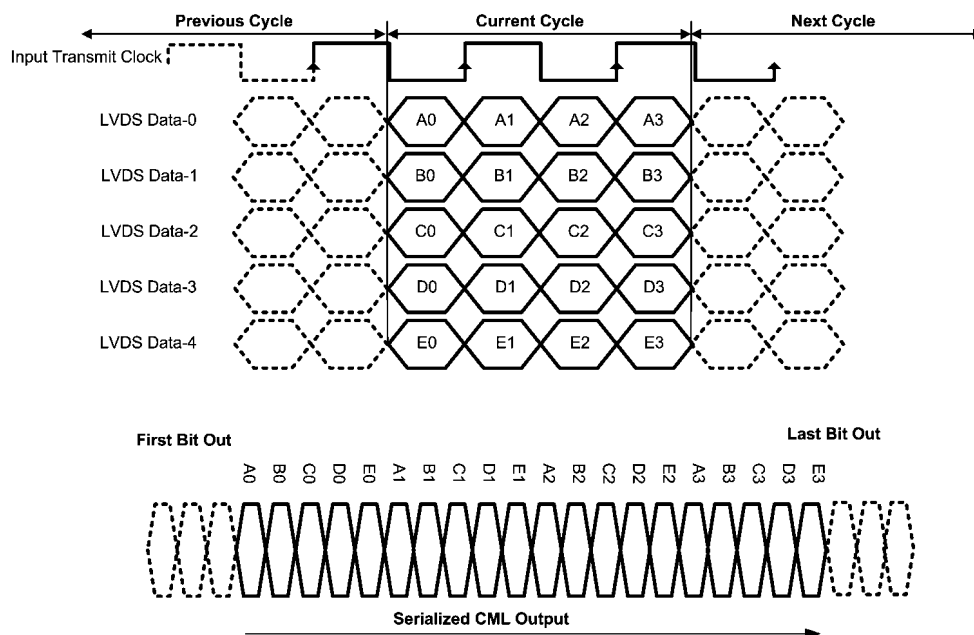
30032113

FIGURE 4. LVDS Input Clock Delay



30032112

FIGURE 5. Propagation Delay Timing Diagram



30032104

FIGURE 6. 5-Bit Parallel LVDS Inputs Mapped to CML Output

Functional Description

POWER SUPPLIES

The DS32EL0421 and DS32ELX0421 have several power supply pins, at 2.5V as well as 3.3V. It is important that these pins all be connected and properly bypassed. Bypassing should consist of parallel 4.7µF and 0.1µF capacitors as a minimum, with a 0.1µF capacitor on each power pin. A 22 µF capacitor is required on the VDDPLL pin which is connected to the 3.3V rail.

These devices have a large contact in the center on the bottom of the package. This contact must be connected to the system GND as it is the major ground connection for the device.

POWER UP

It is recommended, although not necessary, to bring up the 3.3V power supply before the 2.5V supply. If the 2.5V supply is powered up first, an initial current draw of approximately 600mA from the 2.5V rail may occur before settling to its final value. Regardless of the sequence, both power rails should monotonically ramp up to their final values.

POWER MANAGEMENT

These devices have two methods to reduce power consumption. To enter the first power save mode, the on board host FPGA or controlling device can cease to output the DDR transmit clock. To further reduce power consumption, write 40'h to register 26'h and 10'h to register 01'h. This will put the device in its lowest power consumption mode.

RESET

There are three ways to reset these devices. A reset occurs automatically during power-up. The device can also be reset by pulling the RESET pin low, with normal operation resuming when the pin is driven high again. The device can also be reset by writing to the reset register. This reset will put all of the register values back to their default values, except it will not affect the address register value if the SMBus default address has been changed.

LVDS INPUTS

The DS32EL0421 and DS32ELX0421 have standard 2.5V LVDS inputs which are compliant with ANSI/TIA/EIA-644. These inputs have internal 100Ω termination resistors. It is recommended that the PCB trace between the FPGA and the serializer be less than 40-inches. Longer PCB traces may degrade the quality of the input signal. The connection between the host and the DS32EL0421 or DS32ELX0421 should be over a controlled impedance transmission line with impedance that matches the termination resistor – usually 100Ω. Setup and hold times are specified in the LVDS Switching Characteristics table, however the clock delay can be adjusted by writing to register 30'h.

LOOP FILTER

The DS32EL0421 and DS32ELX0421 have an internal PLL which is used to generate the serialization clock from the parallel clock input. The loop filter for this PLL is external; and for optimum results, a 100nF capacitor and a 1.5 kΩ resistor in series should be connected between pins 26 and 27. See typical interface circuit ([Figure 12](#)).

CML LAUNCH AMPLITUDE

The launch amplitude of the CML output(s) is controlled by placing a single resistor from the VOD_CTRL pin to ground.

Use the following equation to obtain the desired V_{OD} by selecting the corresponding resistor value.

$$R = (1400 \text{ mV} / V_{OD}) \times 9.1 \text{ k}\Omega$$

The CML output launch amplitude can also be adjusted by writing to SMBus register 69'h, bits 2:0. This register is meant to assist system designers during the initial prototype design phase. For final production, it is recommended that the appropriate resistor value be selected for the desired V_{OD} and that register 69'h be left to its default value.

REMOTE SENSE

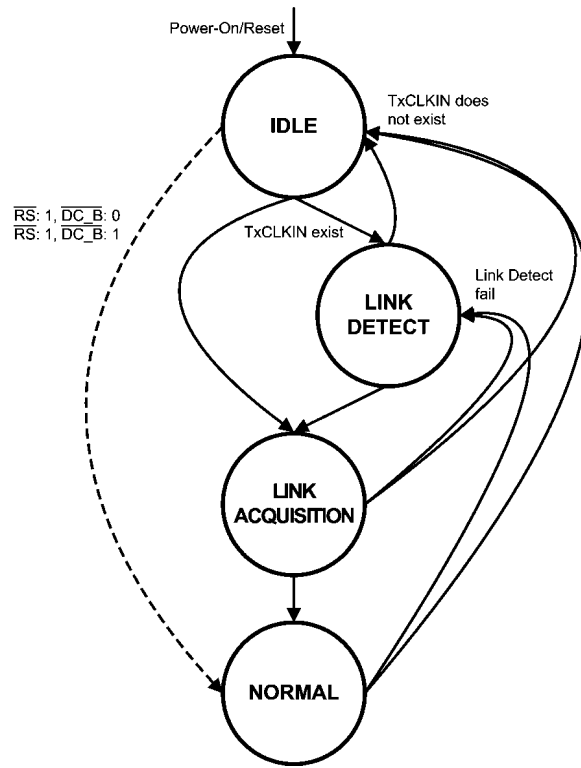
The remote sense feature can be used when a DS32EL0421 or DS32ELX0421 serializer is directly connected to a DS32EL0124 or DS32ELX0124 deserializer. Active components in the signal path between the serializer and the deserializer may interfere with the back channel signaling of the devices.

When remote sense is enabled, the serializer will cycle through four states to successfully establish a link and align the data. The state diagram for the serializer is shown in [Figure 7](#). The serializer will remain in the low power IDLE state until it receives an input clock. Once the PLL of the serializer has locked to the input clock, the device will enter the LINK DETECT state. While in this state, the serializer will monitor the line to see if the deserializer is present. If a deserializer is detected, the serializer will enter the LINK ACQUISITION state. The serializer will transmit the entire training pattern and then enter the NORMAL state. If the deserializer is unable to successfully lock or maintain lock it will break the link, sending the serializer back to the IDLE or LINK DETECT states.

With the Remote Sense feature active, the serializer can be forced out of lock due to events on the high speed serial line in two ways, a serial channel reset signal is sent upstream from the deserializer or the near end termination detect circuit signals and open termination was detected. The upstream signal sent from the deserializer that resets the serializer is called the link detect signal. Since the serializer and deserializer may power up at different times, the deserializer will transmit this link detect signal periodically, once it detects that a serializer is active on the other side of the high speed line. When a serializer receives the link detect signal, it will return to the LINK DETECT state. The near end open termination detection circuit will trigger only for near end open termination events, such as unplugging the cable on the serializer end of the line.

DC-BALANCE ENCODER

The DS32EL0421 and DS32ELX0421 have a built-in DC-balance encoder to support AC-coupled applications. When enabled, the input signal on TXIN4+/- is treated as a data valid bit. If TXIN4+/- is low, then the four bit nibbles from TXIN0-TXIN3 are taken to form a 16 bit word. This 16 bit word is processed as two 8 bit words and converted to two 10 bit words by using the standard 8b/10b data coding scheme. The two 10 bit words are then combined to create a 20 bit code. This 20 bit word is serialized and driven on the output. The nibble taken in on the rising edge of the clock is the most significant nibble and the nibble taken in on the falling edge is the least significant nibble. If TXIN4+/-TXIN4- is high, then the inputs TXIN0 -TXIN3 are ignored and a programmable DC-balanced SYNC character is inserted in the output stream. The default character is a K28.5 code. In order to send other K codes, they must first be programmed into the serializer via the SMBus. The SMBus registers allows for only a single programmable character.



30032115

FIGURE 7. Serializer State Diagram

SCRAMBLER and NRZI Encoder

The CDR of the DS32EL0124 and the DS32ELX0124 expect a transition density of 20% for a period of 200 μ s. If the scrambler and NRZI encoder are enabled, the raw or DC-balanced serialized data is scrambled to improve transition density. The scrambler accepts 20 bits of data and encodes it using the polynomial $X^9 + X^4 + 1$. The data can then be sent to the NRZ-to-NRZI converter before being output.

Enabling the scrambler can help to lower EMI emissions by spreading the spectrum of the data. Scrambling also creates transitions for the deserializer's CDR to properly lock onto.

The scrambler and NRZI encoder are enabled or disabled by default depending on how the $\overline{DC_B}$ and \overline{RS} pins are configured. To override the default scrambler setting two register writes must be performed. First, write to register 22'h and set bit 3 to unlock the scrambler register. Next write to register 21'h and change bit 4 to the desired value. The NRZI encoder can be enabled or disabled independently of the scrambler by controlling bit 7 of register 21'h and bit 4 of register 22'h.

CML OUTPUT DATA INTERFACING

The serial outputs provide low-skew differential signals. Internal resistors connected from TxOUTn+ and TxOUTn- to VDD25 terminate the outputs. The output level can be programmed by adjusting the pull-down resistor to the VOD_CTRL pin. The output terminations can also be programmed to be either 50 Ω or 75 Ω .

The output buffer consists of a current mode logic (CML) driver with user configurable de-emphasis control, which can be used to optimize performance over a wide range of transmission line lengths and attenuation distortions resulting from low cost CAT(-5, -6, -7) cable or FR-4 backplane. Output de-em-

phasis is user programmable through either device pins DE_EMPH0 and DE_EMPH1 or SMBus interface. Users can control the strength of the de-emphasis to optimize for a specific system environment. Please see the De-Emphasis Control Table for details.

De-Emphasis Control Table

DE_EMPH[1:0]	Output De-Emphasis Level
00'b	Off
01'b	Low
10'b	Medium
11'b	High

The DS32ELX0421 provides a secondary serial output, supporting redundancy applications. The redundant output driver can be enabled by setting TXOUT1_EN pin to HIGH or by activating it through the SMBus registers.

DEVICE CONFIGURATION

There are four ways to configure the DS32EL0421 and DS32ELX0421 serializers, these combinations are shown in [Table 1](#). Refer to [Figure 7](#) to see how the combinations of the \overline{RS} and $\overline{DC_B}$ pins change the link startup behavior of the serializers. When connecting to a deserializer other than the DS32EL0124 or DS32ELX0124, Remote Sense should be disabled. The scrambler and NRZI encoder shown in [Table 1](#) can be enabled or disabled through register programming. When Remote Sense is enabled, with \overline{RS} pin tied low, the serializer must be connected directly to a DS32EL0124 or DS32ELX0124 deserializer without any active components between them. The Remote Sense module features an upstream communication method for the serializer and deseri-

alizer to communicate. This feature is used to pass link status information between the 2 devices. When Remote Sense is enabled the serializer will send a training pattern to the deserializer to establish lock and lane alignment.

If DC-Balance is enabled, a maximum of 4 parallel LVDS lanes can be used to receive data. The fifth lane (TXIN4±) is used for Data Valid signaling. Each time a serializer establishes a link to a deserializer with DC-Balance enabled and Remote Sense disabled, the Data Valid input to the serializer must be held high for 110 LVDS clock periods. If the Data Valid input to the serializer is logic HIGH, then SYNC characters are transmitted. If the deserializer receives a SYNC character, then the LVDS data outputs will all be logic low and the Data Valid output will be logic high. If the deserializer detects a DC-Balance code error, the output data pins will be set to logic high with the Data Valid output also set to logic high.

In the case where DC-Balance is enabled and Remote Sense is disabled, with $\overline{\text{RS}}$ set to high and $\overline{\text{DC_B}}$ set to low, it is recommended that the host device periodically toggle the Da-

ta Valid input to the serializer, to transmit SYNC symbols on the line, to ensure that the deserializer is and remains locked. In this configuration the deserializer or receiving device does not have a way to directly notify the serializer if it has lost lock. Periodically sending SYNC symbols will allow the receiving system to reacquire lock if a problem has occurred. With these pin settings the DS32EL0421/DS32ELX0421 and DS32EL0124/DS32ELX0124 devices can interface with other active component in the high speed signal path, such as fiber modules.

When both Remote Sense and DC-Balance are disabled, $\overline{\text{RS}}$ and $\overline{\text{DC_B}}$ pins set to high, the LVDS lane alignment is not maintained. In this configuration, data formatting is handled by an FPGA or external source. This pin setting combination also allows for the DS32EL0421/DS32ELX0421 devices to interface with active components other than the DS32EL0124/DS32ELX0124 in the high speed signal path. In this configuration the host device is responsible for DC balancing the data in an AC coupled application.

TABLE 1. Device Configuration Table

Remote Sense Pin ($\overline{\text{RS}}$)	DC-Balance Pin ($\overline{\text{DC_B}}$)	Configuration
0	0	Remote Sense enabled DC-Balance enabled Data Alignment Scrambler and NRZI encoder disabled by default
0	1	Remote Sense enabled DC-Balance disabled Data Alignment Scrambler and NRZI encoder enabled by default
1	0	Remote Sense disabled DC-Balance enabled Data Alignment Scrambler and NRZI encoder enabled by default
1	1	Remote Sense disabled DC-Balance disabled No Data Alignment Scrambler and NRZI encoder disabled by default

SMBus INTERFACE

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. The use of the Chip Select signal is **required**. Holding the SMB_CS pin HIGH enables the SMBus port, allowing access to the configuration registers. Holding the SMB_CS pin LOW disables the device's SMBus, allowing communication from the host to other slave devices on the bus. In the STANDBY state, the System Management Bus remains active. When communication to other devices on the SMBus is active, the SMB_CS signal for the serializer must be driven LOW.

The address byte for all DS32EL0421 and DS32ELX0421 devices is AE'h. Based on the SMBus 2.0 specification, these devices have a 7-bit slave address of 1010111'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1010 1110 'b or AE'h.

The SCK and SDA pins are 3.3V LVCMOS signaling and include high-Z internal pull up resistors. External low impedance pull up resistors maybe required depending upon SMBus loading and speed. Note, these pins are not 5V tolerant.

Transfer of Data via the SMBus

During normal operation the data on SDA must be stable during the time when SCK is HIGH.

There are three unique states for the SMBus:

- START** A HIGH to LOW transition on SDA while SCK is HIGH indicates a message START condition
- STOP** A LOW to HIGH transition on SDA while SCK is HIGH indicates a message STOP condition.
- IDLE** If SCK and SDA are both high for a time exceeding t_{BUF} from the last detected STOP condition or if they are HIGH for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus Transactions

The devices support WRITE and READ transactions. See Register Description Table for register address, type (Read/Write, Read Only), default value and function information.

Writing to a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (SMB_CS) signal HIGH.
2. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
3. The Device (Slave) drives the ACK bit ("0").
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit ("0").
6. The Host drive the 8-bit data byte.
7. The Device drives an ACK bit ("0").
8. The Host drives a STOP condition.

9. The Host de-selects the device by driving its SMBus CS signal Low.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (SMB_CS) signal HIGH.
2. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
3. The Device (Slave) drives the ACK bit ("0").
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit ("0").
6. The Host drives a START condition.
7. The Host drives the 7-bit SMBus Address, and a "1" indicating a READ.
8. The Device drives an ACK bit "0".
9. The Device drives the 8-bit data value (register contents).
10. The Host drives a NACK bit "1" indicating end of the READ transfer.
11. The Host drives a STOP condition.
12. The Host de-selects the device by driving its SMBus CS signal Low.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

SMBus Configurations

Many different configurations of the SMBus are possible and depend upon the specific requirements of the applications. Several possible applications are described.

Configuration 1

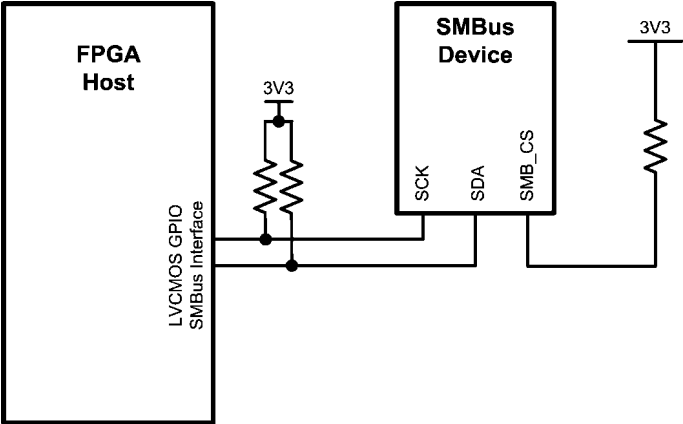
The deserializer SMB_CS may be tied High (always enabled) since it is the only device on the SMBus. See [Figure 8](#).

Configuration 2

Since the multiple SER devices have the same address, the use of the individual SMB_CS signals is required. To communicate with a specific device, its SMB_CS is driven High to select the device. After the transaction is complete, its SMB_CS is driven Low to disable its SMB interface. Other devices on the bus may now be selected with their respective chip select signals and communicated with. See [Figure 9](#).

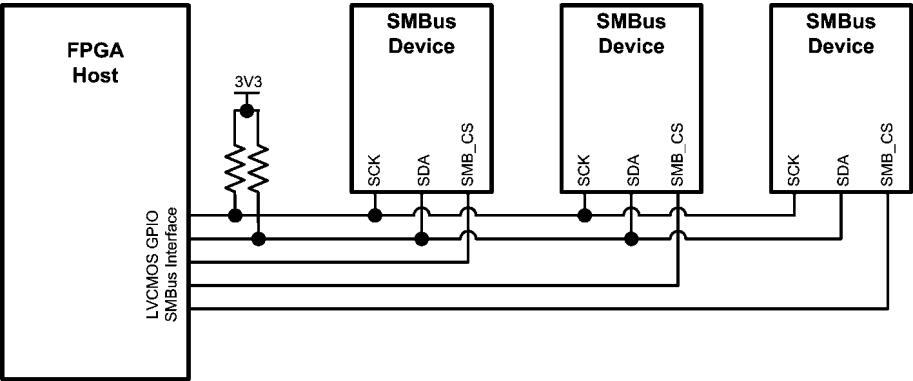
Configuration 3

The addressing field is limited to 7-bits by the SMBus protocol. Thus it is possible that multiple devices may share the same 7-bit address. An optional feature in the SMBus 2.0 specification supports an Address Resolution Protocol (ARP). This optional feature is not supported by the DS32EL0421/DS32ELX0421 devices. Solutions for this include: the use of the independent SMB_CS signals, independent SMBus segments, or other means.



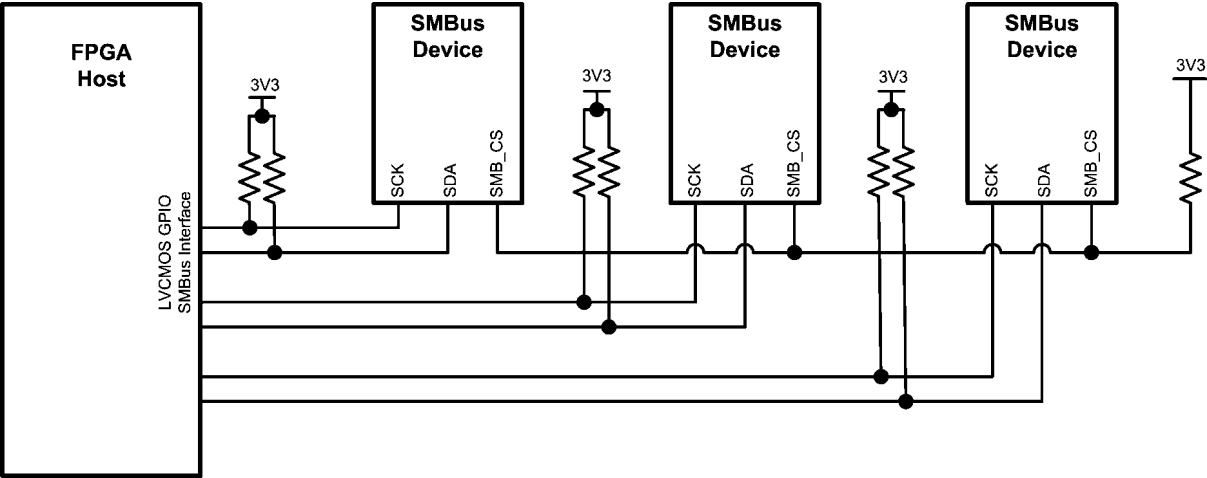
30032107

FIGURE 8. SMBus Configuration 1



30032108

FIGURE 9. SMBus Configuration 2




30032109

FIGURE 10. SMBus Daisy Chained CS Configuration

PROPAGATION DELAY

Once the serializer is locked, the amount of time it takes for a bit to travel into the device through the DDR LVDS inputs and out through the CML serial output is defined to be the propagation delay. The propagation delay through the DS32EL0421/DS32ELX0421 due to the analog circuitry is considered negligible compared to the time delay caused by the digital components. The information presented in this section allows system designers to predict the propagation delay through the device in terms of clock cycles which are proportional to the high speed serial line rate.

Each clock cycle shown in [Figure 11](#) is defined to be 1/20th of the high speed serial bit rate. For example, at a serial line rate of 3.125 Gbps the clock frequency of each delay cycle would be 156.25 MHz. Note, this is not the same frequency as the LVDS inputs, which would be 312.5 MHz (625 Mbps) for a serial line rate of 3.125 Gbps. Dashed lines in [Figure 11](#) indicate that the feature is disabled by default in that mode and therefore add no more time to the total propagation delay.

Config Pins (\overline{RS} , $\overline{DC_B}$)	LVDS Interface	DC Balance Encoder	Scrambler	NRZ Encoder	CML Interface	Total Propagation Delay
						
0, 0	3 clocks	1 clock	— —	— —	5-6 clocks	9-10 clocks
0, 1	3 clocks	1 clock	1 clock	1 clock	5-6 clocks	11-12 clocks
1, 0	3 clocks	— —	1 clock	1 clock	5-6 clocks	10-11 clocks
1, 1	3 clocks	— —	— —	— —	5-6 clocks	8-9 clocks

30032116

FIGURE 11. Serializer Propagation Delay

Applications Information

GPIO PINS

The GPIO pins can be useful tools when debugging or evaluating the system. For specific GPIO configurations and functions refer to registers 2, 3, 4, 5 and 6 in the device register map.

GPIO pins are commonly used when there are multiple serializers on the same SMBus. In order to program individual settings into each serializer, they will each need to have a unique SMBus address. To reprogram multiple serializers on a single SMBus, configure the first serializer such that the SMBus lines are connected to the FPGA or host controller. The CS pin of the second serializer should be tied to GPIO0 of the first serializer, with the CS pin of the next serializer tied to GPIO0 of its preceding serializer. By holding all of the GPIO0 pins low, the first serializer's address may now be reprogrammed by writing to register 0. The first serializer's GPIO pin can now be asserted and the second serializer's address may now be reprogrammed.

HIGH SPEED COMMUNICATION MEDIA

Using the serializer's integrated de-emphasis blocks in combination with the DS32EL0124 or DS32ELX0124's integrated equalization blocks allows data to be transmitted across a variety of media at high speeds. Factors that can limit device performance include excessive input clock jitter, noisy power rails, EMI from nearby noisy components and poor layout techniques. Although many cables contain wires of similar gauge and shielding, performance can vary greatly depending on the quality of the connector.

REDUNDANCY APPLICATIONS

The DS32ELX0421 has two high speed CML serial outputs. SMBus register control allows the device to use a single output exclusively, or both outputs simultaneously. This allows a single serializer to transmit data to two independent receiving systems, a primary and secondary endpoint. Some applications require a redundancy measure in case the primary signal path is compromised. The secondary output can be activated "on-the-go", if a problem is detected on the primary

link. See the [Redundancy / Fail Over Configuration](#) section located under [Register Recipes](#).

LINK AGGREGATION

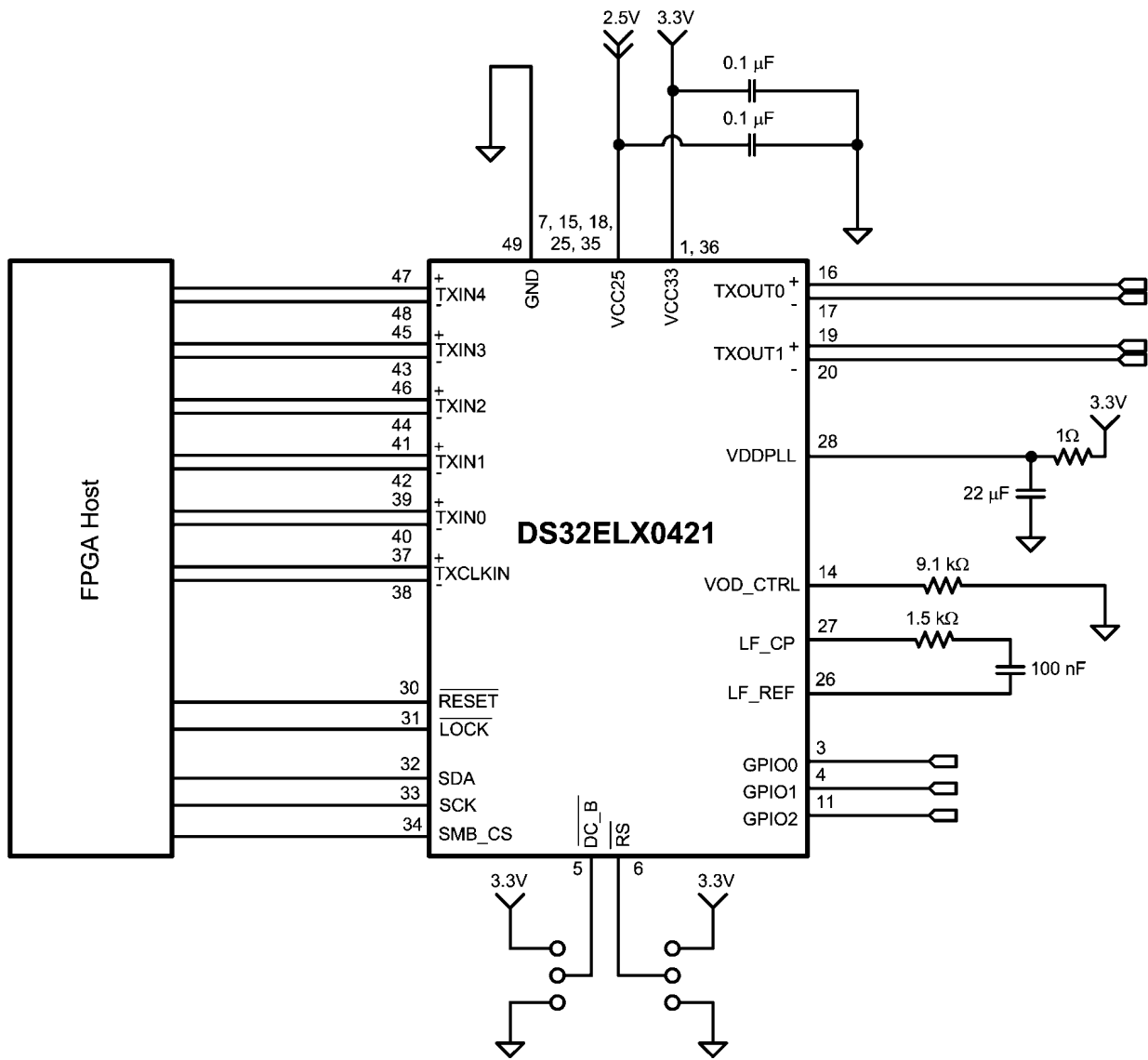
Multiple DS32EL0421/DS32ELX0421 serializers and DS32EL0124/DS32ELX0124 deserializers can be aggregated together if an application requires a data throughput of more than 3.125 Gbps. By utilizing the data valid signal of each device, the system can be properly deskewed to allow for a single cable, such as CAT-6, DVI-D, or HDMI, to carry data payloads beyond 3.125 Gbps.

Link aggregation configurations can also be implemented in applications which require longer cable lengths. In these type of applications the data rate of each serializer and deserializer chipset can be reduced, such that the applications' net data throughput is still the same. Since each high speed channel is now operating at a fraction of the original data rate, the loss over the cable is reduced, allowing for greater lengths of cable to be used in the system.

For more information regarding link aggregation please see Application Note 1887, Expanding the Payload with National's FPGA-Link DS32ELX0421 and DS32ELX0124 Serializer and Deserializer.

LAYOUT GUIDELINES

It is important to follow good layout practices for high speed devices. The length of LVDS input traces should not exceed 40 inches. In noisy environment the LVDS traces may need to be shorter to prevent data corruption due to EMI. Noisy components should not be placed next to the LVDS or CML traces. The LVDS and CML traces must have a controlled differential impedance of 100 Ω . Do not place termination resistor at the LVDS inputs or CML outputs, the DS32EL0421 and DS32ELX0421 have internal termination resistors. It is recommended to avoid using vias. Vias create an impedance mismatch in the transmission line and result in reflections, which can greatly lower the maximum distance of the high speed data link. If vias are required, they should be placed symmetrically on each side of the differential pair. For more tips and detailed suggestions regarding high speed board layout principles, please consult the LVDS Owner's Manual.



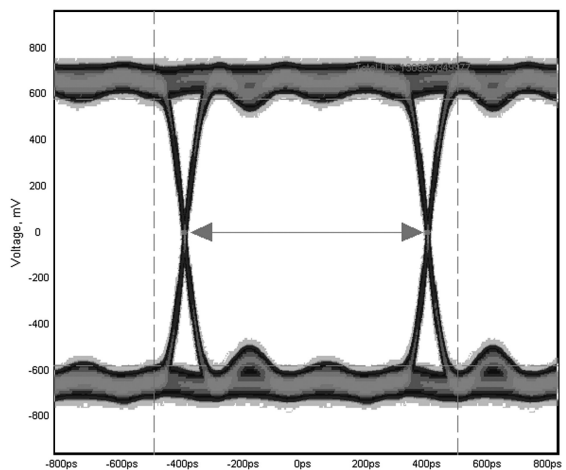
30032105

FIGURE 12. Typical Interface Circuit

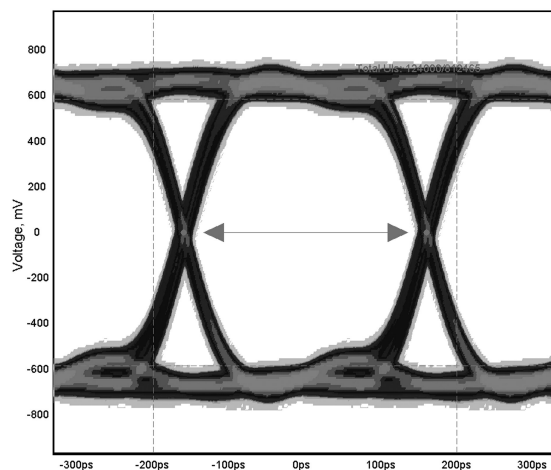
Typical Performance Characteristics

The eye diagrams shown below illustrate the typical performance of the DS32ELX0421/DS32EL0421 configured with RS = 0, DC_B = 0, for the conditions listed below each figure.

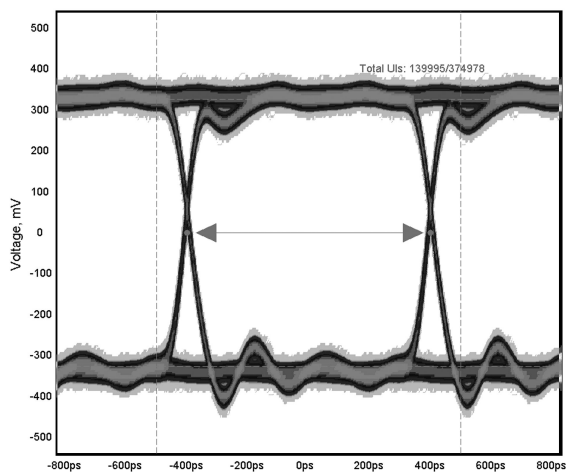
The PRBS-15 data was generated by a low cost FPGA, which used an LMK03000C to generate the various clock frequencies.



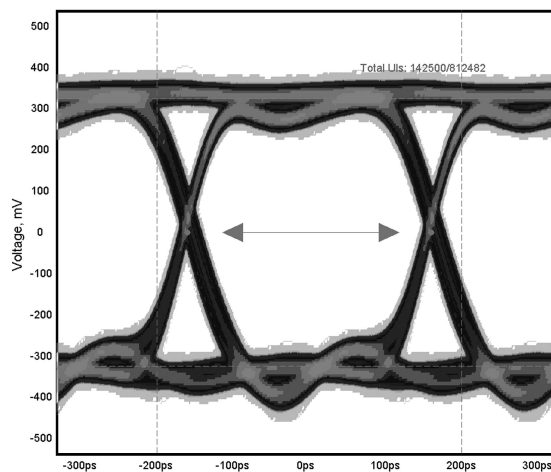
CML Serial Differential Output 1.25 Gbps



CML Serial Differential Output 3.125 Gbps



CML Serial Singled Ended Output (+) 1.25 Gbps



CML Serial Single Ended Output (+) 3.125 Gbps

Register Map

The register information for the serializer is shown in the table below. Some registers have been omitted or marked as re-

served; these are for internal testing and should not be written to. Some register bits require an override bit to be set before they can be written to.

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
00	Device ID	7:1	SMBus Address	R/W	57'h	Some systems will use all 8 bits as the device ID. This will shift the value from 57'h to AE'h
		0	Reserved		0	
01	Reset	7:5	Reserved		0	
		4	Analog Disable	R/W	0	1: Disables analog blocks. Power save feature
		3:1	Reserved		0	
		0	Software Reset		0	1: Reset the device. Does not affect device ID.
02	GPIO0 Config	7:4	GPIO0 Mode	R/W	0	0000: GP out register 0001: Link loss indicator 0011: TxCLKIN loss of signal 0100: TxCLKIN detect All others: Reserved
		3:2	GPIO0 R Enable	R/W	01'b	00: Pullup/down disabled 01: Pulldown enabled 10: Pullup enabled 11: Reserved
		1	Input Enable	R/W	0	0: Input buffer disabled 1: Input buffer enabled
		0	Output Enable	R/W	1'b	0: Output Tri-State™ 1: Output enabled
03	GPIO1 Config	7:4	GPIO1 Mode	R/W	0	0000: Power on reset 0001: GP out register 0010: PLL lock indicator 0011: TxIN0 loss of signal 0100: TxIN1 loss of signal 0101: TxIN2 loss of signal 0110: TxIN3 loss of signal 0111: TxIN4 loss of signal All others: Reserved
		3:2	GPIO1 R Enable	R/W	01'b	00: Pullup/down disabled 01: Pulldown enabled 10: Pullup enabled 11: Reserved
		1	Input Enable	R/W	0	0: Input buffer disabled 1: Input buffer enabled
		0	Output Enable	R/W	1'b	0: Output Tri-State™ 1: Output enabled
04	GPIO2 Config	7:4	GPIO2 Mode	R/W	0	0000: GP out register 0001: Always on clock out 0010: Parallel-to-serial clock out 0100: Digital clock out All others: Reserved
		3:2	GPIO2 R Enable	R/W	01'b	00: Pullup/down disabled 01: Pulldown enabled 10: Pullup enabled 11: Reserved
		1	Input Enable	R/W	0	0: Input buffer disabled 1: Input buffer enabled
		0	Output Enable	R/W	1'b	0: Output Tri-State™ 1: Output enabled

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
05	GP In	7:3	Reserved		0	
		2	GP In 2	R	0	Input value on GPIO2
		1	GP In 1	R	0	Input value on GPIO1
		0	GP In 0	R	0	Input value on GPIO0
06	GP Out	7:3	Reserved		0	
		2	GP Out 2	R/W	0	Output value on GPIO2
		1	GP Out 1	R/W	0	Output value on GPIO1
		0	GP Out 0	R/W	0	Output value on GPIO0
07–1F Reserved						
20	De-Emphasis	7:3	Reserved		0	
		2	Pin Override	R/W	0	0: Pin values determine setting 1: Register overrides pin values
		1:0	De-emphasis level	R/W	0	00: No de-emphasis 01: Low 10: Medium 11: High
21	Device Config	7	NRZI enable	R/W	0	1: Enable NRZI, if override bit is set
		6	DV disable	R/W	0	1: Disable Data Valid
		5	Reserved	R/W	0	
		4	Scrambler Enable	R/W	0	1: Scrambler enable, requires override bit to change setting
		3	DC Bal encoder bypass	R/W	0	1: Bypass encoder, requires override bit to change setting
		2	Training Sequence Enable	R/W	0	1: Enable training sequence, requires override bit to change setting
		1:0	Device Configuration	R/W	0	MSB: Remote Sense enable, active low LSB: DC balance encoder enable, active low Requires override bit to change settings through registers. Normally controlled by pins. See Table 1 for more information.
22	Device Config Override	7:5	Reserved		0	
		4	NRZ bypass override	R/W	0	1: Unlock reg 21'h bit 7
		3	Scrambler bypass override	R/W	0	1: Unlock reg 21'h bit 4
		2	DC Bal encoder bypass override	R/W	0	1: Unlock reg 21'h bit 3
		1	Training sequence enable override	R/W	0	1: Unlock reg 21'h bit 2
		0	Config pin override	R/W	0	1: Unlock reg 21'h bits 1 and 0
23 Reserved						
24	LVDS Clock Delay Enable	7	TxCLKIN Delay Bypass	R/W	0	0: TxCLKIN delay enable 1: Bypass TxCLKIN delay
		6:0	Reserved		0	
25 Reserved						

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
26	Power Down	7	Channel Reset	R/W	0	1: Reset high speed channel. Self-clearing bit.
		6	Clock Powerdown	R/W	0	1: Power down parallel, parallel-to-serial, and always on clock
		5	LVDS Clock enable	R/W	1'b	0: Disable TxCLKIN 1: Enable TxCLKIN
		4	TxIN4 Enable	R/W	1'b	0: Disable TxIN4 1: Enable TxIN4
		3	TxIN3 Enable	R/W	1'b	0: Disable TxIN3 1: Enable TxIN3
		2	TxIN2 Enable	R/W	1'b	0: Disable TxIN2 1: Enable TxIN2
		1	TxIN1 Enable	R/W	1'b	0: Disable TxIN1 1: Enable TxIN1
		0	TxIN0 Enable	R/W	1'b	0: Disable TxIN0 1: Enable TxIN0
27	Event Disable	7:5	Reserved	R/W	0	
		4	PLL Lock Disable	R/W	0	0: Count clock errors 1: Clock error count disabled
		3	FIFO Error Disable	R/W	0	0: Count FIFO errors 1: FIFO error count disabled
		2	Parallel Clock Detect Disable	R/W	0	0: Count clock detect errors 1: Clock detect count disabled
		1	Clock Loss of Signal Disable	R/W	0	0: Count clock loss of signal errors 1: Clock loss of signal count disabled
		0	Data Loss of Signal Disable	R/W	0	0: Count data loss of signal errors 1: Clock data of signal count disabled
28	LVDS Operation	7:2	Reserved		0	
		1	LVDS Loss of Signal Preset	R/W	0	1: Preset signal for LVDS loss of signal register
		0	LVDS Loss of Signal Reset	R/W	0	1: Clear signal for LVDS loss of signal register
29	Loss of Signal Status	7:6	Reserved		0	
		5	Clock Loss of Signal	R	0	0: Clock present 1: No clock present on TxCLKIN
		4:0	Data Loss of Signal	R	0	0: Data present 1: No data present on TxIN4:0
2A	Event Status	7:4	Reserved		0	
		3	TxCLKIN Detect	R/W	0	0: TxCLKIN not detected 1: TxCLKIN detected
		2	Reserved		0	
		1:0	Link Detect 1:0	R/W	0	0: Link not detected 1: Link detected

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
2B	Event Config	7	Reserved		0	
		6	PLL Lock Event	R/W	0	0: Count PLL lock events 1: Do not count PLL lock events
		5	Link Event	R/W	0	0: Count link events 1: Do not count link events
		4	Loss of Signal Event	R/W	0	0: Count loss of signal events 1: Do not count loss of signal events
		3	Event Count Select	R/W	0	0: Select PLL event count for reading 1: Select link event count for reading
		2	Clear PLL Error Count	R/W	0	1: Reset PLL error count. Self clearing bit.
		1	Clear Link Error Count	R/W	0	1: Reset link error count. Self clearing bit.
		0	Enable Count	R/W	0	0: Disable event counters 1: Enable event counters
2C	Event Count	7:0	Event Counter	R	0	
2D Reserved						
2E	Analog Driver	7	Reserved		0	
		6	Reverse Data Order	R/W	0	0: Normal 1: Reverse output data order
		5:2	Reserved	R/W	0	
		1	Link Detect 1	R/W	0	Link detect value for channel 1
		0	Link Detect 0	R/W	0	Link detect value for channel 0
2F	Tx Config	7:6	Reserved		0	
		5	Output Termination	R/W	1'b	0: 75 Ω terminations 1: 50 Ω terminations
		4	Link Start	R/W	1'b	0: Start when TxOUT0 or TxOUT1 link 1: Start when TxOUT0 and TxOUT1 linke
		3	Link Stop	R/W	1'b	0: Stop when TxOUT0 and TxOUT1 both links invalid 1: Stop when TxOUT0 or TxOUT1 break link, either link is invalid
		2	TxOUT Override	R/W	0	0: TxOUT0 enabled by default, TxOUT1_en pin controls channel1 1: Override enable of TxOUT0 and TxOUT1
		1	TxOUT1 Enable	R/W	0	0: TxOUT1 disabled 1: TxOUT1 enabled For proper operation of TxOUT1, the TxOUT1_EN pin must be held high.
		0	TxOOUT0 Enable	R/W	0	0: TxOUT0 disabled 1: TxOUT0 enabled
		30	Clock Delay	7:5	TxCLKIN Delay	R/W
4:0	Reserved				00010'b	
31–68 Reserved						

Addr (Hex)	Name	Bits	Field	R/W	Default	Description
69	Output Amplitude Adjust	7:3	Reserved		0	
		2:0	Amplitude Adjust	R/W	011'b	000: Level 7 001: Level 8 (Highest output) 010: Level 5 011: Level 6 (Normal output) 100: Level 4 101: Level 3 110: Level 2 111: Level 1 (Lowest output)

Register Recipes

Many features of the serializer contained within the SMBus registers require multiple writes to configure and enable. This methodology was implemented to prevent accidental register writes from causing undesired device behavior. Several recipes for common features are listed below. When experimenting with other SMBus register features, be sure to read through the register map for override and enable bits.

SCRAMBLER OVERRIDE CONTROL

The scrambler's default settings are described in the device configuration section. However, the scrambler's setting can be overridden if desired.

Reg 22'h, write 08'h

Reg 21'h, write to bit 3 to enable/disable

75Ω MODE

The serializer can be programmed to interface with 75Ω media by using the recipe shown below. The inverting serial output should be terminated when interfacing with single ended media.

Reg 2F'h, write 0 to bit 5

OUTPUT CHANNEL MUX CONTROL

DS32ELX0421 only. TxOUT0 is the output channel enabled by default. By using the external pin TxOUT1_EN, TxOUT1 will be activated along with TxOUT0. If an application requires that only one channel be active at a time, the following recipe allows for each channel to be enabled or disabled independent of the other.

Reg 2F'h, write 1'b to bit 2

Reg 2F'h, write to bits 1 or 0 to control the output channels

OUTPUT THE SERIAL CLOCK ON GPIO2

It is very helpful to be able to monitor high speed communication systems and observe their signal integrity. Generally,

this is done with a high speed real time oscilloscope or a sampling oscilloscope. Sampling oscilloscopes require a reference clock to trigger on. The following recipe can be used to bring out the serial clock on GPIO2 to provide a trigger for sampling oscilloscopes.

Reg 04'h, write 21'h

Power Save Mode

When a system does not need to transmit high speed data from the DS32EL0421 or DS32ELX0421, the power consumption of the device can be managed as described in the Power Management section on the Functional Description page. The following recipe powers down many of the analog and digital blocks in the serializer, but leaves the SMBus module operational. Please note that in order to resume normal operation the recipe below will have to be unwritten.

Reg 01'h, write 10'h

Reg 26'h, write 40'h

Redundancy / Fail Over Configuration

DS32ELX0421 only. Implementing a redundancy system with the DS32ELX0421 can be done in several ways. One method would be to program the redundancy or fail over logic into the host device or FPGA. The recipe below will describe a different method, for which a DS32ELX0421 will communicate to two different DS32EL0124 deserializers. The recipe below will configure the DS32ELX0421 serializer to automatically switch to the alternate output when the current high speed link fails.

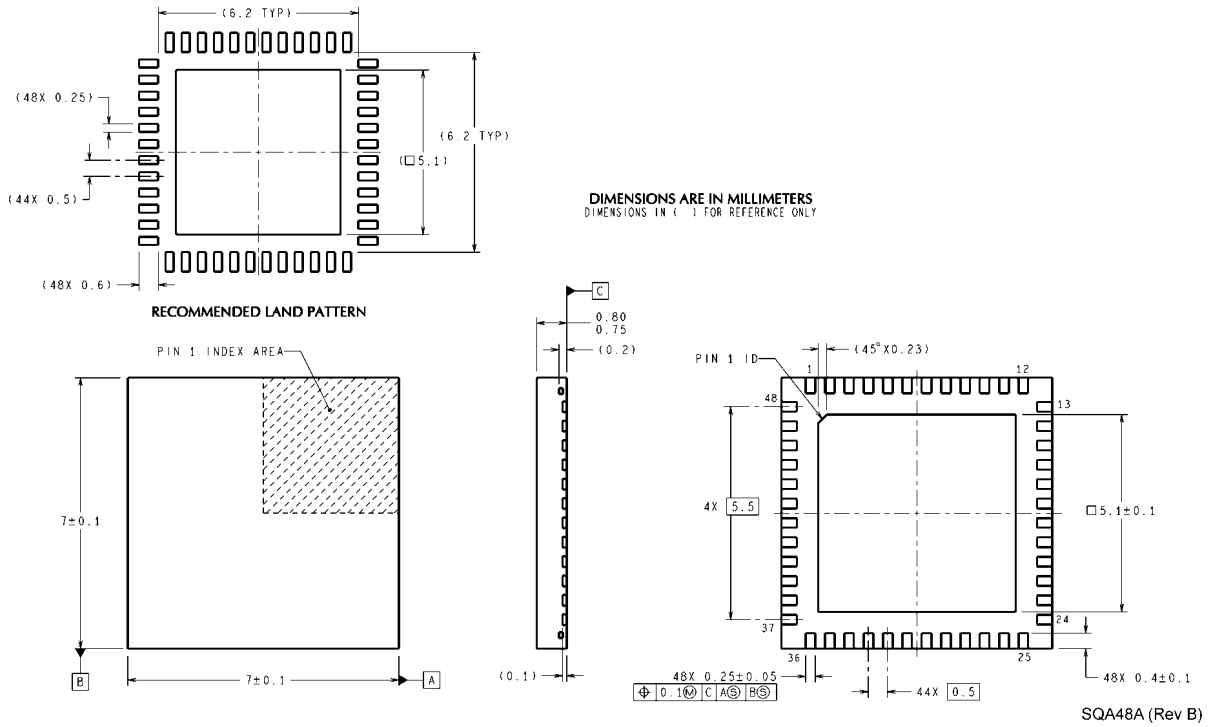
Configure all device with Remote Sense enabled either by pin or register control.

Pull TxOUT1_EN pin high

reg 2F'h, write 2D'h

Reg 2F'h, write 28'h

Physical Dimensions inches (millimeters) unless otherwise noted



Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:
www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/lido	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2010 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor
Americas Technical
Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe
Technical Support Center
Email: europe.support@nsc.com

National Semiconductor Asia
Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan
Technical Support Center
Email: jpn.feedback@nsc.com