National Semiconductor

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LM4312
Mobile Pixel Link Two (MPL-2), RGB Display Differential Interface Serializer with Optional Dithering and Look Up Table

General Description

The LM4312 is a MPL-2 Serializer (SER) that accepts a 24- or 18-RGB interface and serializes this wide bus to 3 differential signals. The optional Dithering feature can reduce 24-bit RGB to 18-bit RGB. The optional Look Up Table (Three X 256 X 8 bit RAM) is provided for independent color correction. 18-bit Bufferless displays from QVGA (320 x 240) up to >VGA (640 x 480) pixels are supported.

The interconnect is reduced from 28 LVCMOS signals (RGB888+V+H+DE+PCLK) to only 3 active differential signals (DD0P/M, DCP/M, DD1P/M) with the LM4312 Serializer and companion LM4310 Deserializer easing flex interconnect design, size constraints and cost.

The LM4312 SER resides by the application, graphics or baseband processor and translates the wide parallel video bus from LVCMOS levels to serial MPL-2 levels for transmission over a flex cable and PCB traces to the DES located in the display module.

When in Power_Down, the SER is put to sleep and draws less than 10µA. The SER can be powered down by stopping the PCLK or by asserting its PD* input pin.

The LM4312 implements the physical layer of the MPL-2 Interface and features robust common-mode noise rejection.

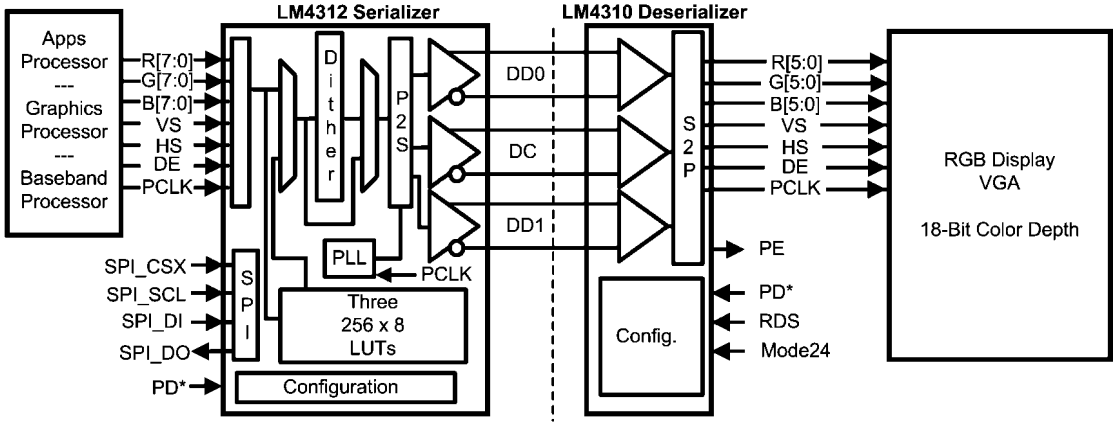
Features

- RGB Display Interface to >640 x 480 (VGA) Resolution
- 24 or 18-bit RGB Transport
- 24–to–18-bit RGB Dithering option
- Look Up Table option for independent color correction option
- Robust MPL-2 Differential SLVS Interface
- SPI Interface for configuration / control and LUT options
- Low Power Consumption & SLEEP state
- Auto Power Down on STOP PCLK
- Automatically generates frame sequence bits for resync upon data or clock error
- Odd Parity Generation

System Benefits

- Dithered Data Reduction
- Independent RGB Color Correction
- 24-bit Color Input
- Small Robust Interface
- Low Power & Low EMI

Typical Application Diagram - Bridge Chips - 24-bit to 18-bit RGB



[Supply, all Configuration pins, and bypass caps. and grounding not shown]

30011601

Ordering Information

NSID	Package Type	Package ID
LM4312	48L LLP, 6mm x 6mm x 0.4mm, 0.4mm pitch	TBD

Pin Descriptions

Pin Name	No. of Pins	I/O, Type	Description RGB Serializer
MPL-2 SERIAL BUS PINS			
DD0P, DD0M, DD1P, DD1M	4	O, MPL-2	MPL-2 Differential Data Line Driver True (Plus) and Compliment (Minus) Outputs Channel 0 and 1
DCP, DCM	2	O, MPL-2	MPL-2 Differential Clock Line Driver True (Plus) and Compliment (Minus) Outputs
SPI INTERFACE and CONFIGURATION PINS			
SPI_CSX	1	I, LVCMOS	SPI_Chip Select Input SPI port is enabled when: SPI_CSX is Low, PD* is High.
SPI_SCL	1	I, LVCMOS	SPI_Clock Input
SPI_DI	1	I, LVCMOS	SPI Data Input
SPI_DO	1	O, LVCMOS	SPI Data Output
PD*	1	I, LVCMOS	Power Down Mode Input PD* = Low, SER is in SLEEP Mode, SPI Registers are RESET, LUT Data is retained.
			PD* = High and PCLK = Stopped, SER is in SLEEP Mode, SPI Register settings are retained and LUT data is retained.
			PD* = High, Device is enabled.
RES1	1	I, LVCMOS	**Tie High**
TM	1	I LVCMOS	**Tie Low** H = Test Mode (Reserved)
VIDEO INTERFACE PINS			
PCLK	1	I, LVCMOS	Pixel Clock Input Video Signals are latched on the **RISING** edge.
R[7:0] G[7:0] B[7:0]	24	I, LVCMOS	RGB Data Bus Inputs – Bit 7 is the MSB. 24-bit Mode - use RGB[7:0] 18-bit Mode - use RGB[7:2], tie off RGB[1:0] to GND, do not float.
VS	1	I, LVCMOS	Vertical Sync. Input **This signal is used as a frame start for the Dither block and is required when Dither option is selected.** The VS signal is serialized unmodified.
HS	1	I, LVCMOS	Horizontal Sync. Input
DE	1	I, LVCMOS	Data Enable Input
POWER/GROUND PINS			
V_{DD}	7	Power Supply	Power Supply Pins. All VDD pins must be connect to power supply. 1.6V to 2.0V
V_{SS}	1	Ground	Ground Pin DAP pad must be connected to Ground.

Note:
I = Input, O = Output, IO = Input/Output. **Do not float unused input pins.**

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.3V to +2.2V
LVCMOS Input/Output Voltage	−0.3V to (V_{DD} +0.3V)
MPL-2 Output Voltage	−0.3V to V_{DD}
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
ESD Ratings:	
HBM, 1.5 kΩ, 100 pF	≥±2 kV
EIAJ, 0Ω, 200 pF	≥±200V
Maximum Package Power Dissipation Capacity at 25°C	
LLP Package	2.25 W
Derate LLP Package above 25°C	22.57 mW/°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DD} to V_{SS}	1.6	1.8	2.0	V
Pixel Clock Frequency (6X)	5		30	MHz
Pixel Clock Frequency (8X)	5		30	MHz
DC Frequency	30		240	MHz
Ambient Temperature	−40	25	85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
MPL-2								
V_{OD}	Differential Output Voltage	100 Ω Load	(Note 12)	V_{OD} setting	95	150	211	mV
				V_{OD} setting	140	200	270	
ΔV_{OD}	Delta Differential Output Voltage	Match of Differential Output Voltage magnitude between logic states.	(Note 12)	V_{OD} = 150		0	10	|mV|
				V_{OD} = 200		0	10	
V_{OS}	Differential Driver Offset Voltage	100 Ω Load	(Note 12)	V_{OD} = 150	112	150	188	mV
				V_{OD} = 200	150	200	250	
ΔV_{OS}	Differential Driver Offset Voltage Match	Match of Driver Offset Voltage magnitude between logic states.	(Note 12)	V_{OD} = 150		0	5	|mV|
				V_{OD} = 200		0	5	
R_{OUT}	Driver Output Impedance					50		Ω
LVCMOS (1.6V to 2.0V Operation)								
V_{IH}	Input Voltage High Level				0.7 V_{DD}		V_{DD}	V
V_{IL}	Input Voltage Low Level				GND		0.3 V_{DD}	V
V_{HY}	Input Hysteresis					100		mV
I_{IN}	Input Current				−1	0	+1	µA
V_{OH}	Output Voltage High Level	SPI_DO		I_{OH} = −1 mA	0.8 V_{DD}		V_{DD}	V
V_{OL}	Output Voltage Low Level			I_{OL} = 1 mA	V_{SS}		0.2 V_{DD}	V

Symbol	Parameter	Conditions		Min	Typ	Max	Units
SUPPLY CURRENT							
I_{DD}	Total Supply Current - RGB24 Mode. (Note 4)	DC = 240 MHz, Checker Board, LUT Enable, Dither Disable. (Note 5)	V_{OD} = 150		20		mA
			V_{OD} = 200		22	33	
		DC = 160 MHz, Checker Board, LUT Enable, Dither Disable	V_{OD} = 150		15		mA
			V_{OD} = 200		17		
	Total Supply Current - RGB18 Mode.	DC = 180 MHz, Checker Board, LUT Enable, Dither Disable.	V_{OD} = 150		17		mA
			V_{OD} = 200		19		
		DC = 120 MHz, Checker Board, LUT Enable, Dither Disable.	V_{OD} = 150		13		mA
			V_{OD} = 200		15		
I_{DDZ}	Supply Current—Disable Power Down Modes	PD* = L	Ta = 25°C		1	10	µA
		Stop Clock: PD* = H and PCLK = L or H			1	10	µA
PD	Power Dissipation	V_{OD} = 200 mV, V_{DD} = 1.8 V			27		mW

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PARALLEL BUS TIMING						
t_{SET}	Set Up Time	SER Inputs: RGB, VS, HS, DE to PCLK *Figure 1*	5			ns
t_{HOLD}	Hold Time	SER Inputs: PCLK to RGB, VS, HS, DE *Figure 1*	5			ns
MPL-2 SERIAL BUS TIMING						
t_{DVBC}	Serial Data Valid before Clock Edge	SER Data Pulse Width *Figure 2*, (Notes 11, 12)	0.3		0.7	UI
t_{DVAC}	Serial Data Valid after Clock Edge		0.3		0.7	UI
t_T	Transition Time	(Note 9)		300		ps
POWER UP TIMING						
t_{PLL}	PLL Lock Time			1024		PCLK cycles
t_{PZXclk}	Enable Time - Clock Start	PCLK to DC_{OUT} *Figures 4*, *8*		(Note 6)		
MPL-2 POWER OFF TIMING						
t_{PAZ}	Disable Time to Power Down	(Note 8)			15	ms
t_{PXZclk}	Disable Time - Clock Stop	PCLK to DC_{OUT} *Figure 3* (Note 10)		2		PCLK cycles
SPI INTERFACE						
t_{ACC}	SPI Data Active (SPI_DO)	*Figure 15*	0		50	ns
t_{OHR}	SPI Data Tri-State (SPI_DO)	*Figure 15*(Note 12)	0		50	ns

Recommended Input Timing Requirements (PCLK and SPI)

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PIXEL CLOCK (PCLK)							
f_{PCLK}	Pixel Clock Frequency	18-bit RGB Mode (6X)		5		30	MHz
		24-bit RGB Mode (8X)		5		30	MHz
$PCLK_{DC}$	Pixel Clock Duty Cycle			30	50	70	%
t_T	Input Transition Time	(Notes 7, 12)		2	>2		ns
$t_{STOPpclk}$	Clock Stop Gap	(Notes 10, 12)		4	2		PCLK cycles
SPI INTERFACE							
f_{SCLw}	SPI_SCL Frequency	WRITE				10	MHz
f_{SCLr}		READ				6.67	MHz
t_{s0}	SPI_CSX Set Time	*Figure 14*		60			ns
t_{s1}	SI Set Time			30			ns
t_{h1}	SI Hold Time			30			ns
t_{w1h}	SPI_SCL Pulse Width High	*Figures 14, 15*	WRITE	35			ns
			READ	60			ns
t_{w1l}	SPI_SCL Pulse Width Low		WRITE	35			ns
			READ	60			ns
t_r	SPI_SCL Rise Time	*Figure 14*			5		ns
t_f	SPI_SCL Fall Time				5		ns
t_{0H}	SI Hold Time			30			ns
t_{h0}	SPI_CSX Hold Time			65			ns
t_{w2}	SPI_CSX OFF Time			100			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{DD} =1.8V and T_A = 25°C.

Note 3: Current into a device pin is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to Ground unless otherwise specified.

Note 4: For IDD tests - input signal conditions are: (swing, edge, freq, DE = H, VS = L, HS = L, RGB Checkerboard Pattern: AAAAAA-555555)

Note 5: Total Supply Current Conditions: SER C_L= 15 pF, TYP V_{DD} = 1.8V.

Note 6: Enable Time is a complete MPL-2 start up t1+t2+t3. See also *Figure 8*.

Note 7: Maximum transition time is a function of clock rate and should be less than 30% of the clock period to preserve signal quality.

Note 8: Guaranteed functionally by the I_{DDZ} parameter. See also *Figure 9*.

Note 9: MPL-2 serial link transition time is measured from 20% to 80 %.

Note 10: This is the minimum time that the PCLK needs to be held off for in order for the device to be reset. Once PCLK is reapplied, a PLL Lock is required and start up sequence before video data is serialized.

Note 11: 1 UI is the serial data DD pulse width = 1 / 12xPCLK (18-bit mode), 1 UI is the serial data DD pulse width = 1 / 16xPCLK (24-bit mode)

Note 12: Specification is guaranteed by design or characterization

Timing Diagrams

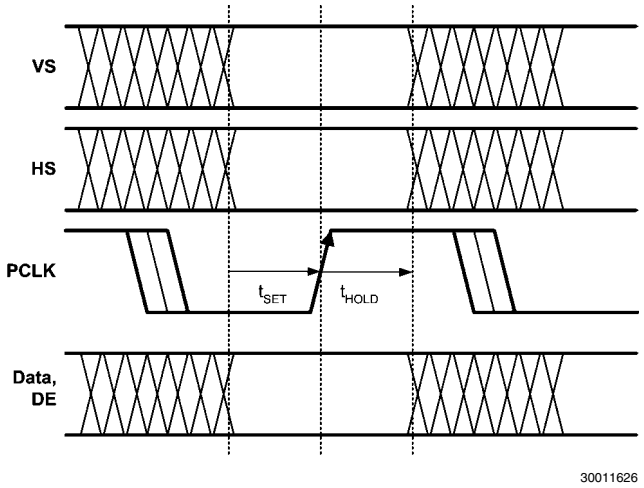


FIGURE 1. Input Timing for RGB Interface

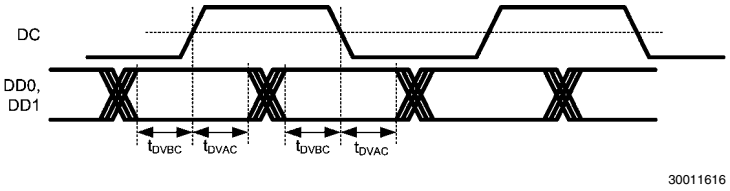


FIGURE 2. Serial Data Valid

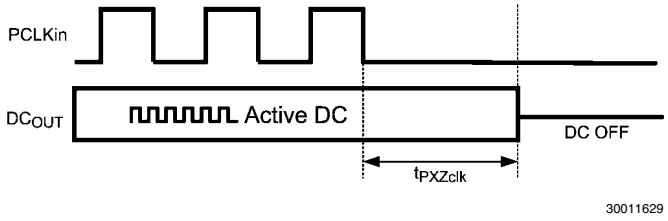


FIGURE 3. Stop Pixel Clock (PCLK) Power Down

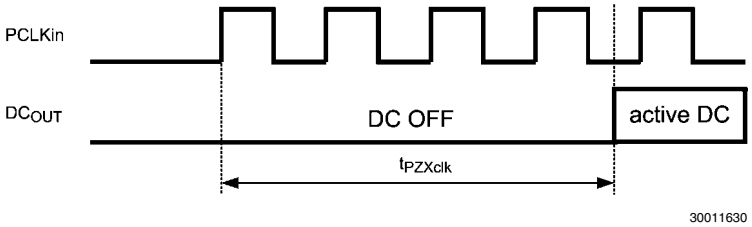


FIGURE 4. Stop Pixel Clock (PCLK) Power Up

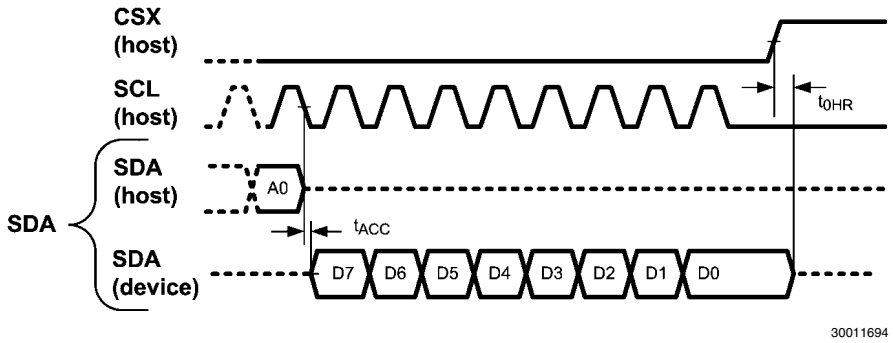


FIGURE 5. SPI Interface

Functional Description

The LM4312 is a Mobile Pixel Link two Serializer that serializes a 24-bit RGB plus three control signals (VS, HS, and DE) to two MPL-2 DD lines plus the serial clock DC line. 18-bit RGB, 24-bit RGB, or optionally 24-bit RGB data is dithered to 18 bits and then serialized and level translated to MPL-2 by the SER. An optional Look Up Table consisting of three 256 X 8-bit RAMs may also be used and is controlled via a 3 or 4-wire SPI interface. The LM4312 is compatible with the LM4310 Deserializer and also Display Drivers with integrated MPL-2 Deserializers.

Three link configurations are provided by the LM4312 SER. 24-bit RGB can be serialized onto the 2 DD + DC configuration using a 8X DC clock. 24-bit RGB can be dithered to 18-bit RGB and serialized onto the 2 DD + DC configuration using a 6X DC clock. Or 18-bit RGB can be serialized onto the 2 DD + DC configuration using a 6X DC clock. See *2DD+DC MPL-2 Link Options*. The device's default configuration is for 18 bits input, Dither OFF, and 6X mode.

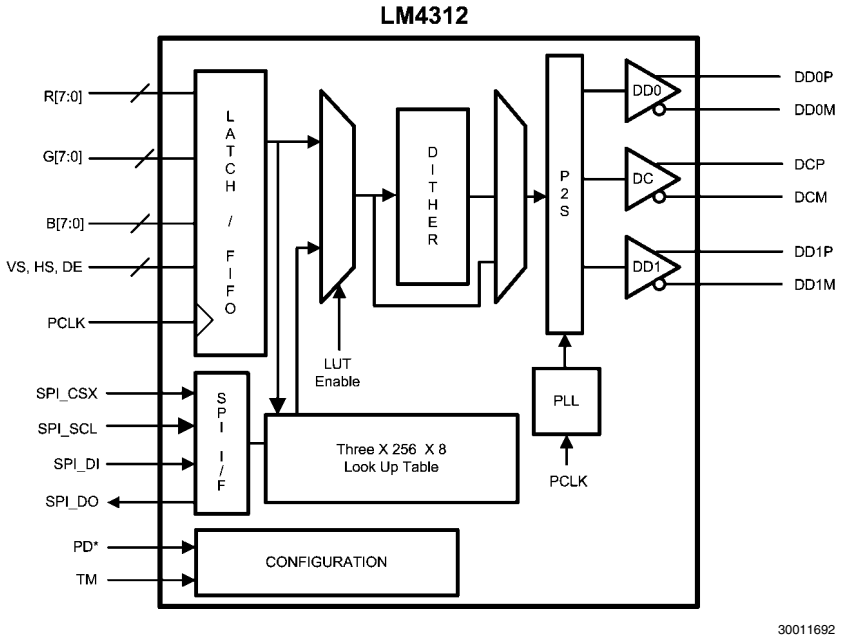


FIGURE 6. General LM4312 Block Diagram

2DD+DC MPL-2 Link Options

Input	Serial	Output	Notes
24-bit RGB	2 DD + DC, *Figure 10*	24-bit RGB	Dither OFF, DC = 8X PCLK
24-bit RGB	2 DD + DC, *Figure 11*	18-bit RGB	Dither ON, DC = 6X PCLK
18-bit RGB	2 DD + DC, *Figure 11*	18-bit RGB	Dither OFF, DC = 6X PCLK

BUS OVERVIEW

The LM4312 is a multi-lane MPL-2 Serializer that supports an 18-bit or 24-bit RGB source interface. The MPL-2 physical layer is purpose-built for robustness, low power and low EMI data transmission while requiring the fewest number of signal lines. No external line components are required, as termination is provided internal to the MPL-2 receiver. The differential interface conforms to the JEDEC SLVS (Scalable Low Voltage Signalling) Interface standard. A maximum raw throughput of >900 Mbps (2-lane raw) is possible with this chipset. The MPL-2 interface is designed for use with 80Ω to 100Ω differential lines. Lines may be microstrip or stripline construction.

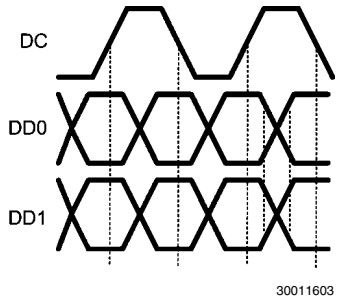


FIGURE 7. Dual Link Timing

SERIAL BUS TIMING

Data valid is relative to both edges of a RGB transaction as shown in *Figure 7*. Data valid is specified as: Data Valid before Clock, Data Valid after Clock, and Skew between data lines should be less than 500ps.

SERIAL BUS PHASES

There are three bus phases on the RGB MPL-2 serial bus. These are determined by the state of the DC and DD lines. The MPL-2 bus phases are shown in *Table 1*.

TABLE 1. Link Phases

Name	DC State	DDn State	Phase Description	Pre-Phase	Post-Phase
OFF (O)	GND	GND	Link is Off	A, or LU	LU
LINK-UP (LU)	L	L	Start Up	O	A or O
ACTIVE (A)	A	X	Streaming Data	LU	O

SERIAL BUS START UP TIMING

In the Serial Bus OFF phase, SER differential outputs are all driven to Ground.

When the SER is enabled, the differential outputs are driven to valid static High state until the SER PLL is locked. Then the DC becomes active and data is streamed to the DES.

Link-Up is shown in *Figure 8*. The DC and DDn signals are shown both as single-ended and differential waveforms.

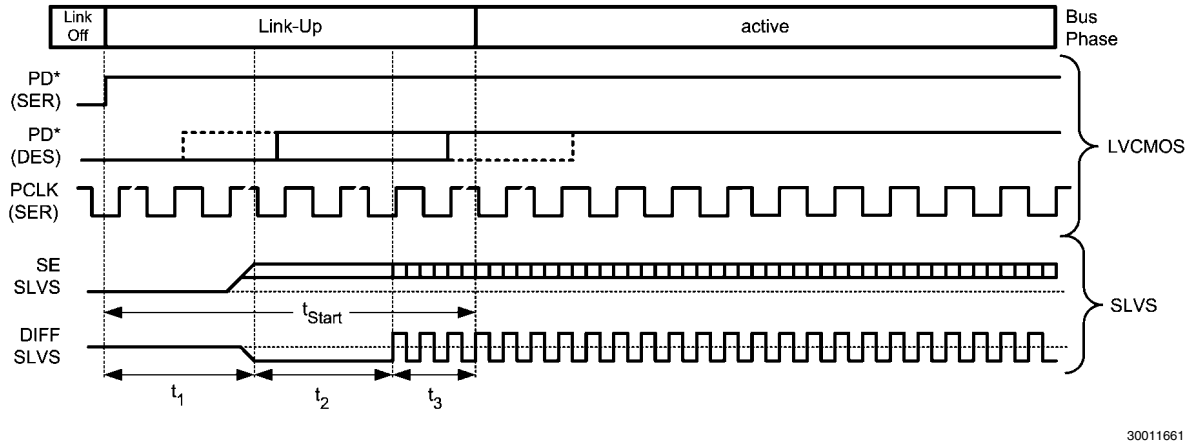


FIGURE 8. MPL-2 - LM4312 Link Up Timing

OFF PHASE

In the Serial Bus OFF phase, SER differential outputs are all driven to Ground. *Figure 9* shows the transition of the MPL-2 bus into the OFF phase.

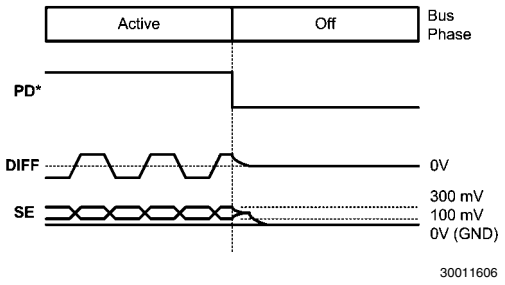


FIGURE 9. MPL-2 - LM4312 Link Off Timing

RGB VIDEO INTERFACE

The LM4312 is transparent to data format and control signal polarity timing. Each PCLK, RGB inputs, HS, VS and DE are sampled on the **rising edge** of the PCLK. A PCLK by PCLK representation of these signals is duplicated on the opposite device after being transferred across the MPL-2 interface.

The LM4312 can accommodate a wide range of display formats. QVGA to >VGA can be supported within the 5MHz to 30 MHz PCLK input range.

Three operating modes of the link are possible (see *2DD+DC MPL-2 Link Options*).

The 24-bit RGB (R[7:0], G[7:0], B[7:0]) color information is serialized, followed by the control bits VS (VSYNC), HS (HSYNC), DE (Data Enable) and PE (Odd Parity) and Frame Sequence (F[1:0]) bits. The DC clock is 8X the PCLK, and 32 serial bits are sent per PCLK. The two additional Reserved (Low) bits are sent to complete the payload.

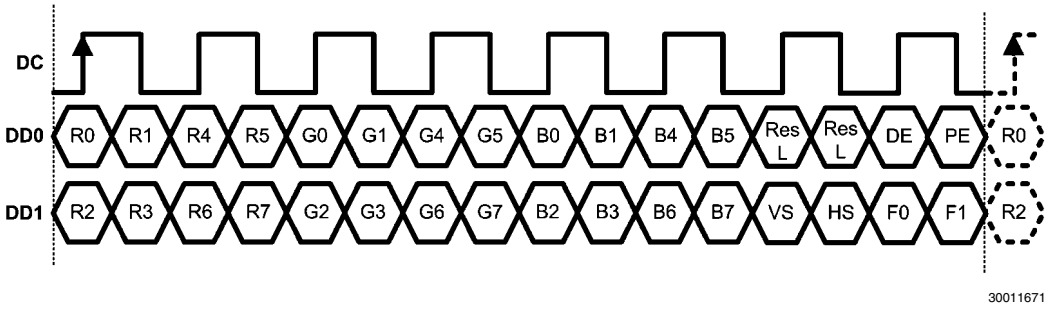


FIGURE 10. 24-bit RGB, 2 DD + DC Lane Serial Payload (8X)

When Dither option is enabled, the 24-bit RGB (R[7:0], G[7:0], B[7:0]) color information is Dithered to 18 bits, then serialized, followed by the control bits VS (VSYNC), HS (HSYNC), DE (Data Enable) and PE (Odd Parity) and Frame Sequence (F[1:0]) bits. The DC clock is 6X the PCLK, and 24 serial bits are sent per PCLK

With Dithering disabled, 18-bit RGB (R[7:2], G[7:2], B[7:2]) color information is serialized, followed by the control bits VS (VSYNC), HS (HSYNC), DE (Data Enable) and PE (Odd Parity) and Frame Sequence (F[1:0]) bits. Unused inputs (RGB[1:0]) must be tied off, do not float. The DC clock is 6X the PCLK, and 24 serial bits are sent per PCLK.

At a PCLK of 20.8 MHz, a 125 MHz DC clock is generated. The data lanes use both clock edges, thus 250 Mbps (raw) are sent per DD lane for a 500Mbps maximum throughput for the 2DD+DC configuration.

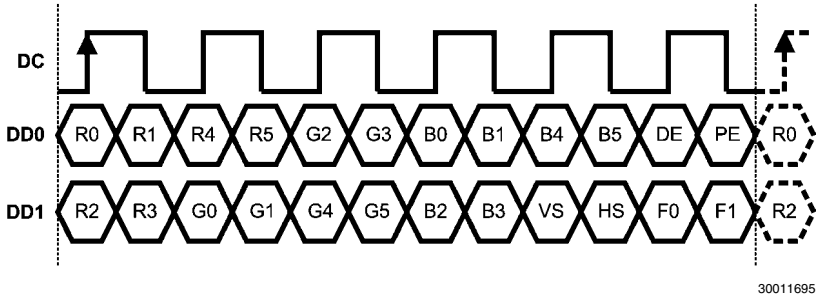


FIGURE 11. 24-bit dithered to 18-bit RGB / 18-bit RGB, 2 DD + DC Lane Serial Payload (6X)

SERIAL PAYLOAD PARITY BIT

Odd Parity is calculated on the RGB bits, control (VS, HS, and DE) bits and F0, F1 bits and then sent from the SER to the DES via the serial PE bit. See DES Data sheets to determine how the parity bit is handled by the DES device.

FRAME SEQUENCE — SYNC DETECT AND RECOVERY

If a data error or clock slip error occurs over the MPL-2 link, the RGB MPL-2 Deserializer can detect this condition and quickly recover from it. The method chosen is a data transparent method, and has very little overhead because it does not use a data expansion coding method. For the 18-bit RGB color transaction, it uses two bits that are already required in the 6 DC cycle transaction. Total overhead for each pixel is 3/24 or 12.5%, where the 3 bits are PE, F0 and F1.

The LM4312 MPL-2 RGB Serializer simply increments the two bit field F[1:0] on every pixel (MPL-2 frame) transmitted. Therefore every four MPL-2 frames, the pattern will repeat. It is very unlikely that this pattern would be found within the payload data, and if it were found, the probability that it would repeat for many frames becomes infinitely small. This code is used by the MPL-2 Deserializer to detect any frame alignment problems and quickly recover.

The RGB MPL-2 Deserializer, upon a normal power up sequence, uses the FS bits to obtain bit alignment. Once this is obtained, correct pixel data is recovered and driven to the display. If synchronization is lost for any reason, the DES searches for the incrementing pattern. Once found, it resynchronizes the output pixel data and timing signals. See MPL-2 DES Datasheet for details on how the specific DES handles the Frame Sequence.

OPTIONAL DITHERING FEATURE

The LM4312 provides an optional Dithering mode. When selected, 24-bit RGB input data is internally dithered to 18-bits

using a high-quality stochastic dithering process. This process has a "blue noise" characteristic that minimizes the visibility of the dither patterns. The resulting data stream of 18-bit data is then serialized and transmitted via MPL-2.

The Dither circuitry requires the VS control signal for proper operation. This signal is used to generate an internal signal that marks the start of the (video) frame. The serializer samples and sends the VS information unmodified.

Dithering parameters are controlled by two registers. When the dithering is bypassed, only RGB[7:2] is serialized and transmitted for 18-bit input RGB [5:0] (MSB aligned). Input RGB[1:0] should not be connected and the unused inputs should be tied low; do not float. **Dithering option is off by default.**

OPTIONAL LOOK UP TABLE

The look up table is comprised of three 256 Byte SRAMs. It may be used for independent color correction. When the LM4312 is in the 24-bit RGB mode, the full 8-bits per color are used for addressing the 256 Bytes for each color. When the LM4312 is used in an 18-bit RGB mode and the LUT is desired, all 8-bits per color are still used for the LUT look-up. The 6 active bits from each color are used for addressing 64 locations in the LUT. The two LSBs of the 8-bit bus can be tied to 00, and every fourth location of the SRAM where the two LSBs equal 00, (addresses 0x00, 0x04, 0x08, 0x0c, etc.) will be used." Or, the two LSBs of the 8-bits can be tied to 01 and every fourth location of the SRAM where the low two bits equal 01(addresses 0x01, 0x05, 0x09, 0x0d, etc.) will be used and so on. Selecting the two LSBs with GPIOs (0x0, 0x1, 0x2, and 0x3) allows for four different color correction tables to be accessed. The LUT is disabled by default and also after a device PD* cycle. The PD* cycle can be entered via the PD* input pin directly, or by stopping the PCLK. When stop PCLK is used to disable the device, LUT data is retained. Before using the LUT, the SRAM must be loaded with its contents. If power is cycled to the device, the LUT must be loaded again.

To enable the LUT:

1. Select/Unlock the LM4312 SPI Interface - Write 0xFF to REG 0x16
2. Write the LUT contents to the SRAM using Writes or Page Writes
3. Enable the LUT - Write a 0x01 to REG 0x00
4. De-Select/Lock the LM4312 SPI interface - Write 0x00 to REG 0x16

When waking up the LM4312 from the power down mode (PD*=L), the LUT needs to be enabled if it is desired, and the contents to the SRAM are still held and valid.

1. Select/Unlock the LM4312 SPI Interface - Write 0xFF to REG 0x16
2. Enable the LUT - Write a 0x01 to REG 0x00
3. Optional -select desired Level Select - if not using default value
4. De-Select/Lock the LM4312 SPI interface - Write 0x00 to REG 0x16

If power is cycled to the device, the LUT SRAMs must be loaded again.

SPI INTERFACE

The Serial Peripheral Interface (SPI) allows control over various aspects of the LM4312, the Look Up Table operation, and access to the three 256 x 8-RAM blocks. Three SPI transactions are supported, which are: 16-bit WRITE, PAGE WRITE, and a 16-bit READ. The SPI interface is disabled when the device is in the sleep mode via the PD* pin (PD* = L). The SPI interface may be used when PD* = H or when the device is in SLEEP via the PCLK stop feature. A device (SER) reset function is also available via the Configuration 3 register bit 1.

Due to the Select/Unlock – De-Select/Lock feature of the device the SPI interface may be shared with the display driver. Several connection configurations are possible. A couple examples are shown in *Figure 12* and *Figure 13*. SPI_DI and SPI_DO may be tied together to form a bi-directional SDA line. If READs are not required, leave the SPI_DO pin as a NC.

16-bit WRITE

The 16-bit WRITE is shown in *16-bit WRITE – SPI*. The SPI_DI payload consists of a "0" (Write Command), seven address bits and eight data bits. The SPI_CSX signal is driven Low, and 16-bits of DI (data input) are sent to the device. Data is latched on the rising edge of the SPI_SCL. After each 16-bit WRITE, SPI_CSX must return HIGH.

16-bit WRITE – SPI

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DI	0	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

16-bit READ

The 16-bit READ is shown in *16-bit READ – SPI*. The SPI_DI payload consists of a "1" (Read Command), seven address bits. The SPI_DO consists of eight data bits which are driven from the device. The SPI_CSX signal is driven Low, and the host drives the first 8 bits of the DI ("1" and seven address bits), the device then drives the respective 8 bits of the data on the DO signal.

16-bit READ – SPI

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DI	1	A6	A5	A4	A3	A2	A1	A0	Z	Z	Z	Z	Z	Z	Z	Z
DO	Z	Z	Z	Z	Z	Z	Z	Z	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

PAGE WRITE

The PAGE WRITE is shown in *Figure 16*. The SPI_DI payload consists of a "0" (Write Command), seven address bits of the start address and then the consecutive data bytes. 256 bytes maximum can be sent. The SPI_CSX signal is driven Low, and the host drives the SDA signal with a "0" (Write Command), the seven start address bits and the variable length data bytes. The Page Write is denoted by the SPI_CSX signal staying low while the data bytes are streamed. Data is latched on the rising edge of the SPI_SCL.

There are four SPI Interface signals: SPI_CSX - SPI Chip Select, SPI_SCL - SPI Clock, DI - SPI Data In and DO - SPI Data Out. SPI_CSX, SPI_SCL and SPI_DI are inputs on the LM4312. SPI_DO is the Data Output line for the READ_DATA portion of a READ operation. READs are optional and are not required.

PAGE WRITE

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DI	0	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
		(start address)							(Data Byte 0)							
DI	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
	(Data Byte 1)								(Data Byte n, 256 max.)							

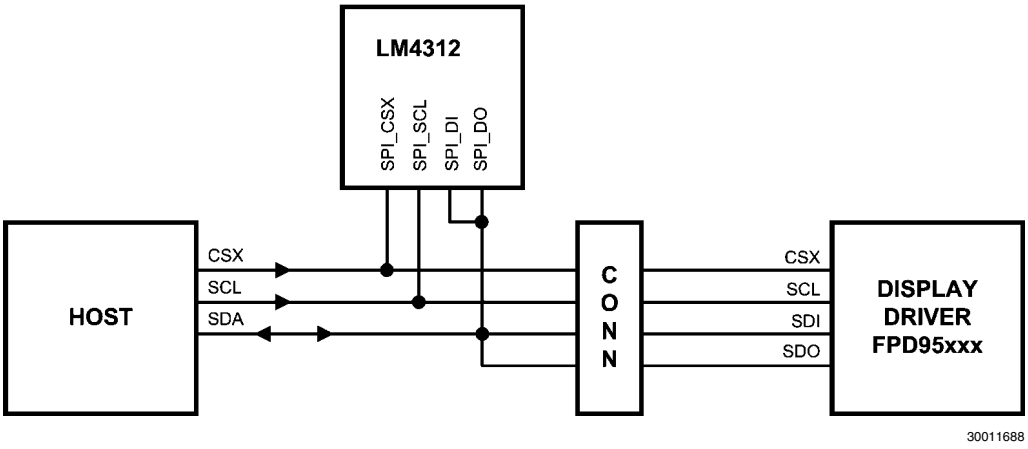


FIGURE 12. LM4312 WRITE & READ to 3-signal SPI HOST

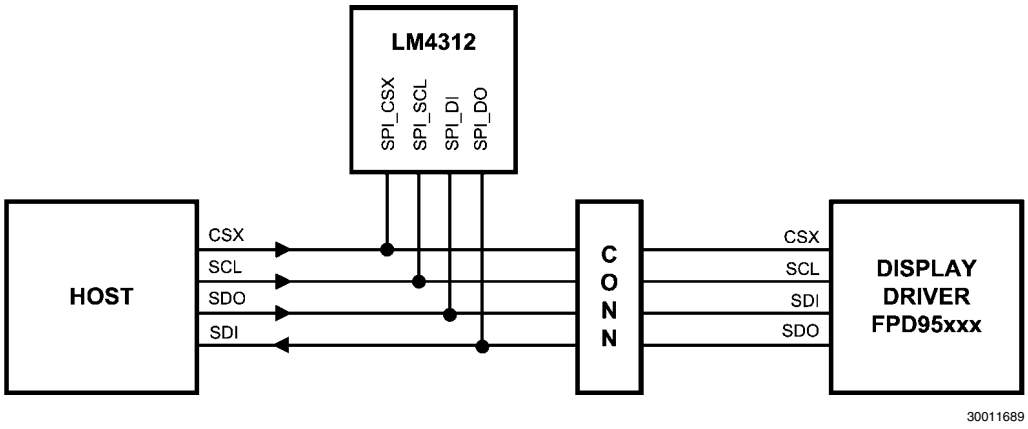


FIGURE 13. LM4312 WRITE & READ to 4-signal SPI HOST

LM4312 SPI Registers

Name	Address	Type	Description	Default
Command	0x00	R/W	Bit 0 = LUT Enable 0'b = LUT Disabled, 1'b = LUT Enabled Bit 4 = Special Register Access 0'b = SRA Locked, 1'b = SRA Unlocked For access to Registers 0x08, 0x09, 0x0B, the Special Register Access bit must be unlocked. Must write all 8 bits.	0x00
Reserved, (Note 15)	0x01	na	**Reserved**	
LUT Red RAM Address	0x02	R/W	Red Address - This register contains the address for the next access to the Red LUT RAM. After every read or write access to the Red Data Register, this register auto-increments.	0x00
LUT Red RAM Data	0x03	R/W	Red Data	0xXX
LUT Green RAM Address	0x04	R/W	Green Address - This register contains the address for the next access to the Green LUT RAM. After every read or write access to the Green Data Register, this register auto-increments.	0x00
LUT Green RAM Data	0x05	R/W	Green Data	0xXX
LUT Blue RAM Address	0x06	R/W	Blue Address - This register contains the address for the next access to the Blue LUT RAM. After every read or write access to the Blue Data Register, this register auto-increments.	0x00
LUT Blue RAM Data	0x07	R/W	Blue Data	0xXX
Dither Configuration1 (Note 14)	0x08	R/W	Bit 0 - Dither Bypass 1'b = Bypass Dither, 0'b = Dither ON Bit 1 - DE INV 1'b = Active Low DE, 0'b = Active High DE Does not alter DE signal, dither block input only. Bit 2 - VS INV 1'b = Active Low VS signal, 0'b = Active High VS signal. Does not alter VS signal, dither block input only. Bit 4 - Tempen0 1'b = Transposed Dither Pattern, 0'b = Even and odd frames use same dither pattern Bit 5 - Tempen1 1'b = Temporal Dithering is Enabled, 0'b = Disabled Bit 6 - Dith3 - Dither Amplitude 1'b = set to 3 bits, 0'b = set to 4 bits	0x65
Dither Configuration2 (Note 14)	0x09	R/W	Dither Parameter **Reserved**, Default value recommended.	0x67
Reserved	0x0A	na	**Reserved**	
Configuration 3, (Note 14)	0x0B	R/W	Bit 0 - Mode 24 1'b = 24-bit RGB Mode, 0'b= 18-bit RGB Mode Bit 1 - SER_PD 1'b = RESET the SER, 0'b = normal mode Bit[5:4] - Driver Level Select 00'b = VOD = 200mV 01'b = VOD = 150mV	0x00
Reserved, (Note 15)	0x0C-0x15	na	**Reserved**	
Device Select (Unlock/Lock)	0x16	R/W	0xFF'h enables LM4312 SPI All other values disables LM4312 SPI (0x00 to 0xFE)	0x00
Reserved, (Note 15)	0x17-0x7F	na	**Reserved**	

Note 13: If a WRITE is done to a reserved bits, data should be all 0's. If a READ is done to a reserved location, either 1's or 0's may be returned. Mask reserved data bits.

Note 14: This register must be unlocked first through bit 4 of register 0. This register is currently a write only register, read is not supported.

Note 15: DO NOT write to Reserved Registers.

SPI RESET BIT

Configuration 3 register, bit 1 is a device RESET function. When this bit is set to a 1, the device is placed into reset. When this bit is a 0, the device is in normal mode and is controlled by the PCLK and PD* signal pins.

SPI Timing

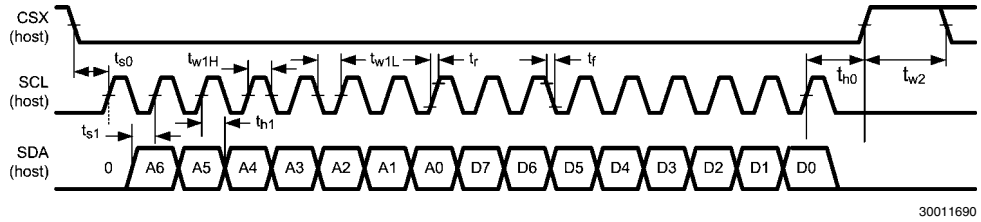


FIGURE 14. 16-bit SPI WRITE

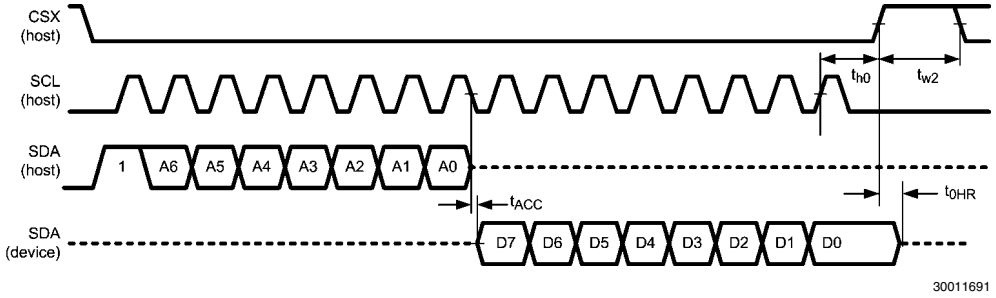


FIGURE 15. 16-bit SPI READ

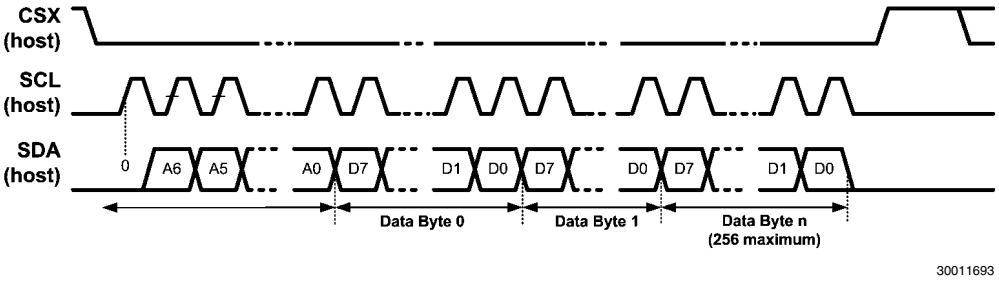


FIGURE 16. SPI Page Write

Figures 14, *15*, *16* show a 3–wire SPI Interface with the (LM4312) SPI_DI and (LM4312) SPI_DO pins tied together to form a bi-directional SPI data signal SDA. In the 16–bit READ, the SPI HOST drives the first 8 bits of the operation, and the SPI target (LM4312) drives the last 8 bits as shown in *Figure 15*.

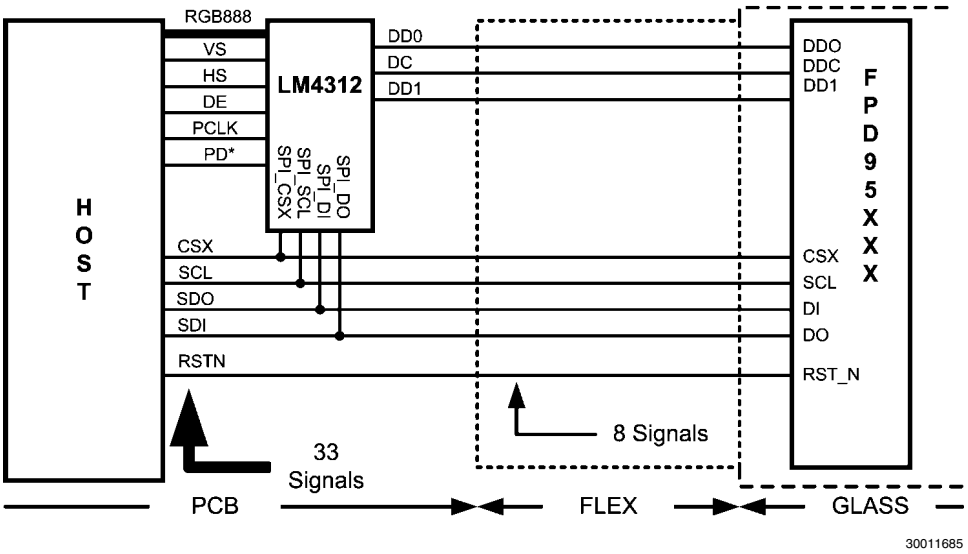


FIGURE 17. Typical Application Connection Diagram

In *Figure 17*, 33 host signals are reduced to only 7 or 8 signals. The reduced width interface to the display includes: 3 differential signals (DD0, DC, DD1), a Display Driver Reset signal (RSTN) and 3 or 4 wire SPI interface.

LM4312 Operation

POWER SUPPLY & BYPASS RECOMMENDATION

The V_{DD} power supply pins are intended to be connected together to the same plane.

Bypass capacitors should be placed near the power supply pins of the device. Use high frequency ceramic (surface mount recommended) 0.1 µF capacitors. A 2.2 to 4.7 µF Tantalum capacitor is recommended near the SER for PLL bypass. Connect bypass capacitors with wide traces and use dual or larger via to reduce resistance and inductance of the feeds. Utilizing a thin spacing between power and ground planes will provide good high frequency bypass above the frequency range where most typical surface mount capacitors are less effective. To gain the maximum benefit from this, low inductance feed points are important. Also, adjacent signal layers can be filled to create additional capacitance. Minimize loops in the ground returns also for improved signal fidelity and lowest emissions.

UNUSED INPUT PINS

Unused inputs **must** be tied to the proper input level — do not float.

PHASE-LOCKED LOOP

A PLL is enabled to generate the serial link clock. The Phase-locked loop system generates the serial data clock at 6 or 8 of the input clock depending upon 18 or 24-bit RGB transport mode (set by SPI Register).

SLEEP MODE & STOP CLOCK

The LM4312 (SER) can eneter SLEEP (Low Power state) by two methods. The PD* pin is one method, the other is by stopping the PCLK input (to a static level).

The PD* Input pin may be controlled by the Host. When PD* = High, the SER is enabled. When the PD* = Low, the SER is in SLEEP Mode. Note that SPI Registers are reset to defult values, and LUT data is retained.

When using the auto power down mode, the PD* input needs to be held High. When the PCLK is held static, the SER will detect this condition and power down. When the PCLK is restarted, the SER powers up. See *Figures 3*, *4* and *Figure 8*. The stopping of the pixel clock should be done cleanly. The minimum clock stop gap should be at least 4 PCLK cycles wide. Floating of the PCLK input pin is not recommended. Consult the MPL-2 DES datasheet to determine requirements that the DES requires. When the SER is in SLEEP by the STOP CLOCK feature, SPI Register and LUT contents are retained.

If power is removed from the device, SPI Register and LUT contents are reset upon power up.

LM4312 Memory Status (LUT and SPI Registers)

Mode	LUT	SPI Registers
Power Cycle VDDs = 0V	LUT contents are reset	Registers RESET to Defaults
Sleep State PD* = L	LUT contents retained	Registers RESET to Defaults
Sleep State PD* = H and PCLK = static (H or L)	LUT contents retained	Register contents retained

Application Information

SYSTEM BANDWIDTH CALCULATIONS

For a HVGA (320 X 480) application with the following assumptions: 60 Hz refresh rate, 10% blanking, RGB666, the following calculations can be made:

Calculate PCLK - 320 X 480 X 1.1 X 60 = 10.14 MHz PCLK

Calculate DC rate - since the application is 2 DD + DC and RGB666, PCLK X 6 is the DC rate or 60.83 MHz. Also check that this DC rate does not exceed the DC maximum rate for the chipset.

Calculate DD rate - MPL-2 uses both edges of the DC to send serialized data, thus data rate is 2X the DC rate, or 121.7 Mbps per DD lane in our example.

Calculate the application throughput - using 2 DD lanes, throughput is 2 X of the DD rate or 243.3 Mbps of raw band width.

For a VGA (640 X 480) application with the following assumptions: 60 Hz refresh rate, 35% blanking, RGB888, the following calculations can be made:

Calculate PCLK - 640 X 480 X 1.35 X 60 = 24.88 MHz PCLK

Calculate DC rate - since the application is 2 DD + DC and RGB888, PCLK X 8 is the DC rate or ~ 200 MHz.

Calculate DD rate - MPL-2 uses both edges of the DC to send serialized data, thus data rate is 2X the DC rate, or 400 Mbps per DD lane in our example.

Calculate the application throughput - using 2 DD lanes, throughput is 2X of the DD rate or 800 Mbps of raw band width.

SYSTEM CONSIDERATIONS

Typical VGA RGB888 Operation

A Smart Display application is shown in *Figure 18*. The Serializer (SER) resides by the host (BBP) and connects to a Memory Interface. BBP Bus signals are connected as shown (PCLK, Data, DE, PD*, VS, HS, and SPI signals). The device can be configured for 18-bit or 24-bit RGB interfaces. RGB signals are samples on the rising edge of the PCLK, and the serial data lines use both edge of the serial clock. The SER requires a pixel clock reference which is typically 25 MHz in a VGA application. This signal is used to generate the serial DC clock. The PCLK input is multiplied by the selected PLL multiplier to determine the serial clock rate. In the 25 MHz PCLK and 8X application, the DC rate will be 200 MHz. Due to the serial transmission scheme using both clock edges, the raw bandwidth is 400 Mbps per lane and device throughput is 800 Mbps. Dither and LUT options are OFF by default and can be turned ON by device SPI programming. The SER has a SLEEP mode to save power when the display is not active. The Sleep state is entered when the PD* signal is driven Low. It is also entered if the PD* signal is High and the PCLK input is stopped. When PCLK stop is used to place SER into Sleep mode, the SPI registers and the LUT content are retained. In the Sleep state, supply current into the SER is >1µA typical. Several configuration pins are also required to be set. For a SER, tie TM = L and RES1 = H. The DES recovers the serial signals and generates the parallel bus for the Display.

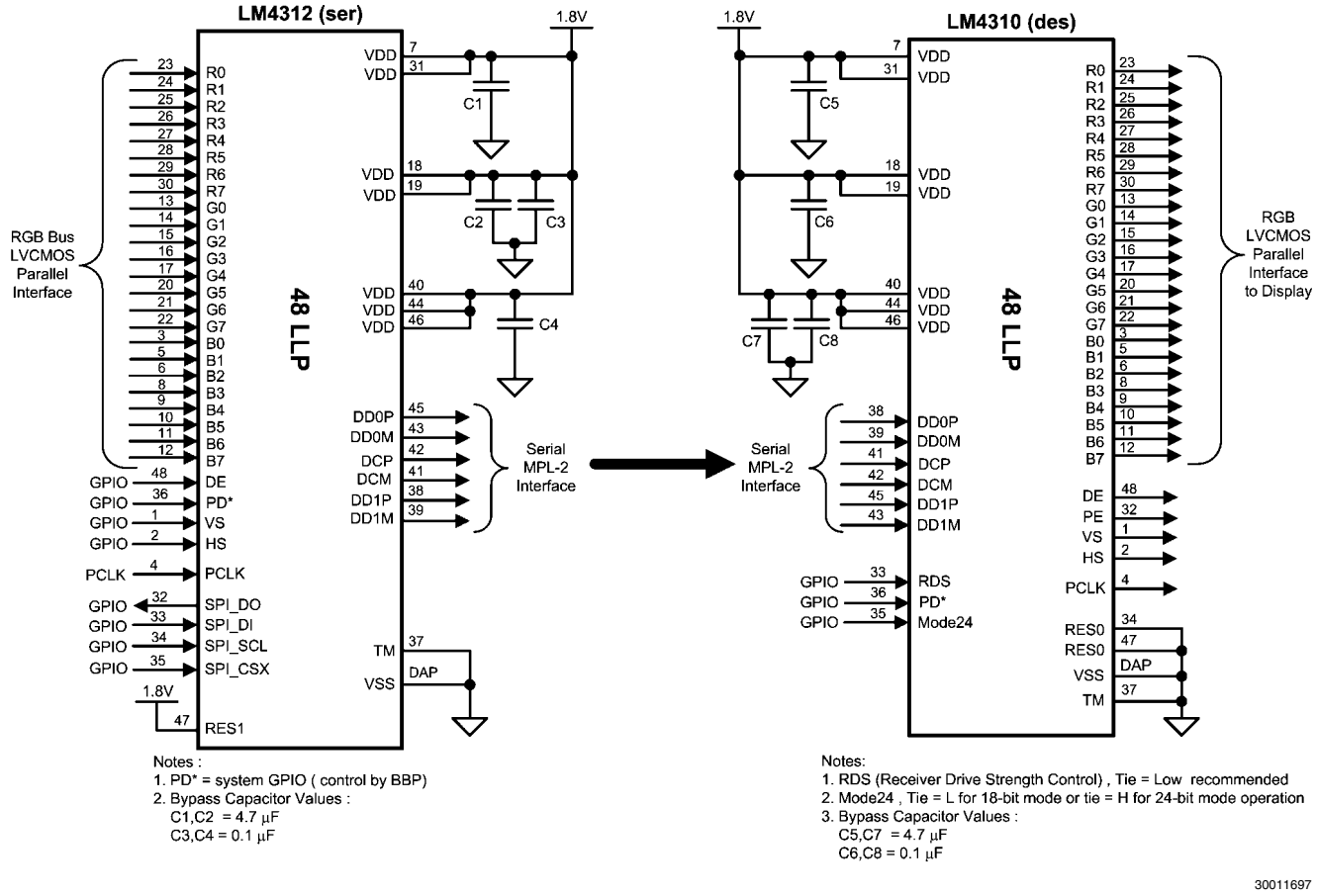


FIGURE 18. Typical VGA RGB888 Connection Diagram

The DES VDD is set to be compatible with the Display(s) employed. Depending on application, the Mode24 and RDS may be tie to high, low or connected to BBP (GPIO) pins. The PD* should be tied to PD* pin on SER device. The other signals DE, VS, and HS signals are outputs only. The connection between the DES device and the display(s) should be done such that long stubs are avoided. The DES has user adjustable edge rate controls for the parallel bus outputs. This can be used to optimize the edge rate vs. the required VDD magnitude. This allows for using softer edges on the wide parallel data bus signals. The DES also provides a PE pin to flag any parity errors detected. This signal maybe routed back to the host for monitoring, or bought out to a test point. The DES supports 18-bit for 24-bit mode. These modes are obtained by setting the MODE24 pin to a logic Low for 18-bit mode or to logic High for 24-bit mode. The Sleep state of the display may be entered by driving the PD* signal to a logic Low. This pin should be connected SED PD* pin. Several configuration pins are also required to be set. For a DES, tie TM = L and RES0 = L.

FLEX CIRCUIT RECOMMENDATIONS

The MPL-2 lines should generally run together to minimize any trace length differences (skew). For impedance control and also noise isolation (crosstalk), guard ground traces are recommended in between the signals. Commonly a Ground-Signal-Signal-Ground (GSSGSSG) layout is used. Locate fast edge rate and large swing signals further away to also minimize any coupling (unwanted crosstalk). In a stacked flex interconnect, crosstalk also needs to be taken into account in the above and below layers (vertical direction). To minimize any coupling locate MPL-2 traces next to a ground layer. Power rails also tend to generate less noise than LVCMOS so they are also good candidates for use as isolation and separation.

The interconnect from the SER to the DES may act like a transmission line. Thus impedance control and ground returns are an important part of system design. Impedance should be in the 80 to 100 Ohms for the differential pair.

GROUNDING

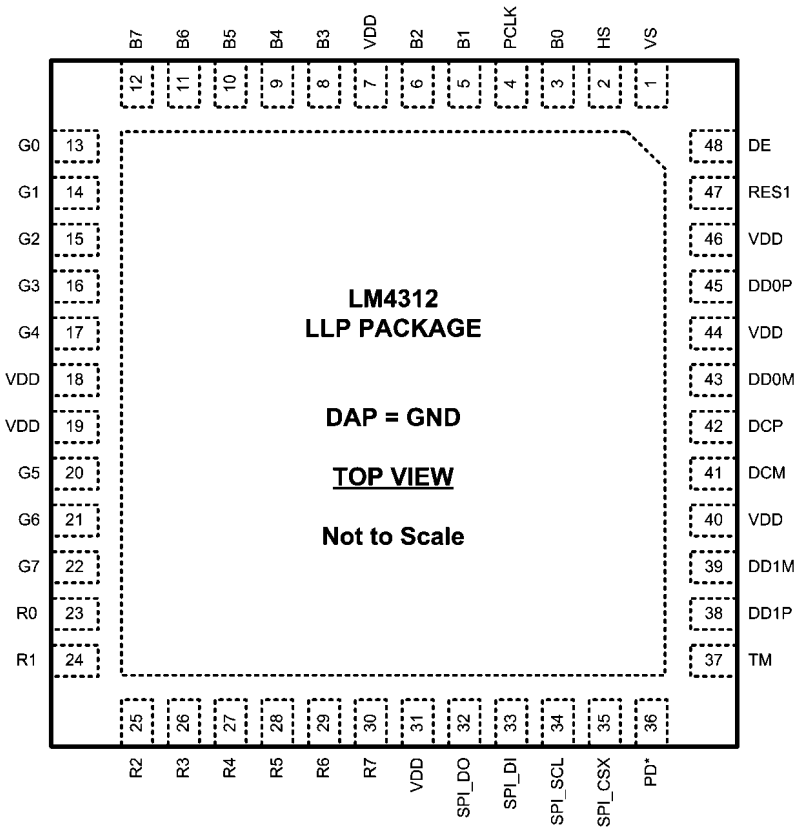
The LM4312 offered in the 48 LLP package uses the center DAP Pad for the Ground connection. This pad **MUST** be connected to Ground for proper device operation.

PCB RECOMMENDATIONS

General guidelines for the PCB design:

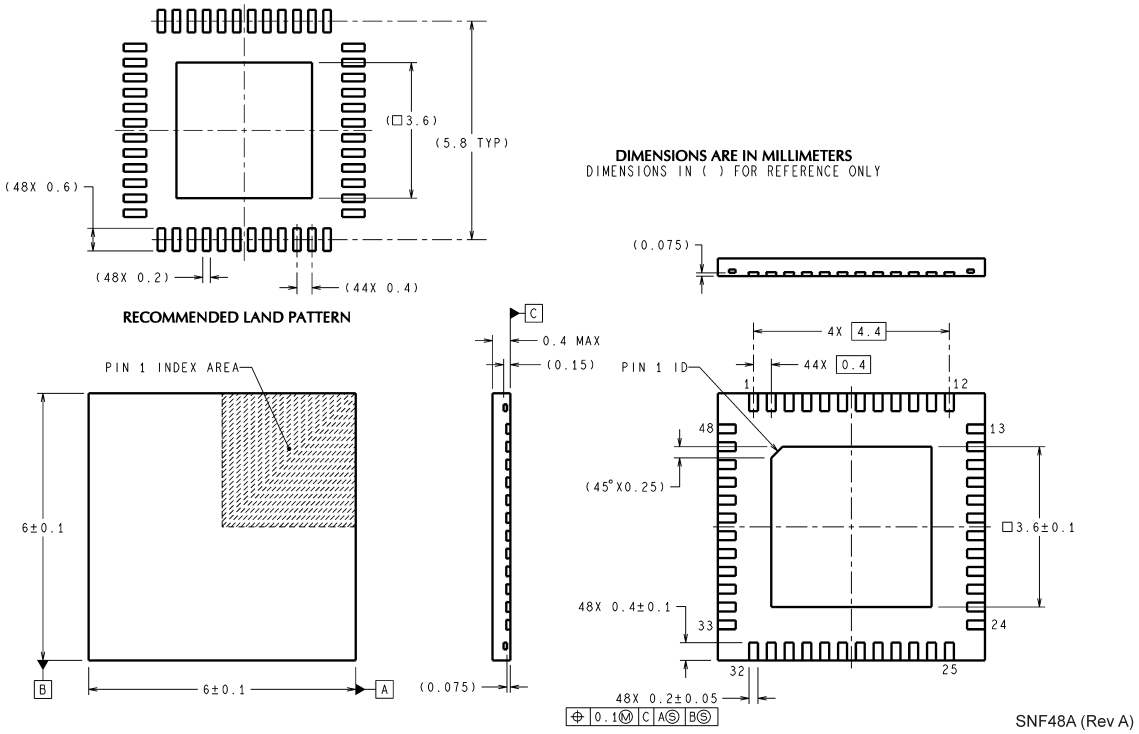
- Floor plan - locate MPL-2 SER near the connector to limit chance of cross talk to high speed serial signals.
- Route serial traces together, minimize the number of layer changes to reduce loading.
- Use ground lines as guards to minimize any noise coupling (guarantees distance).
- Avoid parallel runs with fast edge, large LVCMOS swings.
- Also use a GSSG pinout in connectors (Board to Board or ZIF).
- DES device - follow similar guidelines.
- Bypass the device with MLC surface mount devices and thinly separated power and ground planes with low inductance feeds.
- High current returns should have a separate path with a width proportional to the amount of current carried to minimize any resulting IR effects.
- See AN-1187 LLP Package Application Note for SMT Assembly Recommendations

Connection Diagram 48L LLP Package



TOP VIEW
(not to scale)

Physical Dimensions inches (millimeters) unless otherwise noted



48L LLP, 0.4mm pitch
Order Number LM4312SM
NS Package Number SNF48A

Notes

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