GENERAL DESCRIPTION

The main function of the SX8722 is to acquire signal from Wheatstone bridges or single ended sensors.

The input can be a pressure sensor, a GMR or AMR magnetic sensor, a chemical sensor, a thermistor or a mix of several of these sensors.

The SX8722 Sensor interface is totally configurable through an I2C compatible interface.

Several parameters are configurable through this interface such as alarms or signal post processing.

APPLICATION

- Pressure sensing (industrial, altimeter, diving computer)
- Chemical sensing (monitoring, security)
- Magnetic sensing (compass)

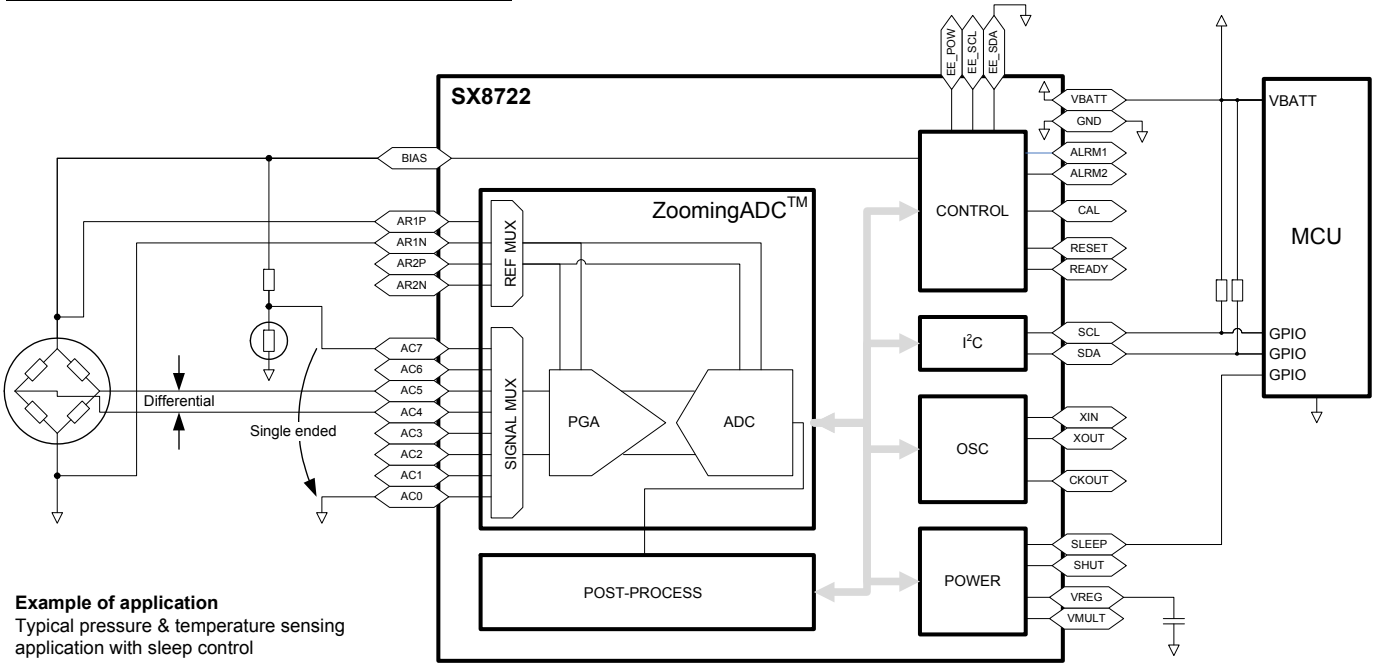
ORDERING INFORMATION

Part Number	Temperature Range	Package
SX8722I070LF	-40°C to 125°C	MLPQ44-7x7

Tools	Part number
Evaluation Kit	XE8000EV120

KEY PRODUCT FEATURES

- 16 + 10 bits differential acquisition
- Preamplifier programmable gain up to 1000
- Sensor offset compensation up to 15 times full scale of input signal
- 4 differential or 7 single ended signal inputs
- 2 differential reference inputs
- I2C compatible connection to application
- Internal RC and 32 kHz Oscillators
- Low power modes
  - Sleep
  - Shutdown
- 4 Full configuration pre selections including:
  - ZoomingADC™ configuration
  - 2 alarms with on & off thresholds
  - Digital filtering
- I2C EEPROM interface
- Stand alone mode for alarm monitoring
- Clock out pin
- Calibration pin
- Reset pin
- Ready / Busy pin



Example of application
Typical pressure & temperature sensing application with sleep control

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1. Specifications

1.1. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter	Symbol	Condition	Min	Max	Units
Power supply	V_{BAT}		VSS - 0.3	6	V
Storage temperature	T_{STORE}		-55	150	°C
Max sensor common mode	$V_{VR\ P}$ $V_{VR\ N}$		VSS - 300	V_{BATT} + 300	mV
Input voltage			VSS - 300	V_{BATT} + 300	mV
Peak soldering temperature	T			260	°C

Note: This device is ESD sensitive. Use of standard ESD handling precautions is required.

1.2. Operating conditions

All values are valid whithin the operating conditions unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OPERATING CONDITIONS						
Power supply	V_{BAT}		2.4		5.5	V
Operating temperature	T_{OP}		-40		125	°C
CURENT CONSUMPTION						
Active current	I_{OP}			300		µA
Sleep current (1)	I_{SLEEP}	Temperature < 85°C		1	5.0	µA
Sleep current (2)	I_{SLEEP}	Temperature < 85°C		3	10.0	µA
Shutdown current	I_{SHUT}	Temperature < 85°C		0.5	3.5	µA
DIGITAL I/O						
Input logic high	V_{IH}		0.7 x V_{BAT}			V
Input logic low	V_{IL}				0.3 x V_{BAT}	V
Output logic high	V_{OH}	I_{OH} < 4 mA			V_{BAT} - 0.4	V
Output logic low	V_{OL}	I_{OL} < 4 mA	0.4			V

(1) With external 32.768kHz Xtal connected

(2) Without external 32.768kHz Xtal connected

1.3. ZoomingADC Specifications

Unless otherwise specified: Temperature T_A = +25°C, V_{BATT} = +5V, GND = 0V, V_{REF} = +5V, V_{IN} = 0V, RC frequency f_{RC} = 2MHz, sampling frequency f_S = 300 kHz, Overall PGA gain GD_{TOT} = 1, offsets GD_{Off2} = GD_{Off3} = 0. Power operation: normal (IB_AMP_ADC[1:0] = IB_AMP_PGA[1:0] = '11'). For resolution n = 12 bits: OSR = 32 and N_{ELCONV} = 4. For resolution n = 16 bits: OSR = 512 and N_{ELCONV} = 2.

PARAMETER		COMMENTS/CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
ANALOG INPUT CHARACTERISTICS						
Differential Input Voltage Range $V_{IN} = V_{INP} - V_{INN}$		Gain = 1, OSR = 32 (Note 1)	-2.42		+2.42	V
		Gain = 100, OSR = 32	-24.2		+24.2	mV
		Gain = 1000, OSR = 32	-2.42		+2.42	mV
Reference Voltage Range $V_{REF,ADC} = V_{REFP} - V_{REFN}$					V_{BATT}	V
PROGRAMMABLE GAIN AMPLIFIER						
Total PGA Gain	GD_{TOT}		0.5		1000	V/V
PGA1 Gain	GD_1	See Table 15	1		10	V/V
PGA2 Gain	GD_2	See Table 16	1		10	V/V
PGA3 Gain	GD_3	Step = 1/12 V/V, See Table 47			127/12	V/V
Gain Settings Precision (each stage)			-3	+/- 0.5	+3	%
Gain Temperature Dependance Offset				+/- 5		ppm / °C
PGA2 Offset	GD_{off2}	Step = 0.2 V/V, See Table 46	-1		+1	V/V
PGA3 Offset	GD_{off3}	Step = 1.12 V/V, See Table 48	-63/12		+63/12	V/V
Offset Settings Precision (PGA2 or PGA3)		(note 2)	-3	+/- 0.5	+3	%
Offset Temperature Dependance				+/-5		ppm / °C
Input Impedance PGA1		PGA1 Gain = 1 (Note 3)	1500			kΩ
		PGA1 Gain = 10 (Note 3)	150			kΩ
Input Impedance PGA2 ,PGA3		Maximal gain = 1 (Note 3)	150			kΩ
Output RMS Noise		PGA1 (Note 4)		205		µV
		PGA2 (Note 5)		340		µV
		PGA3 (Note 6)		365		µV

PARAMETER		COMMENTS/CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
ADC STATIC PERFORMANCES						
Resolution	n	(Note 7)	6		16	Bits
No Missing Codes		(Note 8)				
Gain Error		(Note 9)		+/- 0.15		% of FS
Offset Error		n = 16 bits (Note 10)		+/- 1		LSB
Integral Non-Linearity	INL	resolution n = 16 bits (Note 11)		+/- 1.0		LSB
Differential Non-Linearity	DNL	resolution n = 16 bits (Note 12)		+/- 0.5		LSB
Power Supply Rejection Ratio	PSRR	V_{BATT} = 5V +/- 0.3V (Note 13)		78		dB
		V_{BATT} = 3V +/- 0.3V (Note 13)		72		dB
ADC DYNAMIC PERFORMANCES						
Throughput Rate (Continuous Mode)	$\mathbf{T_{CONV}}$	n = 12 bits (Note 14)	3	133		cycles / f_S
		n = 16 bits (Note 14)	0	1027		cycles / f_S
Throughput Rate (Continuous Mode)	$\mathbf{1/T_{CONV}}$	n = 12 bits, f_S		3.76		kS/s
		n = 16 bits, f_S		0.49		kS/s
Nbr of Initialization Cycles	N_{INIT}		0		2	cycles
Nbr of End Conversion Cycles	N_{END}		0		5	cycles
PGA Stabilization Delay		(Note 15)		OSR		cycles
TIME BASE						
Max ADC oversampling frequency	f_{Smax}	@ 25°C, with a 32k XTAL	270	300	330	kHz
Min ADC oversampling frequency	f_{Smin}	@ 25°C, with a 32KXTAL	33	37.5	42	kHz
DIGITAL OUTPUT						
ADC Output Data Coding		See Table 55 and Table 56	Binary Two's Complement			
TEMPERATURE						
Specified Range			-40		+85	°C
Operating Range			-40		+125	°C

Table 1. ZoomingADC specifications

Notes

(1) Gain defined as overall PGA gain GDTOT = GD1 x GD2 x GD3. Maximum input voltage is given by:

$V_{IN,MAX} = (V_{REF}/2) (OSR/OSR+1)$.

(2) Offset due to tolerance on GDoff2 or GDoff3 setting. For small intrinsic offset, use only ADC and PGA1.

(3) Measured with block connected to inputs through AMUX block. Normalized input sampling frequency for input impedance is f_S = 512 kHz. This figure must be multiplied by 2 for f_S = 256 kHz, 4 for f_S = 128 kHz. Input impedance is proportional to $1/f_S$.

(4) Figure independent from PGA1 gain and sampling frequency f_S. See equation Eq. 21 to calculate equivalent input noise.

(5) Figure independent on PGA2 gain and sampling frequency f_S. See equation Eq. 21 to calculate equivalent input noise.

(6) Figure independent on PGA3 gain and sampling frequency f_S. See equation Eq. 21 to calculate equivalent input noise.

(7) Resolution is given by $n = 2 \log_2(OSR) + \log_2(N_{ELCONV})$. OSR can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.

(8) If a ramp signal is applied to the input, all digital codes appear in the resulting ADC output data.

(9) Gain error is defined as the amount of deviation between the ideal (theoretical) transfer function and the measured transfer function (with the offset error removed).

(10) Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). For 1 LSB offset, N_{ELCONV} must be 2.

(11) INL defined as the deviation of the DC transfer curve of each individual code from the best-fit straight line. This specification holds over the full scale.

(12) DNL is defined as the difference (in LSB) between the ideal (1 LSB) and measured code transitions for successive codes.

(13) Values for Gains = 1 to 100. PSRR is defined as the amount of change in the ADC output value as the power supply voltage changes.

(14) Conversion time is given by: $T_{CONV} = (N_{ELCONV} (OSR + 1) + 1) / f_S$. OSR can be set between 8 and 1024, in powers of 2. N_{ELCONV} can be set to 1, 2, 4 or 8.

*(15) PGAs are reset after each writing operation to registers **CxRegAdc1-5**. The ADC must be started after a PGA or inputs common-mode stabilisation delay. This is done by writing bit Start several cycles after PGA settings modification or channel switching. Delay between PGA start or input channel switching and ADC start should be equivalent to OSR (between 8 and 1024) number of cycles. This delay does not apply to conversions made without the PGAs.*

*(16) Nominal (maximum) bias currents in PGAs and ADC, i.e. **IB_AMP_PGA[1:0]** = '11' and IB_AMP_ADC[1:0] = '11'.*

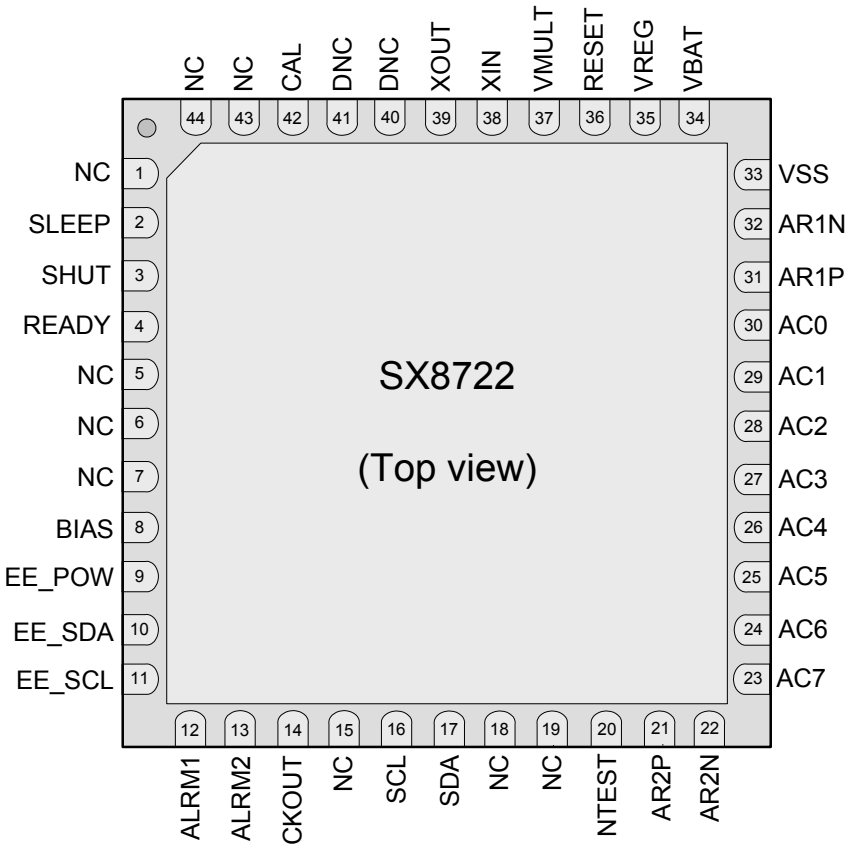
*(17) Bias currents in PGAs and ADC set to 3/4 of nominal values, i.e. **IB_AMP_PGA[1:0]** = '10', IB_AMP_ADC[1:0] = '10'.*

*(18) Bias currents in PGAs and ADC set to 1/2 of nominal values, i.e. **IB_AMP_PGA[1:0]** = '01', IB_AMP_ADC[1:0] = '01'.*

*(19) Bias currents in PGAs and ADC set to 1/4 of nominal values, i.e. **IB_AMP_PGA[1:0]** = '00', IB_AMP_ADC[1:0] = '00'.*

2. Pin configuration and marking information

2.1. Pin configuration



2.2. Marking information

nnnnnn = Part Number (Example: SX8722)
yyww = Date Code (Example: 0752)
xxxxxxxxx = Semtech Lot No. (Example A01E90101)

3. Pin Description

Pin	Symbol	Type	Function	Status at POR
1	NC		Not connected	
2	SLEEP	Digital input	Setting this pin to 0 puts the SX8722 in sleep mode, power consumption ~1.5uA, otherwise the pin can be floating	Internal pull-up
3	SHUT	Digital input	Setting this pin to 0 puts the SX8722 in shutdown mode, power consumption ~0.5uA, otherwise the pin can be floating	Internal pull-up
4	READY	Digital output	Is high when a measurement data is available	Low
5	NC		Not connected	
6	NC		Not connected	
7	NC		Not connected	
8	BIAS	Digital output	Bias pin, is set to V_{BAT} voltage when a measurement is performed	Low
9	EE_POW	Digital output	Must be used to power the optional I2C EEPROM	Low
10	EE_SDA	Digital IO	Must be connected to SDA pin of the optional EEPROM when used. Otherwise must remain floating (see chapter EEPROM connection)	Low
11	EE_SCL	Digital IO	Must be connected to SCL pin of the optional EEPROM when used. Otherwise must remain floating (see chapter EEPROM connection)	Low
12	ALRM1	Digital output	Alarm1 pin, is high when "on" threshold is reached and low when "off" threshold is reached, when not used can reamin floating	Low
13	ALRM2	Digital output	Alarm2 pin, is high when "on" threshold is reached and low when "off" threshold is reached, when not used can reamin floating	Low
14	CKOUT	Digital output	System clock output	Low
15	NC		Not connected	
16	SCL	Digital IO	Serial clock line of the I2C compatible interface	Input
17	SDA	Digital IO	Serial data line of the I2C compatible interface	Input
18	NC		Not connected	
19	NC		Not connected	
20	NTEST	Digital input	Must be connected to V_{BAT}	
21	AR2P	Analog input	Second analog input reference (positive input)	
22	AR2N	Analog input	Second analog input reference (negative input)	
23	AC7	Analog input	ZoomingADC^{TM} input 7	

Pin	Symbol	Type	Function	Status at POR
24	AC6	Analog input	ZoomingADC™ input 6	
25	AC5	Analog input	ZoomingADC™ input 5	
26	AC4	Analog input	ZoomingADC™ input 4	
27	AC3	Analog input	ZoomingADC™ input 3	
28	AC2	Analog input	ZoomingADC™ input 2	
29	AC1	Analog input	ZoomingADC™ input 1	
30	AC0	Analog input	ZoomingADC™ input 0	
31	AR1P	Analog input	First Analog reference input (positive input)	
32	AR1N	Analog input	First Analog reference input (negative input)	
33	VSS	Power	Negative power supply	
34	VBAT	Power	Positive power supply	
35	VREG	Analog input	Connected to the internal voltage regulator. Must be connected through 1uF capacitor to the ground.	
36	RESET	Digital input	Reset pin, active high, must be tied to ground through a 3k3 resistor.	
37	VMULT	Analog input	External capacitor for the internal voltage multiplier. Vmult capacitor must be connected through 2nF to the ground when VBAT < 3V	
38	XIN	Digital input	XTAL connection, left unconnected when not used	
39	XOUT	Digital output	XTAL connection, left unconnected when not used	
40	DNC		Do not connect	
41	DNC		Do not connect	
42	CAL	Digital input	Calibration pin, set low to use XTAL.	Internal pull-up
43	NC		Not connected	
44	NC		Not connected	

4. Timing Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
I2C TIMING SPECIFICATIONS (1)						
SCL clock frequency	f_{SCL}		0		100	kHz
SCL low period	t_{LOW}		4.7			µs
SCL high period	t_{HIGH}		4.0			µs
Data setup time	$t_{SU;DAT}$		250			ns
Data hold time	$t_{HHD;DAT}$		4.0			ns
Repeated start setup time	$t_{SU;STA}$		4.7			µs
Start condition hold time	$t_{HD;STA}$		4.0			µs
Stop condition hold time	$t_{SU;STO}$		4.0			µs
Bus free time between stop and start	t_{BUF}		4.7			µs

(1) All timings specifications are referred to VILMIN and VIHMAX voltage levels defined for the SCL and SDA pins. With 32'768 Hz Xtal presence.

4.1. I2C timing Waveforms

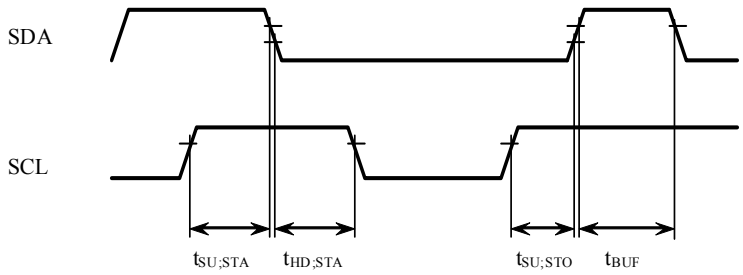


Figure 1. I2C Start and Stop timing

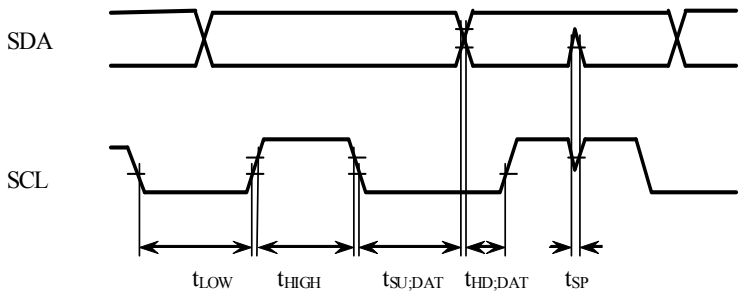


Figure 2. I2C Data timings

4.2. Time specification without the 32.768 kHz Xtal

The internal SX8722 RC oscillator accuracy depends on technology tolerance. It can reach ± 50% difference from one chip to another

In this case, and if no calibration is done, the RC clock is centred around 1.2 MHz.

SX8722 timing values without Xtal can thus differ of ± 50% to these with a Xtal.

4.3. Start-up time with the 32.768 kHz Xtal presence

The mean time of EEPROM loading at the start-up is typically 140 ms if configuration data are saved in.

In this case SX8722 will provide the first sample after typically 180ms.

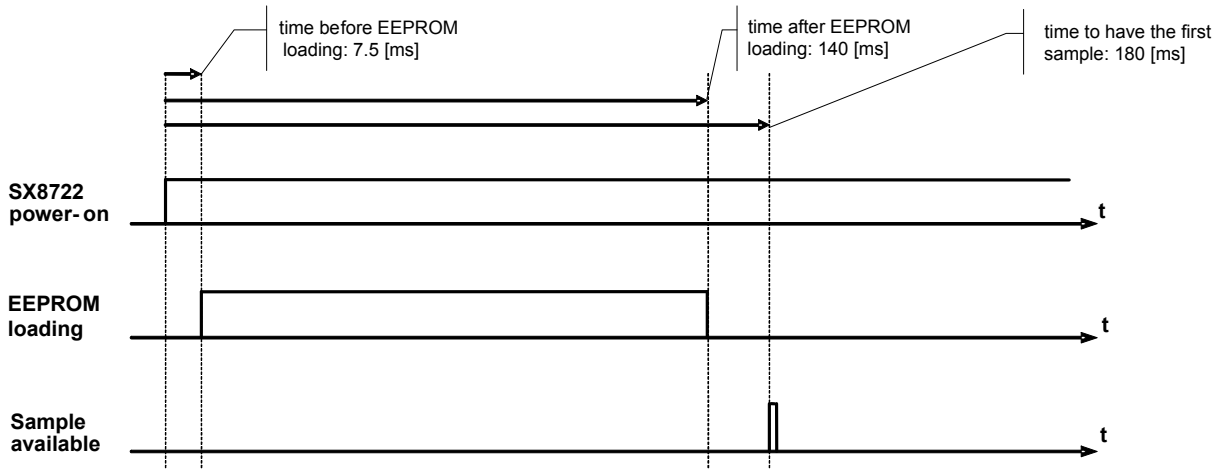


Figure 3. Start-up timing diagram with EEPROM loading

4.4. Changing power mode by pin signal

To	From		
	SHUT	SLEEP	ACTIVE
SHUT		640ms	650ms
SLEEP			660ms
ACTIVE	inst. (1)	inst. (1)	

Table 2. Power mode changing timings by pin setting

(1) instantaneous

4.5. Changing power mode by I2C command

To	From		
	SHUT	SLEEP	ACTIVE
SHUT		770us	700us
SLEEP			470us
ACTIVE		inst. (1)	

Table 3. Power mode changing timings by I2C command

(1) instantaneous

Note: When time to change a power mode is instantaneous, it doesn't mean that the chip is totally ready to work. There are for example initialization times, EEPROM loading or code execution.

The transition time is considered as not low power.

5. Circuit description

5.1. Detailed bloc diagram

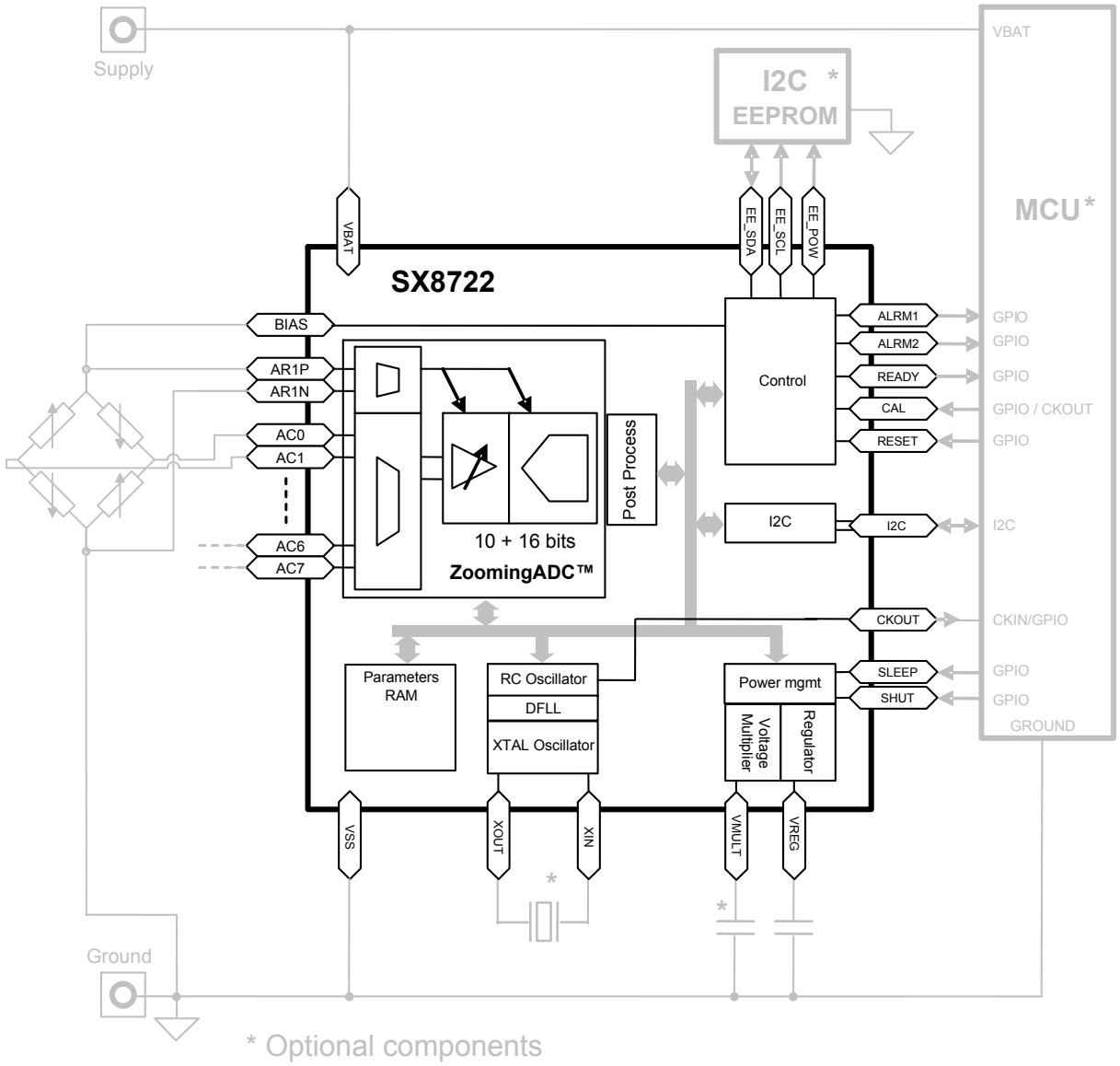


Figure 4. SX8722 detailed bloc diagram

5.2. Functional description

- The SX8722 is a ZoomingADC™ with I2C compatible interface allowing multiple setups.
- The major modules of the SX8722 are the ZoomingADC™, the signal post processing, the control unit and the power management
- The SX8722 offers several configuration possibilities allowing the developer to use it as a peripheral of its system or to use it as a stand alone system generating alarms.

- The ZoomingADC™ is made of 1 input multiplexer, 3 programmable gain amplifiers and a 16 bits Sigma-Delta ADC. The input multiplexer allows measuring 4 differential sensors or 7 single ended sensors or a combination of differential and single-ended. The total gain of the PGA enables an amplification of 1000 and the offset correction can reach up to 15 times the full scale input signal.

- The SX8722 is not only giving access to the very efficient ZoomingADC™ technology, it also gives access to a very low power acquisition system entirely configurable to reach as low as 0.5uA in shutdown mode. The low power modes can be reached through pins or specific serial commands.

- The whole chip is controlled by a set of registers; these registers have factory default settings and can be modified in 2 ways: the serial interface commands or an optional external EEPROM. At Startup the SX8722 checks for EEPROM presence and updates its registers with EEPROM contents.

- The whole chip is working at 1.2MHz using its internal RC oscillator, this frequency can be calibrated.

- The clock calibration can be done using several methods: External 32.768 kHz XTAL, External 32.768 kHz reference signal, or EEPROM parameter configuration.

- Several corrections can be applied on the measured signal such as different digital filters.

- The SX8722 offers two alarm pins. "on" and "off" thresholds can be set independently.

- A Clock out pin can be enabled to have the exact frequency of RC oscillator.

- External EEPROM and sensors can be biased by the dedicated SX8722 pins EE_POW and BIAS allowing the most efficient power management.

- The pin READY is a single signal that can be used to interrupt the host microcontroller.

- The RESET pin enables the host system to reset the SX8722 to its startup settings at any time.

- The internal voltage multipliers is automatically enabled when working below 3 Volts.

- The SX8722 implements 4 configuration register sets. Each of these sets completely defines the behavior of the ZoomingADC™. This allows the user to preset 4 different measurement configurations that can be activated by setting a single bit.

The diagram below page explains the registers system more in details.

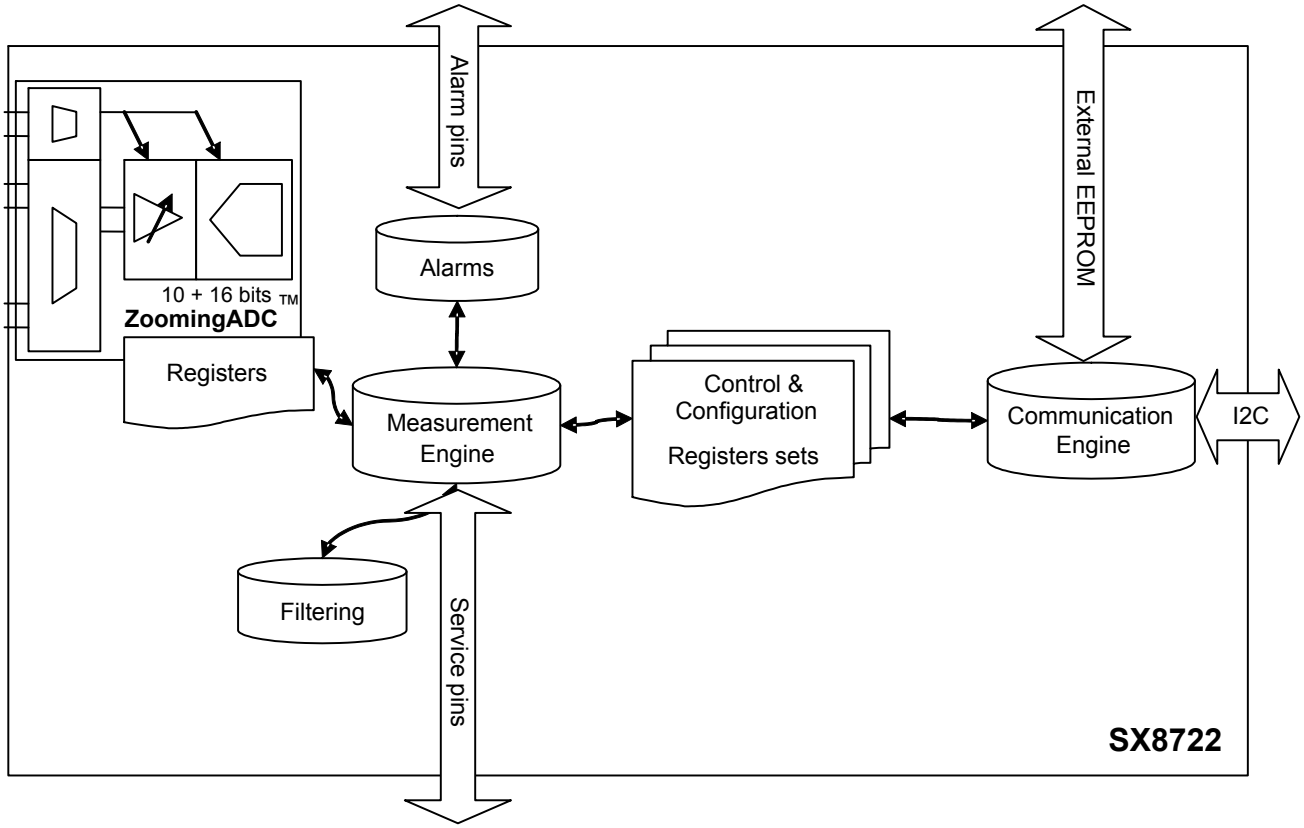


Figure 5. Register sets system

The measurement engine copies the configuration register sets in the ZoomingADC™ physical registers and writes back the conversion results.

The communication engine controls read/write access from the I2C or the external EEPROM.

5.3. ZoomingADC

The SX8722 core is the ZoomingADC™, the diagram below shows more in detail the architecture of this acquisition chain.

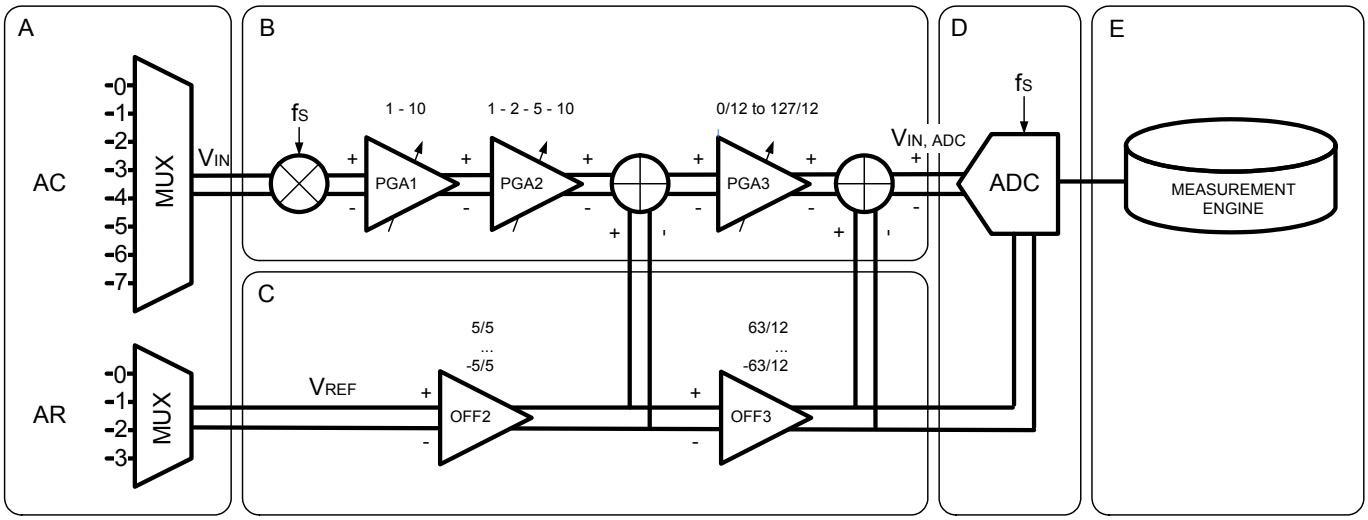


Figure 6. Acquisition chain architecture

The block schematic above is separated in function boxes:

A. Input multiplexers

- Routing of the input signal.
- Routing of the reference.

B. Programmable gain amplifiers

- Can be enabled/disabled separately.
- Each PGA has programmable gain from 1 to 10.
- Total PGA gain available = PGA1 x PGA2 x PGA3 = 1000.

C. Offset cancellation

- Subtract or add a reference multiple to the input signal.
- Can compensate up to 15 times the full scale signal.

D. ADC

- Sigma-Delta ADC.
- Offers several sampling frequencies.
- Over sampling rates and elementary conversion combinations allow setting the ideal resolution for the ideal conversion time.

E. Measurement engine

- Manages up to 4 ZoomingADC™ configurations.
- Updates the measured values.

6. Access the SX8722

6.1. Description

The SX8722 is configured trough register sets and general control registers.

All the accesses to the SX8722 registers are done through the I2C interface using read and write commands.

The next paragraph describes two approaches to configure the SX8722

6.2. SX8722 configuration

As it will be shown in the next chapter there are two ways to write data in the SX8722 registers:

- Direct write: This command writes 8 bits to a defined address. This implies knowledge of the value to be written to this address.
- Masked write: This command can write a single bit in a byte using a mask.

7. I2C Commands

This chapter describes the commands that are coded in the SX8722.

The SX8722 commands are summarized below, detailed timing diagrams can be found “Serial Communication” chapter.

Type	Command	Description	Byte
Data access	write_direct	Writes 8bit data to a given address	0x10
	write_masked	Writes bits to given address using a given mask	0x20
	read	Reads 8bit data from a given address	0x30
Power modes	sleep	Sets the SX8722 to sleep mode	0x40
	shutdown	Sets the SX8722 to sleep mode	0x50
	reset	Resets the SX8722	0x60
EEPROM	save_eeprom	Saves the SX8722 registers in the external EEPROM (if present)	0x70
	load_eeprom	Loads the SX8722 registers in the external EEPROM (if present)	0x80

Table 4. SX8722 commands

8. Serial communication

The serial interface is a read-write 2 wire slave device. The SCL wire carries the clock information and SDA carries the data. The output drivers on the bus are open drain current sinks.

The SCL wire is controlled by the master on the bus. Since the SX8722 is fairly slow, it may stretch the low clock phase when required. The SDA wire is controlled by the master or the slave depending on the operation.

SDA only changes while the clock signal is low except for the (repeated) start or stop conditions.

The (repeated) start condition for the transmission is a high to low transition on SDA while SCL is high. The stop condition is a low to high transition while SCL is high.

To read data from the SX8722, the master has to send successively a start bit, the slave address, a write bit. If the slave address corresponds to the address of the SX8722 and the preceding operation is completed, the SX8722 sends an acknowledge bit. The master then sends the read command which is acknowledged by the salve, the memory address that it would like to read which is also acknowledged by the slave. The master issues a repeated start, repeats the slave address and read bit. The slave acknowledges and returns the data to the master. The master terminates the communication by a "not acknowledge" and a stop bit.

To write data to the SX8722, the format is very similar. Only the data direction is different and the acknowledgement of the slave after the data reception.

8.1. Write data direct

The diagram below shows the write operation.

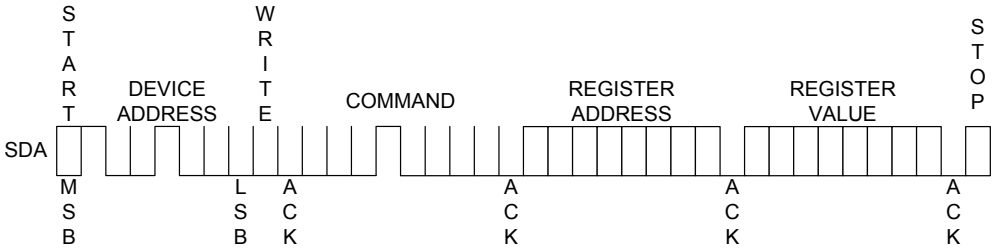


Figure 7. I2C frame: write register, command 0x10

The diagram below shows the write operation at successive addresses (burst mode)

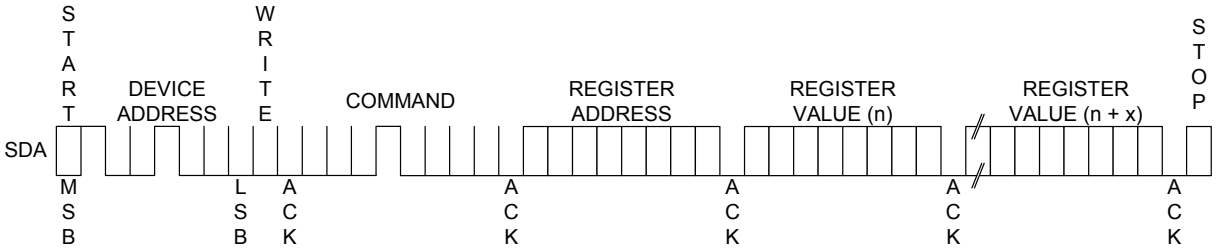


Figure 8. I2C frame: write burst register, command 0x10

8.2. Write data masked

The diagram below show the write masked operation.

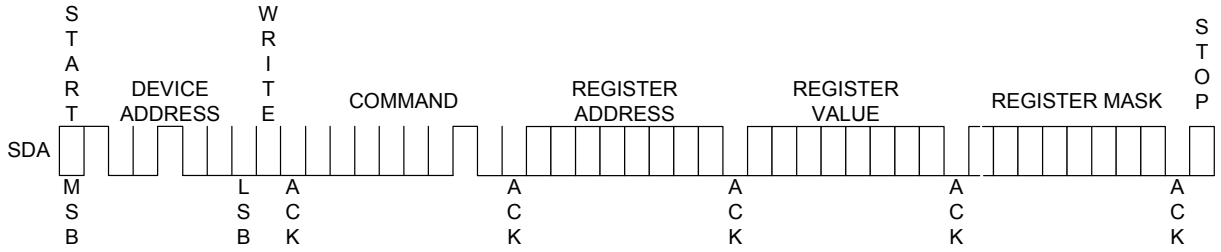


Figure 9. I2C frame: write mask register, command 0x20

8.3. Read data

Read data diagram.

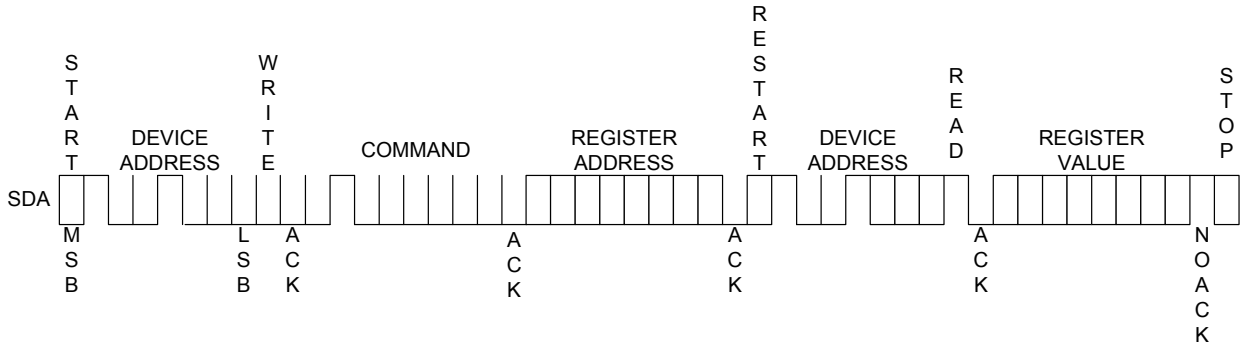


Figure 10. I2C frame: read register, command : 0x30

Read data diagram successive addresses (burst mode)

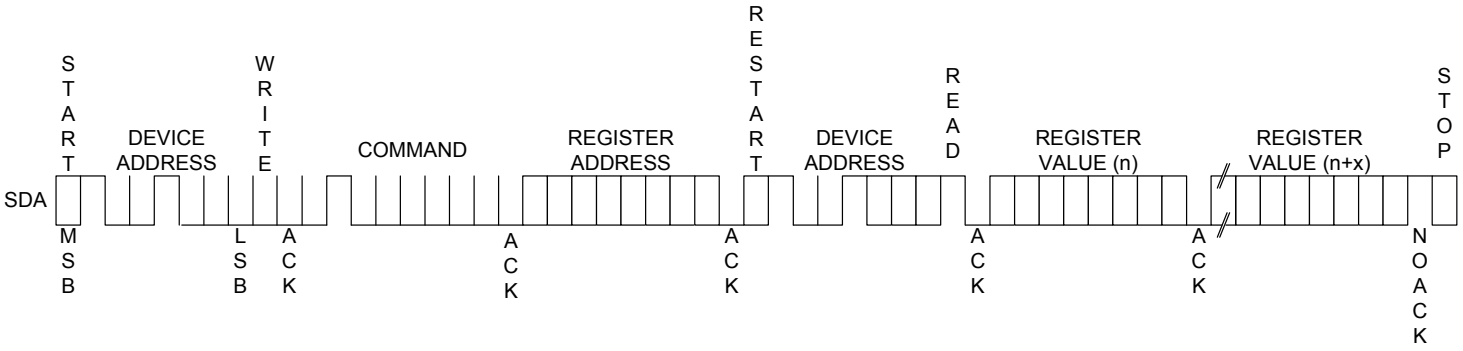


Figure 11. I2C frame: read burst register, command 0x30

Note: If a read sequence is initiated without sending previously an address, the data shifted out will be the latest conversion result and its corresponding configuration ID (24 bits). See next page for more information.

8.4. Other commands

The diagram below shows the other commands syntax.

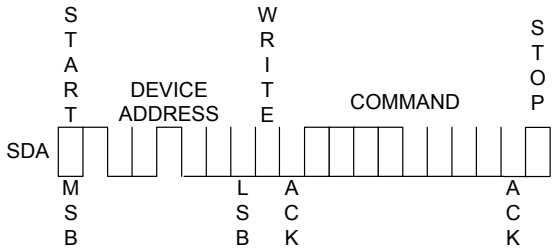


Figure 12. I2C frame: other commands, 0x40 - 0x80

8.5. Unknown commands

The SX8722 does not answer to unknown commands.

8.6. Reading data after a measurement.

The SX8722 performs measurements successively and stores the latest results in the enabled configurations data out registers.

Every time a measurement is performed the pin READY makes a positive pulse allowing the host microcontroller to retrieve data from the SX8722.

When the SX8722 is addressed and read the output is as shown below. Config ID indicates which channel is shifted out.

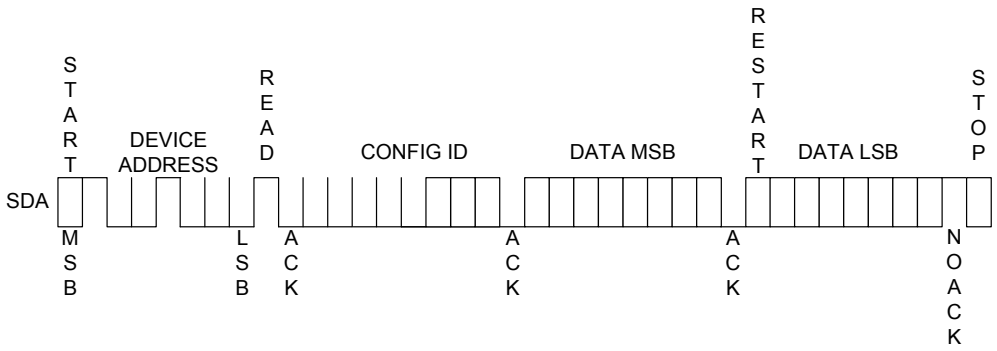


Figure 13. I2C frame: reading after a measurement

9. Predefined settings

9.1. Introduction

This chapter intends to ease the handling of the SX8722 using a set of predefined settings.
These settings are covering a large range of the SX8722 possibilities.

However to avoid too much complexity some features are not handled by these settings.

A more detailed use of the SX8722 can be found under the "advanced configuration" of this document.
This chapter contains predefined command using the masked write mode.

All the settings described in this chapter use the addresses of the 1st configuration register set, use the registers definition table to translate them to other register sets.

9.2. Features covered by predefined settings

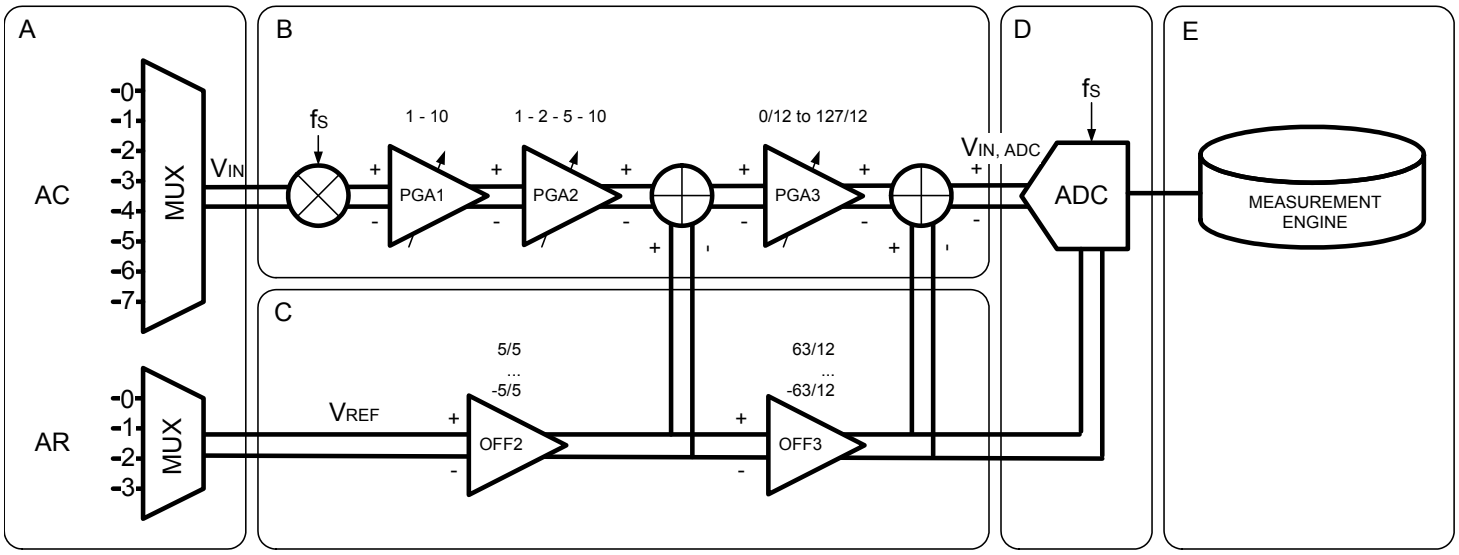


Figure 14. Features covered by predefined settings

The block schematic above shows the functions covered and controlled by the predefined settings set.
It includes:

A. The input multiplexers
B. The programmable gain amplifiers
C. The offset cancellation
D. The ADC
E. The Measurement engine

Note: Grayed out blocks in the schematic means that they are used in the current function.

9.3. Input multiplexers

9.3.1. Overview

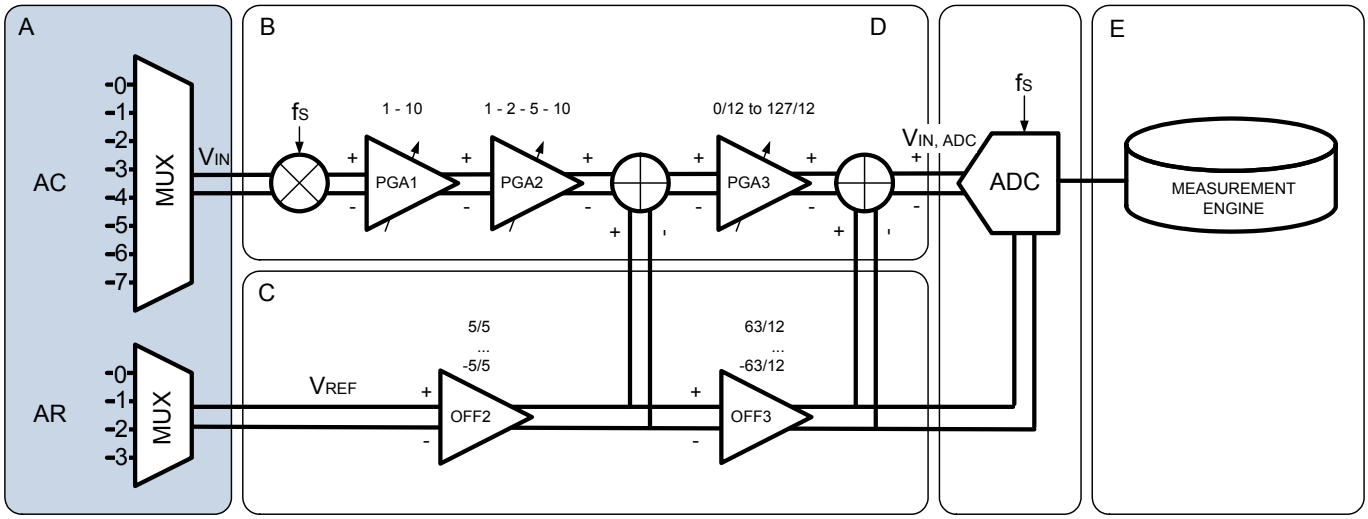


Figure 15. Input multiplexer overview

The diagram above shows the input multiplexer organization; these are enabling the selection of both the input and the reference sources.

9.3.2. Input channel selection

The following settings allow configuring the input multiplexers of the ZoomingADC™

Function	Address	Data	Mask
AC0 - AC1	0x0F	0x00	0x06
AC2 - AC3		0x02	
AC4 - AC5		0x04	
AC6 - AC7		0x06	

Table 5. Differential mode

.

Function	Address	Data	Mask
AC0 - AC1	0x0F	0x22	0x2E
AC0 - AC2		0x24	
AC0 - AC3		0x26	
AC0 - AC4		0x28	
AC0 - AC5		0x2A	
AC0 - AC6		0x2B	
AC0 - AC7		0x2C	

Table 6. Single-ended mode

Function	Address	Data	Mask
Sign inversion	0x0F	0x10	0x10

Table 7. Invert input polarity

9.3.3. Reference channel selection

Function	Address	Data	Mask
AR1P - AR1N	0x0F	0x00	0x01
AR2P - AR2N		0x01	

Table 8. Reference channel selection

9.3.4. Application example

In this example we want to measure a signal between AC0 and AC1 in single ended having a reference voltage between AR1P and AR1N.

The following settings must be sent to SX8722:

Function	Address	Data	Mask
Set input to AC1 - AC2	0x0F	0x00	0x06
Set reference to AR1P - AR1N	0x0F	0x00	0x01

Table 9. Reference channel selection

Note: This command can be optimized, since the reference and input setting are sharing the same address the mask and the settings can be added.

The following command shows the optimized way

Function	Address	Data	Mask
Set input to AC1 - AC0, set reference to AR1P - AR1N	0x0F	0x00	0x07

Table 10. Optimized command

9.4. Programmable gain amplifier settings

9.4.1. Overview

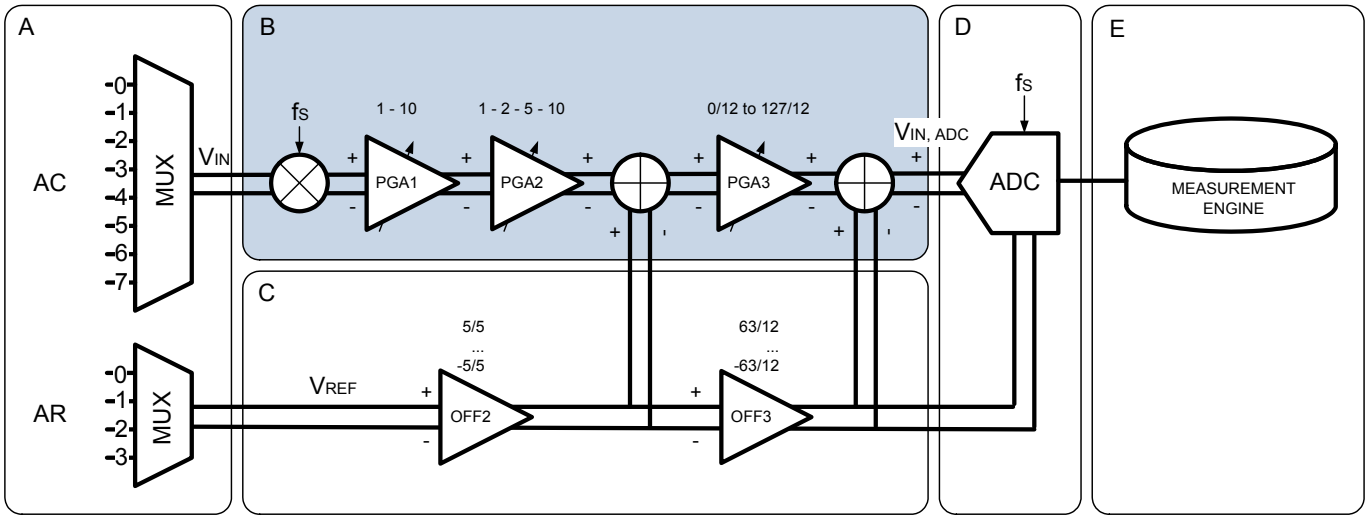


Figure 16. Programmable gain amplifiers (PGA) in the acquisition chain

The diagram above shows the programmable gain amplifier organization, these are 3 PGA that are cascaded, the gain is made by multiplying them (disabled PGAs have the equivalent gain of 1).

9.4.2. Configuration flow

The diagram below shows the flow to set the gain of your configuration:

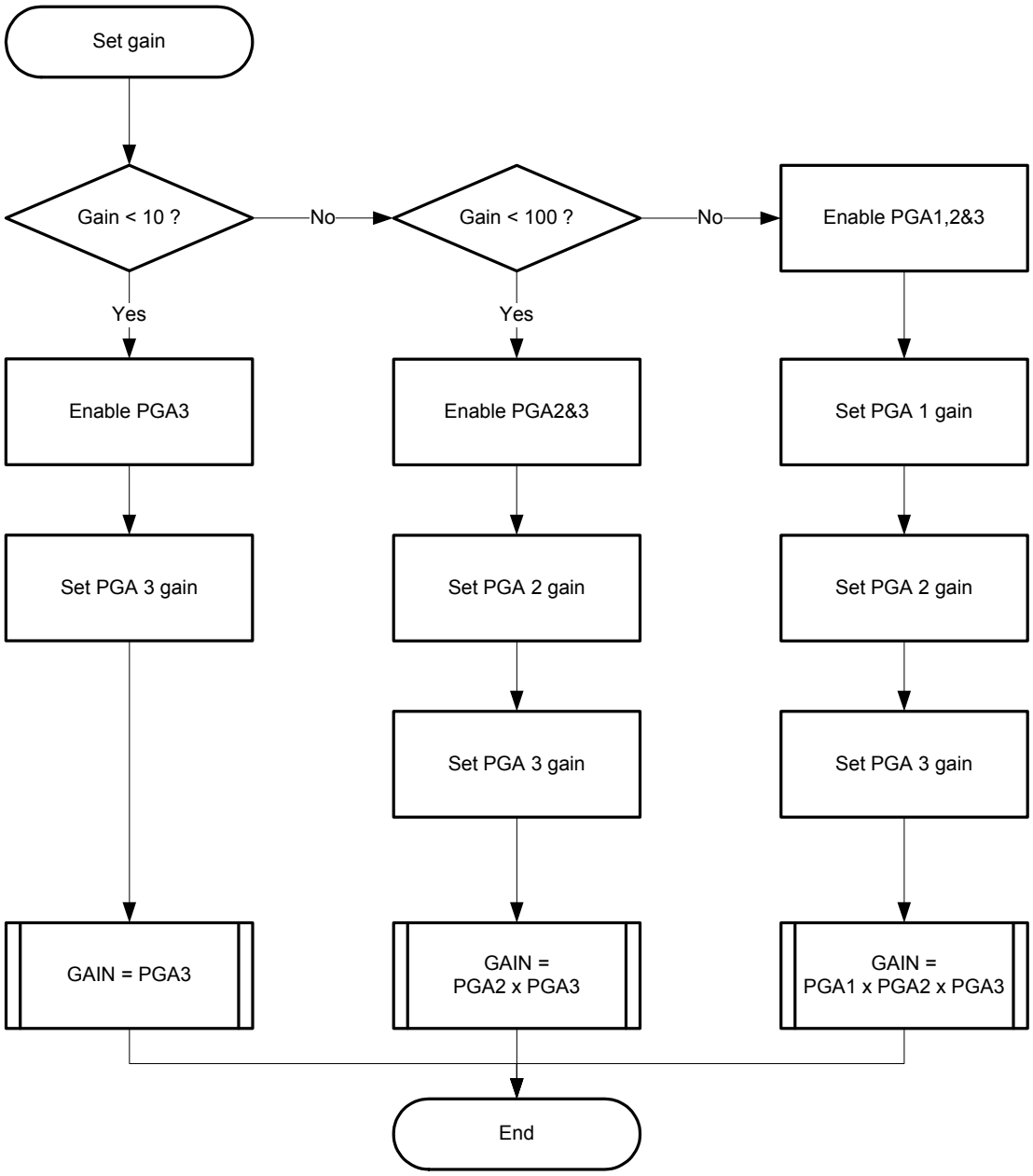


Figure 17. Gain configuration flowchart

9.4.3. Enable/disable PGAs

Function	Address	Data	Mask
Enable PGA3	0x0B	0x08	0x08
Disable PGA3		0x00	
Enable PGA2&3		0x0A	0x0A
Disable PGA2&3		0x00	
Enable PGA1,2&3		0x0E	0x0E
Disable PGA1,2&3		0x00	

Table 11. PGA enable/disable settings

9.4.4. PGA3 gain configuration

Function	Address	Data	Mask
Gain = 1	0x0D	0x0C	0x7F
Gain = 2		0x18	
Gain = 3		0x24	
Gain = 4		0x30	
Gain = 5		0x3C	
Gain = 6		0x48	
Gain = 7		0x54	
Gain = 8		0x60	
Gain = 9		0x6C	
Gain = 10		0x78	

Table 12. PGA3 gain configuration

9.4.5. PGA2 gain configuration

Function	Address	Data	Mask
Gain = 1	0x0C	0x00	0x30
Gain = 2		0x10	
Gain = 5		0x20	
Gain = 10		0x30	

Table 13. PGA2 gain configuration

9.4.6. PGA1 gain configuration

Function	Address	Data	Mask
Gain = 1	0x0D	0x00	0x80
Gain = 10		0x80	

Table 14. PGA1 gain configuration

9.4.7. Application example

The total gain to set in this example is 300.

The following settings must be sent to SX8722:

Function	Address	Data	Mask
Enable PGA1,2&3	0x0B	0x0E	0x0E
PGA3 gain = 3	0x0D	0x24	0x7F
PGA2 gain = 10	0x0C	0x30	0x30
PGA1 gain = 10	0x0D	0x80	0x80

Table 15. Application example of PGA gain settings

Note: This command can be optimized, since PGA1 and PGA3 gains are sharing the same address the mask and the settings can be added.

The following list of settings shows the optimized

Function	Address	Data	Mask
Enable PGA1,2&3	0x0B	0x0E	0x0E
PGA3 gain = 3, PGA1 gain = 10	0x0D	0xA4	0xFF
PGA2 gain = 10	0x0D	0x80	0x30

Table 16. Optimized command of PGA gain settings

9.5. Offset cancellation

9.5.1. Overview

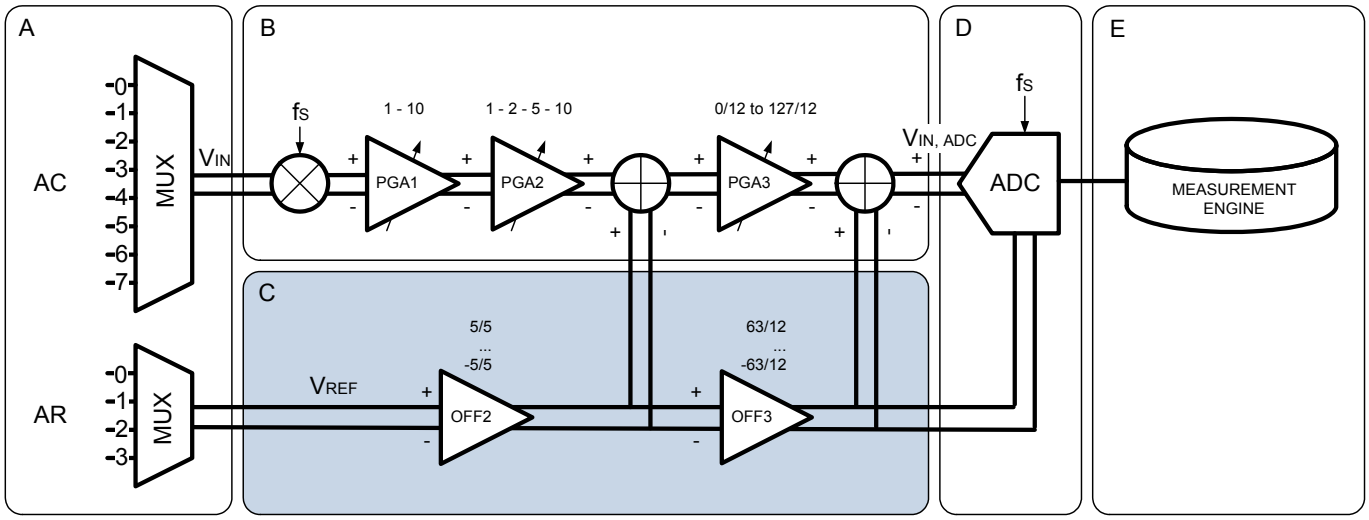


Figure 18. Offset cancellation in the acquisition chain

The offset cancellation consists in adding or subtracting a fraction or a multiple of the reference to the signal before the ADC input.

In the predefined settings only the addition or the subtraction of VREF/2 is implemented.

More offsets configuration can be defined using the "advanced configuration" at the end of this document.

The drawings below explain the offset concept.

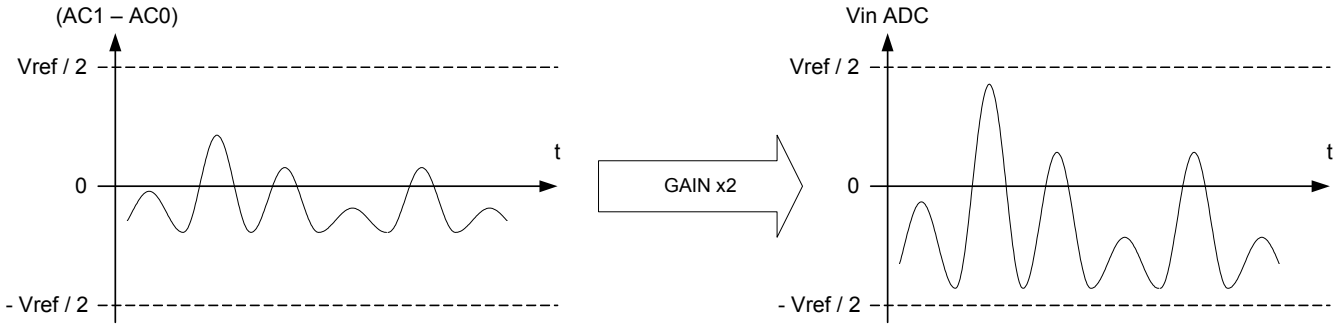


Figure 19. Differential signal

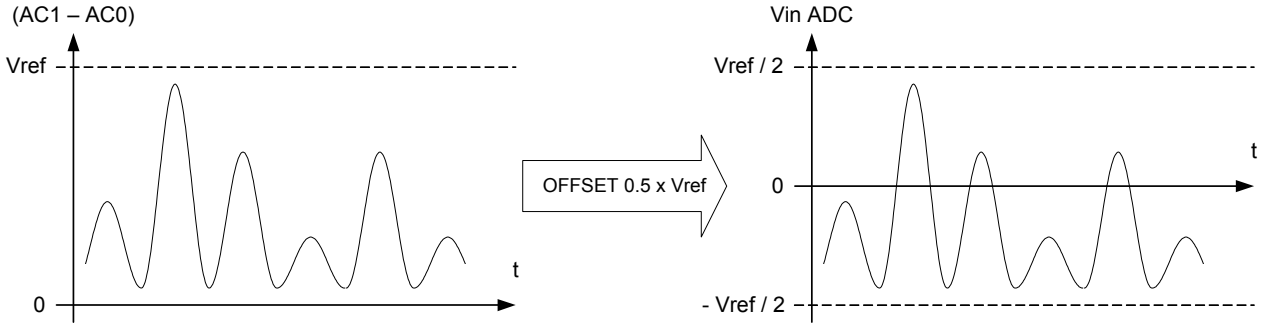


Figure 20. Single ended signal, AC0 = V_{SS}

The following settings add 0.5 x V_{REF} or subtract 0.5 x $V_{REF}$from the signal.

Function	Address	Data	Mask
Offset 3 = 0.5 x V_{REF}	0x0E	0x06	0x7F
Offset 3 = -0.5 x V_{REF}		0x46	

Table 17. Example: Adding or remove 0.5 x Vref

9.5.2. Application example

Case 1

Input signal = V_{REF} / 2

Input selection = AC0 - AC1. (see "input multiplexers" chapter)

Offset to remove is V_{REF} / 2.

The following command must be sent to SX8722:

Function	Address	Data	Mask
Offset 3 = 0.5 x V_{REF}	0x0E	0x06	0x7F

Case 2

Input signal = V_{REF}

Input selection = AC0 - AC1. (see "input multiplexers" chapter)

Offset to remove is -V_{REF} / 2.

The following command must be sent to SX8722:

Function	Address	Data	Mask
Offset 3 = -0.5 x V_{REF}	0x0E	0x46	0x7F

9.6. ADC parameters

9.6.1. Overview

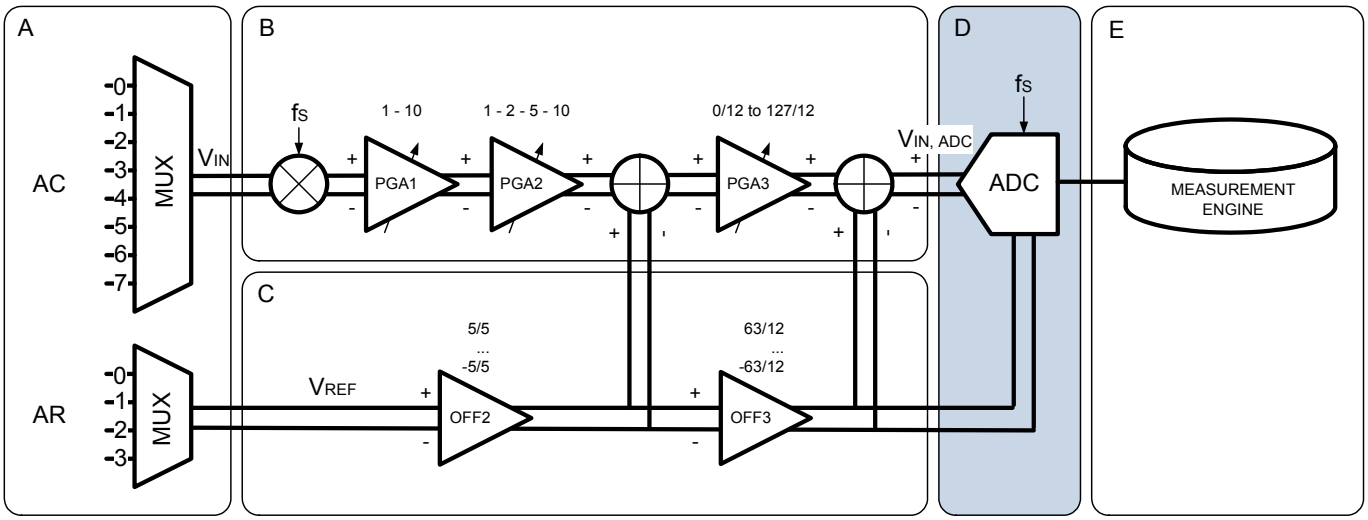


Table 18 ADC in the acquisition chain

The ADC parameters are mainly the resolution and acquisition speed.
Detailed ADC parameters and configuration can be found in the "advanced configuration" chapter

The table below gives the main configurations available using the predefined settings and their main characteristics:

Name	Resolution [bits]	Conversion time [ms] (typ)	Sampling frequency [kHz] (typ)	Over-sampling ratio	Number of elementary conversion	Comments
S16	16	27.3	300	1024	8	Maximum resolution, thermal noise reduced to its minimum
N16	16	6.8		1024	2	Standard 16 bits resolution
F16	16	3.4		1024	1	Fastest 16 bits resolution
N12	12	0.22		64	1	Standard 12 bits resolution
N8	8	0.06		16	1	Standard 8 bits resolution

Table 19. ADC predefined settings

9.6.2. ADC settings

Function	Address	Data	Mask
S16	0x0C	0x7C	0x7C
N16		0x3C	
F16		0x1C	
N12		0x0C	
N8		0x04	

Table 20. ADC register settings

9.7. Measurement engine

9.7.1. Overview

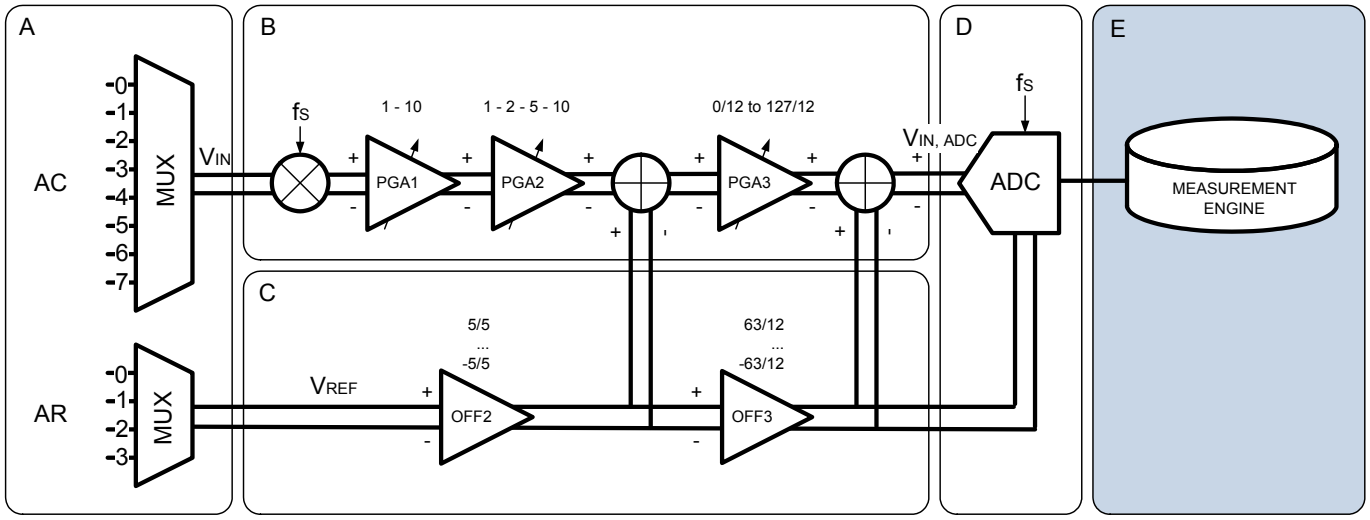


Figure 21. Measurement engine

The measurement engine manages the configuration register sets and controls registers contents.

Based on these parameters it configures the ZoomingADC™, supervises post processing of the measurements, stores the results and flags the READY signal.

Once enabled the configuration 1 will be applied to the ZoomingADC™ and measurement will be done until the configuration is disabled using the disable command.

Note: All the predefined settings refer to configuration 1, to change other configurations simply adapt the address value. More detailed functionalities are described in "Advanced configuration" chapter.

9.7.2. Measurement engine settings

Application	Address	Data	Mask
Configuration 1 enabled	0x02	0x01	0x01
Configuration 1 disabled		0x00	

Table 21. Measurement engine settings

10. Default configuration

The SX8722 default configuration is described in this chapter.

The SX8722 default hardware configuration is as follow:

- 1uF Vreg capacitor connected to Vreg pin
- EE_SDA connected to ground
- 3.0 - 5.0 power supply on Vbat, 0V on GND
- Wheatstone bridge type sensor connected to AC0-AC1 biased through bias pin
- VRef = VBias = VBat
- Host micro controller I2C connected to SDA and SCL of the SX8722
- Host micro controller GPIO connected to RESET input of the SX8722

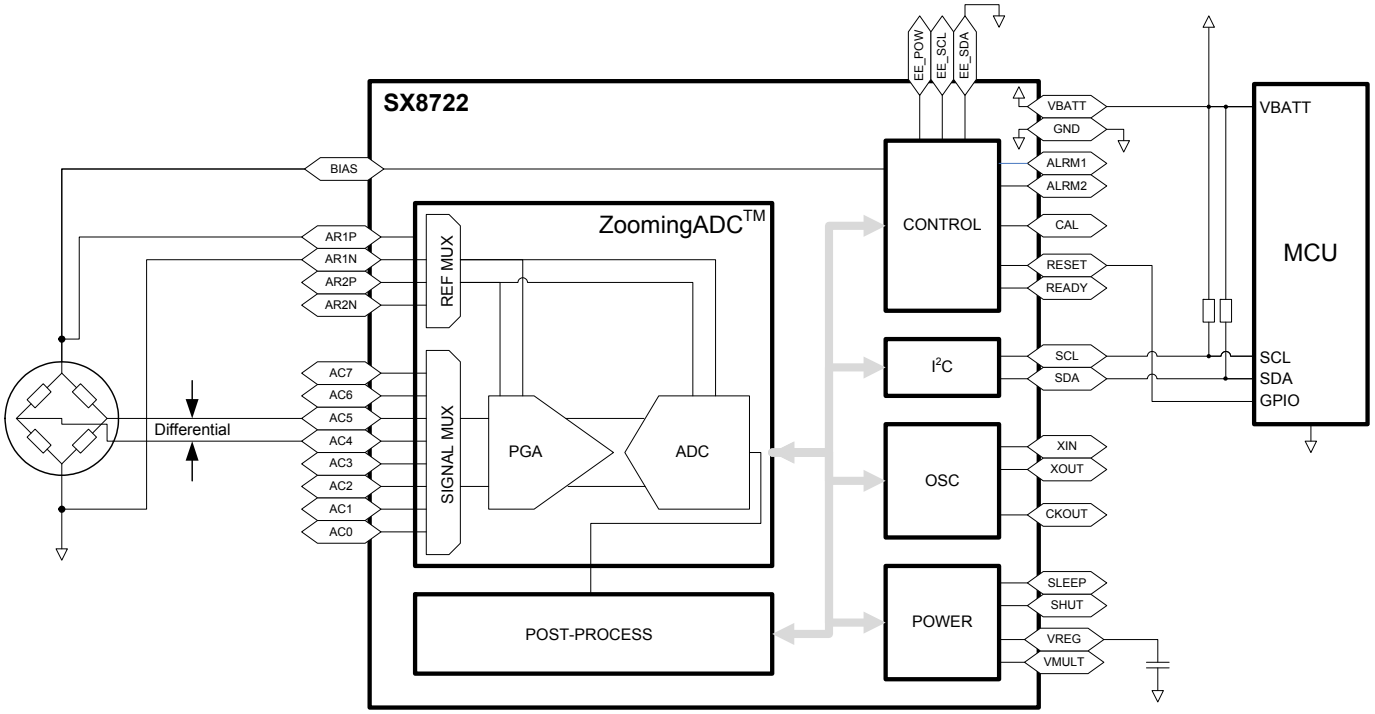


Figure 22. Schematic of the default configuration

Note: Startup conditions Reset = '0'

10.1. ZoomingADC default settings

The SX8722 starts upon a power on reset and then goes into measurement mode.

By default the measurement mode parameters are as follows:

Differential measurement on channel AC0 - AC1, gain 1, 16 bits resolution, reference on AR1P - AR1N, no filtering, continuous measurements.

The READY pin will pulse from "0" to "1" at every sample available. The host microcontroller can then read the data.

11. Advanced configuration

11.1. Overview

The advanced configuration section is entering more in depth in the SX8722 usage. In this section you will find:

- Measurement engine
- Configuration control
- Filtering
- Alarms
- I2C EEPROM
- Using the SX8722 Stand alone
- Calibration process
- Working below 3 Volts
- Control registers

11.2. Measurement engine

11.2.1. Overview

The measurement engine is the interface between the configuration register sets and the ZoomingADC™.

11.2.2. Functional flowchart

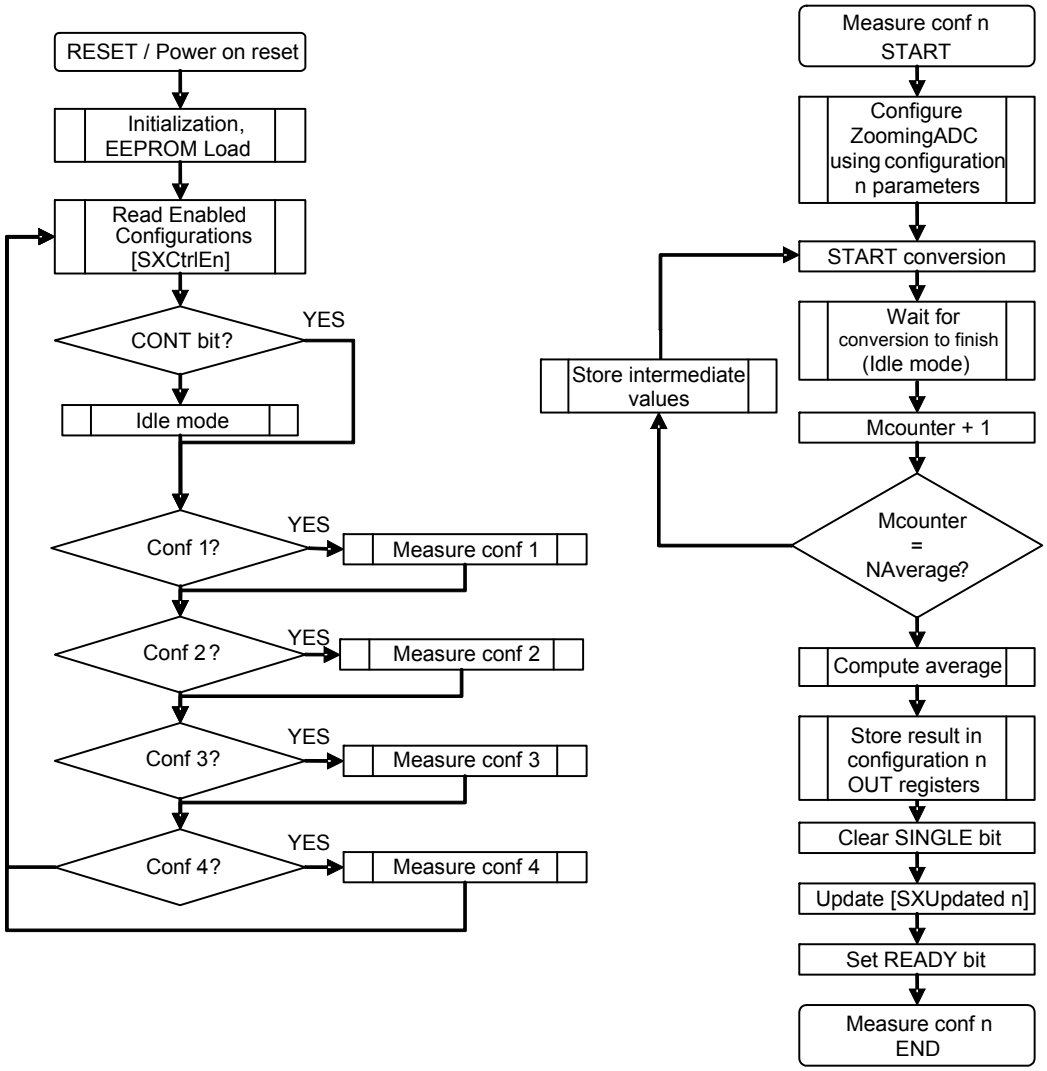


Figure 23. Measurement engine flowchart

The flowchart above shows the measurement engine function. It performs successively the measurements for each enabled configuration.

If in one or more configurations the bit CONT is set to 1, the measurements are performed again until the CONT bit is set to 0 through the I2C interface.

The engine goes out from the Idle mode every time an event occurs on the I2C interface.

11.3. Control registers

The parameters available on these registers affect the whole SX8722 and are common to all configuration register sets.

11.3.1. SXCtrl1 - SX8722 Control register 1

Register	7	6	5	4	3	2	1	0
SXCtrl1	EE_D	XTAL_D	CKOUT	reserved	EE	SLEEP	SHUT	CAL

Table 22. Control register; address 0x00

Bit	SXCtrl1	rw	Reset	Description
7	EE_D	r	x	Indicates if an EEPROM was detected at startup
6	XTAL_D	r	x	Indicates if an XTAL was detected at startup
5	CKOUT	rw	0	Enabled the clock output on CKOUT pin
4	RESERVED	rw	0	
3	EE	r	0	Is set to 1 when SX8722 loaded its configuration from the EEPROM at startup
2	SLEEP	rw	0	When set to 1 his bit activates the Sleep mode of the SX8722. Setting pin SLEEP to 1 has the same effect.
1	SHUT	rw	0	When set to 1 his bit activates the Shutdown mode of the SX8722. Setting pin SHUT to 1 has the same effect.
0	CAL	r	0	This flag shows if the SX8722 clock has been successfully calibrated.

11.3.2. SXCtrl2 - SX8722 Control register 2

Register	7	6	5	4	3	2	1	0
SXCtrl2	reserved	reserved	reserved	reserved	AL1OnC	AL1OffC	AL2OnC	AL2OffC

Table 23. Control register 2; address 0x01

Bit	SXCtrl1	rw	Reset	Description
3	AL1OnC	rw	0	Sets the logical condition for alarm 1 on (0 = OR, 1 = AND)
2	AL1OffC	rw	0	Sets the logical condition for alarm 1 on (0 = OR, 1 = AND)
1	AL2OnC	rw	0	Sets the logical condition for alarm 1 on (0 = OR, 1 = AND)
0	AL2OffC	rw	0	Sets the logical condition for alarm 1 on (0 = OR, 1 = AND)

Note: More information about the alarms condition usage on Alarm section

11.3.3. SXCfgEn - Configuration enabling register

Writing this register allows enabling or disabling the different configuration register sets.

Note: When the configuration is set to SINGLE, the bit CONFx is cleared automatically after the measurement is done.

Register	7	6	5	4	3	2	1	0
SXCfgEn	reserved	reserved	reserved	reserved	CONF4	CONF3	CONF2	CONF1

Table 24. Configuration enabling register; address 0x02

11.3.4. SXUpdated - Updated configuration register

The configuration update registers contain which configuration has been updated by a measurement result.

Register	7	6	5	4	3	2	1	0
SXUpdated	OVF4	OVF3	OVF2	OVF1	UCONF4	UCONF3	UCONF2	UCONF1

Table 25. Updated configuration register; address 0x03

These bits are set to 1 every time a measurement is done on one of the 4 configurations. When the registers are read, these bits are set back to 0 by the communication engine, the bits 4 to 7 indicates an overflow.

11.3.5. Configuration register - measurement mode

This register is present in each configuration; the bits 0 & 1 are controlling the measurement mode.

Register	7	6	5	4	3	2	1	0
CxSXCfg	reserved	FILTER TYPE[2:0]			ALRM1	ALRM2	SINGLE	CONT

Table 26. Measurement mode in configuration registers; addresses 0x10, 0x30, 0x50, 0x70

The bit SINGLE is set by the user, once the measurement is done; the measurement engine clears the CONF bit of the configuration.

The bit CONT is set by the user, the measurement is done continuously until this bit is cleared by the user.

11.4. Filtering

11.4.1. Filter types

There are 2 different filtering types:

1. Average filtering.
2. Moving average filtering.

The average filtering is an addition of n values divided by n, this kind of filter is useful when having a very noisy signal; the maximum average value is 256.

Advantage: Reduces noise due to the high quantity of samples.
Disadvantage: Takes the acquisition time of n samples to have a result.

The sliding window averaging is a filter that takes the n last measurements and gives the mean value of them.

- Advantage: result on each acquisition.
- Disadvantage: limited at ten samples. Additional delay.

Important note: ***The ADC filtering is faster, these additional filters should be used only if the number of conversion (NELCONV) and the over sampling rate (OSR) are set to their maximum.***

11.4.2. Configuration register - filtering

This register is present in each configuration; the bits 4 to 6 are controlling the filtering mode.

Register	7	6	5	4	3	2	1	0
CxSXCfg	reserved	FILTER TYPE[2:0]			ALRM1	ALRM2	SINGLE	CONT

Table 27. Filtering mode in configuration registers; addresses 0x10, 0x30, 0x50, 0x70

The table below shows the filter selection.

Filter type [6:4]	
Code	**Mode**
000	none
001	average filtering
010	moving average filtering
011	reserved

Table 28. Filter selection

11.4.3. Filter size register

This register is present in each configuration; the bits 0 to 7 are controlling the filter size.

Register	7	6	5	4	3	2	1	0
CxFParam	Filter size [7:0]							

Table 29. Filter size registers; addresses 0x11, 0x31, 0x51, 0x71

This register contains the number of samples used for the filtering.

Note that for a moving average filtering, this number is limited to 10.
(Putting a higher value will be interpreted as 10.)

11.5. Alarms

The SX8722 offers two alarms pins that have configurable on & off thresholds; these thresholds are on 16 bits.

Each configuration register set has 2 alarms, which can be enabled, when more than one configuration is using the same alarm pin, logical function is interacting between the two alarms sources. This condition can be a logical OR (default) or a logical AND.

11.5.1. Configuration register - alarms

The bits 2 & 3 enable the alarm 1 & 2 when set to 1.

Register	7	6	5	4	3	2	1	0
CxSXCfg	reserved	FILTER TYPE [2:0]			ALRM1	ALRM2	SINGLE	CONT

Table 30. Alarm enabling in configuration registers; addresses 0x10, 0x30, 0x50, 0x70

11.5.2. Alarm threshold registers

Registers	7	6	5	4	3	2	1	0
CxAlrm1OnMsb	S1ALRM1ON							
CxAlrm1OnLsb	S1ALRM1ON							
CxAlrm1OffMsb	S1ALRM1OFF							
CxAlrm1OffLsb	S1ALRM1OFF							
CxAlrm2OnMsb	S1ALRM2ON							
CxAlrm2OnLsb	S1ALRM2ON							
CxAlrm2OffMsb	S1ALRM2OFF							
CxAlrm2OffLsb	S1ALRM2OFF							

Table 31. Alarm threshold registers; addresses 0x12 to 0x19, 0x32 to 0x39, 0x52 to 0x59 and 0x72 to 0x79

11.5.3. SXCtrl2 - SX8722 Control register 2

This register is common to all configurations; it sets the relationship between the different alarm sources.

Register	7	6	5	4	3	2	1	0
SXCtrl2	reserved	reserved	reserved	reserved	AL1OnC	AL1OffC	AL2OnC	AL2OffC

Table 32. Alarm sources in Control register 2; address 0x02

When set to 1 the condition is AND and when set to 0 the condition is OR.
The diagram below shows the interaction between alarms sources.

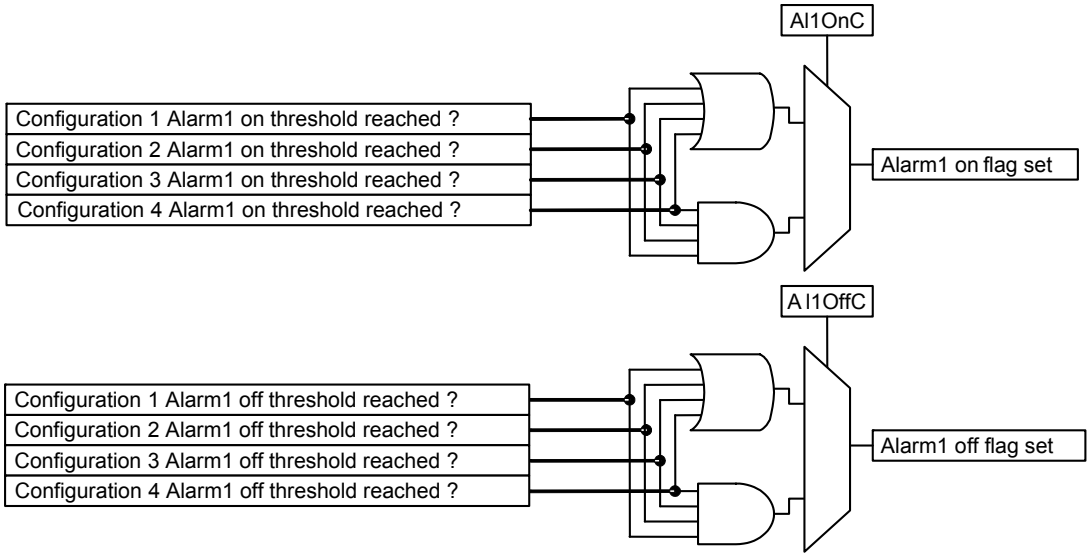


Figure 24. Alarms sources interaction

The flowchart below shows the management of the alarms flag (when at least one alarm is on).

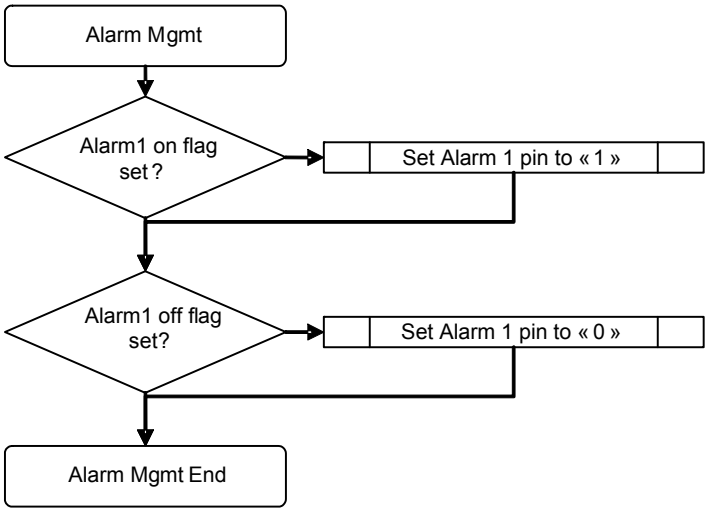


Figure 25. Alarms flag managment

11.6. I2C EEPROM

11.6.1. Overview

The SX8722 can interface a Standard I2C EEPROM. This allows:

- Stand alone usage.
- Parameters saving by save command.
- Parameters restore by load command.

The EE_POW pin allows the SX8722 to power the EEPROM in order to guarantee the lowest power having the EEPROM unpowered when unused.

When no EEPROM is used, the EE_SDA pin must be tied to ground.

11.6.2. Schematic

The schematic below shows the connections using standard I2C EEPPROM.

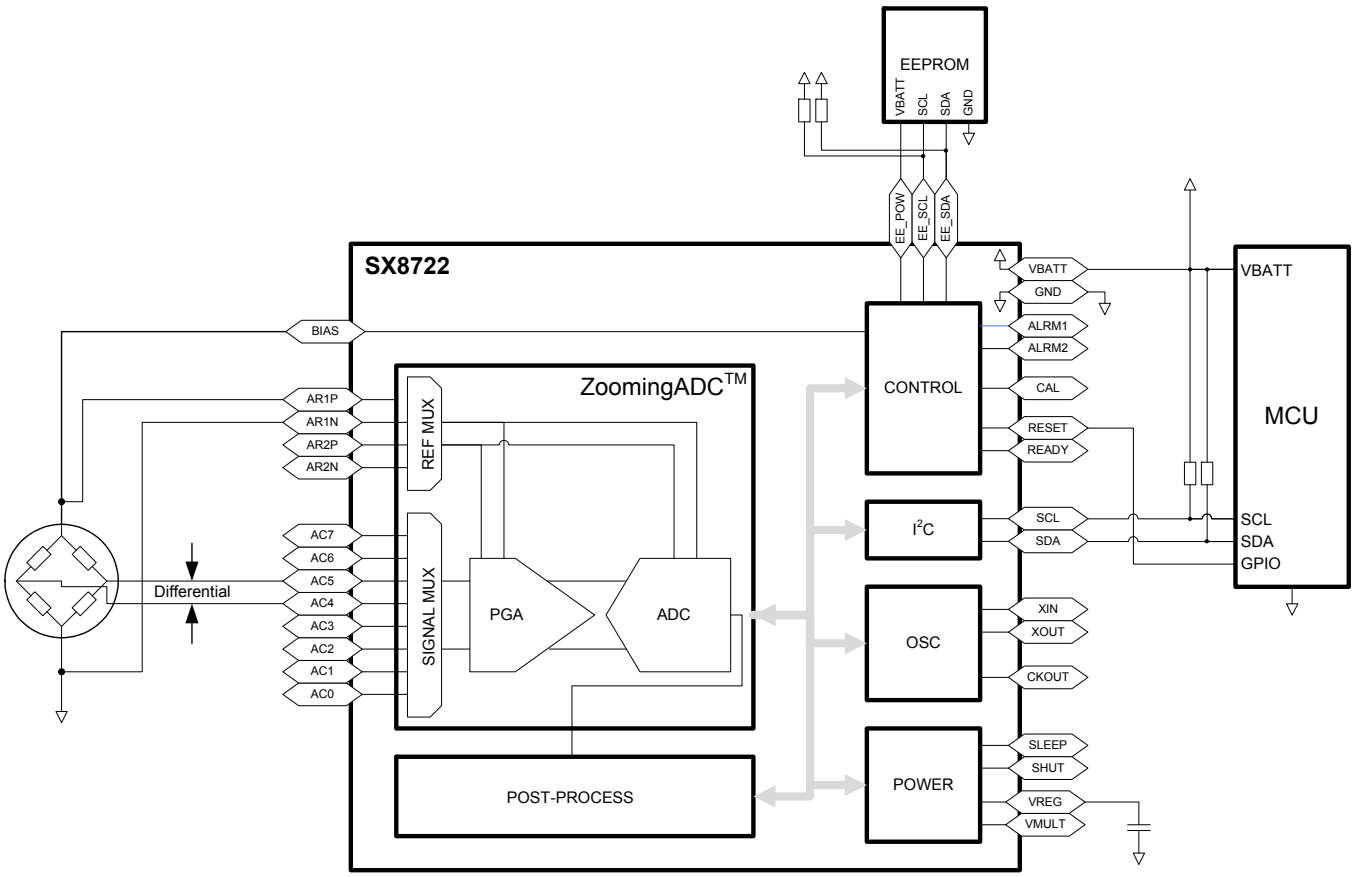


Figure 26. EEPROM connection

11.7. Using the SX8722 Stand alone

The SX8722 can be used stand alone to monitor signals and to generate alarms on configured thresholds.

Using a preprogrammed EEPROM allows the setup of these monitoring tasks.

11.7.1. Schematic

The schematic below shows an example of a stand alone configuration.

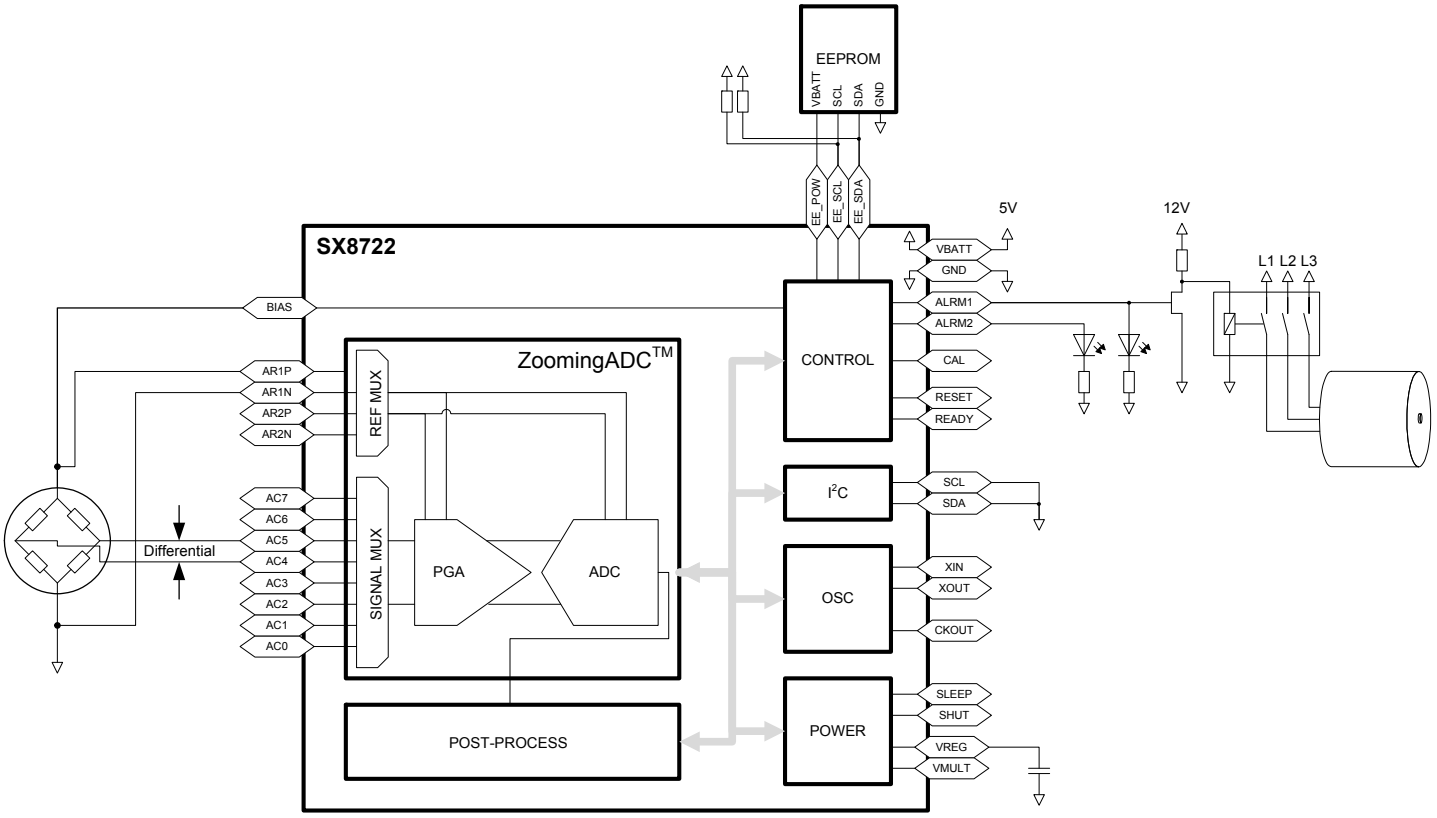


Figure 27. Example of stand alone configuration

11.8. Frequency calibration process

11.8.1. Overview

The SX8722 has an internal RC Oscillator working at 1.2 MHz +/- 600kHz. The calibration is optional. The main reason to calibrate the RC frequency is to fix the input impedance of the acquisition chain, function of the RC frequency.

This frequency can be calibrated using 2 methods.

- 32.768 kHz Xtal
- Input of a 32.768 kHz signal on the CAL pin.

11.8.2. Using an 32.768 kHz XTAL

When the SX8722 is connected to a 32.768 XTAL between XIN & XOUT, the CAL pin must be grounded. This indicates to SX8722 that an XTAL is present and allows frequency auto-calibration at power on.

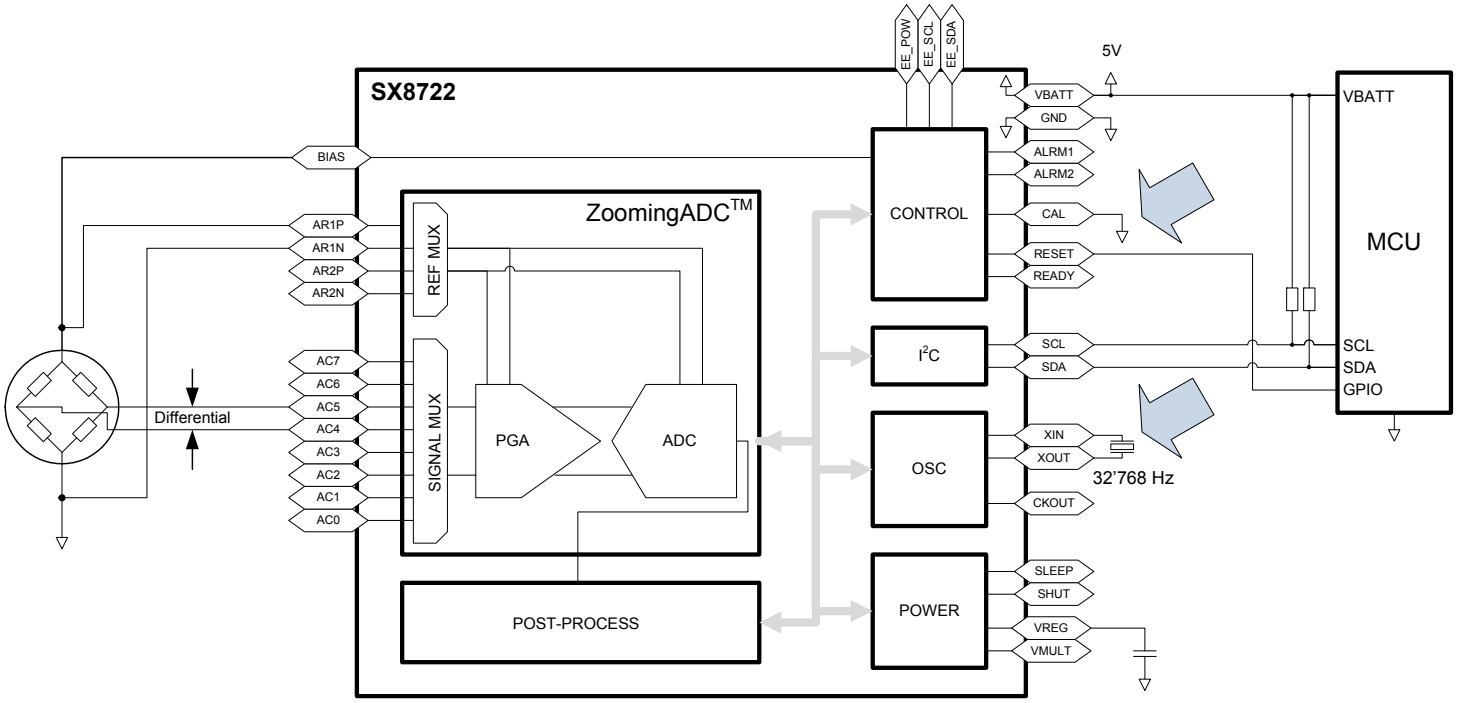


Figure 28. Calibration : using a 32'768 Hz XTAL

11.8.3. Using a 32.768 kHz External clock source

The host microcontroller can at any time send a 32.768kHz signal on CAL pin, the detection of a rising edge on the this pin initiates a calibration process. When the chip is calibrated, the pin READY rises to high level.

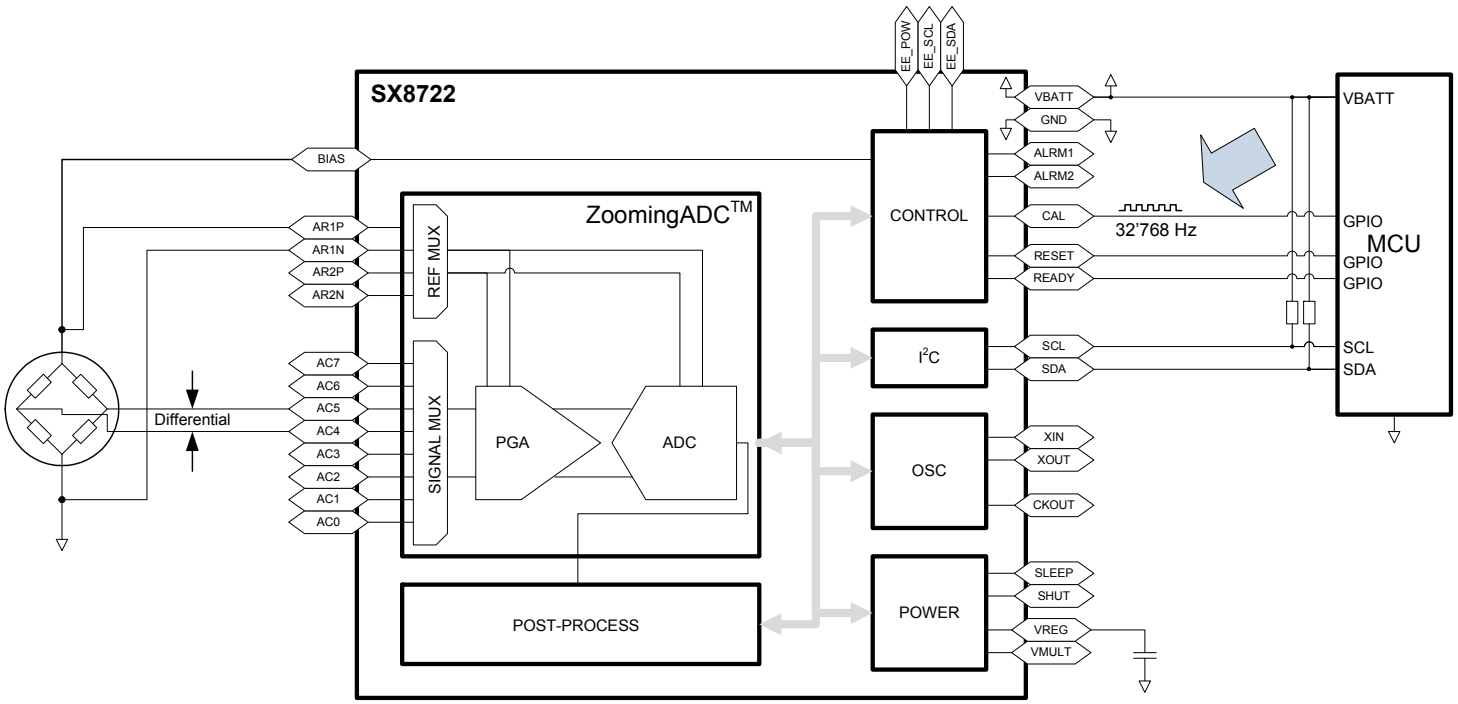


Figure 29. Calibration : using a 32'768 Hz signal

NOTE: If an external EEPROM is present, the calibration value is saved in it.

The tolerance signal must remain around 32.768 kHz +/- 10%

11.9. Working below 3 V

11.9.1. Operating range

The SX8722 operating range is 5.5 Volts downto 2.4 Volts. However, below 3 Volts the SX8722 enables an internal voltage multiplier to power the ZoomingADC™.

11.9.2. Internal voltage multiplier

This internal voltage multiplier is automatically enabled when the power supply goes below 3 Volts but the internal voltage multiplier requires an external capacitor between VMULT pin and ground, the value of this capacitor must be between 1 and 3 nF.

11.9.3. Schematic

The schematic below shows the capacitor connection:

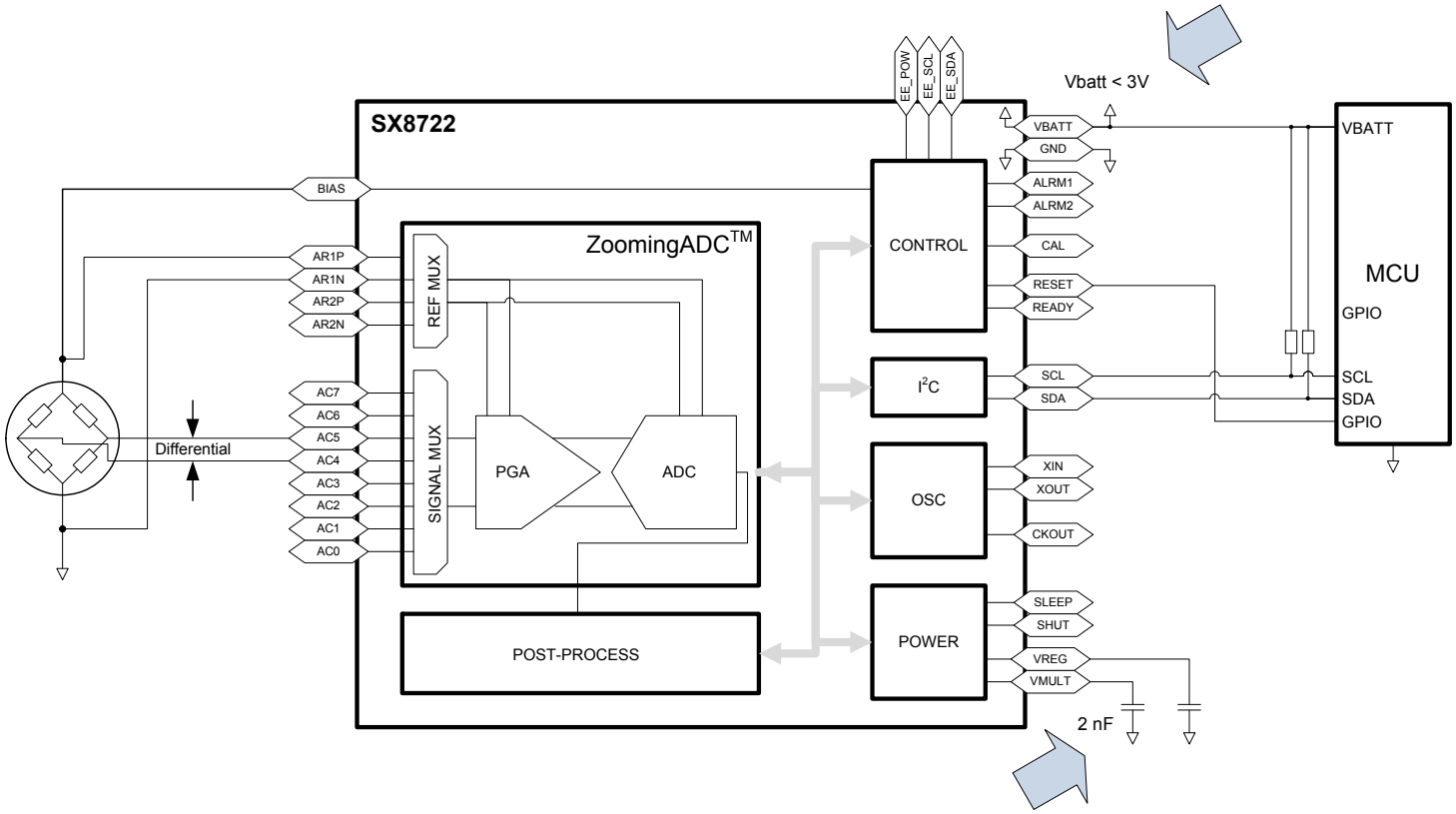


Figure 30. SX8722 working below 3V schematic

12. ZoomingADC

12.1. ZoomingADC Features

The ZoomingADC is a complete and versatile low-power analog front-end interface typically intended for sensing applications.

The key features of the ZoomingADC are:

- Programmable 6 to 16-bit dynamic range oversampled ADC
- Flexible gain programming between 0.5 and 1000
- Flexible and large range offset compensation
- 4-channel differential or 8-channel single-ended input multiplexer
- 2-channel differential reference inputs
- Power saving modes

12.1.1. Overview

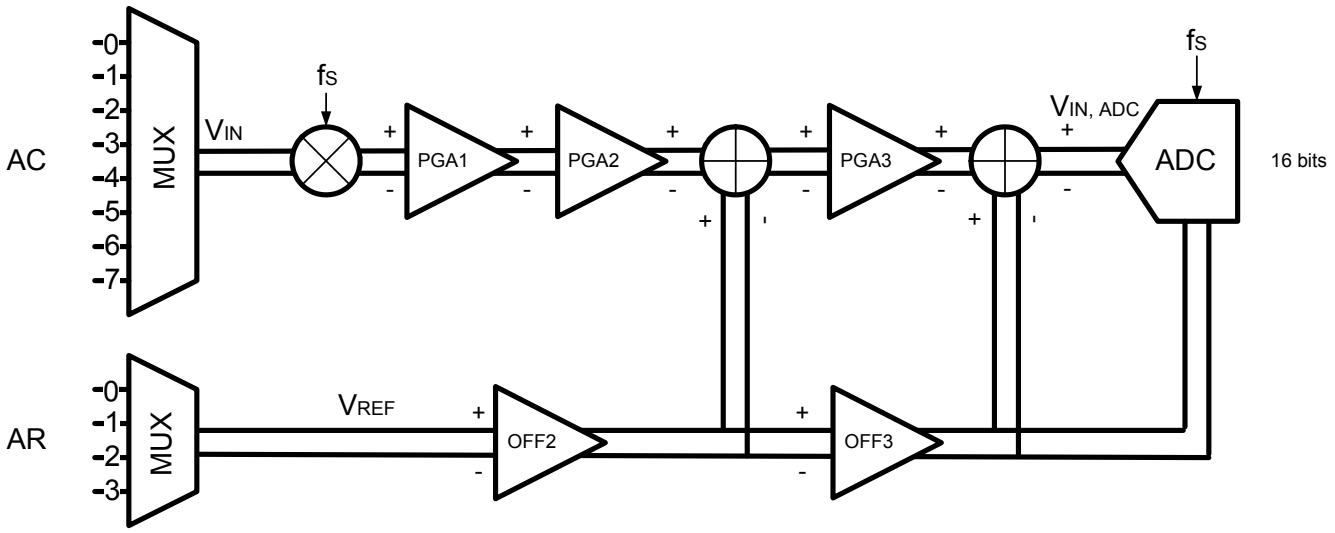


Figure 31. ZoomingADC general functional block diagram

The total acquisition chain consists of an input multiplexer, 3 programmable gain amplifier stages and an oversampled A/D converter. The reference voltage can be selected on two different channels. Two offset compensation amplifiers allow for a wide offset compensation range. The programmable gain and offset allow to zoom in on a small portion of the reference voltage defined input range.

12.2. Acquisition Chain

The figure above shows the general block diagram of the acquisition chain (AC).

Analog inputs can be selected among eight input channels, while reference input is selected between two differential channels.

The core of the zooming section is made of three differential programmable amplifiers (PGA). After selection of a combination of input and reference signals V_{IN} and V_{REF}, the input voltage is modulated and amplified through stages 1 to 3. Fine gain programming up to 1'000V/V is possible. In addition, the last two stages provide programmable offset. Each amplifier can be bypassed if needed.

The output of the PGA stages is directly fed to the analog-to-digital converter (ADC), which converts the signal $V_{IN,ADC}$ into digital.

Like most ADCs intended for instrumentation or sensing applications, the ZoomingADC is an over-sampled converter (See Note1). The ADC is a so-called incremental converter with bipolar operation (the ADC accepts both positive and negative input voltages). In first approximation, the ADC output result relative to full-scale (FS) delivers the quantity:

$$\frac{OUT_{ADC}}{FS/2} \cong \frac{V_{IN,ADC}}{V_{REF}/2}$$

(Eq. 1)

in two's complement (see Section 12.8.7 for details). The output code OUT_{ADC} is -FS/2 to +FS/2 for $V_{IN,ADC}$, $-V_{REF}/2$ to $+V_{REF}/2$ respectively. As will be shown in section 0, $V_{IN,ADC}$ is related to input voltage V_{IN} by the relationship:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot V_{REF} \quad [V]$$

(Eq. 2)

where GD_{TOT} is the total PGA gain, and $GDoff_{TOT}$ is the total PGA offset.

Note: Over-sampled converters are operated with a sampling frequency fs much higher than the input signal's Nyquist rate (typically fs is 20-1'000 times the input signal bandwidth). The sampling frequency to throughput ratio is large (typically 10-500). These converters include digital decimation filtering. They are mainly used for high resolution, and/or low-to-medium speed applications.

12.3. ZoomingADC Detailed block diagram

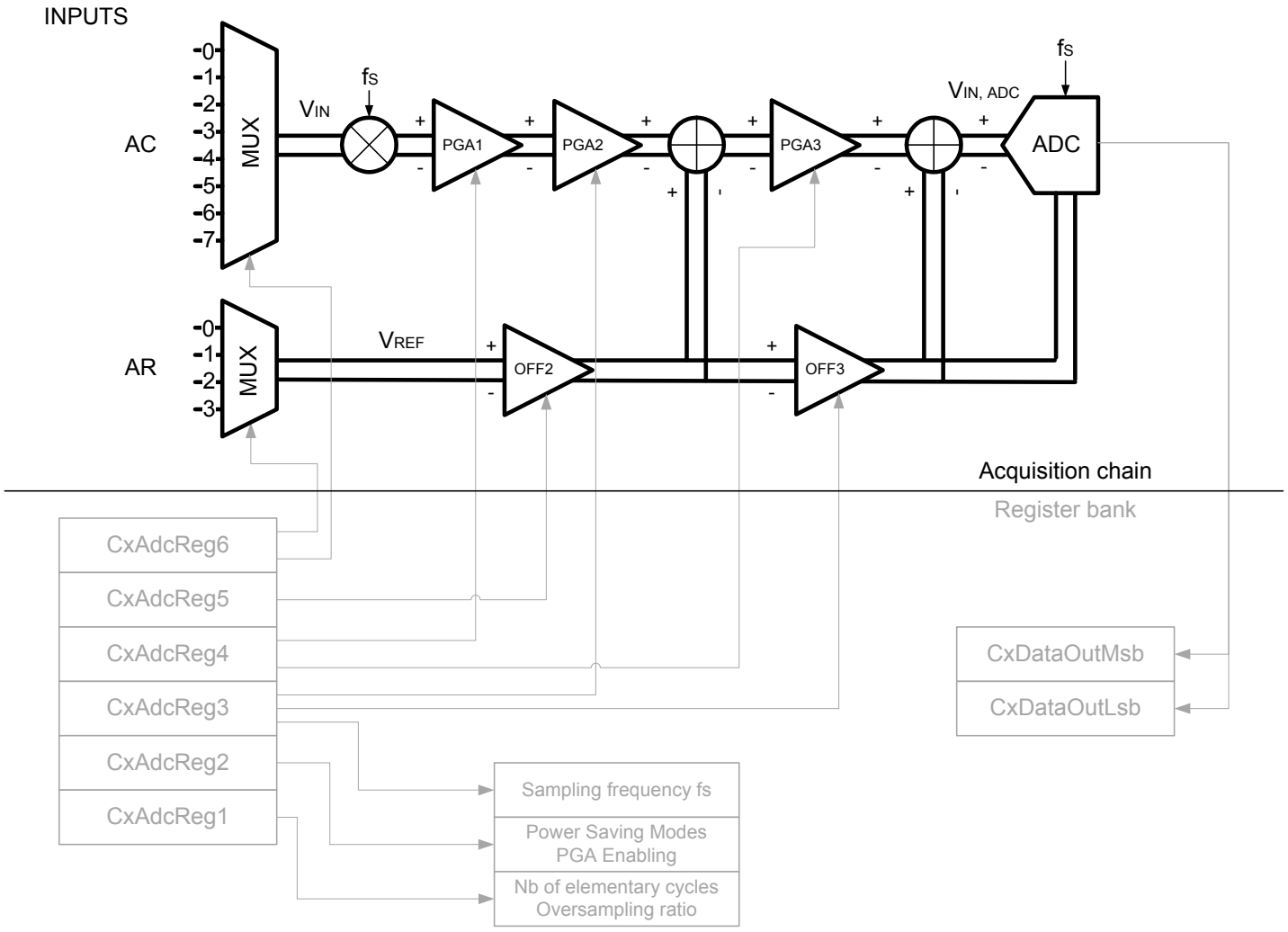


Figure 32. ZoomingADC detailed functional block diagram

12.4. ZoomingADC register map

There are six registers in the acquisition chain (AC), namely *CxZadcReg1*, *CxZadcReg2*, *CxZadcReg3*, *CxZadcReg4*, *CxZadcReg5* and *CxZadcReg6*. Tables below shows the mapping of control bits and functionality of these registers while Table 33 gives an overview of these six.

The register map only gives a short description of the different configuration bits. More detailed information is found in subsequent sections.

Registers	Addresses
CxZadcReg1	0x0A - 0x2A - 0x4A - 0x6A
CxZadcReg2	0x0B - 0x2B - 0x4B - 0x6B
CxZadcReg3	0x0C - 0x2C - 0x4C - 0x6C
CxZadcReg4	0x0D - 0x2D - 0x4D - 0x6D
CxZadcReg5	0x0E - 0x2E - 0x4E - 0x6E
CxZadcReg6	0x0F - 0x2F - 0x4F - 0x6F

Table 33. ADC settings registers

Bit	CxZadcReg1	rw	Reset	Description
7	reserved	rw	0	
6:5	SET_NELCONV [1:0]	rw	01	Sets the number of elementary conversions
4:2	SET_OSR [2:0]	rw	010	sets the oversampling rate of an elementary conversion
1	reserved	rw	0	
0	reserved	rw	0	

Table 34. CxZadcReg1; addresses 0x0A - 0x2A - 0x4A - 0x6A

Bit	CxZadcReg2	rw	Reset	Description
7:6	IB_AMP_ADC[1:0]	rw	11	Bias current selection of the A/D converter
5:4	IB_AMP_PGA[1:0]	rw	11	Bias current selection of the PGA stages
3:0	ENABLE[3:0]	rw	0000	Enabled the different PGA stages and the ADC

Table 35. CxZadcReg2; addresses 0x0B - 0x2B - 0x4B - 0x6B

Bit	CxZadcReg3	rw	Reset	Description
7:6	FIN[1:0]	rw	00	Sampling frequency selection
5:4	PGA2_PGA[1:0]	rw	00	PGA2 stage gain selection
3:0	PGA2_OFFSET[3:0]	rw	0000	PGA2 stage offset selection

Table 36. CxZadcReg3; addresses 0x0C - 0x2C - 0x4C - 0x6C

Bit	CxZadcReg4	rw	Reset	Description
7	PGA1_GAIN	rw	0	PGA1 stage gain selection
6:0	PGA3_PGA[6:0]	rw	0000000	PGA3 stage gain selection

Table 37. CxZadcReg4; addresses 0x0D - 0x2D - 0x4D - 0x6D

Bit	CxZadcReg5	rw	Reset	Description
7	reserved	r	0	
6:0	PGA3_OFFSET[6:0]	rw	0000000	PGA3 stage offset selection

Table 38. CxZadcReg5; addresses 0x0E - 0x2E - 0x4E - 0x6E

Bit	CxZadcReg6	rw	Reset	Description
7	PGA1_GAIN	r	0	Activity flag
6	PGA3_PGA[6:0]	r	0	Select default configuration
5:1	AMUX[4:0]	rw	00000	Input channel configuration selector
0	VMUX	rw	0	Reference channel selector

Table 39. CxZadcReg6; addresses 0x0F - 0x2F - 0x4F - 0x6F

12.5. ZoomingADC™ registers table

In table below the configuration of the peripheral registers is detailed. The system has a bank of eight 8-bit registers: six registers are used to configure the acquisition chain (CxZAdcReg1 to 6), and two registers are used to store the output code of the analog-to-digital conversion (CxDataOutMSB & LSB).

Register Name	Bit position							
	7	6	5	4	3	2	1	0
CxDataOutLSB	OUT[7:0]							
CxDataOutMSB	OUT[15:8]							
CxZadcReg1 Default values	R 0	SET_NC[1:0] 01		SET_OSR[2:0] 010			R 0	R 0
CxZadcReg2 Default value	IB_AMP_ADC[1:0] 11		IB_AMP_PGA[1:0] 11		ENABLE[3:0] 0001			
CxZadcReg3 Default value	FIN[1:0] 00		PGA2_GAIN[1:0] 00		PGA2_OFFSET 0000			
CxZadcReg4 Default value	PGA1_GAIN 0	PGA3_GAIN[6:0] 0000000						
CxZadcReg5 Default value	0	PGA3_OFFSET[6:0] 0000000						
CxZadcReg6 Default value	R 0	R 0	AMUX[4:0] 00000					VMUX 0

Table 40. ZoomingADC registers

Note Bits labelled R are reserved

With:

OUT: *(r) digital output code of the analog-to-digital converter. (MSB = OUT[15])*

SET_NELC: *(rw) sets the number of elementary conversions to $2^{SET\_NELC[1:0]}$. To compensate for offsets, the input signal is chopped between elementary conversions (1,2,4,8).*

SET_OSR: *(rw) sets the over-sampling rate (OSR) of an elementary conversion to $2^{(3+SET\_OSR[2:0])}$. OSR = 8, 16, 32, ..., 512, 1024.*

CONT: *(rw) setting this bit starts a conversion. A new conversion will automatically begin as long as the bit remains at 1.*

IB_AMP_ADC: *(rw) sets the bias current in the ADC to 0.25 x (1+ IB_AMP_ADC[1:0]) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.*

IB_AMP_PGA: *(rw) sets the bias current in the PGAs to 0.25 x (1+ IB_AMP_PGA[1:0]) of the normal operation current (25, 50, 75 or 100% of nominal current). To be used for low-power, low-speed operation.*

ENABLE: *(rw) enables the ADC modulator (bit 0) and the different stages of the PGAs (PGAi by bit i = 1,2,3). PGA stages that are disabled are bypassed.*

FIN: *(rw) These bits set the sampling frequency of the acquisition chain. Expressed as a fraction of the oscillator frequency, the sampling frequency is given as: 00 ' 1/4 f_{RC}, 01 ' 1/8 f_{RC}, 10 ' 1/32 f_{RC}, 11' ~8kHz.*

PGA1_GAIN: *(rw) sets the gain of the first stage: 0 ' 1, 1 ' 10.*

PGA2_GAIN: *(rw) sets the gain of the second stage: 00 ' 1, 01 ' 2, 10 ' 5, 11 ' 10.*

PGA3_GAIN: *(rw) sets the gain of the third stage to PGA3_GAIN[6:0] 1/12.*

PGA2_OFFSET: *(rw) sets the offset of the second stage between -1 and +1, with increments of 0.2. The MSB gives the sign (0 positive, 1 negative); amplitude is coded with the bits PGA2_OFFSET[5:0].*

PGA3_OFFSET: *(rw) sets the offset of the third stage between -5.25 and +5.25, with increments of 1/12. The MSB gives the sign (0 positive, 1 negative); amplitude is coded with the bits PGA3_OFFSET[5:0].*

AMUX(4:0): *(rw) AMUX[4] sets the mode (0 ' 4 differential inputs, 1 ' 7 inputs with A(0) = common reference) AMUX(3) sets the sign (0 ' straight, 1' cross) AMUX[2:0] sets the channel.*

VMUX: *(rw) sets the differential reference channel (0 ' R(1) and R(0), 1 ' R(3) and R(2)).*

(r = read; w = write; rw = read & write)

12.6. Input Multiplexers

The ZoomingADC has eight analog inputs AC_A(0) to AC_A(7) and four reference inputs AC_R(0) to AC_R(3). Let us first define the differential input voltage VIN and reference voltage VREF respectively as:

$$V_{IN} = V_{INP} - V_{INN} \quad [V]$$

(Eq. 3)

and:

$$V_{REF} = V_{REFP} - V_{REFN} \quad [V]$$

(Eq. 4)

As shown in Table 41 the inputs can be configured in two ways: either as 4 differential channels (VIN1 = AC_A(1) - AC_A(0),..., VIN4 = AC_A(7) - AC_A(6)), or AC_A(0) can be used as a common reference, providing 7 signal paths all referred to AC_A(0). The control word for the analog input selection is AMUX[4:0]. Notice that the bit AMUX[3] controls the sign of the input voltage.

AMUX [4:0] (RegACCfg5[5:1])	V_{INP}	V_{INN}	AMUX [4:0] (RegACCfg5[5:1])	V_{INP}	V_{INN}
00x00	AC_A(1)	AC_A(0)	01x00	AC_A(0)	AC_A(1)
00x01	AC_A(3)	AC_A(2)	01x01	AC_A(2)	AC_A(3)
00x10	AC_A(5)	AC_A(4)	01x10	AC_A(4)	AC_A(5)
00x11	AC_A(7)	AC_A(6)	01x11	AC_A(6)	AC_A(7)
10000	AC_A(0)	AC_A(0)	11000	AC_A(0)	AC_A(0)
10001	AC_A(1)		11001		AC_A(1)
10010	AC_A(2)		11010		AC_A(2)
10011	AC_A(3)		11011		AC_A(3)
10100	AC_A(4)		11100		AC_A(4)
10101	AC_A(5)		11101		AC_A(5)
10110	AC_A(6)		11110		AC_A(6)
10111	AC_A(7)		11111		AC_A(7)

Table 41. Analog input selection

Similarly, the reference voltage is chosen among two differential channels (VREF1 = AC_R(1)-AC_R(0) or VREF2 = AC_R(3)-AC_R(2)) as shown in Table 42 The selection bit is VMUX. The reference inputs VREFP and VREFN (common-mode) can be up to the power supply range.

VMUX (RegACCfg5[0])	V_{REFP}	V_{REFN}
0	AC_R(1)	AC_R(0)
1	AC_R(3)	AC_R(2)

Table 42. Analog input reference selection

12.7. Programmable Gain Amplifiers

The zooming function is implemented with three programmable gain amplifiers (PGA). These are:

- PGA1: coarse gain tuning
- PGA2: medium gain and offset tuning
- PGA3: fine gain and offset tuning

All gain and offset settings are realized with ratios of capacitors. The user has control over each PGA activation and gain, as well as the offset of stages 2 and 3. These functions are examined hereafter.

12.7.1. PGA & ADC Enabling

Depending on the application objectives, the user may enable or bypass each PGA stage. This is done according to the word ENABLE and the coding given in Table 43. To reduce power dissipation, the ADC can also be inactivated while idle.

Enable [3:0]	Block
XXX0 XXX1	ADC disabled ADC enabled
XX0X XX1X	PGA1 disabled PGA1 enabled
X0XX X1XX	PGA2 disabled PGA2 enabled
0XXX 1XXX	PGA3 disabled PGA3 enabled

Table 43. PGA and ADC enabling

12.7.2. PGA1

The first stage can have a buffer function (unity gain) or provide a gain of 10 (see Table 44). The voltage V_{D1} at the output of PGA1 is:

$$V_{D1} = GD_1 \cdot V_{IN} \quad [V]$$

(Eq. 5)

where GD1 is the gain of PGA1 (in V/V) controlled with the bit PGA1_GAIN.

PGA1_GAIN	PGA1 gain [V/V]
0	1
1	10

Table 44. PGA1 gain settings

12.7.3. PGA2

The second PGA has a finer gain and offset tuning capability, as shown in Table 45 and Table 46. The voltage VD2 at the output of PGA2 is given by:

$$V_{D2} = GD_2 \cdot V_{D1} - GDoff_2 \cdot V_{REF} \quad [V]$$

(Eq. 6)

where GD2 and GDoff2 are respectively the gain and offset of PGA2 (in V/V). These are controlled with the words PGA2_GAIN[1:0] and PGA2_OFFSET[3:0].

PGA2_GAIN	PGA2 gain [V/V]
00	1
01	2
10	5
11	10

Table 45. PGA2 gain settings

PGA2_OFFSET	PGA2 offset [V/V]
0000	0
0001	+0.2
0010	+0.4
0011	+0.6
0100	+0.8
0101	+1
1000	-0.2
1001	-0.4
1010	-0.6
1011	-0.8

PGA2_OFFSET	PGA2 offset [V/V]
1100	-1

Table 46. PGA2 offset settings

12.7.4. PGA3

The finest gain and offset tuning is performed with the third and last PGA stage, according to the following coding Tables.

PGA3_GAIN[6:0]	PGA3 gain [V/V]
0000000	0
0000001	1/12 (=0.083)
...	...
0000110	6/12
...	...
0001100	12/12
0010000	16/12
...	...
0100000	32/12
...	...
1000000	64/12
...	...
1111111	127/12 (=10.58)

Table 47. PGA3 gain settings

PGA3_GAIN[6:0]	PGA3 gain [V/V]
0000000	0
0000001	+1/12(=0.083)
0000010	+2/12
...	...
0010000	+16/12
...	...
0100000	+32/12
0111111	+63/12 (=+5.25)

PGA3_GAIN[6:0]	PGA3 gain [V/V]
1000000	0
1000001	-1/12(=-0.083)
1000010	-2/12
...	...
1010000	-16/12
...	...
1100000	-32/12
...	...
1111111	-63/12(=5.25)

Table 48. PGA3 offset settings

The output of PGA3 is also the input of the ADC. Thus, similarly to PGA2, we find that the voltage entering the ADC is given by:

$$V_{IN,ADC} = GD_3 \cdot V_{D2} - GDoff_3 \cdot V_{REF} \quad [V]$$

(Eq. 7)

where GD3 and GDoff3 are respectively the gain and offset of PGA3 (in V/V). The control words are PGA3_GAIN[6:0] and PGA3_OFFSET[6:0] . To remain within the signal compliance of the PGA stages, the condition:

$$V_{D1}, V_{D2} < V_{DD} \quad [V]$$

(Eq. 8)

must be verified.

Finally, combining equations Eq. 5 to Eq. 7 for the three PGA stages, the input voltage $V_{IN,ADC}$ of the ADC is related to V_{IN} by:

$$V_{IN,ADC} = GD_{TOT} \cdot V_{IN} - GDoff_{TOT} \cdot V_{REF} \quad [V]$$

(Eq. 9)

where the total PGA gain is defined as:

$$GD_{TOT} = GD_3 \cdot GD_2 \cdot GD_1 \quad [V]$$

(Eq. 10)

and the total PGA offset is:

$$GDoff_{TOT} = GDoff_3 + GD_3 \cdot GDoff_2 \quad [V/V]$$

(Eq. 11)

12.8. ADC Characteristics

The main performance characteristics of the ADC (resolution, conversion time, etc.) are determined by three programmable parameters:

- Oversampling frequency fS,
- over-sampling ratio OSR, and
- number of elementary conversions NELCONV.

The setting of these parameters and the resulting performances are described hereafter.

12.8.1. Conversion Sequence

A conversion is started each time the bit START or the bit DEF is set. As depicted in Figure 3, a complete analog-to-digital conversion sequence is made of a set of N_{ELCONV} elementary incremental conversions and a final quantization step. Each elementary conversion is made of (OSR+1) sampling periods TS=1/fS, i.e.:

$$T_{ELCONV} = (OSR+1)/f_S \quad [s]$$

(Eq. 12)

The result is the mean of the elementary conversion results. An important feature is that the elementary conversions are alternatively performed with the offset of the internal amplifiers contributing in one direction and the other to the output code.

Thus, converter internal offset is eliminated if at least two elementary sequences are performed (i.e. if NELCONV = 2). A few additional clock cycles are also required to initiate and end the conversion properly.

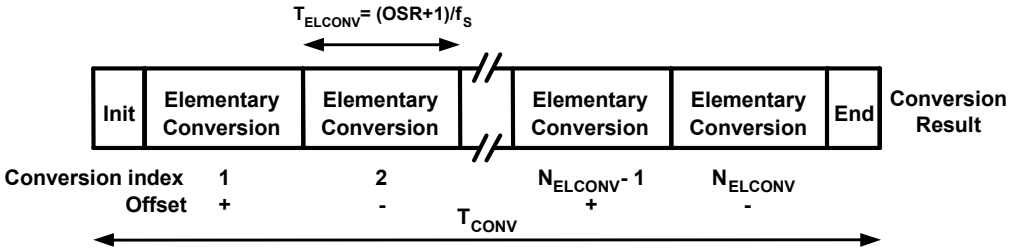


Figure 33. Analog-to-digital conversion sequence

12.8.2. Sampling Frequency

The word FIN[1:0] is used to select the sampling frequency fS (Table 49). Three sub-multiples of the internal RC-based frequency fRCEXT can be chosen. For FIN = "11", sampling frequency is about 8 kHz. Additional information on oscillators and their control can be found in the clock block documentation.

FIN[1:0]	Sampling frequency Fs [Hz]
00	1/4 f_{RC}
01	1/8 f_{RC}
10	1/32 f_{RC}
11	1/64 f_{RC}

Table 49. Sampling frequency settings (f_{RC} = RC-based frequency)

12.8.3. Over-Sampling Ratio

The over-sampling ratio (OSR) defines the number of integration cycles per elementary conversion. Its value is set with the word SET_OSR[2:0] in power of 2 steps (see Table 49) given by:

$$OSR = 2^{3+\mathrm{SET\_OSR}[2:0]}$$

(Eq. 13)

SET_OSR[2:0] (RegACCfg[4:2])	Over-Sampling Ratio OSR [-]
000	8
001	16

SET_OSR[2:0] (RegACCfg[4:2])	Over-Sampling Ratio OSR [-]
010	32
011	64
100	128
101	256
110	512
111	1024

Table 50. Over-sampling ratio settings

12.8.4. Elementary Conversions

As mentioned previously, the whole conversion sequence is made of a set of NELCONV elementary incremental conversions. This number is set with the word SET_NELC[1:0] in power of 2 steps (see Table 50) given by:

$$N_{ELCONV} = 2^{\mathrm{SET\_NELC[1:0]}}$$

(Eq. 14)

SET_OSR[2:0] (RegACCfg[4:2])	# of Elementary Conversion N_{ELCONV} [-]
00	1
01	2
10	4
11	8

Table 51. Number of elementary conversion

As already mentioned, N_{ELCONV} must be equal or greater than 2 to reduce internal amplifier offsets.

12.8.5. Resolution

The theoretical resolution of the ADC, without considering thermal noise, is given by:

$$n = 2 \cdot \log_2(OSR) + \log_2(N_{ELCONV}) \qquad [bits]$$

(Eq. 15)

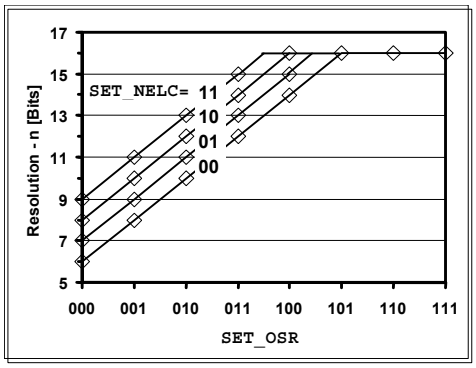


Figure 34. Resolution vs. SET_OSR[2:0] and SET_NELC[2:0]

SET_OSR [2:0]	SET_NELC			
	00	**01**	**10**	**11**
000	6	7	8	9
001	8	9	10	11
010	10	11	12	13
011	12	13	14	15
100	14	15	16	16
101	16	16	16	16
110	16	16	16	16
111	16	16	16	16

*(shaded area: resolution truncated to 16 bits due to output register size **CxDataOutMSB + CxDataOutLSB [15:0]**)*

Table 52. Resolution vs. SET_OSR[2:0] and SET_NELC[1:0] settings

Using look-up Table 52, resolution can be set between 6 and 16 bits. Notice that, because of 16-bit register use for the ADC output, **practical resolution is limited to 16 bits**, i.e. n = 16. Even if the resolution is truncated to 16 bit by the output register size, it may make sense to set OSR and NELCONV to higher values in order to reduce the influence of the thermal noise in the PGA .

12.8.6. Conversion Time & Throughput

As explained using Figure 3, conversion time is given by:

$$T_{CONV} = (N_{ELCONV} \cdot (OSR + 1) + 1) / f_S \quad [s]$$

(Eq. 16)

and throughput is then simply 1/T_{CONV}. For example, consider an over-sampling ratio of 256, 2 elementary conversions, and a sampling frequency of 300 kHz (SET_OSR = "101", SET_NELC = "01", f_{RC} = 1.2MHz, and FIN = "00"). In this case, using Table 53, the conversion time is 515 sampling periods, or 1.71ms. This corresponds to a throughput of 582Hz in continuous-time mode. The plot of figure below illustrates the classic trade-off between resolution and conversion time.

SET_OSR [2:0]	SET_NELC			
	00	**01**	**10**	**11**
000	10	19	37	73
001	18	35	69	137
010	34	67	133	265
011	66	131	261	521
100	130	259	517	1033
101	258	515	1029	2057
110	514	1027	2053	4105
111	1026	2051	4101	8201

Table 53. Normalized conversion time (T_{CONV} x f_S) vs. SET_OSR[2:0] and SET_NELC[1:0]

(normalized to sampling period 1/f_S)

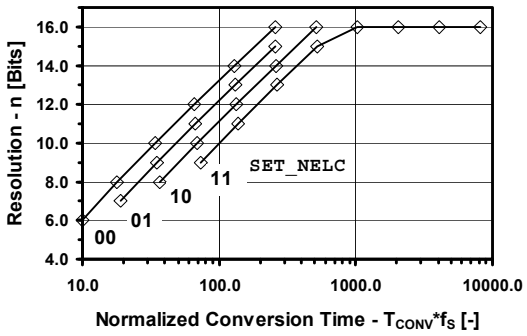


Table 54. Resolution vs. normalized conversion time for different SET_NELC[1:0]

12.8.7. Output Code Format

The ADC output code is a 16-bit word in two's complement format (see Table 55). For input voltages outside the range, the output code is saturated to the closest full-scale value (i.e. 0x7FFF or 0x8000). For resolutions smaller than 16 bits, the non-significant bits are forced to the values shown in Table 56. The output code, expressed in LSBs, corresponds to:

$$OUT_{ADC} = 2^{16} \cdot \frac{V_{IN,ADC}}{V_{REF}} \cdot \frac{OSR+1}{OSR} \qquad [LSB]$$

(Eq. 17)

Recalling equation Eq. 9, this can be rewritten as:

$$OUT_{ADC} = 2^{16} \cdot \frac{V_{IN}}{V_{REF}} \cdot \left(GD_{TOT} - GDoff_{TOT} \cdot \frac{V_{REF}}{V_{IN}} \right) \cdot \frac{OSR+1}{OSR} \qquad [LSB]$$

(Eq. 18)

where, from Eq. 10 and Eq. 11, the total PGA gain and offset are respectively:

$$GD_{TOT} = GD_3 \cdot GD_2 \cdot GD_1 \qquad [V/V]$$

and:

$$GDoff_{TOT} = GDoff_3 + GD_3 \cdot GDoff_2 \qquad [V/V]$$

ADC Input Voltage $V_{IN,ADC}$	% of Full Scale (FS)	Output in LSBs	Output Code in Hex
+2.49505 V	+0.5 x FS	$+2^{15}$-1 = 32'767	7FFF
+2.49497 V	...	$+2^{15}$-2 = 32'767	7FFE
...	...	...	...
+76.145 µV	...	+1	0001
0	0	0	0000
-76.145 µV	...	-1	8FFF
...	...	...	...

ADC Input Voltage $V_{IN,ADC}$	% of Full Scale (FS)	Output in LSBs	Output Code in Hex
+2.49505 V	...	$-2^{15}-1$ = -32'767	8001
+2.49513 V	-0.5 x FS	-2^{15} = -32'768	8000

Table 55. Basic ADC Relationships (example for: V_{REF} = 5V, OSR = 512, n = 16 bits)

SET_OSR[2:0]	SET_NELC = 00	SET_NELC = 01	SET_NELC = 10	SET_NELC = 11
000	1000000000	100000000	10000000	1000000
001	10000000	1000000	100000	10000
010	100000	10000	1000	100
011	1000	100	10	1
100	10	1	-	-
101	-	-	-	-
110	-	-	-	-
111	-	-	-	-

Table 56. Last forced LSBs in conversion output registers for resolution settings smaller than 16 bits (n < 16) (CxDataOutMsb[7:0] & CxDataOutLsb[7:0])

The equivalent LSB size at the input of the PGA chain is:

$$LSB = \frac{1}{2^n} \cdot \frac{V_{REF}}{GD_{TOT}} \cdot \frac{OSR}{OSR+1} \quad [V]$$

(Eq. 19)

Notice that the input voltage $V_{IN,ADC}$ of the ADC must satisfy the condition:

$$\left|V_{IN,ADC}\right| \le \frac{1}{2} \cdot (V_{REFP} - V_{REFN}) \cdot \frac{OSR}{OSR+1} \quad [V/V]$$

(Eq. 20)

to remain within the ADC input range.

IB_AMP_ADC [1:0]	IB_AMP_PGA [1:0]	ADC Bias Current	PGA Bias Current	Max. f_S [KHz]
00		1/4 x I_{ADC}		37.5
01		1/2 x I_{ADC}		75
10		3/4 x I_{ADC}		150
11		I_{ADC}		300
	00		1/4 x I_{ADC}	37.5
	01		1/2 x I_{ADC}	75
	10		3/4 x I_{ADC}	150
	11		I_{ADC}	300

Table 57. ADC & PGA power saving modes and maximum sampling frequency

12.9. Power Saving Modes

During low-speed operation, the bias current in the PGAs and ADC can be programmed to save power using the control words IB_AMP_PGA[1:0] and IB_AMP_ADC[1:0] (see Table 57). If the system is idle, the PGAs and ADC can even be disabled, thus, reducing power consumption to its minimum. This can considerably improve battery lifetime.

12.10. Input impedance

The PGAs of the ZoomingADC are a switched capacitor based blocks (see Switched Capacitor Principle chapter). This means that it does not use resistors to fix gains, but capacitors and switches. This has important implications on the nature of the input impedance of the block.

Using switched capacitors is the reason why, while a conversion is done, the input impedance on the selected channel of the PGAs is inversely proportional to the sampling frequency fs and to stage gain as given in Equation 21.

$$Z_{in} \geq \frac{768 \cdot 10^9 \, \Omega Hz}{f_s \cdot gain} \qquad [Ohm]$$

(Eq. 21)

The input impedance observed is the input impedance of the first PGA stage that is enabled or the input impedance of the ADC if all three stages are disabled.

PGA1 (with a gain of 10), PGA2 (with a gain of 10) and PGA3 (with a gain of 10) each have a minimum input impedance of 256 kOhm at fs = 300 kHz. Larger input impedance can be obtained by reducing the gain and/or by reducing the sampling frequency. Therefore, with a gain of 1 and a sampling frequency of 75 kHz, Zin > 10.2 MOhm.

The input impedance on channels that are not selected is very high (>100MOhm).

12.11. Switched Capacitor Principle

Basically, a switched capacitor is a way to emulate a resistor by using a capacitor. The capacitors are much easier to realize on CMOS technologies and they show a very good matching precision.

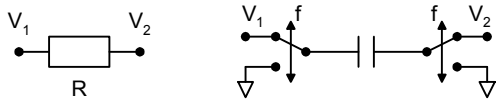


Figure 35. The Switched Capacitor Principle

A resistor is characterized by the current that flows through it (positive current leaves node V_1):

$$I = \frac{V_1 - V_2}{R} \quad [A]$$

(Eq. 22)

One can verify that the mean current leaving node V_1 with a capacitor switched at frequency f is:

$$\langle I \rangle = (V1 - V2) \cdot f \cdot C \quad [A]$$

(Eq. 23)

Therefore as a mean value, the switched capacitor 1/ (f x C) is equivalent to a resistor.

It is important to consider that this is only a mean value. If the current is not integrated (low impedance source), the impedance is infinite during the whole time but the transition.

What does it mean for the ZoomingADC?

If the fs clock is reduced, the mean impedance is increased. By dividing the fs clock by a factor 10, the impedance is increased by a factor 10.

One can reduce the capacitor that is switched by using an amplifier set to its minimal gain. In particular if PGA1 is used with gain 1, its mean impedance is 10x bigger than when it is used with gain 10.

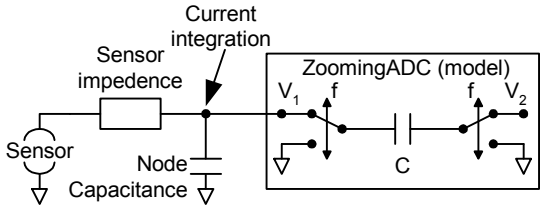


Figure 36. The Switched Capacitor Principle

One can increase the effective impedance by increasing the electrical bandwidth of the sensor node so that the switching current is absorbed through the sensor before the switching period is over. Measuring the sensor node will show short voltage spikes at the frequency fs, but these will not influence the measurement. Whereas if the bandwidth of the node is

lower, no spikes will arise, but a small offset can be generated by the integration of the charges generated by the switched capacitors, this corresponds to the mean impedance effect.

Note:

One can increase the mean input impedance of the ZoomingADC by lowering the acquisition clock fs.

One can increase the mean input impedance of the ZoomingADC by decreasing the gain of the first enabled amplifier.

One can increase the effective input impedance of the ZoomingADC by having a source with a high electrical bandwidth (sensor electrical bandwidth much higher than fs).

12.12. PGA Settling or Input Channel Modifications

PGAs are reset after each writing operation to registers CxZadcReg1-5. Similarly, input channels are switched after modifications of AMUX[4:0] or VMUX. To ensure precise conversion, the ADC must be started after a PGA or inputs common-mode stabilization delay. This is done by writing bit START several cycles after PGA settings modification or channel switching. Delay between PGA start or input channel switching and ADC start should be equivalent to OSR (between 8 and 1024) number of cycles. This delay does not apply to conversions made without the PGAs.

If the ADC is not settled within the specified period, there is most probably an input impedance problem (see previous section).

12.13. PGA Gain & Offset, Linearity and Noise

Hereafter are a few design guidelines that should be taken into account when using the ZoomingADC :

1. Keep in mind that increasing the overall PGA gain, or "zooming" coefficient, improves linearity but degrades noise performance.
2. Use the minimum number of PGA stages necessary to produce the desired gain ("zooming") and offset. Bypass unnecessary PGAs.
3. Put most gain on PGA3 and use PGA2 and PGA1 only if necessary.
4. PGA3 should be always ON for best linearity.
5. For low-noise applications where power consumption is not a primary concern, maintain the largest bias currents in the PGAs and in the ADC; i.e. set IB_AMP_PGA[1:0] = IB_AMP_ADC[1:0] = '11'.
6. For lowest output offset error at the output of the ADC, bypass PGA2 and PGA3. Indeed, PGA2 and PGA3 typically introduce an offset of about 5 to 10 LSB (16 bit) at their output. Note, however, that the ADC output offset is easily calibrated out by software.

12.14. Power Reduction

The ZoomingADC is particularly well suited for low-power applications. When very low power consumption is of primary concern, such as in battery operated systems, several parameters can be used to reduce power consumption as follows:

1. Operate the acquisition chain with a reduced supply voltage V_{BATT}.
2. Disable the PGAs which are not used during analog-to-digital conversion with ENABLE[3:0].
3. Disable all PGAs and the ADC when the system is idle and no conversion is performed.
4. Use lower bias currents in the PGAs and the ADC using the control words IB_AMP_PGA[1:0] and IB_AMP_ADC[1:0].
5. Reduce sampling frequency.

$[V^2]$

Finally, remember that power reduction is typically traded off with reduced linearity, larger noise and slower maximum sampling speed.

12.15. Noise

Ideally, a constant input voltage VIN should result in a constant output code. However, because of circuit noise, the output code may vary for a fixed input voltage. Thus, a statistical analysis on the output code of 1200 conversions for a constant input voltage was performed to derive the equivalent noise levels of PGA1, PGA2, and PGA3. The extracted rms output noise of PGA1, 2, and 3 are given in Table 58: standard output deviation and output rms noise voltage. Figure 37 shows the distribution for the ADC alone (PGA1, 2, and 3 bypassed). Quantization noise is dominant in this case, and, thus, the ADC thermal noise is below 16 bits.

The simple noise model of Figure 38 is used to estimate the equivalent input referred rms noise VN,IN of the acquisition chain in the model of Figure 39. This is given by the relationship:

$$V_{N,IN}{}^2 = \frac{\left(\frac{V_{N1}}{GD_1}\right)^2 + \left(\frac{V_{N2}}{GD_1 \cdot GD_2}\right)^2 + \left(\frac{V_{N3}}{GD_1 \cdot GD_2 \cdot GD_3}\right)^2}{\left(OSR \cdot N_{ELCONV}\right)} \qquad [V^2 rms]$$

(Eq. 24)

where VN1, VN2, and VN3 are the output rms noise figures of Table 58, GD1, GD2, and GD3 are the PGA gains of stages 1 to 3 respectively. As shown in this equation, noise can be reduced by increasing OSR and NELCONV (increases the ADC averaging effect, but reduces noise).

Parameter	PGA1	PGA2	PGA3
Standard deviation at ADC output (LSB)	0.85	1.4	1.5
Output RMS noise(uV)	205 x (VN1)	340 x (VN2)	365 x (VN3)

Table 58. PGA Noise Measurements (n = 16 bits, OSR = 512, NELCONV = 2, VREF = 5 V)

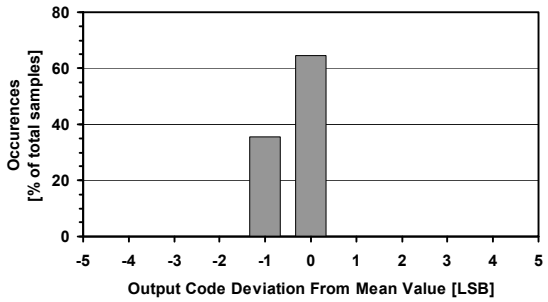


Figure 37. ADC Noise (PGA1, 2 & 3 Bypassed, OSR = 512, NELCONV = 2)

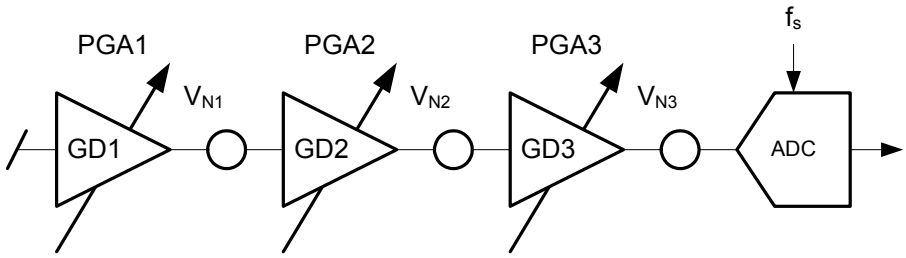


Figure 38. Simple Noise Model for PGAs and ADC

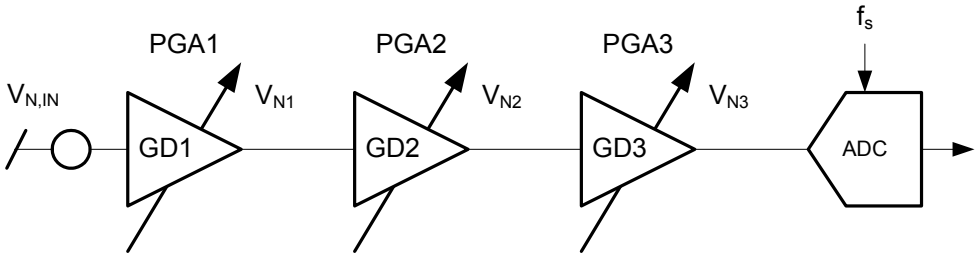


Figure 39. Total Input Referred Noise

As an example, consider the system where: GD2 = 10 (GD1 = 1; PGA3 bypassed), OSR = 512, N_{ELCONV} = 2, V_{REF} = 5 V. In this case, the noise contribution V_{N1} of PGA1 is dominant over that of PGA2. Using Equation 24, we get: $V_{N,IN}$ = 6.4 µV (rms) at the input of the acquisition chain, or, equivalently, 0.85 LSB at the output of the ADC. Considering 0.2 V (rms) maximum signal amplitude, the signal-to-noise ratio is 90dB.

Noise can also be reduced by the additional average filters implemented in the Measurement Engine. These filters are described in section 11.4 Filtering. By making an average on a number of subsequent measurements, the apparent noise is reduced the square root of the number of measurement used to make the average.

12.16. Gain Error and Offset Error

Gain error is defined as the amount of deviation between the ideal transfer function (theoretical Equation 18) and the measured transfer function (with the offset error removed).

The actual gain of the different stages can vary depending on the fabrication tolerances of the different elements. Although these tolerances are specified to a maximum of +/-3%, they will be most of the time around 0.5%. Moreover, the tolerances between the different stages are not correlated and the probability to get the maximal error in the same direction in all stages is very low. Finally, these gain errors can be calibrated by the software at the same time with the gain errors of the sensor for instance.

Figure 40 shows gain error drift vs. temperature for different PGA gains. The curves are expressed in % of Full-Scale Range (FSR) normalized to 25°C.

Offset error is defined as the output code error for a zero volt input (ideally, output code = 0). The offset of the ADC and the PGA1 stage are completely suppressed if NELCONV > 1.

The measured offset drift vs. temperature curves for different PGA gains are depicted in Figure 41. The output offset error, expressed in LSB for 16-bit setting, is normalized to 25°C. Notice that if the ADC is used alone, the output offset error is below +/-1 LSB and has no drift.

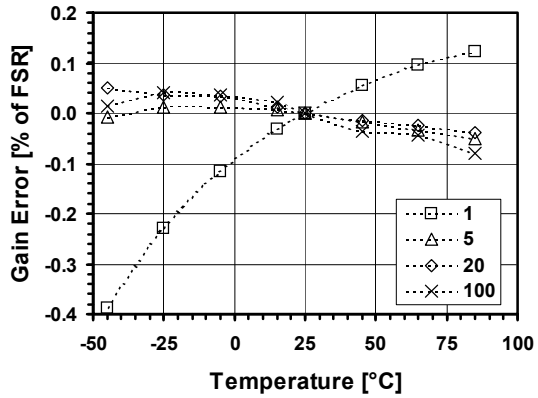


Figure 40. Gain Error vs. Temperature for Different PGA Gains

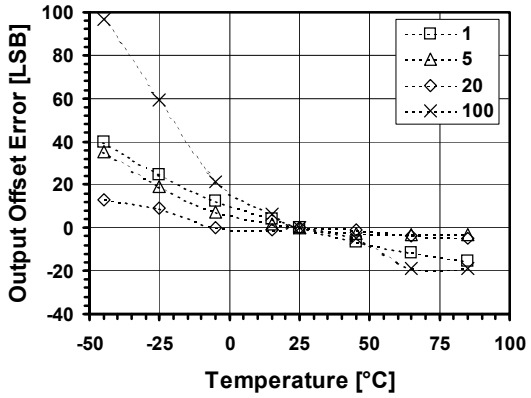


Figure 41. Offset Error vs. Temperature for Different PGA Gains

13. Typical performances

13.1. Current consumption

SX8722 mean current consumption in active mode is around 200 [µA], without enabled PGA. The value of the gain of de PGA can have a negligible influence on consumption in active mode.

Additional consumption depends on the active PGA and on the bias current parameter.

	Current for each amplifier in [uA]		
	I_{PGA1}	I_{PGA2}	I_{PGA3}
bias 25 %	50	40	50
bias 50 %	95	75	98
bias 75 %	140	110	145
bias 100 %	185	145	190

Table 59. PGA current consumption

Example 1 : Bias current 25%

PGA1: enabled
PGA2: enabled
PGA3: enabled

SX8722 measured current consumption: ~330 µA

Example 2 : Bias current 100%

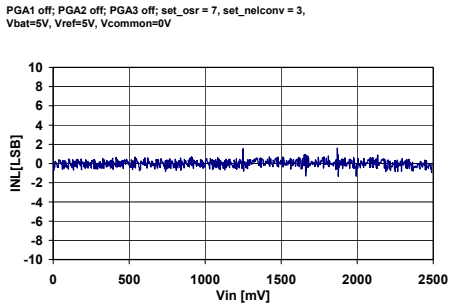
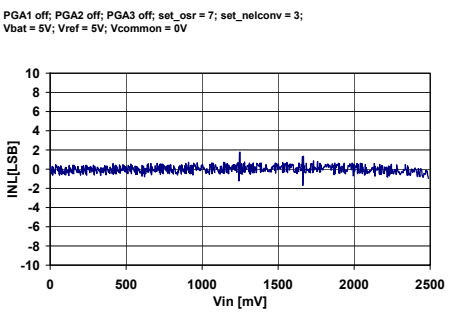
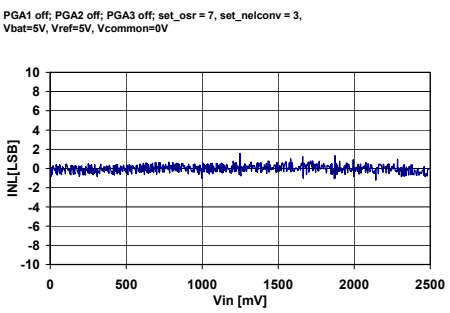
PGA1: enabled
PGA2: enabled
PGA3: enabled

SX8722 measured current consumption: ~710 µA

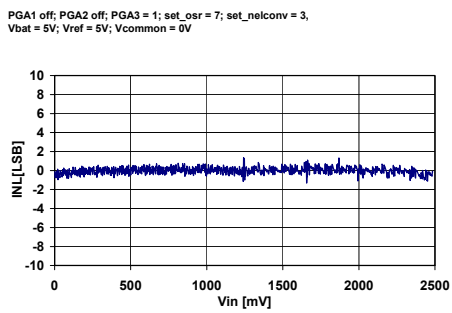
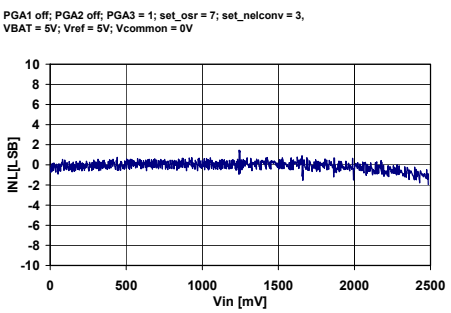
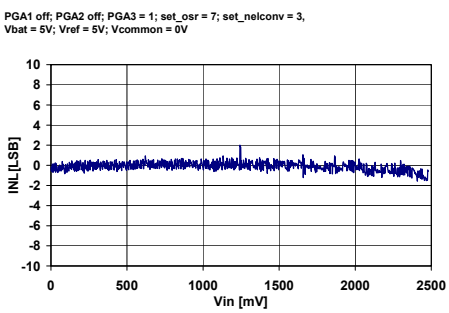
13.2. ZoomingADC

13.2.1. Integral non-linearity

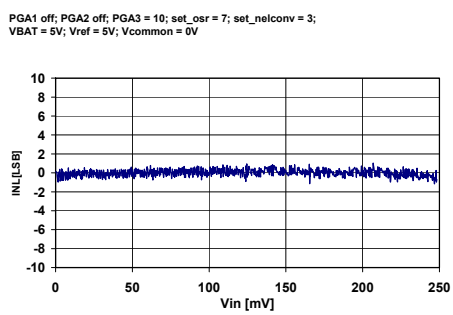
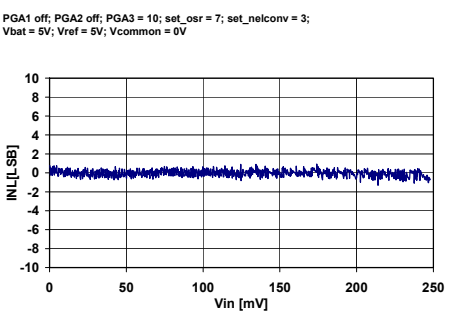
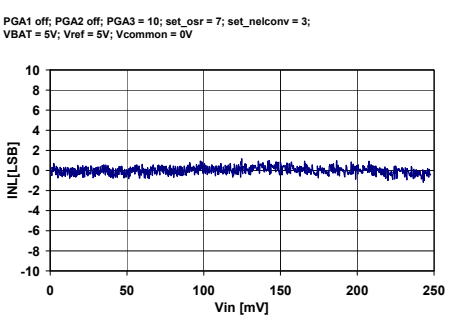
ADC without PGA

-40°C	25°C	85°C
		

Gain 1

-40°C	25°C	85°C
		

Gain 10

-40°C	25°C	85°C
		

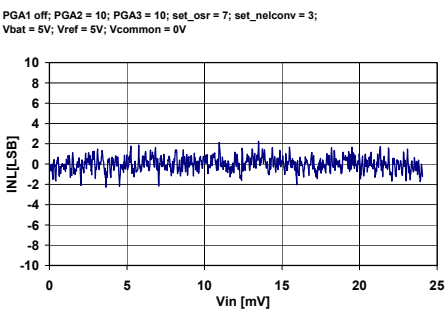
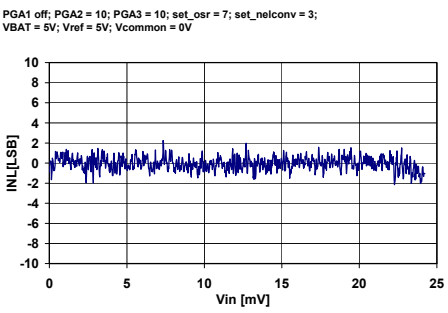
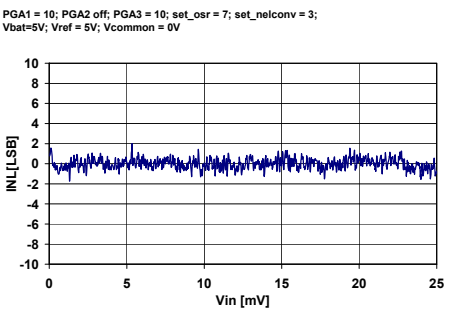
Gain 100		
-40°C	25°C	85°C
		

Figure 42. INL over temperature for different gains

13.2.2. Differential non-linearity

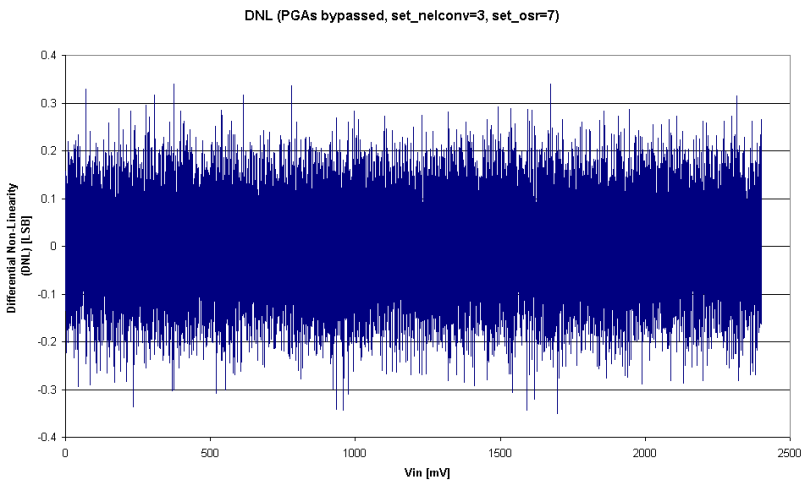
DNL: significantly lower than one LSB	

Figure 43. ADC differential non-linearity

13.2.3. Resolution vs acquisition time

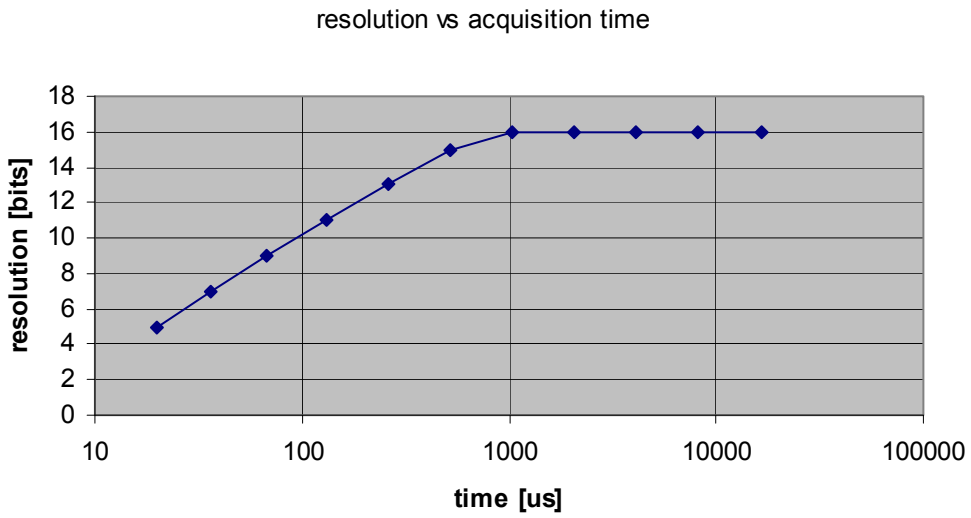


Figure 44. ADC resolution vs Acquisition time

14. Register Memory Map and Description

14.1. Memory Map

The table below describes the register/memory map that can be accessed through the I2C interface. It indicates the register name, register address and the register contents.

Adress	Register	Bit	Description
SX8722 General Configuration			
0x00	SXCtrl1	8	Configuration register of the SX8722
0x01	SXCtrl2	8	Configuration register of the SX8722
0x02	SXCfgEn	8	Configuration enable register,enables configurations from 1 to 4
0x03	SXUpdated	8	Updated value on configuration registers
0x04	SXRcFrequ1	8	Fine RC adjustment register
0x05	SXRcFrequ2	8	Coarse RC adjustment register
0x06	SXTest	8	Test purpose register puts SX8722 in remote mode
0x07	SXAI1	8	Reserved
0x08	SXAI2	8	Reserved
0x09	SXReserved1	8	Reserved
Configuration 1			
0x0A	C1ZAdcReg1	8	ZoomingADC Register 01
0x0B	C1ZAdcReg2	8	ZoomingADC Register 02
0x0C	C1ZAdcReg3	8	ZoomingADC Register 03
0x0D	C1ZAdcReg4	8	ZoomingADC Register 04
0x0E	C1ZAdcReg5	8	ZoomingADC Register 05
0x0F	C1ZAdcReg6	8	ZoomingADC Register 06
0x10	C1SXCfg	8	SX configurations related to this set
0x11	C1FParam	8	Filter size
0x12	C1Alrm1OnMsb	16	Alarm 1 "ON" threshold
0x13	C1Alrm1OnLsb		
0x14	C1Alrm1OffMsb	16	Alarm 1 "OFF" threshold
0x15	C1Alrm1OffLsb		
0x16	C1Alrm2OnMsb	16	Alarm 2 "ON" threshold
0x17	C1Alrm2OnLsb		

Adress	Register	Bit	Description
0x18	C1Alrm2OffMsb	16	Alarm 2 "OFF" threshold
0x19	C1Alrm2OffLsb		
0x1A	C1DataOutLsb	16	Configuration 1 data out
0x1B	C1DataOutMsb		
Configuration 2			
0x2A	C2ZAdcReg1	8	ZoomingADC Register 01
0x2B	C2ZAdcReg2	8	ZoomingADC Register 02
0x2C	C2ZAdcReg3	8	ZoomingADC Register 03
0x2D	C2ZAdcReg4	8	ZoomingADC Register 04
0x2E	C2ZAdcReg5	8	ZoomingADC Register 05
0x2F	C2ZAdcReg6	8	ZoomingADC Register 06
0x30	C2SXCfg	8	SX configurations related to this set
0x31	C2FParam	8	Filter size
0x32	C2Alrm1OnMsb	16	Alarm 1 "ON" threshold
0x33	C2Alrm1OnLsb		
0x34	C2Alrm1OffMsb	16	Alarm 1 "OFF" threshold
0x35	C2Alrm1OffLsb		
0x36	C2Alrm2OnMsb	16	Alarm 2 "ON" threshold
0x37	C2Alrm2OnLsb		
0x38	C2Alrm2OffMsb	16	Alarm 2 "OFF" threshold
0x39	C2Alrm2OffLsb		
0x3A	C2DataOutMsb	16	Configuration 2 data out
0x3B	C2DataOutLsb		
Configuration 3			
0x4A	C3ZAdcReg1	8	ZoomingADC Register 01
0x4B	C3ZAdcReg2	8	ZoomingADC Register 02
0x4C	C3ZAdcReg3	8	ZoomingADC Register 03
0x4D	C3ZAdcReg4	8	ZoomingADC Register 04
0x4E	C3ZAdcReg5	8	ZoomingADC Register 05
0x4F	C3ZAdcReg6	8	ZoomingADC Register 06
0x50	C3SXCfg	8	SX configurations related to this set
0x51	C3FParam	8	Filter size

Adress	Register	Bit	Description
0x52	C3Alrm1OnMsb	16	Alarm 1 "ON" threshold
0x53	C3Alrm1OnLsb		
0x54	C3Alrm1OffMsb	16	Alarm 1 "OFF" threshold
0x55	C3Alrm1OffLsb		
0x56	C3Alrm2OnMsb	16	Alarm 2 "ON" threshold
0x57	C3Alrm2OnLsb		
0x58	C3Alrm2OffMsb	16	Alarm 2 "OFF" threshold
0x59	C3Alrm2OffLsb		
0x5A	C3DataOutMsb	16	Configuration 3 data out
0x5B	C3DataOutLsb		
Configuration 4			
0x6A	C4ZAdcReg1	8	ZoomingADC Register 01
0x6B	C4ZAdcReg2	8	ZoomingADC Register 02
0x6C	C4ZAdcReg3	8	ZoomingADC Register 03
0x6D	C4ZAdcReg4	8	ZoomingADC Register 04
0x6E	C4ZAdcReg5	8	ZoomingADC Register 05
0x6F	C4ZAdcReg6	8	ZoomingADC Register 06
0x70	C4SXCfg	8	SX configurations related to this set
0x71	C4FParam	8	Filter size
0x72	C4Alrm1OnMsb	16	Alarm 1 "ON" threshold
0x73	C4Alrm1OnLsb		
0x74	C4Alrm1OffMsb	16	Alarm 1 "OFF" threshold
0x75	C4Alrm1OffLsb		
0x76	C4Alrm2OnMsb	16	Alarm 2 "ON" threshold
0x77	C4Alrm2OnLsb		
0x78	C4Alrm2OffMsb	16	Alarm 2 "OFF" threshold
0x79	C4Alrm2OffLsb		
0x7A	C4DataOutMsb	16	Configuration 4 data out
0x7B	C4DataOutLsb		

14.2. Register description

The register descriptions are presented here in ascending order of Register Address. Some registers carry several individual data fields of various sizes; from single-bit values (e.g. flags), upwards. Some data fields are spread across multiple registers. Unused bits are 'don't care' and writing either 0 or 1 will not affect any function of the device. After power on reset the registers will have the values indicated in the tables "Reset" column.

14.2.1. SX8722 general configuration

Bit	Bit Name	Mode	Reset	Description
7	EE_D	r	x	Indicates if an EEPROM was detected at startup
6	XTAL_D	r	x	Indicates if an XTAL was detected at startup
5	CKOUT	rw	0	Enabled the clock output on CKOUT pin
4	RESERVED	rw	0	
3	EE	r	0	Is set to 1 when SX8722 loaded its configuration from the EEPROM at startup.
2	SLEEP	rw	0	When set to 1 his bit activates the Sleep mode of the SX8722. Setting pin SLEEP to 1 has the same effect.
1	SHUT	rw	0	When set to 1 his bit activates the Shutdown mode of the SX8722. Setting pin SHUT to 1 has the same effect.
0	CAL	r	0	This flag shows if the SX8722 clock has been successfully calibrated.

Table 60. SXCtrl1 (0x00)

Bit	Bit name	Mode	Reset	Description
7:4	reserved	r	x	
3	AL1OnC	rw	0	Sets the logical condition for alarm 1 on (0 = OR, 1 = AND)
2	AL1OffC	rw	0	Sets the logical condition for alarm 1 off (0 = OR, 1 = AND)
1	AL2OnC	rw	0	Sets the logical condition for alarm 2 on (0 = OR, 1 = AND)
0	AL2OffC	rw	0	Sets the logical condition for alarm 2 off (0 = OR, 1 = AND)

Table 61. SXCtrl2 (0x01)

Bit	Name	Mode	Reset	Description
7:4	reserved	r	x	
3	CONF4	rw	0	Configuration 4 enabling
2	CONF3	rw	0	Configuration 3 enabling
1	CONF2	rw	0	Configuration 2 enabling

Bit	Name	Mode	Reset	Description
0	CONF1	rw	0	Configuration 1 enabling

Table 62. SXCfgEn (0x02)

Bit	Name	Mode	Reset	Description
7	OVF4	r	0	Overflow on configuration 4
6	OVF3	r	0	Overflow on configuration 3
5	OVF2	r	0	Overflow on configuration 2
4	OVF1	r	0	Overflow on configuration 1
3	UCONF4	r	0	Indicates that configuration 4 has been updated by a measurement result.
2	UCONF3	r	0	Indicates that configuration 3 has been updated by a measurement result.
1	UCONF2	r	0	Indicates that configuration 2 has been updated by a measurement result.
0	UCONF1	r	0	Indicates that configuration 1 has been updated by a measurement result.

Table 63. SXUpdated (0x03)

Bit	Name	Mode	Reset	Description
7:0	Fine RC	rw	x	Fine RC adjustment. Set by the calibration procedure.

Table 64. SXRcFrequ1 (0x04)

Bit	Name	Mode	Reset	Description
7:0	Coarse RC	rw	x	Coarse RC adjustment. Set by the calibration procedure.

Table 65. SXRcFrequ2 (0x05)

14.2.2. Configuration 1 registers

Bit	Name	Mode	Reset	Description
7	reserved	r	x	
6:5	SET_NELC	rw	01	Sets the number of elementary conversion to $2^{\mathbf{SET\_NELC[1:0]}}$. To compensate for offset the signal is chopped between elementary conversion.
4:2	SET_OSR	rw	010	Sets the ADC over-sampling rate of an elementary conversion to $2^{\mathbf{3+SET\_OSR[2:0]}}$.
1	reserved	r	x	
0	reserved	r	x	

Table 66. C1ZAdcReg1 (0x0A)

Bit	Name	Mode	Reset	Description
7:6	IB_AMP_ADC[1:0]	rw	11	Bias current selection of the A/D converter.
5:4	IB_AMP_PGA[1:0]	rw	11	Bias current selection of the PGA stages.
3:0	ENABLE[3:0]	rw	0000	Enables the different PGA stages and ADC. ◆ XXX1 - ADC enable ◆ XX1X - PGA3 enable ◆ X1XX - PGA2 enable ◆ 1XXX - PGA1 enable

Table 67. C1ZAdcReg2 (0x0B)

Bit	Name	Mode	Reset	Description
7:6	FIN[1:0]	rw	00	Sampling frequency selection
5:4	PGA2_GAIN[1:0]	rw	00	PGA2 stage gain selection
3:0	PGA2_OFFSET[3:0]	rw	0000	PGA2 stage offset selection

Table 68. C1ZAdcReg3 (0x0C)

Bit	Name	Mode	Reset	Description
7	PGA1_GAIN	rw	0	PGA1 stage gain selection
6:0	PGA3_GAIN[6:0]	rw	0000000	PGA3 stage gain selection

Table 69. C1ZAdcReg4 (0x0D)

Bit	Name	Mode	Reset	Description
7	reserved	r	0	Unused
6:0	PGA3_OFFSET[6:0]	rw	0000000	PGA3 stage offset selection

Table 70. C1ZAdcReg5 (0x0E)

Bit	Name	Mode	Reset	Description
7	reserved	r		
6	reserved	r		
5:1	AMUX[4:0]	rw	00000	Input channel configuration selector
0	VMUX	rw	0	Reference channel selector

Table 71. C1ZAdcReg6 (0x0F)

Bit	Name	Mode	Reset	Description
7	reserved	r		
6:4	FILTER TYPE [2:0]	r		Filter selection selection ◆ 000 - none ◆ 001 - average filtering ◆ 010 - moving average filtering ◆ 011 - reserved
3	ALRM1	rw		Alarm 1 enable
2	ALRM2	rw		Alarm 2 enable
1	SINGLE	rw		Configuration 1 in single acquisition mode
0	CONT	rw		Configuration 1 in continuous acquisition mode

Table 72. C1SXCfg (0x10)

Bit	Name	Mode	Reset	Description
7:0	SIZE	rw	00000000	Filter size. Limited to 10 for a moving average filter.

Table 73. C1FParam (0x11)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold MSB for configuration 1

Table 74. C1Alrm1OnMsb (0x12)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold LSB for configuration 1

Table 75. C1Alrm1OnLsb (0x13)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold MSB for configuration 1

Table 76. C1Alrm1OffMsb (0x14)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold LSB for configuration 1

Table 77. C1Alrm1OffLsb (0x15)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold MSB for configuration 1

Table 78. C1Alrm1OnMsb (0x16)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold LSB for configuration 1

Table 79. C1Alrm1OnLsb (0x17)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold MSB for configuration 1

Table 80 C1Alrm1OffMsb (0x18)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold LSB for configuration 1

Table 81. C1Alrm1OffLsb (0x19)

Bit	Name	Mode	Reset	Description
7:0		r	00000000	Configuration 1 data out MSB

Table 82. C1DataOutMsb (0x1A)

Bit	Name	Mode	Reset	Description
7:0		r	00000000	Configuration 1 data out LSB

Table 83. C1DataOutLsb (0x1B)

14.2.3. Configuration 2 registers

Bit	Name	Mode	Reset	Description
7	reserved	r	x	
6:5	SET_NELC	rw	01	Sets the number of elementary conversion to $2^{\mathbf{SET\_NELC[1:0]}}$. To compensate for offset the signal is chopped between elementary conversion.
4:2	SET_OSR	rw	010	Sets the ADC over-sampling rate of an elementary conversion to $2^{\mathbf{3+SET\_OSR[2:0]}}$.
1	reserved	r	x	
0	reserved	r	x	

Table 84. C2ZAdcReg1 (0x2A)

Bit	Name	Mode	Reset	Description
7:6	IB_AMP_ADC[1:0]	rw	11	Bias current selection of the A/D converter.
5:4	IB_AMP_PGA[1:0]	rw	11	Bias current selection of the PGA stages.
3:0	ENABLE[3:0]	rw	0000	Enables the different PGA stages and ADC. ◆ XXX1 - ADC enable ◆ XX1X - PGA3 enable ◆ X1XX - PGA2 enable ◆ 1XXX - PGA1 enable

Table 85. C2ZAdcReg2 (0x2B)

Bit	Name	Mode	Reset	Description
7:6	FIN[1:0]	rw	00	Sampling frequency selection
5:4	PGA2_GAIN[1:0]	rw	00	PGA2 stage gain selection
3:0	PGA2_OFFSET[3:0]	rw	0000	PGA2 stage offset selection

Table 86. C2ZAdcReg3 (0x2C)

Bit	Name	Mode	Reset	Description
7	PGA1_GAIN	rw	0	PGA1 stage gain selection
6:0	PGA3_GAIN[6:0]	rw	0000000	PGA3 stage gain selection

Table 87. C2ZAdcReg4 (0x2D)

Bit	Name	Mode	Reset	Description
7	reserved	r	0	Unused
6:0	PGA3_OFFSET[6:0]	rw	0000000	PGA3 stage offset selection

Table 88. C2ZAdcReg5 (0x2E)

Bit	Name	Mode	Reset	Description
7	reserved	r		
6	reserved	r		
5:1	AMUX[4:0]	rw	00000	Input channel configuration selector
0	VMUX	rw	0	Reference channel selector

Table 89. C2ZAdcReg6 (0x2F)

Bit	Name	Mode	Reset	Description
7	reserved	r		
6:4	FILTER TYPE [2:0]	r		Filter selection selection ◆ 000 - none ◆ 001 - average filtering ◆ 010 - moving average filtering ◆ 011 - reserved
3	ALRM1	rw		Alarm 1 enable
2	ALRM2	rw		Alarm 2 enable
1	SINGLE	rw		Configuration 1 in single acquisition mode
0	CONT	rw		Configuration 1 in continuous acquisition mode

Table 90. C2SXCfg (0x30)

Bit	Name	Mode	Reset	Description
7:0	SIZE	rw	00000000	Filter size. Limited to 10 for a moving average filter.

Table 91. C2FParam (0x31)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold MSB for configuration 2

Table 92. C2Alrm1OnMsb (0x32)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold LSB for configuration 2

Table 93. C2Alrm1OnLsb (0x33)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold MSB for configuration 2

Table 94 C2Alrm1OffMsb (0x34)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold LSB for configuration 2

Table 95. C2Alrm1OffLsb (0x35)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold MSB for configuration 2

Table 96. C2Alrm1OnMsb (0x36)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold LSB for configuration 2

Table 97. C2Alrm1OnLsb (0x37)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold MSB for configuration 2

Table 98 C2Alrm1OffMsb (0x38)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold LSB for configuration 2

Table 99. C2Alrm1OffLsb (0x39)

Bit	Name	Mode	Reset	Description
7:0		r	00000000	Configuration 2 data out MSB

Table 100. C2DataOutMsb (0x3A)

Bit	Name	Mode	Reset	Description
7:0		r	00000000	Configuration 2 data out LSB

Table 101. C2DataOutLsb (0x3B)

14.2.4. Configuration 3 registers

Bit	Name	Mode	Reset	Description
7	reserved	r	x	
6:5	SET_NELC	rw	01	Sets the number of elementary conversion to $2^{\mathbf{SET\_NELC[1:0]}}$. To compensate for offset the signal is chopped between elementary conversion.
4:2	SET_OSR	rw	010	Sets the ADC over-sampling rate of an elementary conversion to $2^{\mathbf{3+SET\_OSR[2:0]}}$.
1	reserved	r	x	
0	reserved	r	x	

Table 102. C3ZAdcReg1 (0x4A)

Bit	Name	Mode	Reset	Description
7:6	IB_AMP_ADC[1:0]	rw	11	Bias current selection of the A/D converter.
5:4	IB_AMP_PGA[1:0]	rw	11	Bias current selection of the PGA stages.
3:0	ENABLE[3:0]	rw	0000	Enables the different PGA stages and ADC. ◆ XXX1 - ADC enable ◆ XX1X - PGA3 enable ◆ X1XX - PGA2 enable ◆ 1XXX - PGA1 enable

Table 103. C3ZAdcReg2 (0x4B)

Bit	Name	Mode	Reset	Description
7:6	FIN[1:0]	rw	00	Sampling frequency selection
5:4	PGA2_GAIN[1:0]	rw	00	PGA2 stage gain selection
3:0	PGA2_OFFSET[3:0]	rw	0000	PGA2 stage offset selection

Table 104. C3ZAdcReg3 (0x4C)

Bit	Name	Mode	Reset	Description
7	PGA1_GAIN	rw	0	PGA1 stage gain selection
6:0	PGA3_GAIN[6:0]	rw	0000000	PGA3 stage gain selection

Table 105. C3ZAdcReg4 (0x4D)

Bit	Name	Mode	Reset	Description
7	reserved	r	0	Unused
6:0	PGA3_OFFSET[6:0]	rw	0000000	PGA3 stage offset selection

Table 106. C3ZAdcReg5 (0x4E)

Bit	Name	Mode	Reset	Description
7	reserved	r		
6	reserved	r		
5:1	AMUX[4:0]	rw	00000	Input channel configuration selector
0	VMUX	rw	0	Reference channel selector

Table 107. C3ZAdcReg6 (0x4F)

Bit	Name	Mode	Reset	Description
7	reserved	r		
6:4	FILTER TYPE [2:0]	r		Filter selection selection ◆ 000 - none ◆ 001 - average filtering ◆ 010 - moving average filtering ◆ 011 - reserved
3	ALRM1	rw		Alarm 1 enable
2	ALRM2	rw		Alarm 2 enable
1	SINGLE	rw		Configuration 3 in single acquisition mode
0	CONT	rw		Configuration 3 in continuous acquisition mode

Table 108. C3SXCfg (0x50)

Bit	Name	Mode	Reset	Description
7:0	SIZE	rw	00000000	Filter size. Limited to 10 for a moving average filter.

Table 109. C3FParam (0x51)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold MSB for configuration 3

Table 110. C3Alrm1OnMsb (0x52)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold LSB for configuration 3

Table 111. C3Alrm1OnLsb (0x53)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold MSB for configuration 3

Table 112 C3Alrm1OffMsb (0x54)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold LSB for configuration 3

Table 113. C3Alrm1OffLsb (0x55)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold MSB for configuration 3

Table 114. C3Alrm1OnMsb (0x56)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold LSB for configuration 3

Table 115. C3Alrm1OnLsb (0x57)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold MSB for configuration 3

Table 116 C3Alrm1OffMsb (0x58)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold LSB for configuration 3

Table 117. C3Alrm1OffLsb (0x59)

Bit	Name	Mode	Reset	Description
7:0		r	00000000	Configuration 3 data out MSB

Table 118. C3DataOutMsb (0x5A)

Bit	Name	Mode	Reset	Description
7:0		r	00000000	Configuration 3 data out LSB

Table 119. C3DataOutLsb (0x5B)

14.2.5. Configuration 4 registers

Bit	Name	Mode	Reset	Description
7	reserved	r	x	
6:5	SET_NELC	rw	01	Sets the number of elementary conversion to $2^{\mathbf{SET\_NELC[1:0]}}$. To compensate for offset the signal is chopped between elementary conversion.
4:2	SET_OSR	rw	010	Sets the ADC over-sampling rate of an elementary conversion to $2^{\mathbf{3+SET\_OSR[2:0]}}$.
1	reserved	r	x	
0	reserved	r	x	

Table 120. C4ZAdcReg1 (0x6A)

Bit	Name	Mode	Reset	Description
7:6	IB_AMP_ADC[1:0]	rw	11	Bias current selection of the A/D converter.
5:4	IB_AMP_PGA[1:0]	rw	11	Bias current selection of the PGA stages.
3:0	ENABLE[3:0]	rw	0000	Enables the different PGA stages and ADC. ◆ XXX1 - ADC enable ◆ XX1X - PGA3 enable ◆ X1XX - PGA2 enable ◆ 1XXX - PGA1 enable

Table 121. C4ZAdcReg2 (0x6B)

Bit	Name	Mode	Reset	Description
7:6	FIN[1:0]	rw	00	Sampling frequency selection
5:4	PGA2_GAIN[1:0]	rw	00	PGA2 stage gain selection
3:0	PGA2_OFFSET[3:0]	rw	0000	PGA2 stage offset selection

Table 122. C4ZAdcReg3 (0x6C)

Bit	Name	Mode	Reset	Description
7	PGA1_GAIN	rw	0	PGA1 stage gain selection
6:0	PGA3_GAIN[6:0]	rw	0000000	PGA3 stage gain selection

Table 123. C4ZAdcReg4 (0x6D)

Bit	Name	Mode	Reset	Description
7	reserved	r	0	Unused
6:0	PGA3_OFFSET[6:0]	rw	0000000	PGA3 stage offset selection

Table 124. C4ZAdcReg5 (0x6E)

Bit	Name	Mode	Reset	Description
7	reserved	r		
6	reserved	r		
5:1	AMUX[4:0]	rw	00000	Input channel configuration selector
0	VMUX	rw	0	Reference channel selector

Table 125. C4ZAdcReg6 (0x6F)

Bit	Name	Mode	Reset	Description
7	reserved	r		
6:4	FILTER TYPE [2:0]	r		Filter selection selection ◆ 000 - none ◆ 001 - average filtering ◆ 010 - moving average filtering ◆ 011 - reserved
3	ALRM1	rw		Alarm 1 enable
2	ALRM2	rw		Alarm 2 enable
1	SINGLE	rw		Configuration 4 in single acquisition mode
0	CONT	rw		Configuration 4 in continuous acquisition mode

Table 126. C4SXCfg (0x70)

Bit	Name	Mode	Reset	Description
7:0	SIZE	rw	00000000	Filter size. Limited to 10 for a moving average filter.

Table 127. C4FParam (0x71)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold MSB for configuration 4

Table 128. C4Alrm1OnMsb (0x72)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold LSB for configuration 4

Table 129. C4Alrm1OnLsb (0x73)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold MSB for configuration 4

Table 130 C4Alrm1OffMsb (0x74)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 1 threshold LSB for configuration 4

Table 131. C4Alrm1OffLsb (0x75)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold MSB for configuration 4

Table 132. C4Alrm1OnMsb (0x76)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold LSB for configuration 4

Table 133. C4Alrm1OnLsb (0x77)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold MSB for configuration 4

Table 134 C4Alrm1OffMsb (0x78)

Bit	Name	Mode	Reset	Description
7:0		rw	00000000	Alarm 2 threshold LSB for configuration 4

Table 135. C4Alrm1OffLsb (0x79)

Bit	Name	Mode	Reset	Description
7:0		r	00000000	Configuration 4 data out MSB

Table 136. C4DataOutMsb (0x7A)

Bit	Name	Mode	Reset	Description
7:0		r	00000000	Configuration 4 data out LSB

Table 137. C4DataOutLsb (0x7B)

15. Power modes

SX8722 has 3 operating modes:

- active mode
- sleep mode
- shutdown mode

15.1. Power modes transitions

Start-up from shutdown:

- Initializes the SX8722
- Load EEPROM if present
- Restores EEPROM configuration and set the SX8722

Start-up from sleep:

- Restores the RC active value
- Enables VLD
- Restores SX8722 configuration saved in RAM

Sleep sequence:

- Waits for I2C STOP sequence
- Stops the ADC
- Disable VLD
- Bias current off
- Set the clock to RC minimum value or to Xtal if present

Shutdown sequence:

- Waits for I2C STOP sequence
- Stops the ADC
- Disable VLD
- Bias current off
- Stops the SX8722

The timing of the transition states depends mainly on the Xtal presence, the EEPROM presence and if the transition is caused by an I2C command or by a pin signal (SLEEP, SHUT, RESET).

15.2. Active mode

In this chapter you will find:

The description of the active mode

How to set SX8722 in active mode

15.2.1. Description

In active mode, SX8722 and all its peripherals can work and execute the measurement engine. The acquisition chain, the alarms and the signal post processing can be activated and parameterized.

15.2.2. How to set SX8722 in active mode

Start-up

- At start-up SX8722 is automatically set in active mode.
- If there is no EEPROM configuration loaded at start-up, PGA are not active.

From Sleep mode

- Positive pulse on RESET pin
- Negative pulse on the SLEEP pin
- SLEEP bit toggle in the SXCtrl1 register (I2C write mask command)
- Other interruption

From Shutdown mode

- Positive pulse on RESET pin
- Power-on-reset (negative pulse on VBAT pin)

15.3. Sleep mode

15.3.1. Description

The sleep mode is a low power mode. It can be called by an I2C sequence or by sending a negative pulse to SX8722 SLEEP pin.

15.3.2. Operating specifications of the sleep mode

Summary

- SX8722 configuration saved in RAM
- ADC stopped
- VLD stopped (voltage level detector)
- If Xtal present, clock set to Xtal 32k
- If Xtal not present, clock set to RC minimum value (~80kHz)
- Bias current off

- Program HALT, SX8722 needs an interrupt to wake up (I2C communication, SLEEP pin signal, reset, etc).

15.3.3. SX8722 sleep current consumption below 3V Vbat

Below 3 Volts SX8722 enables the internal voltage multiplier to power the ZoomingADC™. This internal voltage multiplier is automatically enabled when the power supply goes below 3V Vbat.

This voltage multiplier increases SX8722 consumption. This is why the chip consumption in sleep mode with 2.5V supply is higher than with 5.5V supply.

There is a possibility to consume less current when the Vbat voltage is lower than 3V: the SLEEP signal has to be sent to the SLEEP pin when Vbat is higher than 3V, and then decrease the Vbat value. In this case, the voltage multiplier is not activated.

15.3.4. SX8722 sleep current consumption with the 32.768 kHz Xtal

The sleep mode current consumption with the presence of the 32.768 kHz Xtal is around 1µA if the supply voltage is above 3V. Below 3V, the current consumption is around 4 µA because the VMULT is enabled.

In addition to set the precise RC frequency, the presence of an external 32.768 kHz Xtal allows SX8722 sleep current consumption 3x lower than without the Xtal.

In this case SX8722 main clock is generated by the Xtal.

15.3.5. SX8722 sleep current consumption without the 32.768 KHz Xtal

The current consumption in sleep mode without the 32.768 kHz Xtal is around 3 µA if the supply voltage is above 3V. Below 3V, the current consumption is around 9 µA because the voltage multiplier is enabled. The RC min frequency is set and its value is around 80 kHz.

15.3.6. How to set SX8722 in sleep mode

I2C sleep

Through the I2C interface, send a write mask command at address 00 and toggle the SLEEP bit of the SXCtrl1 register.

When SX8722 is in sleep mode, send a write mask command at address 00 and toggle the SLEEP bit to restore SX8722 active mode.

WARNING: The I2C SLEEP command does not allow reaching as low current consumption as the SLEEP pin command or writing the SXCtrl1 register SLEEP bit. The sleep mode called by I2C SLEEP command (0x40) has a current consumption around 80µA.

SLEEP pin

Put the SLEEP input signal to VSS, the SLEEP input is active on negative edge.

Is the SX8722 in SLEEP mode?

There are pulses on the READY pin in active mode every 36ms. In sleep mode there is no pulse on the READY pin.

15.3.7. Wake up from sleep mode to active mode

In sleep mode the internal program is in "HALT" assembler equivalent mode. The SLEEP bit toggling in SXCtrl1 or a signal on the SLEEP pin can wake up the SX8722.

See active mode section for more information.

15.4. Shutdown mode

15.4.1. Description

This is a very low-power mode because all circuit clocks and all peripherals are stopped. Only some service blocks remain active.

15.4.2. Operating specifications in shutdown mode

Summary

- ADC stopped
- VLD stopped
- If Xtal present, clock set to Xtal 32k
- If Xtal not present, clock set to RC minimum value (~80kHz)
- Bias current off
- Program HALT, interrupt off
- No possible I2C communication

Internal voltage multiplier

Like in sleep mode, internal voltage multiplier is automatically enabled when the power supply goes below 3 Volts but the internal voltage multiplier requires an external capacitor between VMULT pin and Vss, the value of this capacitor must be between 1 and 3nF.

Shutdown mode current consumption

The current consumption in shutdown mode is around 0.5 µA if the supply voltage is above 3V. Below 3V, the current consumption is around 3.5 µA because the voltage multiplier is enabled.

How to set shutdown mode consumption around 0.5µA

By default, with a supply voltage below 3V the shutdown mode current is around 3.5µA. To obtain 0.5µA consumption, the shut command (I2C, pin) has to be received by the SX8722 when the internal voltage multiplier is not enabled. It means when the supply voltage is above 3V.

Then, if the supply voltage is lowered under 3V, the SX8722 will conserve the 0.5µA consumption.

15.4.3. How to set SX8722 in shutdown mode

I2C Shutdown command

Send the 0x50 command through the I2C interface.

I2C SHUT bit toggle

Through the I2C interface, send a write mask command at address 00 and toggle the SHUT bit of the SXCtrl1 register.

SHUT pin

Put the SHUT input signal to VSS, the SHUT input is active on negative edge.

15.4.4. Wake-up from shutdown mode to active mode

There are two possible ways to wake-up from the shutdown mode:

- The POR (power-on-reset caused by a power-down followed by power-on).
- The RESET pin.

In both case the RAM information is lost. SX8722 configuration must be restored from the EEPROM saved configuration.

15.4.5. Change from shutdown mode to sleep mode

This is not possible.

16. PCB Layout Considerations

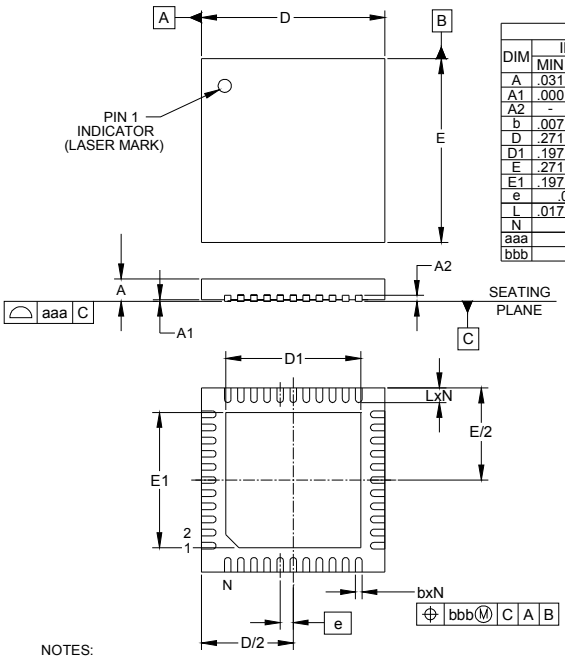
PCB layout considerations to be taken when using the SX8722 are relatively simple to get the highest performances out. The most important to achieve good performances is to have a good voltage reference.

Separating the digital from the analog lines will be also a good choice to reduce the noise induced by the digital lines. It is also advised to have separated ground planes for digital and analog signals with the shortest return path, as well as making the power supply lines as wider as possible and to have good decoupling capacitors.

17. How to Evaluate

For evaluation purposes the XE8000EV120 evaluation kit can be ordered. This kit connects to any PC using a USB port. The "SX8722 Evaluation Tools" software gives the user the ability to control the SX8722 and displaying configurations on the "Graphical User interface". For more information please look at SEMTECH web site (http://www.semtech.com).

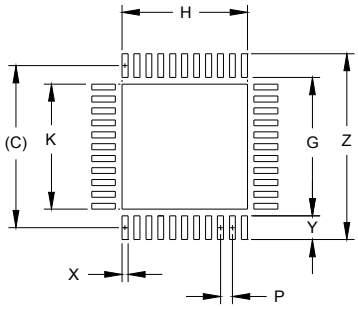
18. Package Outline Drawing: MLPQ44-7x7mm



DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.040	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.271	.275	.279	6.90	7.00	7.10
D1	.197	.203	.207	5.00	5.15	5.25
E	.271	.275	.279	6.90	7.00	7.10
E1	.197	.203	.207	5.00	5.15	5.25
e	.020 BSC			0.50 BSC		
L	.017	.021	.025	0.45	0.55	0.65
N	44			44		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

19. Land Pattern Drawing: MLPQ44-7x7mm



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.268)	(6.80)
G	.228	5.80
H	.207	5.25
K	.207	5.25
P	.021	0.50
X	.011	0.30
Y	.039	1.00
Z	.307	7.80

NOTES:

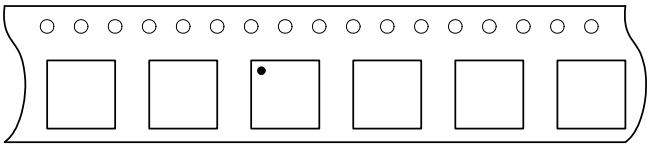
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

20. Tape and Reel Specification

MLP/QFN (0.70mm - 1.00mm package thickness)

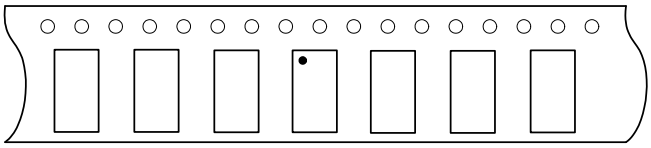
- Single Sprocket holes
- Tolerances for Ao & Bo are +/- 0.20mm
- Tolerances for Ko is +/- 0.10mm
- Tolerance for Pocket Pitch is +/- 0.10mm
- Tolerance for Tape width is +/-0.30mm
- Trailer and Leader Length are minimum required length
- Package Orientation and Feed Direction

MLP (square)

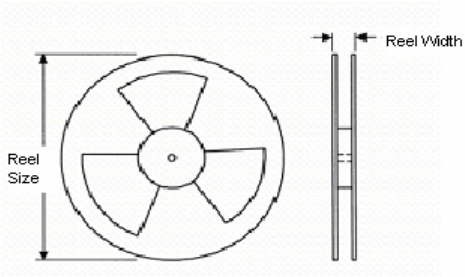


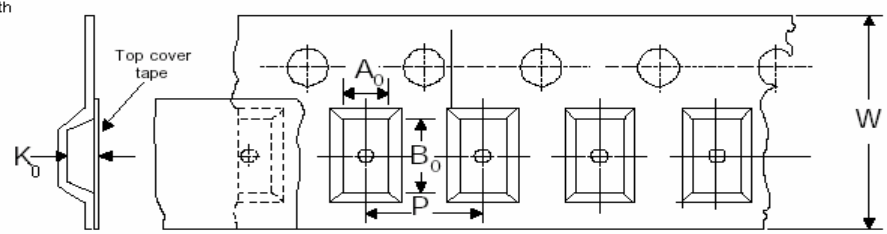
Direction of Feed

MLP (rectangular)



Direction of Feed





User Direction of Feed

Pkg size	carrier tape (mm)					Reel				
	Tape Width (W)	Pocket Pitch (P)	Ao	Bo	Ko	Reel Size (in)	Reel Width (mm)	Trailer Length (mm)	Leader Length (mm)	QTY per Reel
2x2	8	4	2.25	2.25	1.00	7	8.4	160	400	3000
3x3	12	8	3.30	3.30	1.10	13	12.4	400	400	3000
4x4	12	8	4.35	4.35	1.10	13	12.4	400	400	3000
4x3	12	8	3.30	4.30	1.10	13	12.4	400	400	3000
5x5	12	8	5.25	5.25	1.10	7/13	12.4	200/400	400	500/3000
6x6	16	12	6.30	6.30	1.10	13	16.4	400	400	3000
6x5	12	8	5.30	6.30	1.10	13	12.4	400	400	3000
7x7	16	12	7.30	7.30	1.10	13	16.4	400	400	3000
9X9	16	12	9.30	9.30	1.10	13	16.4	400	400	3000
10x10	24	16	10.30	10.30	1.10	13	24.4	400	400	3000
11x11	24	16	11.40	11.40	1.20	13	24.4	400	400	3000

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