

FEATURES

- 14-Bit 30 MSPS A/D Converter
- 30 MSPS Correlated Double Sampler (CDS)
- 4 dB \pm 6 dB 6-Bit Pixel Gain Amplifier (PxGA®)
- 2 dB to 36 dB 10-Bit Variable Gain Amplifier (VGA)
- Low Noise Clamp Circuits
- Analog Preblanking Function
- Auxiliary Inputs with VGA and Input Clamp
- 3-Wire Serial Digital Interface
- 3 V Single-Supply Operation
- Low Power: 153 mW @ 3 V Supply
- Space-Saving 48-Lead LFCSP Package

APPLICATIONS

- High Performance Digital Still Cameras
- Industrial/Scientific Imaging

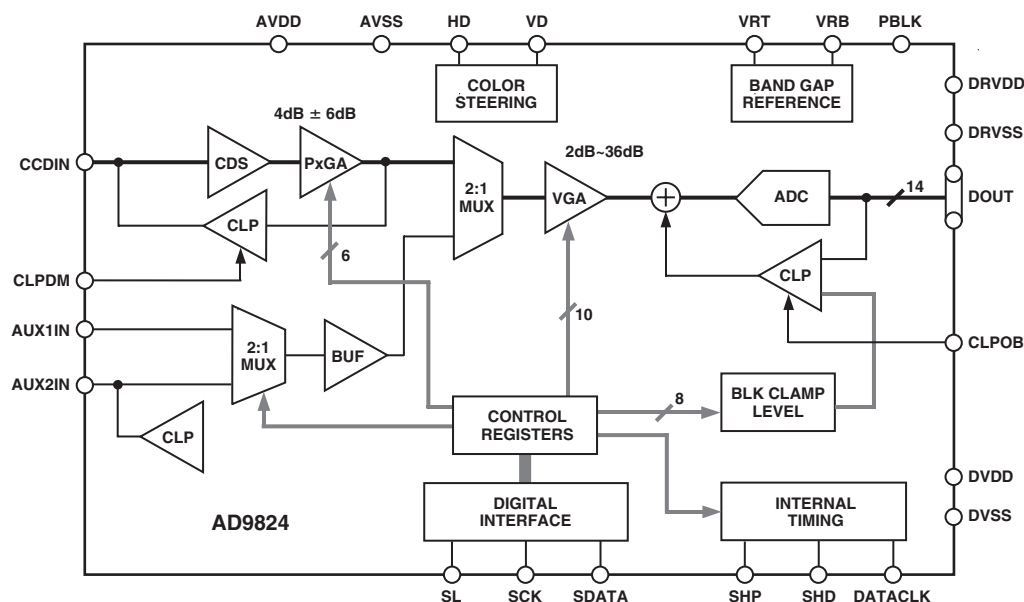
PRODUCT DESCRIPTION

The AD9824 is a complete analog signal processor for CCD applications. It features a 30 MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The AD9824's signal chain consists of an input clamp, a correlated double sampler (CDS), PxGA, a digitally controlled VGA, a black level clamp, and a 14-bit A/D converter. Additional input modes are also provided for processing analog video signals.

The internal registers are programmed through a 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, input configuration, and power-down modes.

The AD9824 operates from a single 3 V power supply, typically dissipates 153 mW, and is packaged in a 48-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM



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AD9824—SPECIFICATIONS

GENERAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = 3.0 V, f_{DATA CLK} = 30 MHz, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit |
|---------------------------------|--|-----------------|------|-----------------|
| TEMPERATURE RANGE | | | | |
| Operating | -20 | | +85 | °C |
| Storage | -65 | | +150 | °C |
| POWER SUPPLY VOLTAGE | | | | |
| Analog, Digital, Digital Driver | 2.7 | | 3.6 | V |
| POWER CONSUMPTION | | | | |
| Normal Operation | (Specified Under Each Mode of Operation) | | | |
| Power-Down Modes | | | | |
| Standby | | 5 | | mW |
| Total Power-Down | | 0.5 | | mW |
| MAXIMUM CLOCK RATE | 30 | | | MHz |
| A/D CONVERTER | | | | |
| Resolution | 14 | | | Bits |
| Differential Nonlinearity (DNL) | | ±0.5 | ±1.0 | LSB |
| No Missing Codes | 14 | | | Bits Guaranteed |
| Full-Scale Input Voltage | | 2.0 | | V |
| Data Output Coding | | Straight Binary | | |
| VOLTAGE REFERENCE | | | | |
| Reference Top Voltage (VRT) | | 2.0 | | V |
| Reference Bottom Voltage (VRB) | | 1.0 | | V |

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (DRVDD = 2.7 V, C_L = 20 pF, unless otherwise noted.)

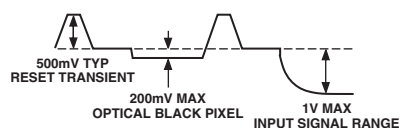
| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-----------------|-----|-----|-----|------|
| LOGIC INPUTS | | | | | |
| High Level Input Voltage | V _{IH} | 2.1 | | | V |
| Low Level Input Voltage | V _{IL} | | | 0.6 | V |
| High Level Input Current | I _{IH} | | 10 | | μA |
| Low Level Input Current | I _{IL} | | 10 | | μA |
| Input Capacitance | C _{IN} | | 10 | | pF |
| LOGIC OUTPUTS | | | | | |
| High Level Output Voltage, I _{OH} = 2 mA | V _{OH} | 2.2 | | | V |
| Low Level Output Voltage, I _{OL} = 2 mA | V _{OL} | | | 0.5 | V |

Specifications subject to change without notice.

CCD-MODE SPECIFICATIONS (T_{MIN} to T_{MAX} , $AVDD = DVDD = 3.0 \text{ V}$, $f_{\text{DATACLK}} = f_{\text{SHP}} = f_{\text{SHD}} = 30 \text{ MHz}$, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Notes |
|--|------|------------|------|---------|--|
| POWER CONSUMPTION | | 153 | | mW | See TPC 1 for Power Curves |
| MAXIMUM CLOCK RATE | 30 | | | MHz | |
| CDS | | | | | |
| Gain | | 0 | | dB | |
| Allowable CCD Reset Transient ¹ | | 500 | | mV | See Input Waveform in Footnote 1 |
| Max Input Range Before Saturation ¹ | 1.0 | | | V p-p | $PxGA$ Gain at 4 dB |
| Max CCD Black Pixel Amplitude ¹ | | 200 | | mV | |
| PIXEL GAIN AMPLIFIER ($PxGA$) | | | | | |
| Max Input Range | 1.0 | | | V p-p | |
| Max Output Range | 1.6 | | | V p-p | |
| Gain Control Resolution | | 64 | | Steps | |
| Gain Monotonicity | | Guaranteed | | | |
| Gain Range (Two's Complement Coding) | | | | | See Figure 28 for $PxGA$ Gain Curve |
| Min Gain ($PxGA$ Gain Code 32) | | -2.5 | | dB | |
| Max Gain ($PxGA$ Gain Code 31) | | 9.5 | | dB | |
| VARIABLE GAIN AMPLIFIER (VGA) | | | | | |
| Max Input Range | 1.6 | | | V p-p | |
| Max Output Range | 2.0 | | | V p-p | |
| Gain Control Resolution | | 1024 | | Steps | |
| Gain Monotonicity | | Guaranteed | | | |
| Gain Range | | | | | See Figure 29 for VGA Gain Curve |
| Low Gain (VGA Gain Code 77) | | 2 | | dB | |
| Max Gain (VGA Gain Code 1023) | | 36 | | dB | |
| BLACK LEVEL CLAMP | | | | | |
| Clamp Level Resolution | | 256 | | Steps | Measured at ADC Output |
| Clamp Level | | | | | |
| Min Clamp Level | | 0 | | LSB | |
| Max Clamp Level | | 1020 | | LSB | |
| SYSTEM PERFORMANCE | | | | | Specifications Include Entire Signal Chain Gain = $(0.0353 \times \text{Code}) + 3.3$ |
| Gain Accuracy ² | | | | | |
| Low Gain (VGA Code 77) | 5.5 | 6 | 6.5 | dB | |
| Max Gain (VGA Code 1023) | 38.2 | 39.4 | 40.2 | dB | |
| Peak Nonlinearity, 500 mV Input Signal | | 0.1 | | % | 12 dB Gain Applied |
| Total Output Noise | | 2.0 | | LSB rms | AC Grounded Input, 6 dB Gain Applied |
| Power Supply Rejection (PSR) | | 40 | | dB | Measured with Step Change on Supply |
| POWER-UP RECOVERY TIME | | | | | Normal Clock Signals Applied |
| Reference Standby Mode | | 1 | | ms | |
| Total Shutdown Mode | | 3 | | ms | |
| Power-Off Condition | | 15 | | ms | |

NOTES

¹Input signal characteristics defined as follows:

² $PxGA$ gain fixed at Code 63 (3.3 dB).

Specifications subject to change without notice.

AD9824—SPECIFICATIONS

AUX1-MODE SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = 3.0 V, f_{DATACLK} = 30 MHz, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit |
|---|-----|------|-----|-------|
| POWER CONSUMPTION | | 120 | | mW |
| MAXIMUM CLOCK RATE | 30 | | | MHz |
| INPUT BUFFER | | | | |
| Gain | | 0 | | dB |
| Max Input Range | 1.0 | | | V p-p |
| VGA | | | | |
| Max Output Range | 2.0 | | | V p-p |
| Gain Control Resolution | | 1023 | | Steps |
| Gain (Selected Using VGA Gain Register) | | | | |
| Min Gain | | 0 | | dB |
| Max Gain | | 36 | | dB |

Specifications subject to change without notice.

AUX2-MODE SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = 3.0 V, f_{DATACLK} = 30 MHz, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit |
|---|---------------------|------|-----|-------|
| POWER CONSUMPTION | | 120 | | mW |
| MAXIMUM CLOCK RATE | 30 | | | MHz |
| INPUT BUFFER | (Same as AUX1-MODE) | | | |
| VGA | | | | |
| Max Output Range | 2.0 | | | V p-p |
| Gain Control Resolution | | 512 | | Steps |
| Gain (Selected Using VGA Gain Register) | | | | |
| Min Gain | | 0 | | dB |
| Max Gain | | 18 | | dB |
| ACTIVE CLAMP | | | | |
| Clamp Level Resolution | | 256 | | Steps |
| Clamp Level (Measured at ADC Output) | | | | |
| Min Clamp Level | | 0 | | LSB |
| Max Clamp Level | | 1020 | | LSB |

Specifications subject to change without notice.

TIMING SPECIFICATIONS ($C_L = 20$ pF, $f_{SAMP} = 30$ MHz, CCD-Mode Timing in Figures 5 and 6, AUX-Mode Timing in Figure 7, Serial Timing in Figures 21–24.)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------------------|------------|-----|------|-----|--------|
| SAMPLE CLOCKS | | | | | |
| DATACLK, SHP, SHD Clock Period | t_{CP} | 33 | 33 | | ns |
| DATACLK High/Low Pulsewidth | t_{ADC} | 13 | 16.7 | | ns |
| SHP Pulsewidth | t_{SHP} | 5 | 8.3 | | ns |
| SHD Pulsewidth | t_{SHD} | 5 | 8.3 | | ns |
| CLPDM Pulsewidth | t_{CDM} | 4 | 10 | | Pixels |
| CLPOB Pulsewidth* | t_{COB} | 2 | 20 | | Pixels |
| SHP Rising Edge to SHD Falling Edge | t_{S1} | 0 | 8.3 | | ns |
| SHP Rising Edge to SHD Rising Edge | t_{S2} | 15 | 16.7 | | ns |
| Internal Clock Delay | t_{ID} | | 3.0 | | ns |
| Inhibited Clock Period | t_{INH} | 10 | | | ns |
| DATA OUTPUTS | | | | | |
| Output Delay | t_{OD} | | 13 | 16 | ns |
| Output Hold Time | t_H | 7.0 | 7.6 | | ns |
| Pipeline Delay | | | 9 | | Cycles |
| SERIAL INTERFACE | | | | | |
| Maximum SCK Frequency | f_{SCLK} | 10 | | | MHz |
| SL to SCK Setup Time | t_{LS} | 10 | | | ns |
| SCK to SL Hold Time | t_{LH} | 10 | | | ns |
| SDATA Valid to SCK Rising Edge Setup | t_{DS} | 10 | | | ns |
| SCK Falling Edge to SDATA Valid Hold | t_{DH} | 10 | | | ns |
| SCK Falling Edge to SDATA Valid Read | t_{DV} | 10 | | | ns |

*Minimum CLPOB pulsewidth is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp performance. Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

| Parameter | With Respect To | Min Max | | Unit |
|---------------------------|-----------------|---------|-------------|------|
| | | Min | Max | |
| AVDD1, AVDD2 | AVSS | -0.3 | +3.9 | V |
| DVDD1, DVDD2 | DVSS | -0.3 | +3.9 | V |
| DRVDD | DRVSS | -0.3 | +3.9 | V |
| Digital Outputs | DRVSS | -0.3 | DRVDD + 0.3 | V |
| SHP, SHD, DATACLK | DVSS | -0.3 | DVDD + 0.3 | V |
| CLPOB, CLPDM, PBLK | DVSS | -0.3 | DVDD + 0.3 | V |
| SCK, SL, SDATA | DVSS | -0.3 | DVDD + 0.3 | V |
| VRT, VRB, CMLEVEL | AVSS | -0.3 | AVDD + 0.3 | V |
| BYP1-3, CCDIN | AVSS | -0.3 | AVDD + 0.3 | V |
| Junction Temperature | | | 150 | °C |
| Lead Temperature (10 sec) | | | 300 | °C |

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|-----------|-------------------|---------------------|----------------|
| AD9824KCP | -20°C to +85°C | LFCSP | CP-48 |

THERMAL CHARACTERISTICS

Thermal Resistance

48-Lead LFCSP Package

$$\theta_{JA} = 26^\circ\text{C/W}^*$$

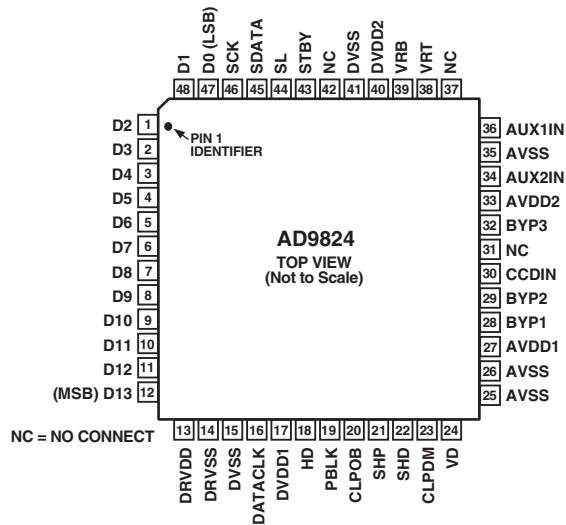
* θ_{JA} is measured using a 4-layer PCB with the exposed paddle soldered to the board.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9824 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTIONS

| Pin Number | Name | Type | Description |
|------------|---------|------|--|
| 1–12 | D2–D13 | DO | Digital Data Outputs. Pin 12 (D13) is MSB. |
| 13 | DRVDD | P | Digital Output Driver Supply |
| 14 | DRVSS | P | Digital Output Driver Ground |
| 15, 41 | DVSS | P | Digital Ground |
| 16 | DATACLK | DI | Digital Data Output Latch Clock |
| 17 | DVDD1 | P | Digital Supply 1 |
| 18 | HD | DI | Horizontal Drive. Used with VD for color steering control. |
| 19 | PBLK | DI | Preblanking Clock Input |
| 20 | CLPOB | DI | Black Level Clamp Clock Input |
| 21 | SHP | DI | CDS Sampling Clock for CCD's Reference Level |
| 22 | SHD | DI | CDS Sampling Clock for CCD's Data Level |
| 23 | CLPDM | DI | Input Clamp Clock Input |
| 24 | VD | DI | Vertical Drive. Used with HD for color steering control. |
| 25, 26, 35 | AVSS | P | Analog Ground |
| 27 | AVDD1 | P | Analog Supply 1 |
| 28 | BYP1 | AO | Internal Bias Level Decoupling |
| 29 | BYP2 | AO | Internal Bias Level Decoupling |
| 30 | CCDIN | AI | Analog Input for CCD Signal |
| 31 | NC | NC | Internally Not Connected |
| 32 | BYP3 | AO | Internal Bias Level Decoupling |
| 33 | AVDD2 | P | Analog Supply 2 |
| 34 | AUX2IN | AI | Analog Input |
| 36 | AUX1IN | AI | Analog Input |
| 37 | NC | NC | Internally Not Connected |
| 38 | VRT | AO | A/D Converter Top Reference Voltage Decoupling |
| 39 | VRB | AO | A/D Converter Bottom Reference Voltage Decoupling |
| 40 | DVDD2 | P | Digital Supply 2 |
| 42 | NC | NC | Internally Not Connected |
| 43 | STBY | DI | Standby Mode, Active High. Same as total power-down mode. |
| 44 | SL | DI | Serial Digital Interface Load Pulse |
| 45 | SDATA | DI | Serial Digital Interface Data |
| 46 | SCK | DI | Serial Digital Interface Clock |
| 47, 48 | D0–D1 | DI | Digital Data Outputs. Pin 47 (D0) is LSB. |

TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power

DEFINITIONS OF SPECIFICATIONS

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus, every code must have a finite width. No missing codes guaranteed to 14-bit resolution indicates that all 16,384 codes, respectively, must be present over all operating conditions.

Peak Nonlinearity

Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9824 from a true straight line. The point used as “zero scale” occurs 1/2 LSB before the first code transition. “Positive full scale” is defined as a Level 1, 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC’s full-scale range.

Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal

chain at the specified gain setting. The output noise can be converted to an equivalent voltage using the relationship $1 \text{ LSB} = (\text{ADC Full Scale}/2^N \text{ codes})$ where N is the bit resolution of the ADC. For the AD9824, 1 LSB is 125 μV .

Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. This represents a high frequency disturbance on the AD9824’s power supply. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

Internal Delay for SHP/SHD

The internal delay (also called aperture delay) is the time delay that occurs from when a sampling edge is applied to the AD9824 until the actual sample of the input signal is held. Both SHP and SHD sample the input signal during the transition from low to high, so the internal delay is measured from each clock’s rising edge to the instant the actual internal sample is taken.

EQUIVALENT INPUT CIRCUITS

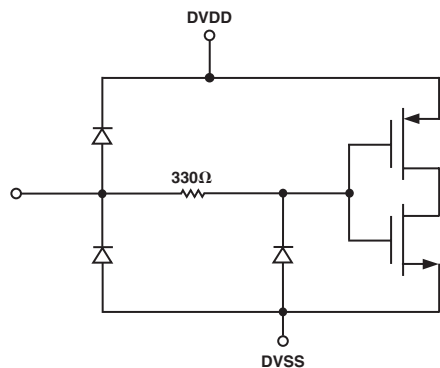


Figure 1. Digital Inputs—SHP, SHD, DATACLK, CLPOB, CLPDM, HD, VD, PBLK, SCK, and SL

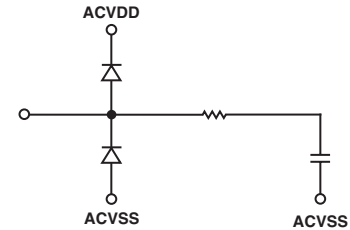


Figure 3. CCDIN (Pin 30)

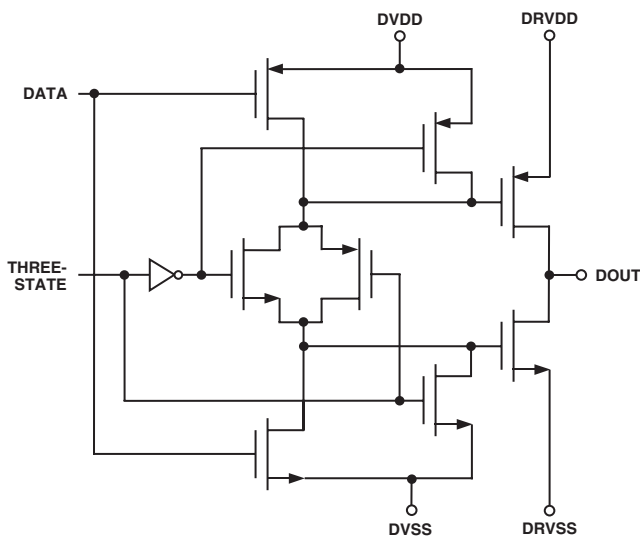


Figure 2. Data Outputs—D0–D13

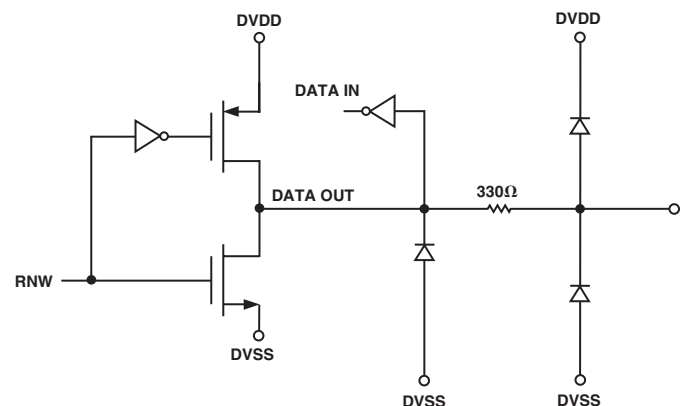
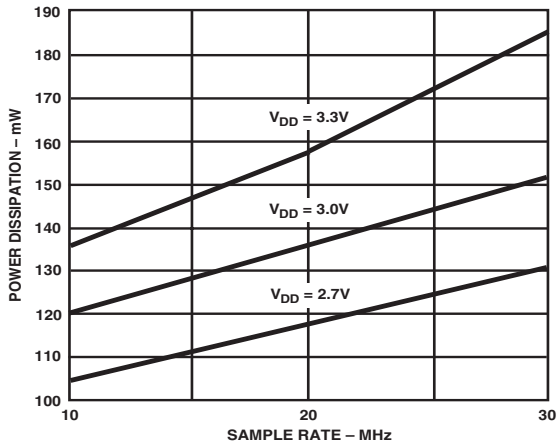
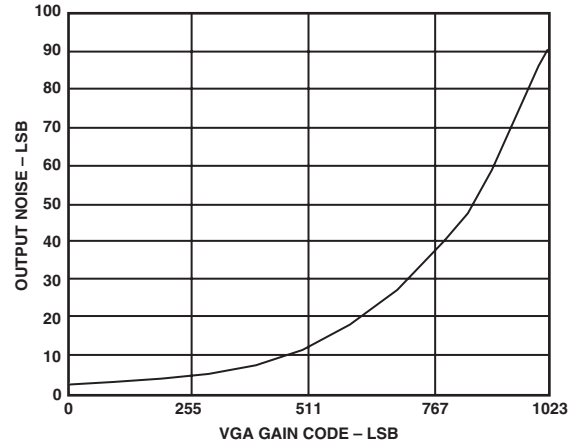


Figure 4. SDATA (Pin 45)

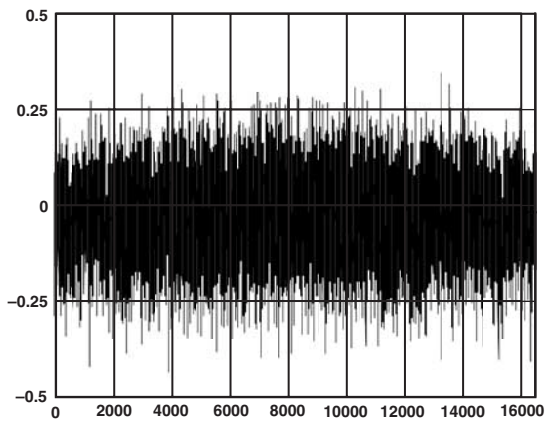
AD9824—Typical Performance Characteristics



TPC 1. Power vs. Sample Rate

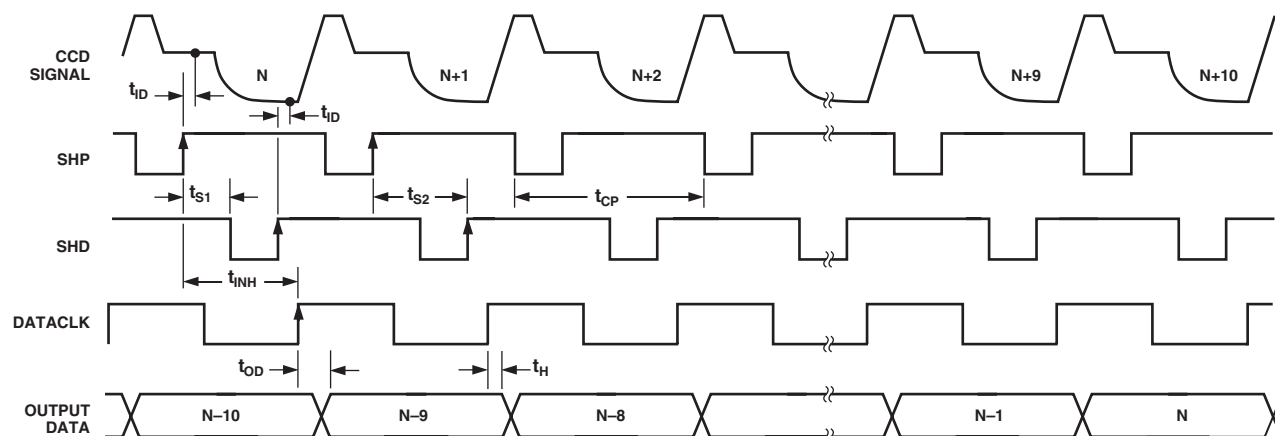


TPC 3. Output Noise vs. VGA Gain



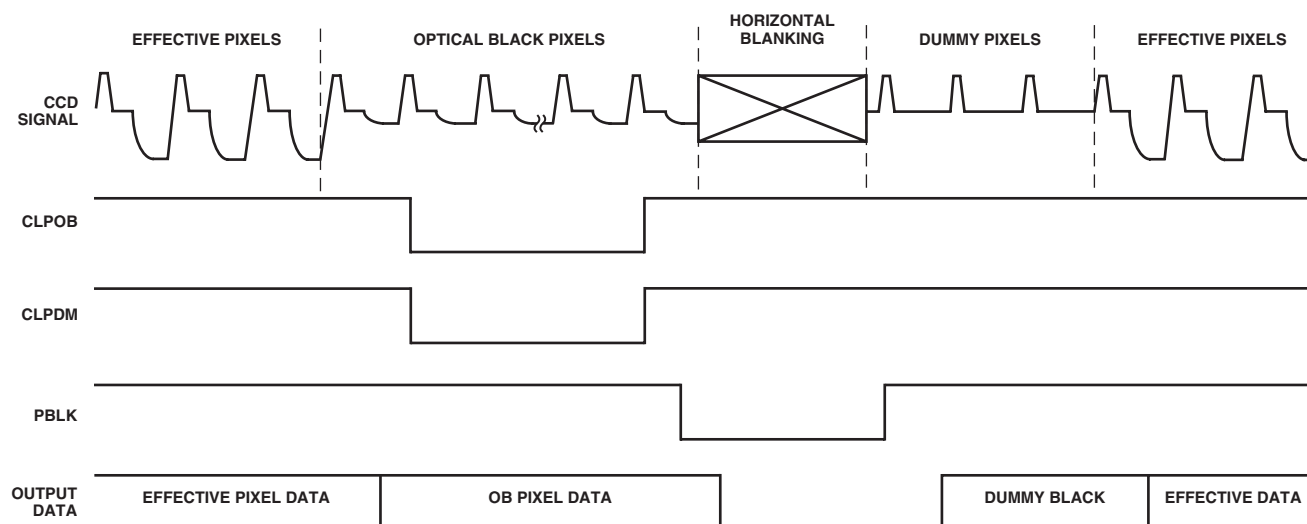
TPC 2. Typical DNL Performance

CCD MODE AND AUX MODE TIMING



- NOTES
 1. RECOMMENDED PLACEMENT FOR DATACLK RISING EDGE IS BETWEEN THE SHD RISING EDGE AND NEXT SHP FALLING EDGE.
 2. CCD SIGNAL IS SAMPLED AT SHP AND SHD RISING EDGES.

Figure 5. CCD Mode Timing



- NOTES
 1. CLPOB AND CLPDM WILL OVERWRITE PBLK. PBLK WILL NOT AFFECT CLAMP OPERATION IF OVERLAPPING CLPDM AND/OR CLPOB.
 2. PBLK SIGNAL IS OPTIONAL.
 3. DIGITAL OUTPUT DATA WILL BE ALL ZEROS DURING PBLK. OUTPUT DATA LATENCY IS 9 DATACLK CYCLES.

Figure 6. Typical CCD Mode Line Clamp Timing

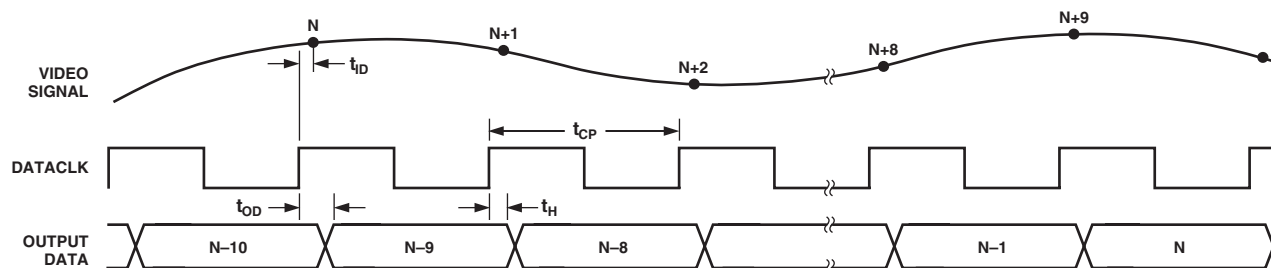


Figure 7. AUX Mode Timing

AD9824

PIXEL GAIN AMPLIFIER (PxGA) TIMING

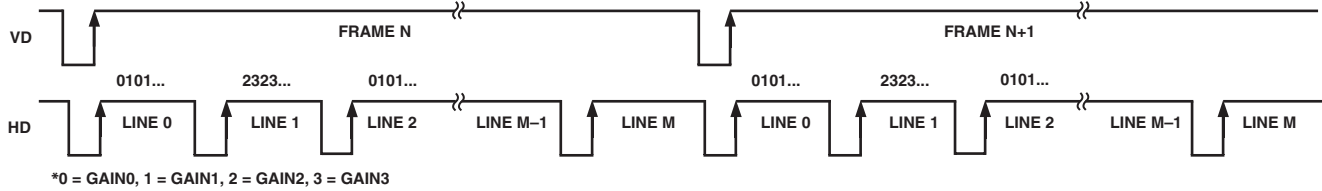
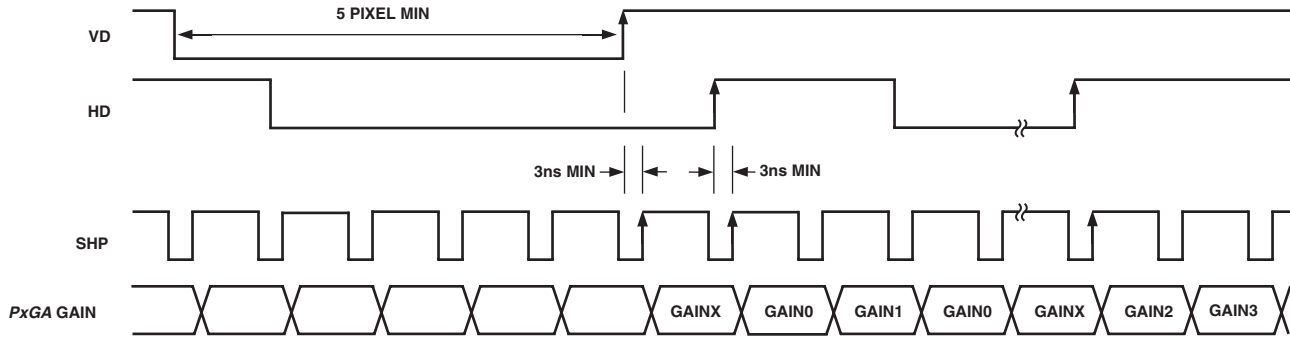


Figure 8. PxGA Mode 1 (Mosaic Separate) Frame/Line Gain Register Sequence



NOTES

1. MINIMUM PULSEWIDTH FOR HD AND VD IS 5 PIXEL CYCLES.
2. BOTH VD AND HD ARE INTERNALLY UPDATED AT SHP RISING EDGES. MINIMUM SETUP TIME IS 3 ns.
3. EVERY HD RISING EDGE WITH A PREVIOUS VD RISING EDGE WILL RESET TO 0101.
4. EVERY HD RISING EDGE WITHOUT A PREVIOUS VD RISING EDGE WILL ALTERNATE BETWEEN 0101... AND 2323.

Figure 9. PxGA Mode 1 (Mosaic Separate) Detailed Timing

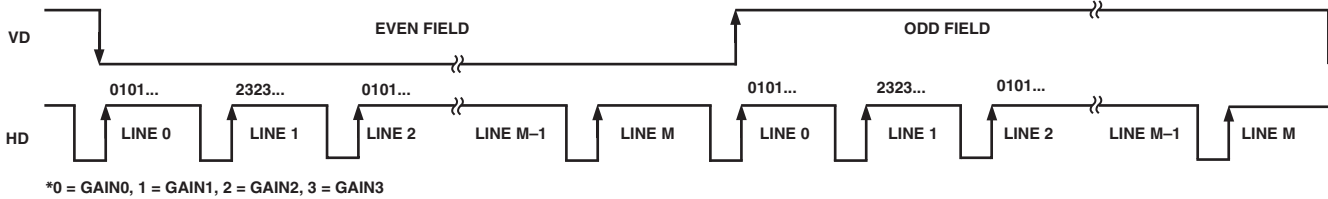
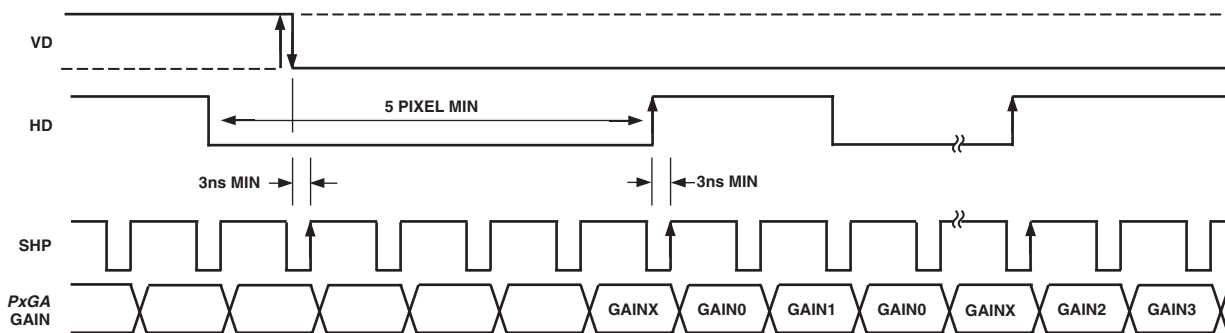


Figure 10. PxGA Mode 2 (Interlace) Frame/Line Gain Register Sequence



NOTES

1. BOTH VD AND HD ARE INTERNALLY UPDATED AT SHP RISING EDGES.
2. EVERY HD RISING EDGE WITH A PREVIOUS VD RISING OR FALLING EDGE WILL RESET TO 0101.
3. EVERY HD RISING EDGE WITHOUT A PREVIOUS VD RISING EDGE WILL ALTERNATE BETWEEN 0101... AND 2323.

Figure 11. PxGA Mode 2 (Interlace) Detailed Timing

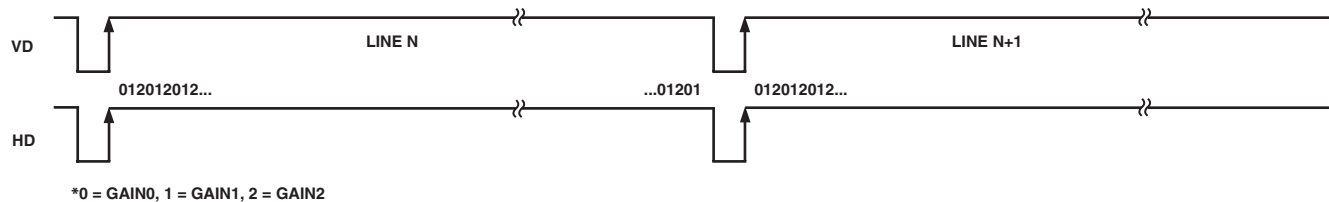


Figure 12. PxGA Mode 3 (3-Color) Frame/Line Gain Register Sequence

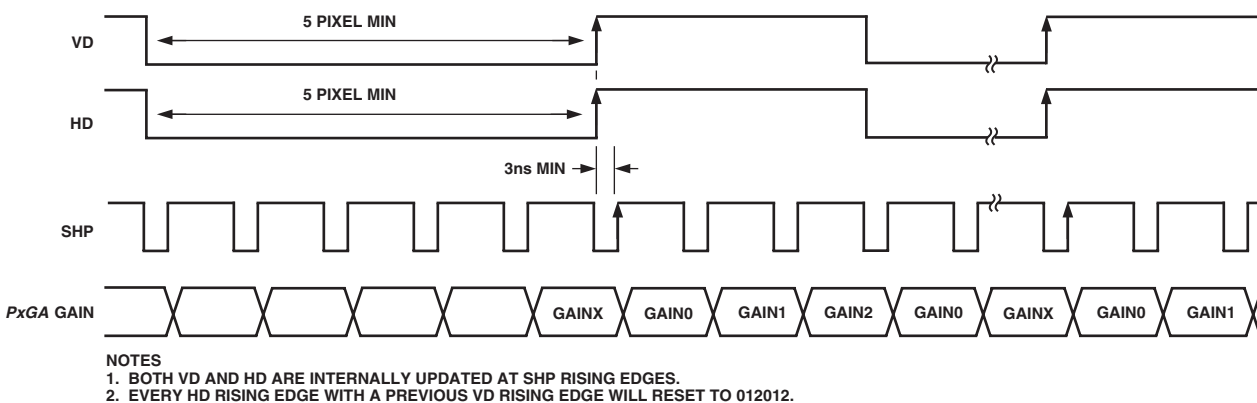


Figure 13. PxGA Mode 3 (3-Color) Detailed Timing

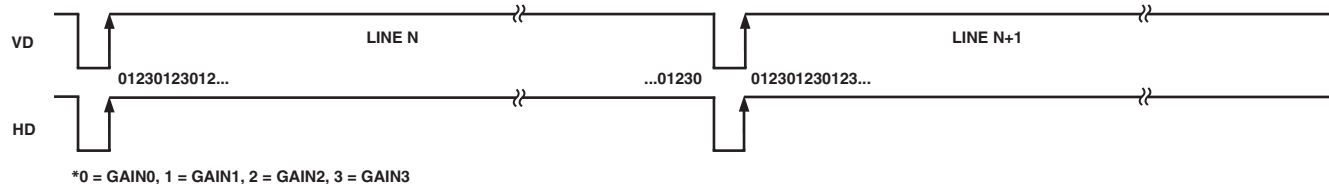


Figure 14. PxGA Mode 4 (4-Color) Frame/Line Gain Register Sequence

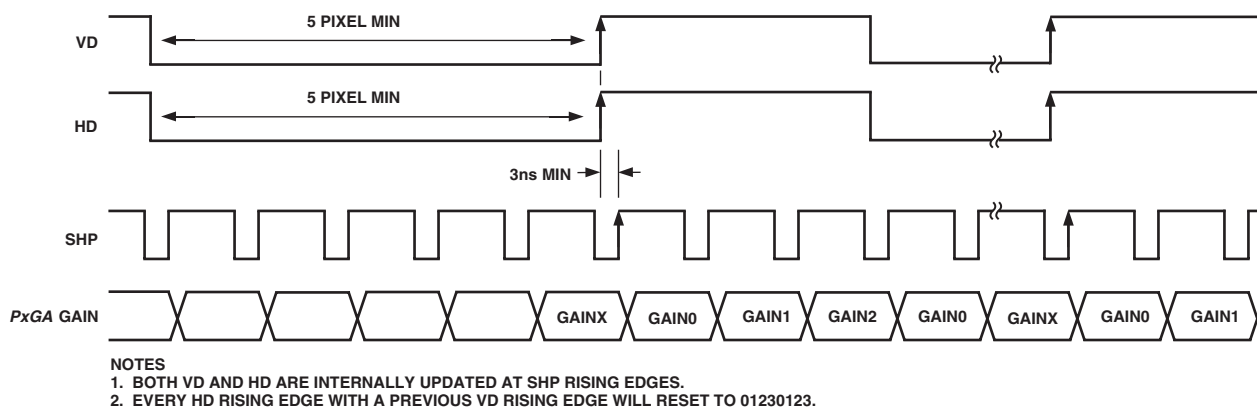


Figure 15. PxGA Mode 4 (4-Color) Detailed Timing

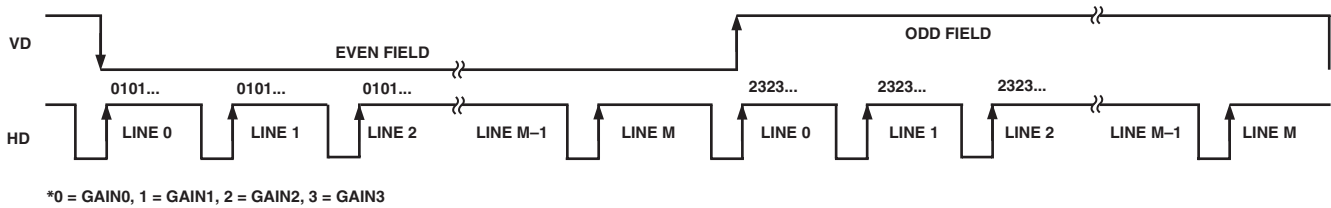


Figure 16. PxGA Mode 5 (VD Selected) Frame/Line Gain Register Sequence

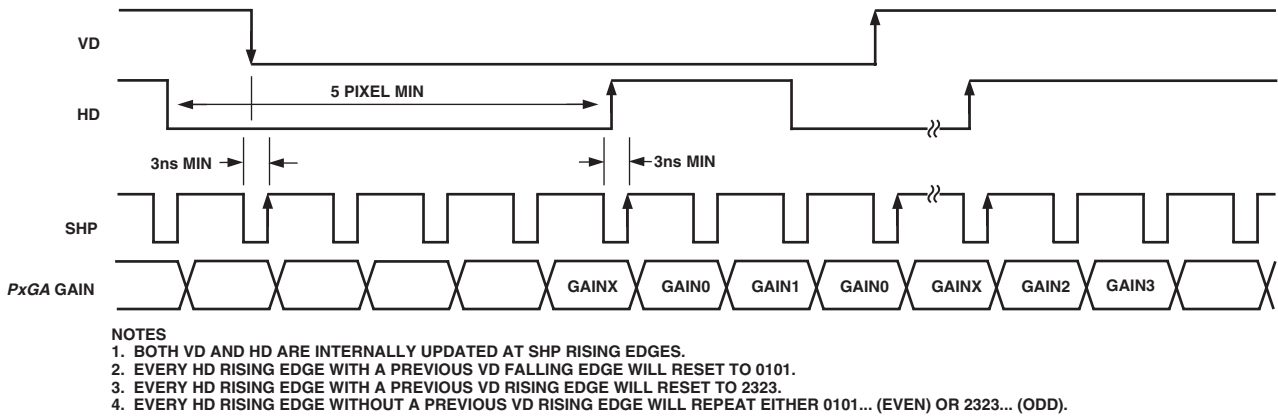


Figure 17. PxGA Mode 5 (VD Selected) Detailed Timing

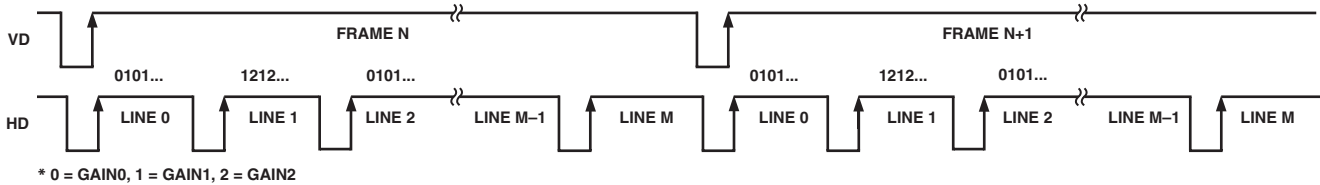


Figure 18. PxGA Mode 6 (Mosaic Repeat) Frame/Line Gain Register Sequence

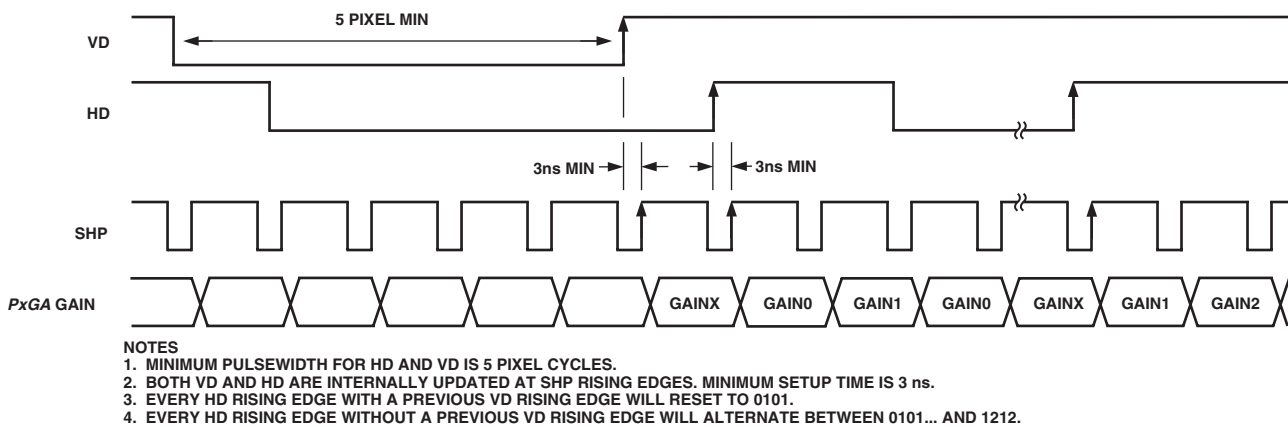
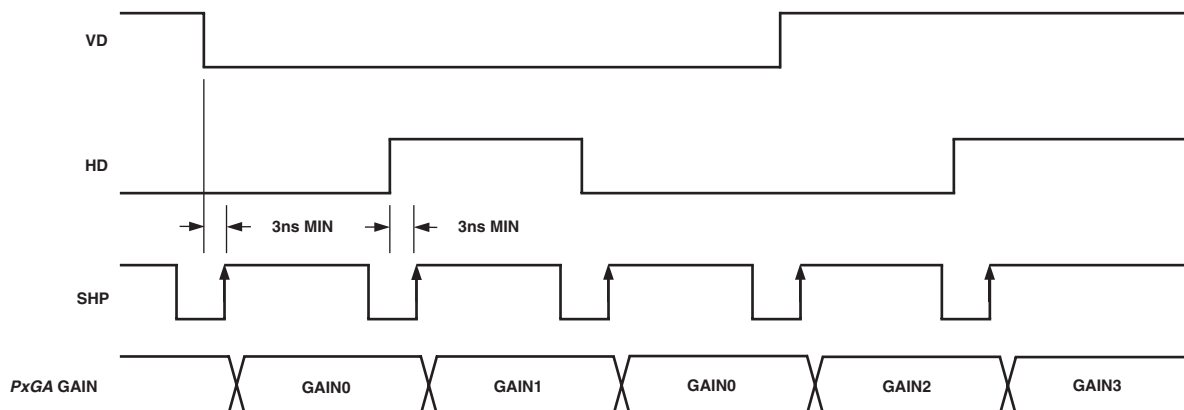


Figure 19. PxGA Mode 6 (Mosaic Repeat) Detailed Timing



NOTES

1. BOTH VD AND HD ARE INTERNALLY UPDATED AT SHP RISING EDGES.
2. VD = 0 AND HD = 0 SELECTS GAIN0.
3. VD = 0 AND HD = 1 SELECTS GAIN1.
4. VD = 1 AND HD = 0 SELECTS GAIN2.
5. VD = 1 AND HD = 1 SELECTS GAIN3.

Figure 20. PxGA Mode 7 (User-Specified) Detailed Timing

SERIAL INTERFACE TIMING AND INTERNAL REGISTER DESCRIPTION

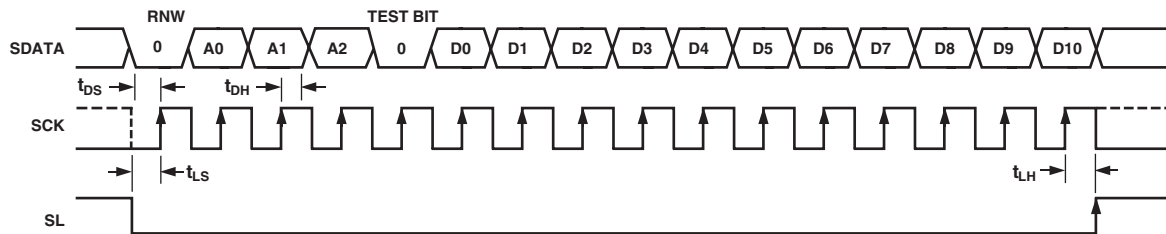
Table I. Internal Register Map

| Register Name | Address A0 A1 A2 | Data Bits | | | | | | | | | | | |
|---------------|---------------------|----------------------------------|----|---------------------|----------------|---|--------------------|-----|----------------|----------------|----------------|-----------------|----------------|
| | | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | |
| Operation | 0 0 0 | Channel Select CCD/AUX1/2 | | Power-Down Modes | | Software Reset | OB Clamp On/Off | | 0 ¹ | 1 ² | 0 ¹ | 0 ¹ | 0 ¹ |
| VGA Gain | 1 0 0 | LSB | | | | | | | | | | MSB | X |
| Clamp Level | 0 1 0 | LSB | | | | | | | | MSB | X | X | X |
| Control | 1 1 0 | Color Steering Mode Selection | | | PxGA On/Off | Clock Polarity Select for SHP/SHD/CLP/DATA | | | | 0 ¹ | 0 ¹ | Three- State | X |
| PxGA Gain0 | 0 0 1 | LSB | | | | | | MSB | X | X | X | X | X |
| PxGA Gain1 | 1 0 1 | LSB | | | | | | MSB | X | X | X | X | X |
| PxGA Gain2 | 0 1 1 | LSB | | | | | | MSB | X | X | X | X | X |
| PxGA Gain3 | 1 1 1 | LSB | | | | | | MSB | X | X | X | X | X |

NOTES

¹Internal use only. Must be set to zero.

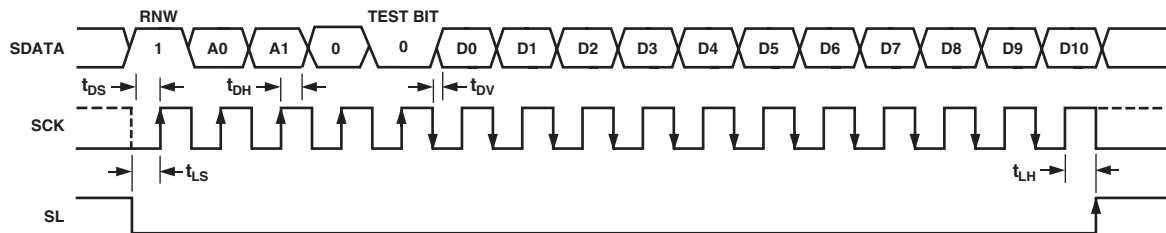
²Must be set to one.



NOTES

1. SDATA BITS ARE INTERNALLY LATCHED ON THE RISING EDGES OF SCK.
2. RNW = READ-NOT-WRITE. SET LOW FOR WRITE OPERATION.
3. TEST BITS = INTERNAL USE ONLY. MUST BE SET LOW.
4. SYSTEM UPDATE OF LOADED REGISTERS OCCURS ON SL RISING EDGE.

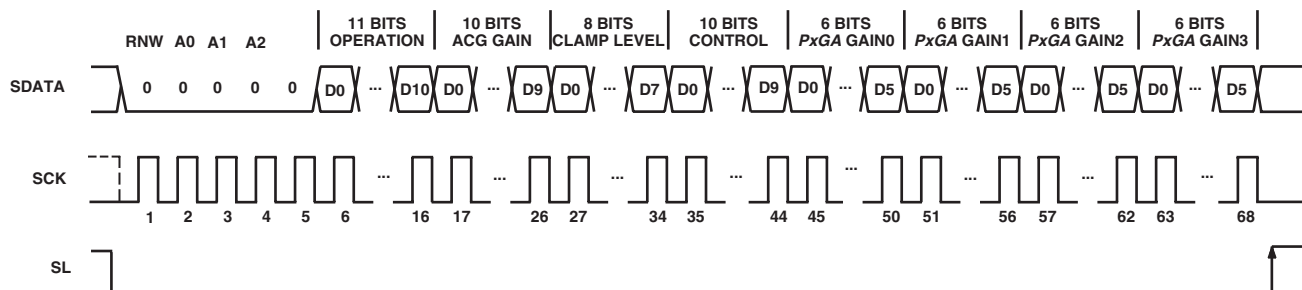
Figure 21. Serial Write Operation



NOTES

1. RNW = READ-NOT-WRITE. SET HIGH FOR READ OPERATION.
2. TEST BITS = INTERNAL USE ONLY. MUST BE SET LOW.
3. SERIAL DATA FROM THE SELECTED REGISTER IS VALID STARTING AFTER THE 5TH SCK FALLING EDGE AND IS UPDATED ON SCK FALLING EDGES.

Figure 22. Serial Readback Operation



NOTES

1. ANY NUMBER OF ADJACENT REGISTERS MAY BE LOADED SEQUENTIALLY, BEGINNING WITH THE LOWEST ADDRESS AND INCREMENTING ONE ADDRESS AT A TIME.
2. WHEN SEQUENTIALLY LOADING MULTIPLE REGISTERS, THE EXACT REGISTER LENGTH (SHOWN ABOVE) MUST BE USED FOR EACH REGISTER.
3. ALL LOADED REGISTERS WILL BE SIMULTANEOUSLY UPDATED WITH THE RISING EDGE OF SL.

Figure 23. Continuous Serial Write Operation to All Registers

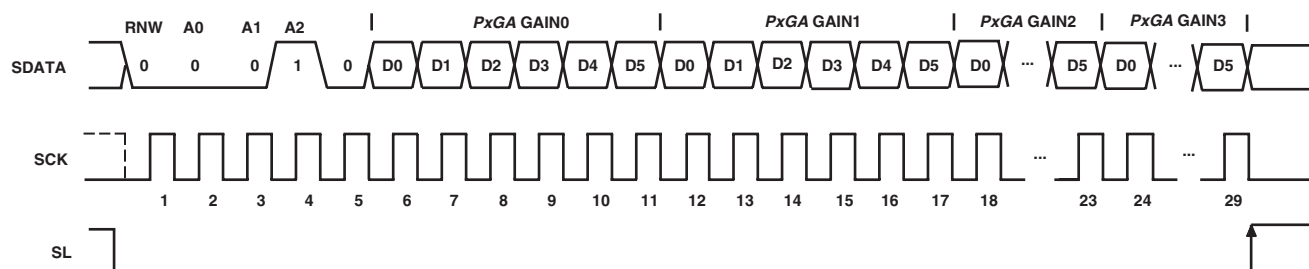


Figure 24. Continuous Serial Write Operation to All PxGA Gain Registers

Table II. Operation Register Contents (Default Value x000)

| D10 | D9 | D8 | D7 | D6 | Optical Black Clamp D5 | Reset D4 | Power-Down Modes D3 D2 | Channel Selection D1 D0 |
|----------------|----------------|----------------|----------------|----------------|---|--|--|---|
| 0 ¹ | 0 ¹ | 0 ¹ | 1 ² | 0 ¹ | 0 Enable Clamping 1 Disable Clamping | 0 Normal 1 Reset All Registers to Default | 0 0 Normal Power 0 1 Test Only 1 0 Standby 1 1 Total Power-Down | 0 0 CCD Mode 0 1 AUX1 Mode 1 0 AUX2 Mode 1 1 Test Only |

NOTES

- ¹Must be set to zero.
- ²Set to one.

Table III. VGA Gain Register Contents (Default Value x000)

| D10 | MSB D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 | Gain (dB) |
|-----|-----------|----|----|----|----|----|----|----|----|-----------|-----------|
| X | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 2.0 |
| | | | | | • | | | | | | • |
| | | | | | • | | | | | | • |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 35.965 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 36.0 |

Table IV. Clamp Level Register Contents (Default Value x080)

| D10 | D9 | D8 | MSB | | | | | | | LSB D0 | Clamp Level (LSB) | |
|-----|----|----|-----|----|----|----|----|----|----|-----------|-------------------|---|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | | |
| X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 4 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 8 | |
| | | | | | | | | | | | • | |
| | | | | | | | | | | | • | |
| | | | | | | | | | | | • | |
| | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1016 | |
| | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1020 | |

Table V. Control Register Contents (Default Value x000)

| D10 | Data Out D9 | D8 | D7 | DATACLK | | CLP/PBLK | SHP/SHD | PxGA | Color Steering Modes | | | | | | | |
|-----|---------------------------|----------------|----------------|---------|----------------------|----------|-------------|-----------------|----------------------|----|----|---|-------------------|---|-----------|----------------|
| | | | | D6 | D6 | D5 | D4 | D3 ² | D2 | D1 | D0 | | | | | |
| X | 0 Enable 1 Three-State | 0 ¹ | 0 ¹ | 0 | Rising Edge Trigger | 0 | Active Low | 0 | Disable | 0 | 0 | 0 | Steering Disabled | | | |
| | | | | 1 | Falling Edge Trigger | 1 | Active High | 1 | Enable | 0 | 0 | 1 | Mosaic Separate | | | |
| | | | | | | | | | | | | 0 | 1 | 0 | Interlace | |
| | | | | | | | | | | | | | 0 | 1 | 1 | 3-Color |
| | | | | | | | | | | | | | 1 | 0 | 0 | 4-Color |
| | | | | | | | | | | | | | 1 | 0 | 1 | VD Selected |
| | | | | | | | | | | | | | 1 | 1 | 0 | Mosaic Repeat |
| | | | | | | | | | | | | | 1 | 1 | 1 | User Specified |

NOTES

¹ Must be set to zero.

² When D3 = 0 (PxGA disabled), the PxGA gain is fixed to Code 63 (3.3dB).

Table VI. PxGA Gain Registers for Gain0, Gain1, Gain2, Gain3 (Default Value x000)

| D10 | D9 | D8 | D7 | D6 | MSB | | | | | LSB D0 | Gain (dB)* | | |
|-----|----|----|----|----|-----|----|----|----|----|-----------|------------|------|---|
| | | | | | D5 | D4 | D3 | D2 | D1 | | | | |
| X | X | X | X | X | 0 | 1 | 1 | | 1 | 1 | 1 | +9.5 | |
| | | | | | | | | | | | | | • |
| | | | | | | | | | | | | | • |
| | | | | | | | | | | | | | • |
| | | | | | | | | | | | | | • |
| | | | | | | | | | | 0 | 0 | 0 | 0 |
| | | | | | 1 | 1 | 1 | 1 | 1 | 1 | +3.3 | | |
| | | | | | | | | | | | • | | |
| | | | | | | | | | | | • | | |
| | | | | | | | | | | | • | | |
| | | | | | 1 | 0 | 0 | 0 | 0 | 0 | -2.5 | | |

*Control Register Bit D3 must be set high (PxGA Enable) to use the PxGA Gain Registers.

CIRCUIT DESCRIPTION AND OPERATION

The AD9824 signal processing chain is shown in Figure 25. Each processing step is essential in achieving a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external $0.1\ \mu\text{F}$ series coupling capacitor. This restores the dc level of the CCD signal to approximately $1.5\ \text{V}$ to be compatible with the $3\ \text{V}$ single supply of the AD9824.

Correlated Double Sampler

The CDS circuit samples each CCD pixel twice to extract the video information and reject low frequency noise. The timing shown in Figure 5 illustrates how the two CDS clocks, SHP and SHD, are used to sample the reference level and data level of the CCD signal, respectively. The CCD signal is sampled on the rising edges of SHP and SHD. Placement of these two clock signals is critical in achieving the best performance from the CCD. An internal SHP/SHD delay (t_{ID}) of $3\ \text{ns}$ is caused by internal propagation delays.

Input Clamp

A line-rate input clamping circuit is used to remove the CCD's optical black offset. This offset exists in the CCD's shielded black reference pixels. Unlike some AFE architectures, the AD9824 removes this offset in the input stage to minimize the effect of a

gain change on the system black level. Another advantage of removing this offset at the input stage is to maximize system headroom. Some area CCDs have large black level offset voltages, which, if not corrected at the input stage, can significantly reduce the available headroom in the internal circuitry when higher VGA gain settings are used.

Horizontal timing is shown in Figure 6. It is recommended that the CLPDM pulse be used during valid CCD dark pixels. CLPDM may be used during the optical black pixels, either together with CLPOB or separately. The CLPDM pulse should be a minimum of 4 pixels wide.

PxGA

The *PxGA* provides separate gain adjustment for the individual color pixels. A programmable gain amplifier with four separate values, the *PxGA* has the capability to "multiplex" its gain value on a pixel-to-pixel basis. This allows lower output color pixels to be gained up to match higher output color pixels. Also, the *PxGA* may be used to adjust the colors for white balance, reducing the amount of digital processing that is needed. The four different gain values are switched according to the color steering circuitry. Seven different color steering modes for different types of CCD color filter arrays are programmed in the AD9824's Control Register. For example, mosaic separate steering mode accommodates the popular "Bayer" arrangement of red, green, and blue filters (see Figure 26).

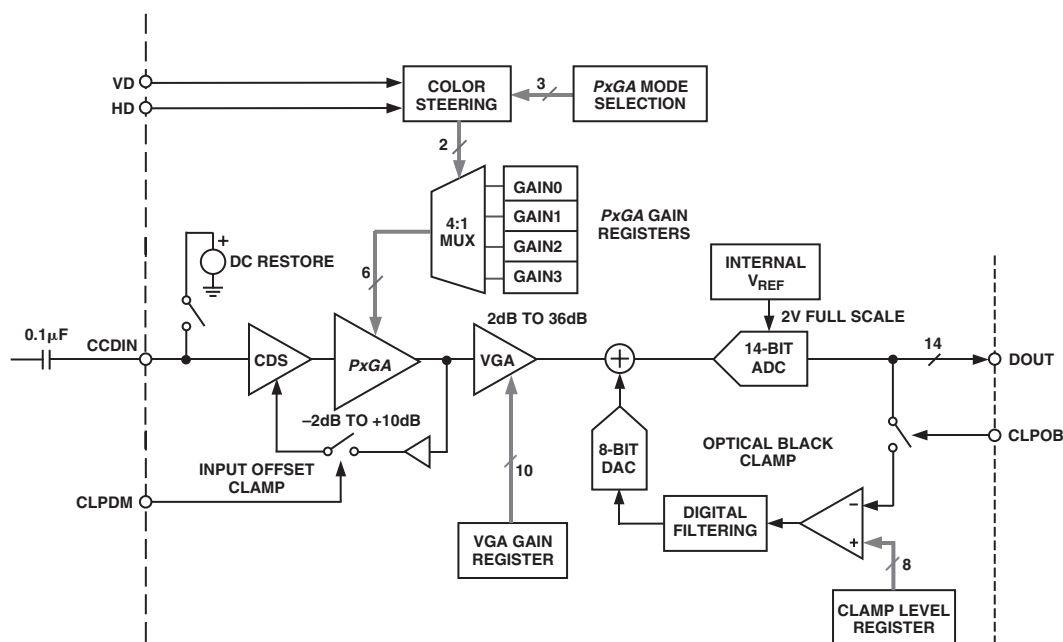


Figure 25. CCD Mode Block Diagram

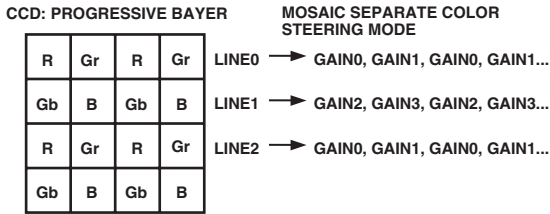


Figure 26. CCD Color Filter Example: Progressive Scan

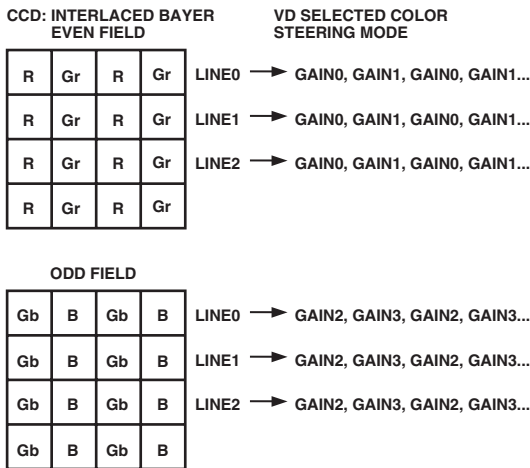


Figure 27. CCD Color Filter Example: Interlaced

The same Bayer pattern can also be interlaced, and the VD selected mode should be used with this type of CCD (see Figure 27). The color steering performs the proper multiplexing of the R, G, and B gain values (loaded into the PxGA gain registers) and is synchronized by the user with vertical (VD) and horizontal (HD) sync pulses. For more detailed information, see the PxGA Timing section. The PxGA gain for each of the four channels is variable from -2.5 dB to +9.5 dB, controlled in 64 steps through the serial interface. The PxGA gain curve is shown in Figure 28.

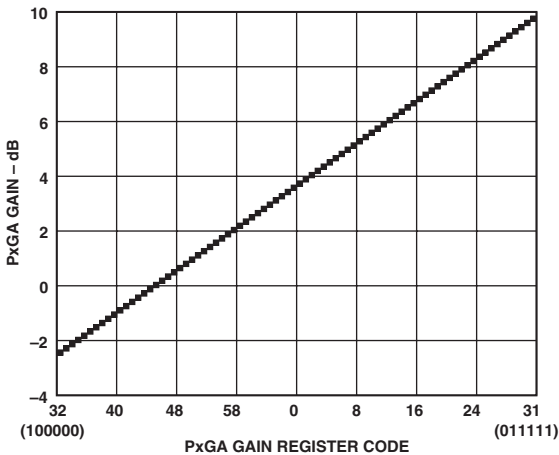


Figure 28. PxGA Gain Curve

Variable Gain Amplifier

The VGA stage provides a gain range of 2 dB to 36 dB, programmable with 10-bit resolution through the serial digital interface. Combined with approximately 4 dB from the PxGA stage, the total gain range for the AD9824 is 6 dB to 40 dB. The minimum gain of 6 dB is needed to match -a 1 V input signal with the ADC full-scale range of 2 V. When compared to 1 V full-scale systems (such as ADI's AD9803), the equivalent gain range is 0 dB to 34 dB.

The VGA gain curve follows a "linear-in-dB" shape. The exact VGA gain can be calculated for any gain register value by using the following equation:

Code Range Gain Equation (dB)
 0-1023 $Gain = (0.0353)(Code)$

As shown in the CCD Mode Specifications, only the VGA gain range from 2 dB to 36 dB has tested and guaranteed accuracy. This corresponds to a VGA gain code range of 77 to 1023. The Gain Accuracy Specifications also include a PxGA gain of approximately 3.3 dB, for a total gain range of 6 dB to 40 dB.

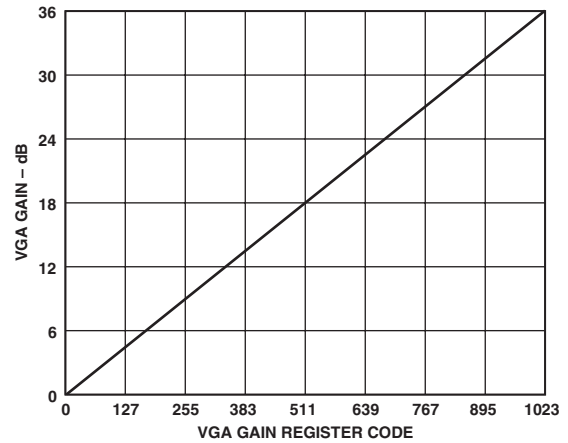


Figure 29. VGA Gain Curve (Gain from PxGA Not Included)

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the clamp level register. The clamp level is adjustable from 0 to 1020 LSB, in 256 steps. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a D/A converter. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the post processing, the AD9824 optical black clamping may be disabled using Bit D5 in the Operation Register (see Serial Interface Timing and Internal Register Description section). When the loop is disabled, the clamp level register may still be used to provide programmable offset adjustment.

Horizontal timing is shown in Figure 6. The CLPOB pulse should be placed during the CCD's optical black pixels. It is recommended that the CLPOB pulse duration be at least 20 pixels wide to minimize clamp noise. Shorter pulsewidths may be used, but clamp noise may increase and the ability to track low frequency variations in the black level will be reduced.

A/D Converter

The AD9824 uses high performance ADC architecture, optimized for high speed and low power. Differential nonlinearity (DNL) performance is typically better than 0.5 LSB, as shown in TPC 2. Instead of the 1 V full-scale range used by the earlier AD9801 and AD9803 products from Analog Devices, the AD9824's ADC uses a 2 V input range. Better noise performance results from using a larger ADC full-scale range (see TPC 3).

AUX1 Mode

For applications that do not require CDS, the AD9824 can be configured to sample ac-coupled waveforms. Figure 30 shows the circuit configuration for using the AUX1 channel input (Pin 36). A single 0.1 μF ac-coupling capacitor is needed between the input signal driver and the AUX1IN pin. An on-chip dc-bias circuit sets the average value of the input signal to approximately 0.4 V, which is referenced to the midscale code of the ADC. The VGA Gain Register provides a gain range of 0 dB to 36 dB in this mode of operation (see VGA Gain Curve, Figure 29).

The VGA gains up the signal level with respect to the 0.4 V bias level. Signal levels above the bias level will be further increased to a higher ADC code, while signal levels below the bias level will be further decreased to a lower ADC code.

AUX2 Mode

For sampling video-type waveforms, such as NTSC and PAL signals, the AUX2 channel provides black level clamping, gain adjustment, and A/D conversion. Figure 31 shows the circuit configuration for using the AUX2 channel input (Pin 34). An external 0.1 μF blocking capacitor is used with the on-chip video clamp circuit to level shift the input signal to a desired reference level. The clamp circuit automatically senses the most negative portion of the input signal and adjusts the voltage across the input capacitor. This forces the black level of the input signal to be equal to the value programmed into the Clamp Level Register (see Serial Interface Timing and Internal Register Description). The VGA provides gain adjustment from 0 dB to 18 dB. The same VGA Gain Register is used, but only the 9 MSBs of the gain register are used (see Table VII.)

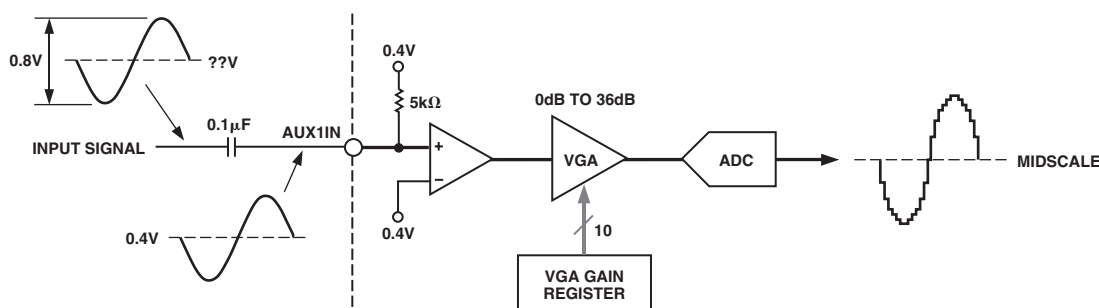


Figure 30. AUX1 Circuit Configuration

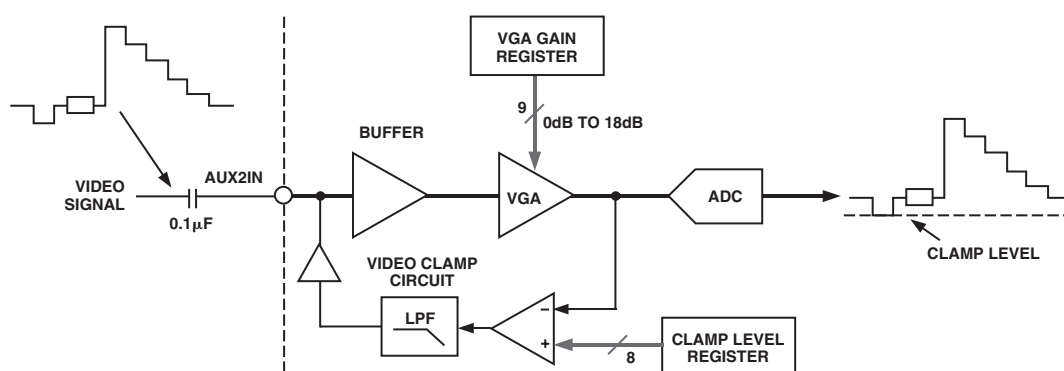


Figure 31. AUX2 Circuit Configuration

Table VII. VGA Gain Register Used for AUX2-Mode

| D10 | MSB D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 | Gain (dB) |
|-----|-----------|----|----|----|----|----|----|----|----|-----------|-----------|
| X | 0 | X | X | X | X | X | X | X | X | X | 0.0 |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.0 |
| | | | | | • | | | | | | • |
| | | | | | • | | | | | | • |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 18.0 |

AD9824

APPLICATIONS INFORMATION

The AD9824 is a complete analog front end (AFE) product for digital still camera and camcorder applications. As shown in Figure 32, the CCD image (pixel) data is buffered and sent to the AD9824 analog input through a series input capacitor. The AD9824 performs the dc restoration, CDS, gain adjustment, black level correction, and analog-to-digital conversion.

The AD9824's digital output data is then processed by the image processing ASIC. The internal registers of the AD9824—used to control gain, offset level, and other functions—are programmed by the ASIC or microprocessor through a 3-wire serial digital interface. A system timing generator provides the clock signals for both the CCD and the AFE.

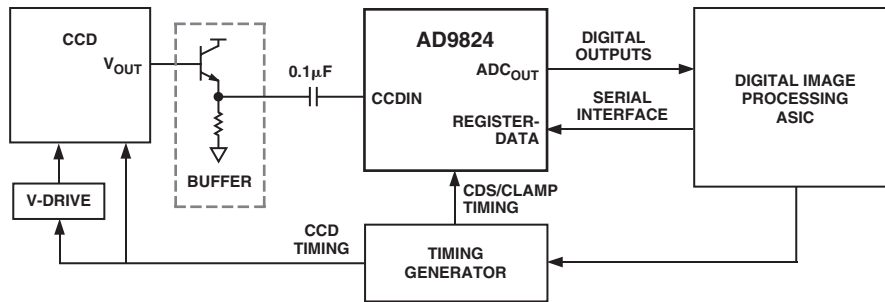


Figure 32. System Applications Diagram

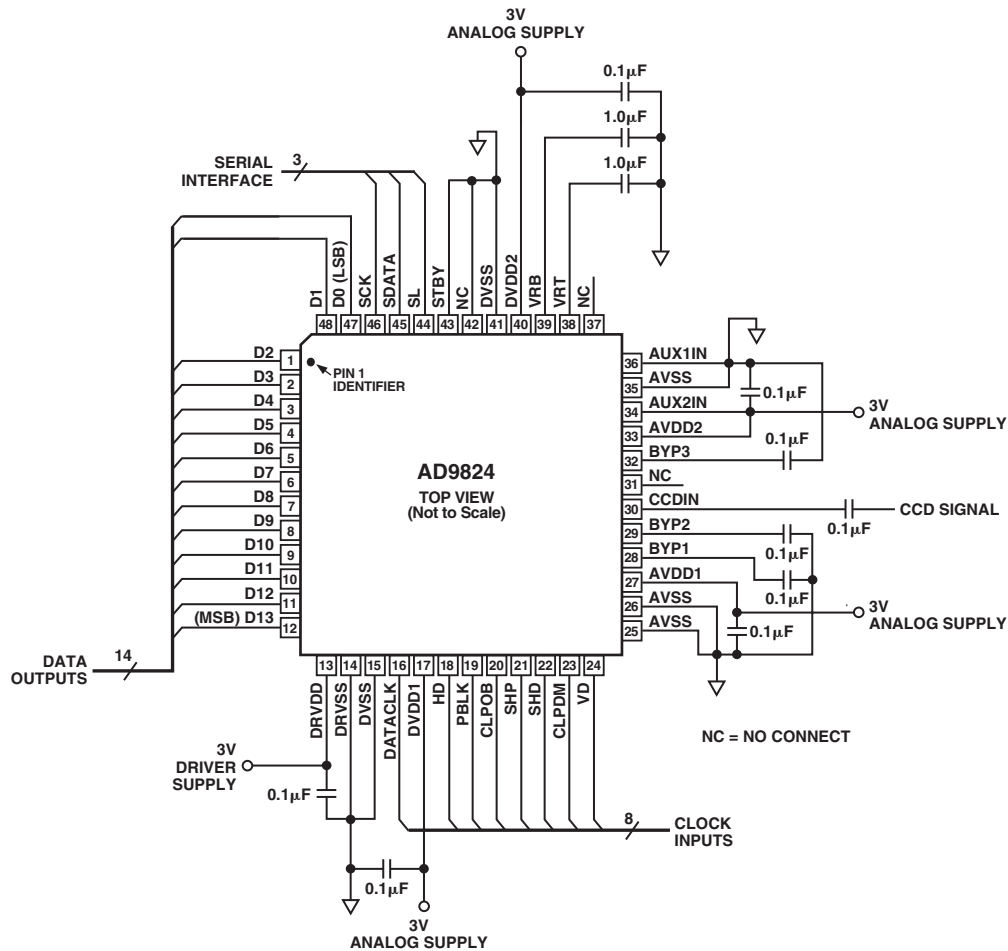


Figure 33. Recommended Circuit Configuration for CCD-Mode

Internal Power-On Reset Circuitry

After power-on, the AD9824 will automatically reset all internal registers and perform internal calibration procedures. This takes approximately 1 ms to complete. During this time, normal clock signals and serial write operations may occur. However, serial register writes will be ignored until the internal reset operation is completed.

Grounding and Decoupling Recommendations

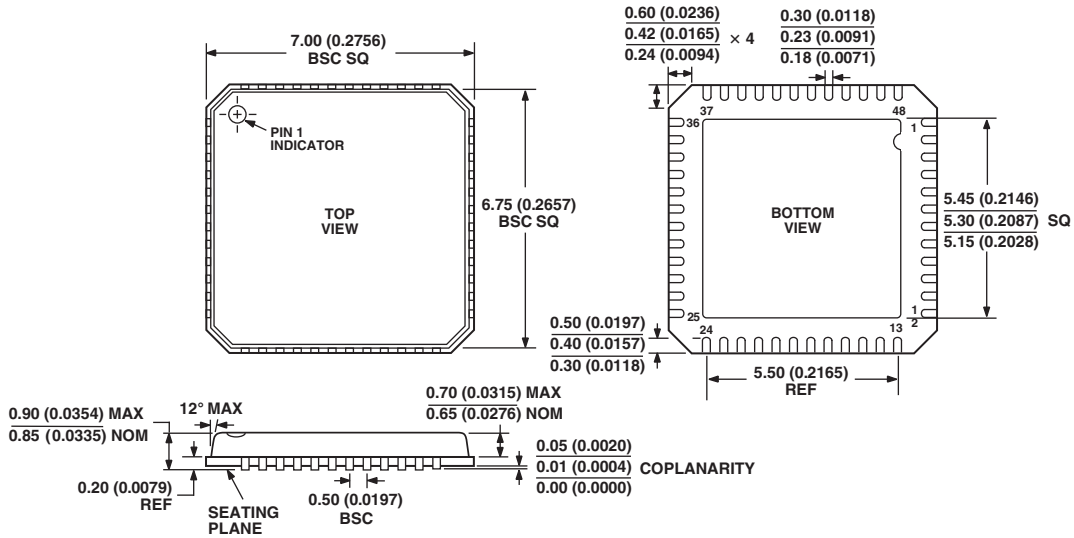
As shown in Figure 33, a single ground plane is recommended for the AD9824. This ground plane should be as continuous as possible, particularly around Pins 25 through 39. This will ensure that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and

their respective ground pins. All decoupling capacitors should be located as close as possible to the package pins. A single clean power supply is recommended for the AD9824, but a separate digital driver supply may be used for DRVDD (Pin 13). DRVDD should always be decoupled to DRVSS (Pin 14), which should be connected to the analog ground plane. Advantages of using a separate digital driver supply include using a lower voltage (2.7 V) to match levels with a 2.7 V ASIC, and reducing digital power dissipation and potential noise coupling. If the digital outputs (Pins 1–12) must drive a load larger than 20 pF, buffering is recommended to reduce digital code transition noise. Alternatively, placing series resistors close to the digital output pins may also help reduce noise.

OUTLINE DIMENSIONS

Dimensions shown in millimeters and (inches)

48-Lead Frame Chip Scale Package LFCSP 7 x 7 mm Body (CP-48)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN
COMPLIANT TO JEDEC STANDARDS MO-220

