

FEATURES

- 40 MSPS Correlated Double Sampler (CDS)
- 6 dB to 40 dB 10-Bit Variable Gain Amplifier (VGA)
- Low Noise Optical Black Clamp Circuit
- Preblanking Function
- 12-Bit 40 MSPS A/D Converter
- No Missing Codes Guaranteed
- 3-Wire Serial Digital Interface
- 3 V Single-Supply Operation
- Low Power: 160 mW @ 3 V Supply
- Space-Saving 32-Lead 5 mm × 5 mm LFCSP

APPLICATIONS

- Digital Still Cameras
- Digital Video Camcorders
- PC Cameras
- Portable CCD Imaging Devices
- CCTV Cameras

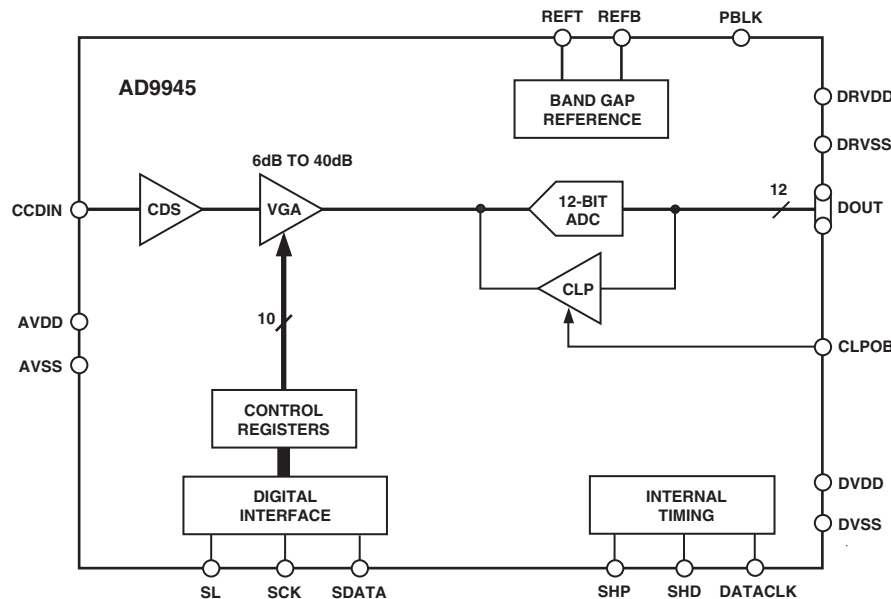
GENERAL DESCRIPTION

The AD9945 is a complete analog signal processor for CCD applications. It features a 40 MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The AD9945's signal chain consists of a correlated double sampler (CDS), a digitally controlled variable gain amplifier (VGA), a black level clamp, and a 12-bit A/D converter.

The internal registers are programmed through a 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, input clock polarity, and power-down modes.

The AD9945 operates from a single 3 V power supply, typically dissipates 160 mW, and is packaged in a space-saving 32-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM



REV. B

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AD9945—SPECIFICATIONS

GENERAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD= 3.0 V, f_{SAMP} = 40 MHz, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	-20		+85	°C
Storage	-65		+150	°C
POWER SUPPLY VOLTAGE				
Analog, Digital, Digital Driver			3.6	V
POWER CONSUMPTION				
Normal Operation (DRVDD Power not Included)				mW
DRVDD Power Only (C _{LOAD} = 20 pF)		10		mW
Power-Down Mode		1.5		mW
MAXIMUM CLOCK RATE	40			MHz

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

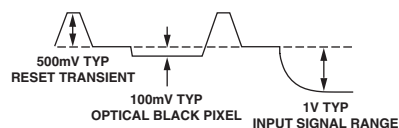
Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V _{IH}	2.1			V
Low Level Input Voltage	V _{IL}			0.6	V
High Level Input Current	I _{IH}		10		μA
Low Level Input Current	I _{IL}		10		μA
Input Capacitance	C _{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, I _{OH} = 2 mA	V _{OH}	2.2			V
Low Level Output Voltage, I _{OL} = 2 mA	V _{OL}			0.5	V

Specifications subject to change without notice.

SYSTEM SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Notes
CDS					
Maximum Input Range before Saturation*		1.0		V _{p-p}	See Input Waveform in Footnote
Allowable CCD Reset Transient*		500		mV	
Maximum CCD Black Pixel Amplitude*		100		mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Minimum Gain	40.0	5.3		dB	
Maximum Gain		41.5		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		256		Steps	Measured at ADC Output
Clamp Level					
Minimum Clamp Level		0		LSB	
Maximum Clamp Level		255		LSB	
A/D CONVERTER					
Resolution	12			Bits	
Differential Nonlinearity (DNL)		±0.5		LSB	
No Missing Codes		Guaranteed			
Data Output Coding		Straight Binary			
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		2.0		V	
Reference Bottom Voltage (REFB)		1.0		V	
SYSTEM PERFORMANCE					Specifications Include Entire Signal Chain
Gain Range					12 dB Gain Applied AC Grounded Input, 6 dB Gain Applied
Low Gain (VGA Code = 0)		5.3		dB	
Maximum Gain (VGA Code = 1023)	40.0	41.5		dB	
Gain Accuracy		±1.0		dB	
Peak Nonlinearity, 500 mV Input Signal		0.1		%	
Total Output Noise		1.2		LSB rms	
Power Supply Rejection (PSR)		40		dB	

*Input Signal Characteristics defined as follows:



Specifications subject to change without notice.

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TIMING SPECIFICATIONS ($C_L = 20$ pF, $f_{SAMP} = 40$ MHz, CCD Mode Timing in Figures 8 and 9, Serial Timing in Figures 4 and 5.)

Parameter	Symbol	Min	Typ	Max	Unit
SAMPLE CLOCKS					
DATACLK, SHP, SHD Clock Period	t_{CONV}	25			ns
DATACLK High/Low Pulse Width	t_{ADC}	10	12.5		ns
SHP Pulse Width	t_{SHP}		6.25		ns
SHD Pulse Width	t_{SHD}		6.25		ns
CLPOB Pulse Width*	t_{COB}	2	20		Pixels
SHP Rising Edge to SHD Falling Edge	t_{S1}		6.25		ns
SHP Rising Edge to SHD Rising Edge	t_{S2}	11.25	12.5		ns
Internal Clock Delay	t_{ID}		3		ns
DATA OUTPUTS					
Output Delay	t_{OD}		9.5		ns
Pipeline Delay			10		Cycles
SERIAL INTERFACE					
Maximum SCK Frequency	f_{SCLK}	10			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns

*Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp performance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect To	Min Max		Unit
		Min	Max	
AVDD	AVSS	-0.3	+3.9	V
DVDD	DVSS	-0.3	+3.9	V
DRVDD	DRVSS	-0.3	+3.9	V
Digital Outputs	DRVSS	-0.3	DRVDD + 0.3	V
SHP, SHD, DATACLK	DVSS	-0.3	DVDD + 0.3	V
CLPOB, PBLK	DVSS	-0.3	DVDD + 0.3	V
SCK, SL, SDATA	DVSS	-0.3	DVDD + 0.3	V
REFT, REFB, CCDIN	AVSS	-0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

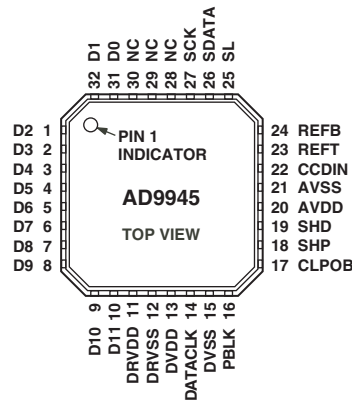
Thermal Resistance
32-Lead LFCSP Package
 $\theta_{JA} = 27.7$ °C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9945 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION

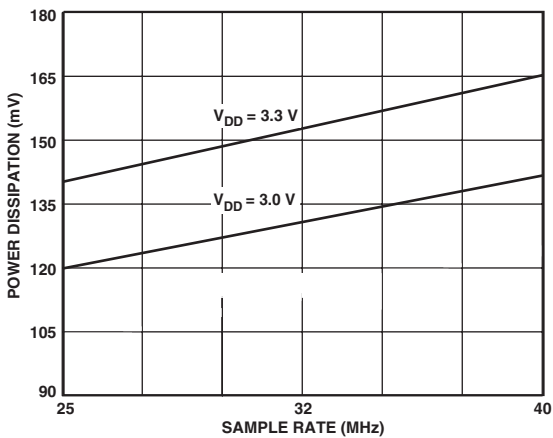


PIN FUNCTION DESCRIPTIONS

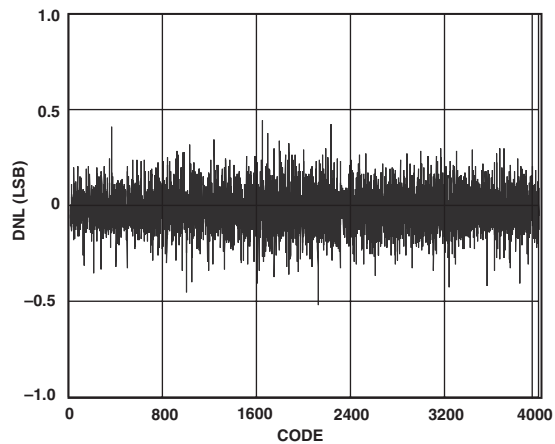
Pin Number	Mnemonic	Type	Description
1 to 10, 31, 32	D2 to D11, D0, D1	DO	Digital Data Outputs
11	DRVDD	P	Digital Output Driver Supply
12	DRVSS	P	Digital Output Driver Ground
13	DVDD	P	Digital Supply
14	DATACLK	DI	Digital Data Output Latch Clock
15	DVSS	P	Digital Supply Ground
16	PBLK	DI	Preblanking Clock Input
17	CLPOB	DI	Black Level Clamp Clock Input
18	SHP	DI	CDS Sampling Clock for CCD's Reference Level
19	SHD	DI	CDS Sampling Clock for CCD's Data Level
20	AVDD	P	Analog Supply
21	AVSS	P	Analog Ground
22	CCDIN	AI	Analog Input for CCD Signal
23	REFT	AO	A/D Converter Top Reference Voltage Decoupling
24	REFBL	AO	A/D Converter Bottom Reference Voltage Decoupling
25	SL	DI	Serial Digital Interface Load Pulse
26	SDATA	DI	Serial Digital Interface Data Input
27	SCK	DI	Serial Digital Interface Clock Input
28 to 30	NC	NC	Internally Pulled Down. Float or connect to GND.

TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

Typical Performance Characteristics—AD9945



TPC 1. Power vs. Sampling Rate



TPC 2. Typical DNL Performance

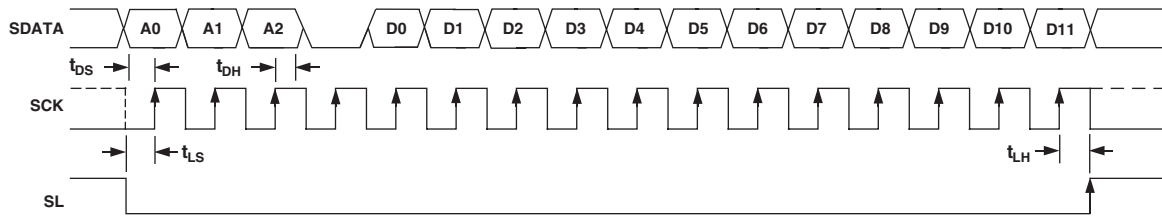
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INTERNAL REGISTER DESCRIPTION

Table I. Internal Register Map

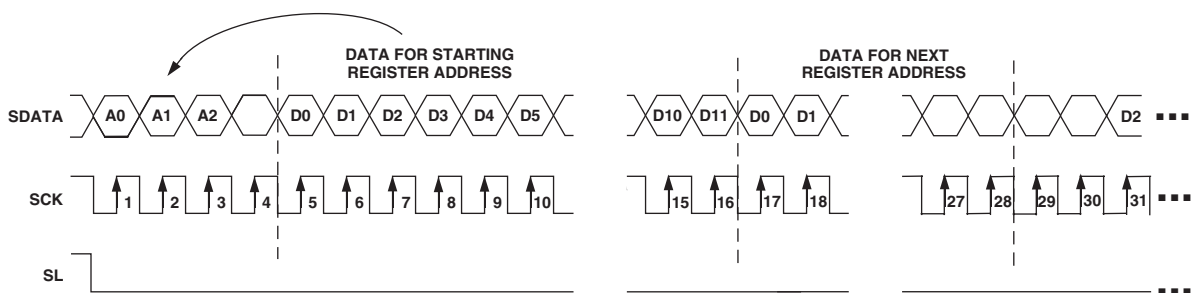
Register Name	Address Bits	Data Bits	Function
Operation		D0 D2, D1 D3 D5, D4 D6	Software Reset (0 = Normal Operation, 1 = Reset all registers to default) Power-Down Modes (00 = Normal Power, 01 = Standby, 10 = Total Shutdown) OB Clamp Disable (0 = Clamp ON, 1 = Clamp OFF) Test Mode. Should always be set to 00. PBLK Blanking Level (0 = Blank Output to Zero, 1 = Blank to OB Clamp Level)
Control		D0 D1 D2 D3 D4 D5 D6 D11 to D7	SHP/SHD Input Polarity (0 = Active Low, 1 = Active High) DATACLK Input Polarity (0 = Active Low, 1 = Active High) CLPOB Input Polarity (0 = Active Low, 1 = Active High) PBLK Input Polarity (0 = Active Low, 1 = Active High) Three-State Data Outputs (0 = Outputs Active, 1 = Outputs Three-States) Data Output Latching (0 = Latched by DATACLK, 1 = Latch is Transparent) Data Output Coding (0 = Binary Output, 1 = Gray Code Output) Test Mode. Should always be set to 00000.
Clamp Level		D7 to D0	OB Clamp Level (0 = 0 LSB, 255 = 255 LSB)
VGA Gain		D9 to D0	VGA Gain (0 = 6 dB, 1023 = 40 dB)

SERIAL INTERFACE



- NOTES
1. SDATA BITS ARE INTERNALLY LATCHED ON THE RISING EDGES OF SCK.
 2. SYSTEM UPDATE OF LOADED REGISTERS OCCURS ON SL RISING EDGE.
 3. ALL 12 DATA BITS D0 TO D11 MUST BE WRITTEN. IF THE REGISTER CONTAINS FEWER THAN 12 BITS, ZEROS SHOULD BE USED FOR THE UNDEFINED BITS.

Figure 4. Serial Write Operation



- NOTES
1. MULTIPLE SEQUENTIAL REGISTERS MAY BE LOADED CONTINUOUSLY.
 2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 12-BIT DATA-WORDS.
 3. THE ADDRESS WILL AUTOMATICALLY INCREMENT WITH EACH 12-BIT DATA-WORD (ALL 12 BITS MUST BE WRITTEN).
 4. SL IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.
 5. NEW DATA IS UPDATED AT THE NEXT SL RISING EDGE.

Figure 5. Continuous Serial Write Operation to All Registers

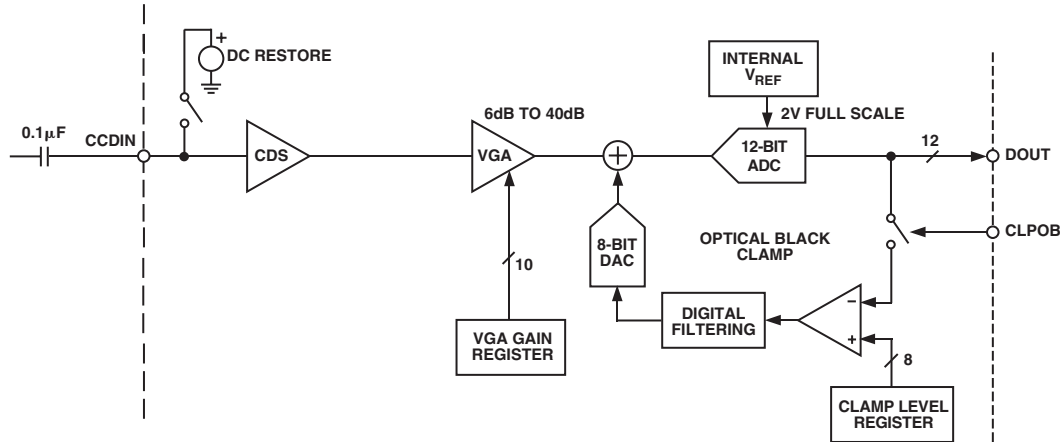


Figure 6. CCD Mode Block Diagram

CIRCUIT DESCRIPTION AND OPERATION

The AD9945 signal processing chain is shown in Figure 6. Each processing step is essential in achieving a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external 0.1 μF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.5 V to be compatible with the 3 V single supply of the AD9945.

Correlated Double Sampler

The CDS circuit samples each CCD pixel twice to extract the video information and reject low frequency noise. The timing shown in Figure 8 illustrates how the two CDS clocks, SHP and SHD, are used to sample the reference level and data level of the CCD signal, respectively. The CCD signal is sampled on the rising edges of SHP and SHD. Placement of these two clock signals is critical in achieving the best performance from the CCD. An internal SHP/SHD delay (t_{ID}) of 3 ns is caused by internal propagation delays.

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with the fixed black level reference, selected by the user in the clamp level register. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a D/A converter. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the postprocessing, the AD9945 optical black clamping may be disabled using Bit D3 in the operation register (see the Serial Interface Timing and Internal Register Description sections).

When the loop is disabled, the clamp level register may still be used to provide programmable offset adjustment.

Horizontal timing is shown in Figure 9. The CLPOB pulse should be placed during the CCD's optical black pixels. It is recommended that the CLPOB pulse be used during valid CCD dark pixels. The CLPOB pulse should be a minimum of 20 pixels wide to minimize clamp noise. Shorter pulse widths may be used, but clamp noise may increase and the loop's ability to track low frequency variations in the black level will be reduced.

A/D Converter

The ADC uses a 2 V input range. Better noise performance results from using a larger ADC full-scale range. The ADC uses a pipelined architecture with a 2 V full-scale input for low noise performance.

Variable Gain Amplifier

The VGA stage provides a gain range of 6 dB to 40 dB, programmable with 10-bit resolution through the serial digital interface. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. A plot of the VGA gain curve is shown in Figure 7.

$$VGA\ Gain(dB) = (VGA\ Code \times 0.035\ dB) + 5.3\ dB$$

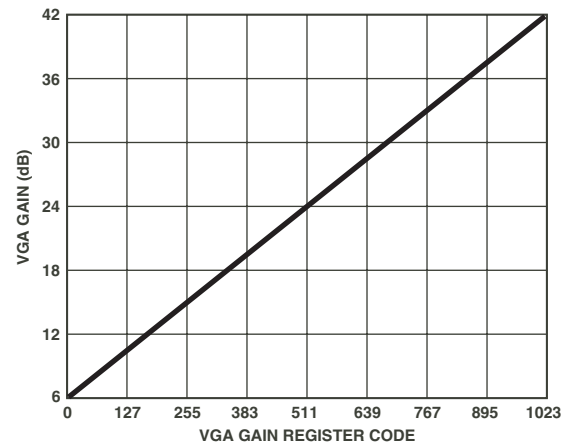
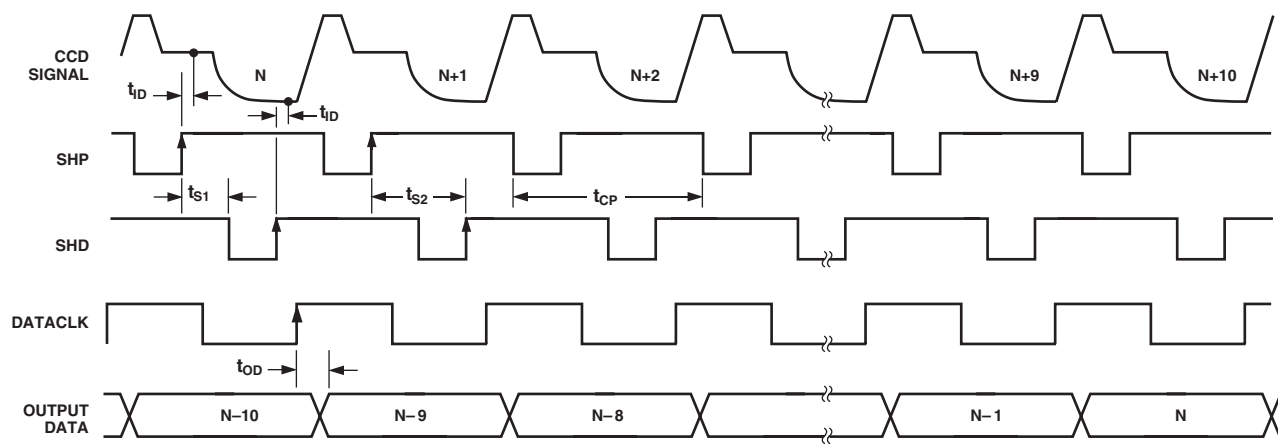


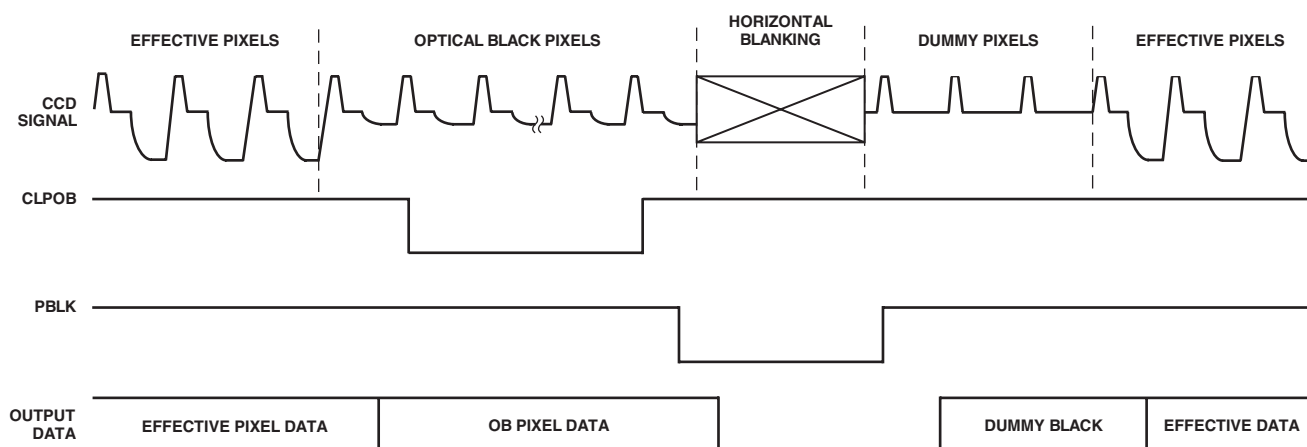
Figure 7. VGA Gain Curve

CCD MODE TIMING



- NOTES
1. RECOMMENDED PLACEMENT FOR DATACLK RISING EDGE IS BETWEEN THE SHD RISING EDGE AND NEXT SHP FALLING EDGE.
 2. CCD SIGNAL IS SAMPLED AT SHP AND SHD RISING EDGES.

Figure 8. CCD Mode Timing



- NOTES
1. CLPOB WILL OVERWRITE PBLK. PBLK WILL NOT AFFECT CLAMP OPERATION IF OVERLAPPING WITH CLPOB.
 2. PBLK SIGNAL IS OPTIONAL.
 3. DIGITAL OUTPUT DATA WILL BE ALL ZEROS DURING PBLK. OUTPUT DATA LATENCY IS NINE DATACLK CYCLES.

Figure 9. Typical CCD Mode Line Clamp Timing

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APPLICATIONS INFORMATION

The AD9945 is a complete analog front end (AFE) product for digital still camera and camcorder applications. As shown in Figure 10, the CCD image (pixel) data is buffered and sent to the AD9945 analog input through a series input capacitor. The AD9945 performs the dc restoration, CDS, gain adjustment, black

level correction, and analog-to-digital conversion. The AD9945's digital output data is then processed by the image processing ASIC. The internal registers of the AD9945—used to control gain, offset level, and other functions—are programmed by the ASIC or microprocessor through a 3-wire serial digital interface. A system timing generator provides the clock signals for both the CCD and the AFE.

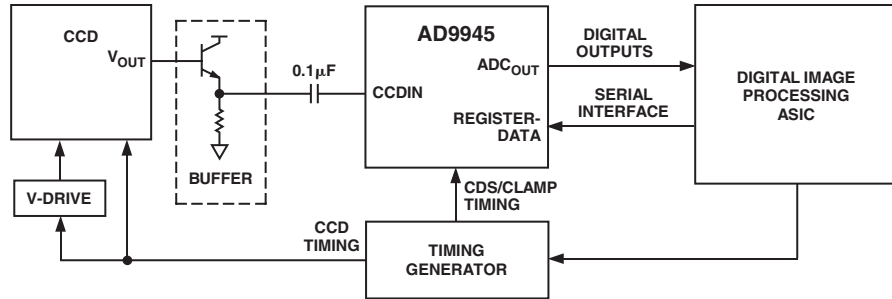
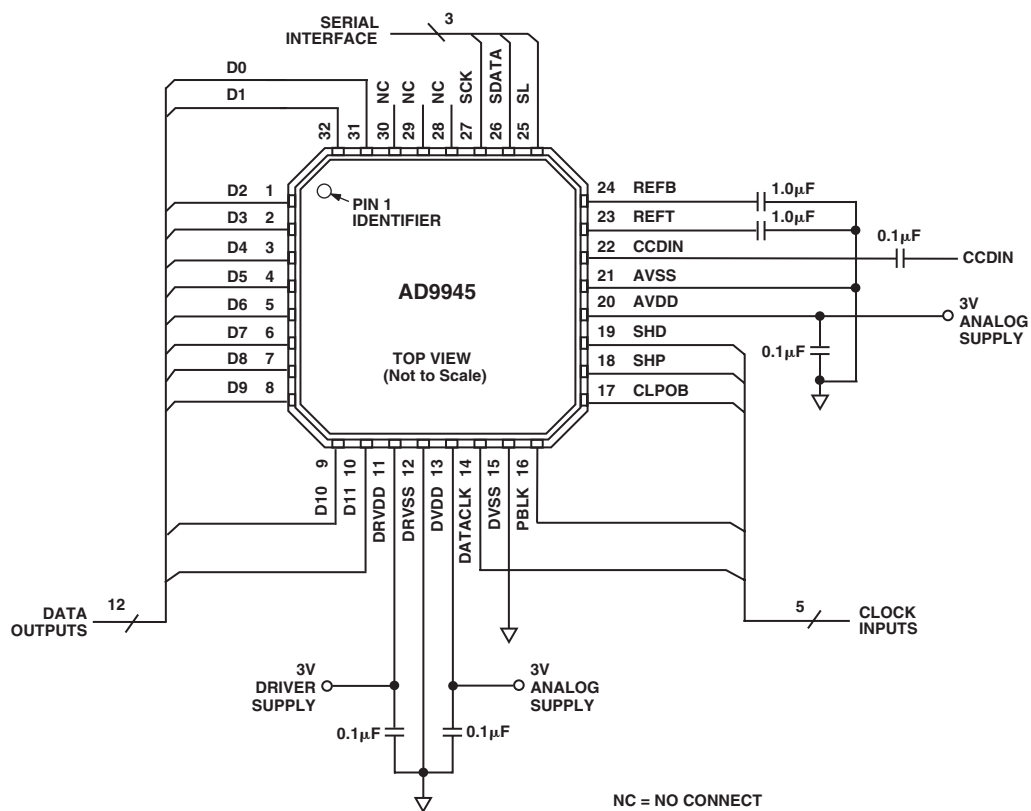


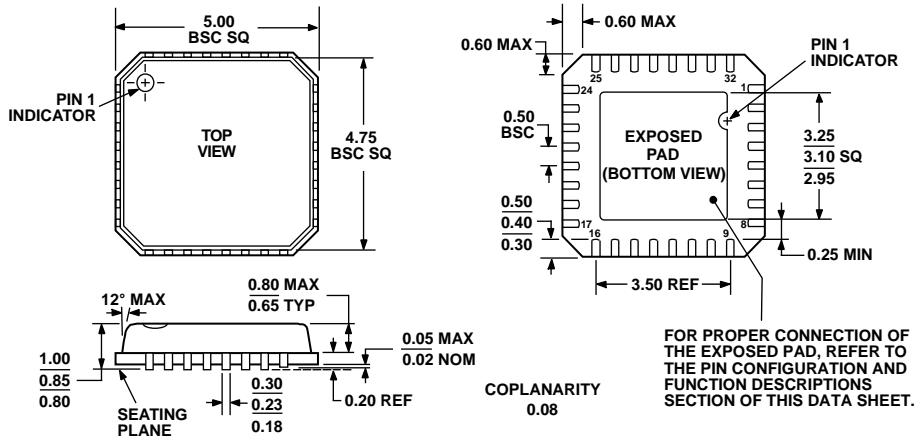
Figure 10. System Applications Diagram



NOTE
 THE EXPOSED PAD ON THE BOTTOM OF THE AD9945 SHOULD BE
 SOLDERED TO THE GND PLANE OF THE PRINTED CIRCUIT BOARD

Figure 11. Recommended Circuit Configuration for CCD Mode

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 1. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
 5 mm × 5 mm Body, Very Thin Quad
 (CP-32-2)
 Dimensions shown in millimeters

011708-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD9945KCPZ	-20°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
AD9945KCPZRL7	-20°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2

¹ Z = RoHS Compliant Part.

REVISION HISTORY

1/11—Rev. A to Rev. B

Changed 140 mW to 160 mW Throughout 1
 Changes to Power Supply Voltage Parameter and Power Consumption, Normal Operation (DRVDD Power not Included) Parameter in General Specifications Table 2
 Changed 2.7 V to 2.85 V in Digital Specifications Table Summary 2
 Changes to System Specifications Table Summary 3
 Added Low Gain Mode Parameter in System Specifications Table 3
 Added Exposed Pad Notation to Pin Configuration 5
 Changes to TPC 1 7

Changes to Table 1 8
 Changes to Figure 4 and Figure 5 9
 Added Required Start-Up Write Section 13
 Changes to Grounding and Decoupling Recommendations Section 13
 Moved Ordering Guide 14
 Changes to Ordering Guide 14

11/03—Rev. 0 to Rev. A

Changes to Timing Specifications 4
 Changes to Ordering Guide 4
 Changes to Figure 11 13
 Updated Outline Dimensions 14