

# FMA1125DC Touch Sensor Controller

#### Overview

The FMA1125DC is a low-power, compact, flexible touch sensor controller that converts capacitance generated between the human body and a conductive touch pad to digital data without any analog signal processing.

Its programmability provides design flexibility, high performance and stability for a broad range of applications. The FMA1125DC's AIC<sup>TM</sup> (Automatic Impedance Calibration) function can be easily configured to support different sensitivities for individual channels independently as well as to change values of parameters such as the calibration interval. AIC<sup>TM</sup> may also be temporarily paused and resumed by a host MCU.

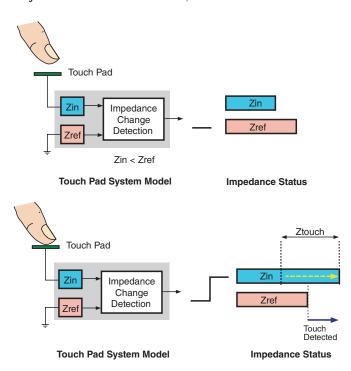
Among the many features of the FMA1125DC is APISTM (Adjacent Pattern Interference Suppression). APIS is a filtering function that eliminates adjacent key or pattern interference. The FMA1125DC also gives touch-strength output in addition to touch on/off output. There are a number of DIOs depending on the package type that can be configured and programmed to meet specific requirements, giving customers greater flexibility and value.

The FMA1125DC comes with various package types to support different numbers of input channels and DIOs.

#### Features

- Patented fully digital architecture
- Extremely low power consumption (100µA in active mode)
- Supports 8 input channels (24QFN, 24SSOP, 24SOP) or 6 input channels (16QFN, 16SOP)
- Programmable registers to characterize applications
- I<sup>2</sup>C interface with the host MCU
- Configurable Touch Input Channels as extended DIOs
- 6-bit resolution of LED dimming control via DIO pins
- Configurable AIC<sup>TM</sup> (Automatic Impedance Calibration)
- Two types of interrupts (GINT for general purpose and TINT for touch detection)

The FMA1125DC touch sensor controller is developed and owned by ATLab Inc., South Korea, and is distributed by Fujitsu Microelectronics America, Inc.



- 8-bit resolution of touch strength data (256 steps)
- Three different modes for APIS<sup>TM</sup> (Adjacent Pattern Interference Suppression)
- Configurable DIO pins as direct touch outputs, extended GPIOs or external interrupt inputs
- Idle and Sleep modes for power saving
- De-bounced touch outputs

#### **Applications**

- Portable devices such as PDAs, cellular phones, MP3 players, remote controllers, and other integrated input devices
- Home appliances and consumer electronic products
- Computer input devices such as mice and keyboards

#### **Confidential**

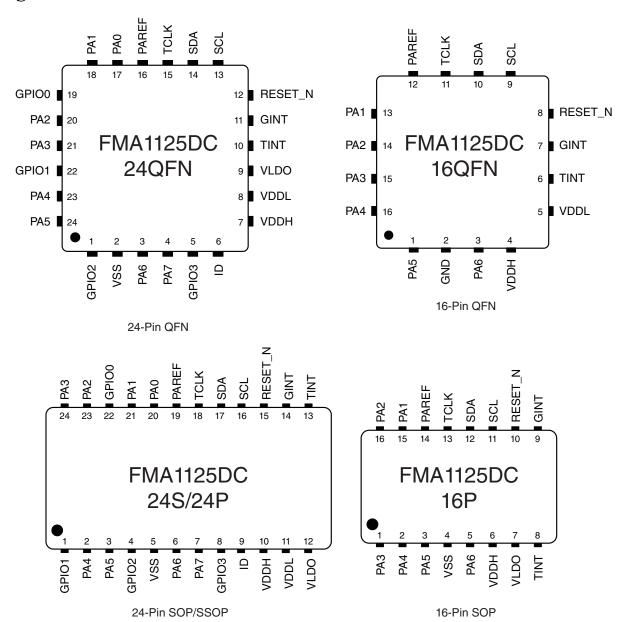
### **Table of Contents**

Ordering Information	l
Package Pinouts	1
Electrical Characteristics	2
Operation Principles	3
Touch Detection	3
AICTM (Automatic Impedance Calibration)	3
APIS™ Touch Output	3
Functional Characteristics	5
Communication Specifications for I <sup>2</sup> C	6
Application Information	8
24-pin Package (24QFN)	8
FMA1125DC 24QFN Typical Application Circuit: Internal LDO	9
FMA1125DC 24QFN Typical Application Circuit: External LDO Case 1	10
FMA1125DC 24QFN Typical Application Circuit: External LDO Case 2	11
16-pin Package (16QFN)	12
FMA1125DC 16QFN Typical Application Circuit: Internal LDO	13
24-pin Package (24SSOP)	14
FMA1125DC 24SSOP / 24SOP Typical Application Circuit: Internal LDO	
16-pin Package (16SOP)	16
FMA1125DC 16SOP Typical Application Circuit: Internal LDO	17
Power Connection	18
Power Sequence	20
Power Connection Type is Case B or Case D.	20
Power Connection Type is Case A, Case C, or Case E	20
Tuning System	21
Hardware	21
Software	22
Package Dimensions	23

### **Ordering Information**

Product Code	Package Type	Package Dimension	Pin Pitch	Number of Sensor Inputs	Number of DIOs
FMA1125DC-24N	24QFN	4mm x 4mm x 0.55mm	0.5mm	8	4
FMA1125DC-16N	16QFN	3mm x 3mm x 0.575mm	0.5mm	6	Configurable
FMA1125DC-24S	24SS0P	8.2mm x 7.8mm x2.0mm	0.65mm	8	4
FMA1125DC-24P	24S0P	15.3mm x 10.3mm x 2.6mm	1.27mm	8	4
FMA1125DC-16P	16SOP	9.9mm x 6.0mm x 1.8mm	1.27mm	6	Configurable

### **Package Pinouts**



#### **Electrical Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
ABSOLUTE	MAXIMUM RATINGS					
Tstg	Storage Temperature		-45		95	°C
Topr	Operating Temperature		-45		95	°C
Hopr	Operating Humidity		5		95	%
VPH	Power Supply Voltage	VPH should be higher than 3V when using internal LDO	2.3	3.3	5.5	V
V25	Power Supply Voltage(V25)		2.3	2.5	2.7	V
Vin	Input Voltage		2.3	2.5	2.7	V
RECOMME	NDED OPERATING CONDITIONS					
Toprr	Operating Temperature		-40	25	90	°C
Vddp	Power Supply Voltage (VPH)		2.4		5	V
Vddc	Power Supply Voltage (V25)		2.4	2.5	2.6	V
Tr_i	Digital Input Rising Time				5	ns
Tf_i	Digital Input Falling Time				5	ns
AC ELECTF	RICAL SPECIFICATIONS (Typical values at Ta	= 25°C and VPH = 3.3V)				
fi	Input frequency		2.5	5	20	KHz
fsmp	Sample frequency		10	500	5000	Hz
Stch	Touch Sensitivity			0.078		pF
Tr_o	Output Rising Time	Load = 100pF		50	60	ns
Tf_o	Output Falling Time	Load = 100pF		50	60	ns
DC ELECT	RICAL SPECIFICATIONS (Typical values at Ta	= 25°C and VPH = 3.3V, using external 2.5V LDO)				
ldd_a	Supply Current (Active mode)		50	100	160	μΑ
ldd_i	Supply Current (Idle mode)		20	60	120	μΑ
Idd_ael	Supply Current (Active mode)	— When using an ext. 2.5V LDO	20	70	140	μΑ
ldd_iel	Supply Current (Idle mode)	Whom doing an oxt. 2.5V LDO	15	40	100	μΑ
Idd_aeo	Supply Current (Active mode)	When using ext. LDO and ext. Clock	15	60	125	μΑ
Idd_ieo	Supply Current (Idle mode)	Whom doing out. 200 and out. Glook	10	30	80	μΑ
ldd_s	Supply Current (Sleep mode)			0.1	1	μΑ
Vil	Digital Input Low Voltage				0.7	V
Vih	Digital Input High Voltage		0.8 x VPH			V
Vol	Digital Output Low Voltage				0.6	V
Voh	Digital Output High Voltage		VPH – 0.5			V
VIdo	Internal LDO Output Voltage		2.3	2.5	3.0	V
Ildo	Internal LDO Driving Current				20	mA
ldr	DIO Sourcing Current				2	mA
lds	DIO Sinking Current				16	mA
Tru	LED Ramp Up Time		400		6200	ms
Trd	LED Ramp Down Time		400		6200	ms

#### **Operation Principles**

#### **Touch Detection**

The FMA1125DC includes the Impedance Change Detection engine\* within the device, which detects impedance differences between the reference input and the sensor input.

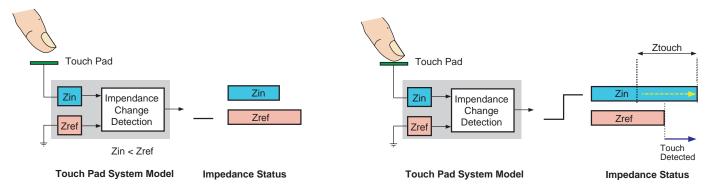


Figure 1: When a Pad is Not Touched.

Figure 2: When a Pad is Touched.

As shown in Figure 1, if the pad is not touched, the impedance of the sensor input Zin should be kept less than the impedance of the reference Zref. If the pad is touched, as shown in Figure 2, Zin is increased by Ztouch. When Ztouch, by touching, becomes greater than the difference of Zin and Zref in the not touched state, i.e., if Zin in touched state becomes greater than Zref by a value higher than 0.1pF, the ICD (Impedance Change Detection) engine within the chip generates the acknowledged output signal indicating it senses the touch.

IDC = 
$$\begin{cases} 1, & \text{if } Zin - Zref > 0.1pF \\ 0, & \text{otherwise} \end{cases}$$

Notice that a value of 0.1pF or higher is needed to maintain stable output against various noises. The sensor input impedance, Zin, includes parasitic capacitance of the input line, tuning capacitance of the input pin and on-chip input impedance, while Zref includes on-chip impedance, AIC control values and external tuning capacitance if necessary.

### **AICTM** (Automatic Impedance Calibration)

The AIC\* function maintains consistent sensitivity against external environmental changes such as temperature, supply voltage/current, humidity, and system-level variations. This helps users to develop their applications more conveniently by providing the actual impedance value of each sensor input. For developers, a Tuning Viewer program is provided, which helps to optimize PCB design and to decide AIC input parameters. More detailed information is available in the FMA1125DC Tuning Guide.

The ICD engine residing in the FMA1125DC controls reference impedance values for each sensor input pin by acquiring each input's impedance data. It periodically updates all reference values under the condition that all touch pads remain in no-touched status. This auto-calibration function absorbs environmental changes and guarantees product stability.

### **APIS**<sup>TM</sup> Touch Output

When touch pads are arranged too closely to each other, it is sometimes difficult to identify which pad is touched. APIS<sup>TM</sup> (Adjacent Pattern Interference Suppression) is a filtering function that identifies which pads are intentionally touched. If APIS mode is not defined, all touch data without APIS filtering are transmitted to the MCU. For example, if the application is a numeric keypad, the user can use APIS mode 1 to get the strongest output and filter out all other weakly touched inputs. Without APIS, the host may have to do this filtering function thus APIS reduces the burden of the host's computing time.

<sup>\*</sup>Proprietary technology of ATLab, Inc.

There are three modes in APIS:

**APIS mode 1**: Reports the strongest output only (Figure 3).

APIS mode 2: Reports all outputs that exceeds pre-defined thresholds (value of Strength Threshold register) (Figure 4).

APIS mode 3: Reports two strongest outputs (suitable for multi-touch applications) (Figure 5).

All three modes are described in the Figures below. The red-colored circles and bars show the output.

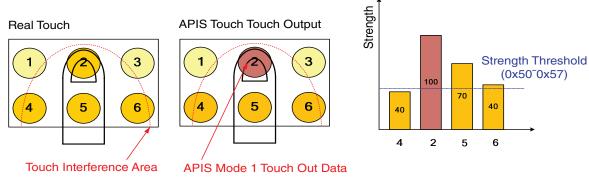


Figure 3: Operation of APIS Mode 1

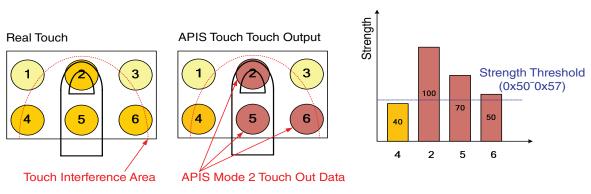


Figure 4: Operation of APIS Mode 2

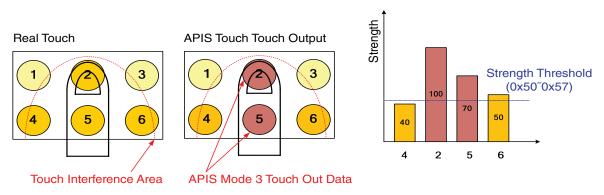


Figure 5: Operation of APIS Mode 3

# FMA1125DC

### **Functional Characteristics**

System Clock	Sensor Clock	Active to Idle	Idle to Active	Active to Sleep	Idle to Sleep	Sleep to Active
1.6MHz	20kHz	0.25 x A sec	Min. 2ns, Max. 10ms	1ns	1ns	10µs
1.6MHz	10kHz	0.5 x A sec	Min. 2ns, Max. 20ms	1ns	1ns	10µs
800kHz	10kHz	0.5 x A sec	Min. 2ns, Max. 20ms	1ns	1ns	10µs
800kHz	5kHz	1 x A sec	Min. 2ns, Max. 40ms	1ns	1ns	10µs
400kHz	5kHz	1 x A sec	Min. 2ns, Max. 40ms	1ns	1ns	10µs
400kHz	2.5kHz	2 x A sec	Min. 2ns, Max. 80ms	1ns	1ns	10µs
200kHz	2.5kHz	2 x A sec	Min. 2ns, Max. 80ms	1ns	1ns	10µs
200kHz	1.25kHz	4 x A sec	Min. 2ns, Max. 160ms	1ns	1ns	10µs

A = IDLE Time Register Value

### Communication Specifications for I<sup>2</sup>C

Table 1: DC Electrical Specifications for I<sup>2</sup>C Bus

Cumbal	Downwater	Standard-Mode		Fast-	lle!4	
Symbol	Parameter	Min.	Max.	Min.	Max	Unit
	LOW Level Input Voltage:					
$V_{IL}$	Fixed Input Levels	-0.5	1.5	n/a	n/a	V
	V <sub>DD</sub> Related Input Levels	-0.5	$0.3\ V_{DD}$	-0.5	$0.3 \times V_{DD}(1)$	V
	HIGH Level Input Voltage:					
$V_{IH}$	Fixed Input Levels	3.0	(2)	n/a	n/a	V
	V <sub>DD</sub> Related Input Levels	$0.7 \times V_{DD}$	(2)	$0.7 \times V_{DD}$	(2)	V
	Hysteresis of Schmitt Trigger Inputs:					
$V_{hys}$	$V_{DD} > 2V$	3.0	(2)	n/a	n/a	V
	$V_{DD} < 2V$	$0.7 \times V_{DD}$	(2)	$0.7 \times V_{DD}$	(2)	V
	LOW Level Output Voltage (open drain or collector) at 3mA Sink Current:					
$V_{OL1}$	V <sub>DD</sub> > 2V	0	0.4	0	0.4	V
$V_{0L3}$	$V_{DD} < 2V$	n/a	n/a	0	$0.2 \times V_{DD}$	V
t <sub>of</sub>	Output Fall Time from V <sub>IHmin</sub> to V <sub>ILmax</sub> with a Bus Capacitance from 10pF to 400pF		250(4)	20 + 0.1C <sub>b</sub> (3)		ns
t <sub>sp</sub>	Pulse Width of Spike Which Must be Suppressed by the Input Filter	n/a	n/a	0	50	ns
l <sub>i</sub>	Input Current Each I/O Pin with an Input Voltage Between 0.1V <sub>DD</sub> and 0.9V V <sub>DDmax</sub>	-10	10	-10(5)	10 <sup>(5)</sup>	μА
C <sub>i</sub>	Capacitance for Each I/O Pin		10		10	pF

#### Note:

5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if  $V_{DD}$  is switched off.

n/a = not applicable

<sup>1.</sup> Devices that use non-standard supply voltages which do not conform to the intended I<sup>2</sup>C bus system levels must relate their input levels to the  $V_{DD}$  voltage to which the pull-up resistors  $R_p$  are connected.

<sup>2.</sup> Maximum  $V_{IH} = V_{DDmax} + 0.5V$ .

<sup>3.</sup>  $C_b$  = capacitance of one bus line in pF.

<sup>4.</sup> The maximum t<sub>f</sub> for the SDA and SCL bus lines quoted in Table 2 (300ns) is longer than the specified maximum t<sub>of</sub> for the output stages (250ns). The allows series protection resistors (R<sub>S</sub>) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Figure 6 without exceeding the maximum specified for t<sub>f</sub>.

Table 2. AC Electrical Specifications for I<sup>2</sup>C Bus

Cumbal	Parameter -	Standar	d-Mode	Fast-M	Hait	
Symbol	ratatileter -	Min.	Max.	Min.	Max	Unit
f <sub>SCL</sub>	SCL Clock Frequency	0	100	0	400	kHz
t <sub>HD:STA</sub>	Hold Time (repeated) START Condition. After this Period, the First Clock Pulse is Generated	4.0		0.6		μѕ
t <sub>LOW</sub>	LOW Period of the SCL Clock	4.7		1.3		μs
t <sub>HIGH</sub>	HIGH Period of the SCL Clock	4.0		0.6		μs
t <sub>SU:STA</sub>	Setup Time for a Repeated START Condition	4.7		0.6		μѕ
t <sub>HD:DAT</sub>	Data Hold Time: For CBUS Compatible Master For I <sup>2</sup> C Bus Devices	5.0 2 <sup>(2)</sup>	- 3.45 <sup>(3)</sup>	_ 0(2)	0.9(3)	μs μs
t <sub>SU:DAT</sub>	Data Setup Time	250		100(4)		ns
t <sub>r</sub>	Rise Time of Both SDA and SCL Signals		1000	20 + 0.1C <sub>b</sub> (5)	300	ns
t <sub>f</sub>	Fall Time of Both SDA and SCL Signals		300 20 + 0.1C <sub>b</sub> (5) 300		300	ns
t <sub>SU:STO</sub>	Setup Time for STOP Condition	4.0		0.6		μs
f <sub>BUF</sub>	Bus Free Time Between a STOP and START Condition	4.7		1.3		μs
C <sub>b</sub>	Capacitive Load for Each Bus Line		400		40	pF
$V_{nL}$	Noise Margin at the LOW Level for Each Connected Device (including Hysteresis)	0.1 x V <sub>DD</sub>		0.1 x V <sub>DD</sub>		V
$V_{nH}$	Noise Margin at the HIGH Level for Each Connected Device (including Hysteresis)	0.2 x V <sub>DD</sub>	0.2 x V <sub>DD</sub>		V	

- 1. All values referred to  $V_{IHmin}$  and  $V_{ILmax}$  levels (see Table 1).
- 2. A device must internally provide a hold time of all least 300ns for the SDA signal (referred to the  $V_{IHmin}$  of the SCL signal) to bridge the undefined regions of the falling edge of SCL.
- 3. The maximum  $t_{HD:DAT}$  has only to be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal.
- 4. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement  $t_{SU:DAT}$  Š 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{max} + t_{SU:DAT} = 1,000 + 250 = 1,250$ ns (according to the Standard-mode I2C bus specification) before the SCL line is released.
- 5.  $C_b$  = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according the Table 2 are allowed. n/a = not applicable.

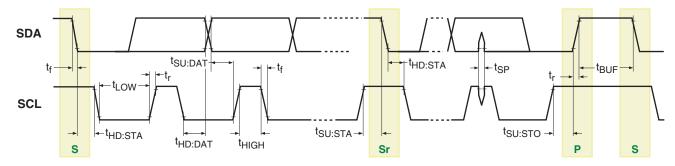
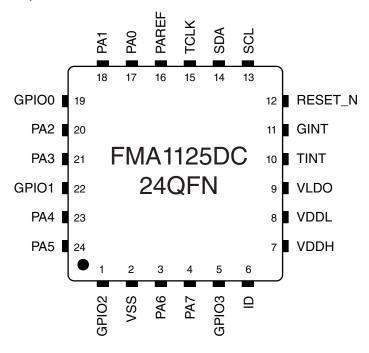


Figure 6: Definition of Timing for F/S-mode Devices on the I<sup>2</sup>C-Bus

### **Application Information**

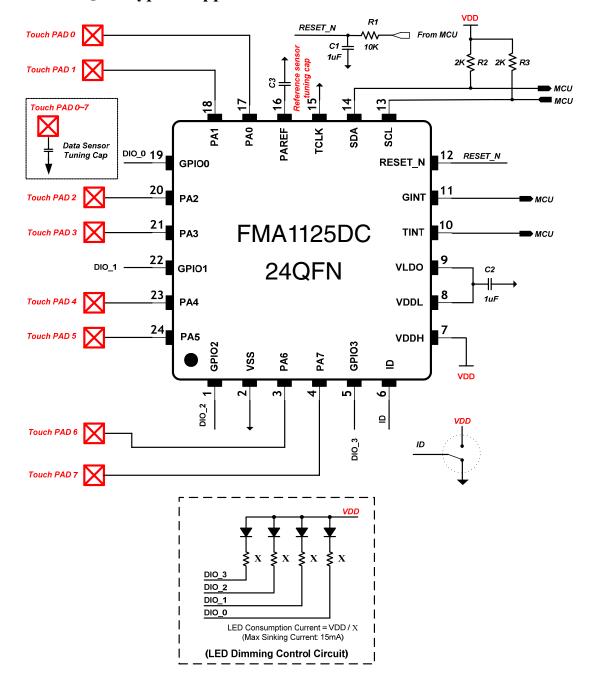
24-pin Package (24QFN)



#### **Pin Description**

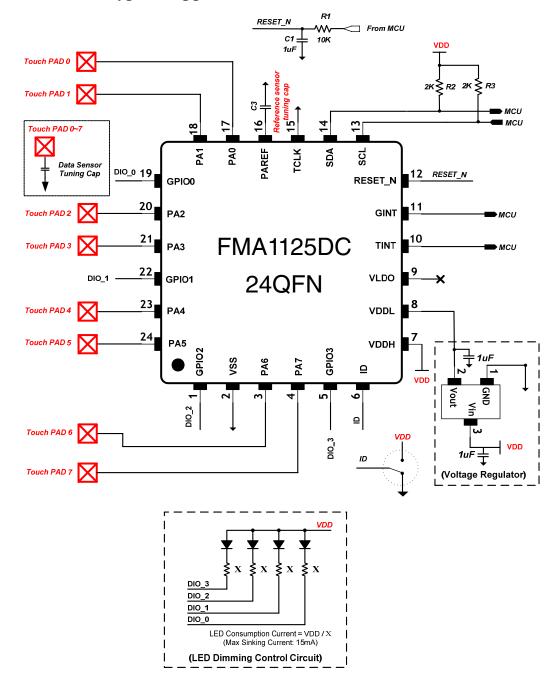
Name	Ю	Pin #	Description
RESET_N	I	15	Reset, active LOW
TCLK	I	18	Test Clock Input
PA	10	20, 21, 23, 24, 2, 3, 6, 7	Eight Sensor Inputs or DIOs configured by the host MCU:  DIOs also can be configured as extended GPIOs, Direct Touch outputs or External Interrupt Inputs.  PA1~PA3 are capable of LED dimming control.
PAREF	I	19	Reference input
GPI0	10	4	Four DIOs configured by the host MCU:  • as Extended GPIOs, Direct Touch Outputs or External Interrupt inputs.  • GPIO0~GPIO3 are capable of LED dimming control.
SDA	10	17	Bidirectional I <sup>2</sup> C Data from/to Host
SCL	I	16	I2C CLK from Host
TINT	0	13	Touch Interrupt generated only when touch status is changed.
GINT	0	14	General Interrupts including touch interrupt (TINT) and external interrupts. They can be masked by the host MCU.
VDDH	Р	10	Power (2.3V–5.5V)
VDDL	Р	11	2.5V Power Input
VLD0	Р	12	2.5V Regulator Power Output
VSS	Р	2	Ground

#### FMA1125DC 24QFN Typical Application Circuit: Internal LDO



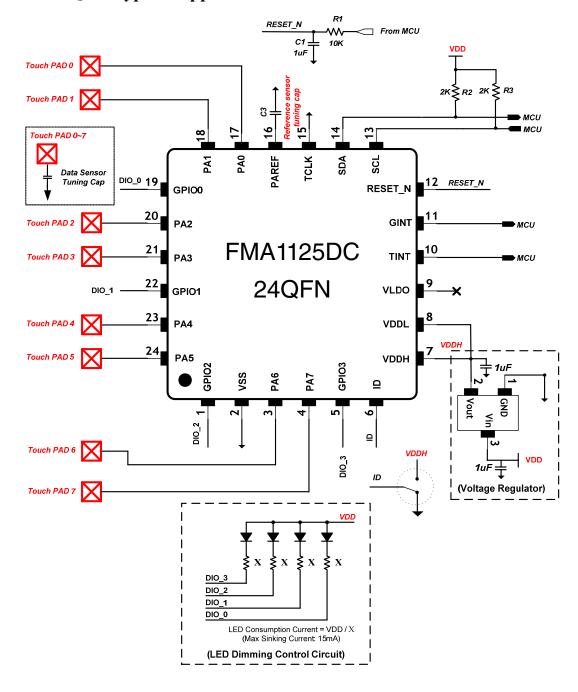
- The voltage range of VDDH can be from 2.5V to 5V.
- 2k¾ pull-up resistors are required for I2C communication.
- PA0 ~ PA7 can be configured as either touch input channels or DIO ports.
- ID selects I<sup>2</sup>C chip ID of the FMA1125DC. When ID is '0', chip ID is 0x68. Otherwise, chip ID is 0x69.
- For LED dimming control through DIO ports, sink current circuit is mandatory as shown above.
- When PA ports are configured as DIO and used for LED dimming control, the circuit should be the same as DIO ports explained above.

#### FMA1125DC 24QFN Typical Application Circuit: External LDO Case 1



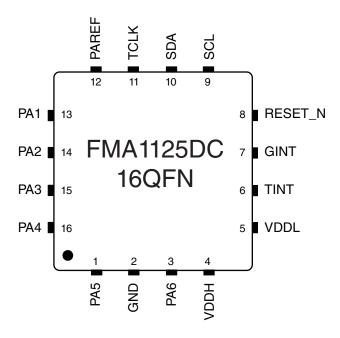
- The voltage range of VDDH can be from 2.5V to 5V.
- 2k¾ pull-up resistors are required for I<sup>2</sup>C communication.
- PA0 ~ PA7 can be configured as either touch input channels or DIO ports.
- ID selects I<sup>2</sup>C chip ID of the FMA1125DC. When ID is '0', chip ID is 0x68. Otherwise, chip ID is 0x69.
- For LED dimming control through DIO ports, sink current circuit is mandatory as shown above.
- When PA ports are configured as DIO and used for LED dimming control, the circuit should be the same as DIO ports explained above.

#### FMA1125DC 24QFN Typical Application Circuit: External LDO Case 2



- The voltage range of VDDH can be from 2.5V to 5V.
- 2k¾ pull-up resistors are required for I<sup>2</sup>C communication.
- PA0 ~ PA7 can be configured as either touch input channels or DIO ports.
- ID selects I<sup>2</sup>C chip ID of the FMA1125DC. When ID is '0', chip ID is 0x68. Otherwise, chip ID is 0x69.
- For LED dimming control through DIO ports, sink current circuit is mandatory as shown above.
- When PA ports are configured as DIO and used for LED dimming control, the circuit should be the same as DIO ports explained above.

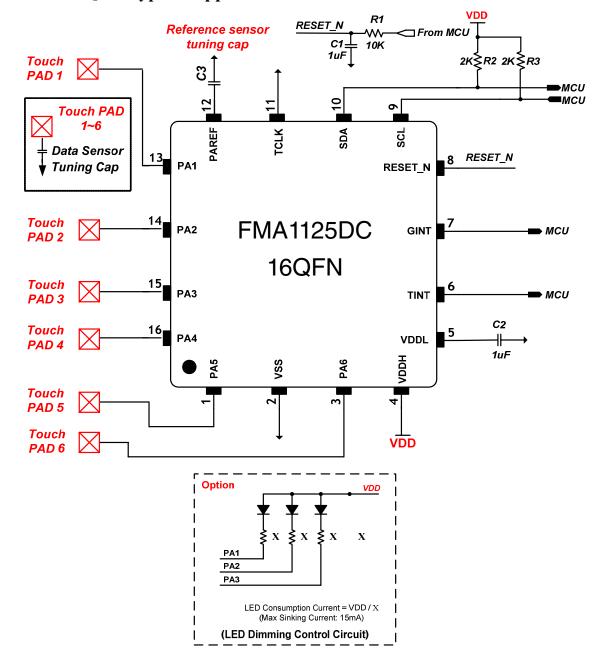
#### 16-pin Package (16QFN)



#### **Pin Description**

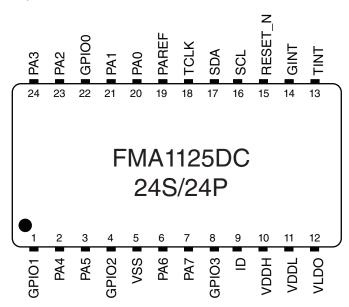
Name	10	Pin #	Description
RESET_N	I	8	Reset, active LOW
TCLK	I	11	Test Clock Input
PA	10	13, 14, 15, 16, 1, 3	Six Sensor Inputs or DIOs configured by the host MCU:  • DIOs also can be configured as extended GPIOs, Direct Touch outputs or External Interrupt Inputs.  • PA1~PA3 are capable of LED dimming control.
PAREF	I	12	Reference input
SDA	10	10	Bidirectional I <sup>2</sup> C Data from/to Host
SCL	ļ	9	I <sup>2</sup> C CLK from Host
TINT	0	6	Touch Interrupt generated only when touch status is changed.
GINT	0	7	General Interrupts including touch interrupt (TINT) and external interrupts. They can be masked by the host MCU.
VDDH	Р	4	Power (2.3V–5.5V)
VDDL	Р	5	2.5V Power Input
VSS	Р	2	Ground

#### FMA1125DC 16QFN Typical Application Circuit: Internal LDO



- The voltage range of VDDH can be from 2.5V to 5V.
- 2k¾ pull-up resistors are required for I2C communication.
- PA1 ~ PA6 can be configured as either touch input channels or DIO ports.
- I<sup>2</sup>C chip ID is fixed to 0x68.
- For LED dimming control through DIO ports, sink current circuit is mandatory as shown above.
- When PA ports are configured as DIO and used for LED dimming control, the circuit should be the same as DIO ports explained above.
- For External LDO connection, please refer to Case 1 and Case 2 in 24QFN's External LDO connections.

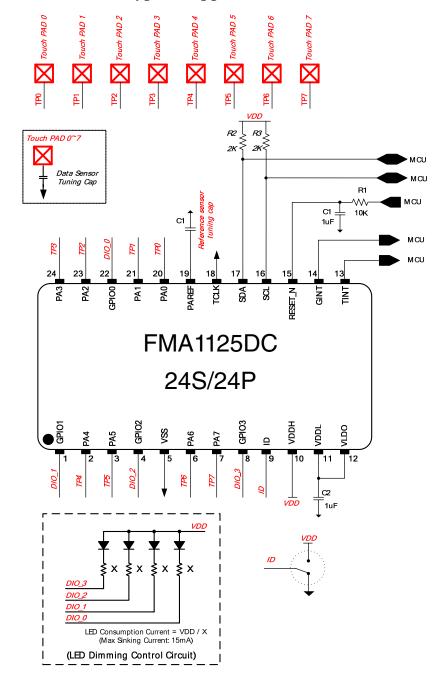
#### 24-pin Package (24SSOP)



#### **Pin Description**

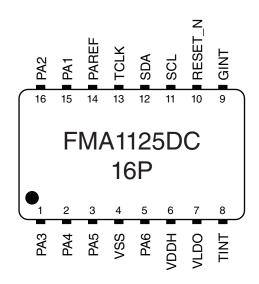
Name	10	Pin #	Description
RESET_N	I	15	Reset, active LOW
TCLK	I	18	Test Clock Input
			Eight Sensor Inputs or DIOs configured by the host MCU:
PA	10	20, 21, 23, 24, 2, 3, 6, 7	• DIOs also can be configured as extended GPIOs, Direct Touch outputs or External Interrupt Inputs.
			<ul> <li>PA1~PA3 are capable of LED dimming control.</li> </ul>
PAREF	I	19	Reference input
			Four DIOs configured by the host MCU:
GPI0	10	4	• as Extended GPIOs, Direct Touch Outputs or External Interrupt inputs.
			GPI00~GPI03 are capable of LED dimming control.
SDA	10	17	Bidirectional I <sup>2</sup> C Data from/to Host
SCL	I	16	I <sup>2</sup> C CLK from Host
TINT	0	13	Touch Interrupt generated only when touch status is changed.
GINT	0	14	General Interrupts including touch interrupt (TINT) and external interrupts. They can be masked by the host
GINI	0	14	MCU.
VDDH	Р	10	Power (2.3V–5.5V)
VDDL	Р	11	2.5V Power Input
VLD0	Р	12	2.5V Regulator Power Output
VSS	Р	2	Ground

#### FMA1125DC 24SSOP / 24SOP Typical Application Circuit: Internal LDO



- The voltage range of VDDH can be from 2.5V to 5V.
- 2k¾ pull-up resistors are required for I<sup>2</sup>C communication.
- ~ PA7 can be configured as either touch input channels or DIO ports.
- ID selects I<sup>2</sup>C chip ID of the FMA1125DC. When ID is '0', chip ID is 0x68. Otherwise, chip ID is 0x69.
- For LED dimming control through DIO ports, sink current circuit is mandatory as shown above.
- When PA ports are configured as DIO and used for LED dimming control, the circuit should be the same as DIO ports explained above.

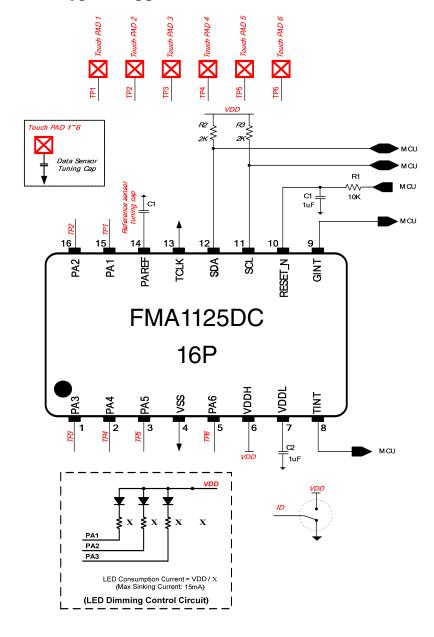
#### 16-pin Package (16SOP)



#### **Pin Description**

l I	10 13	Reset, active LOW
I	13	
		Test Clock Input
		Six Sensor Inputs or DIOs configured by the host MCU:
10	1, 2, 3, 5, 15, 16	DIOs also can be configured as extended GPIOs, Direct Touch outputs or External Interrupt Inputs.
		PA1~PA3 are capable of LED dimming control.
I	14	Reference input
10	12	Bidirectional I <sup>2</sup> C Data from/to Host
I	11	I <sup>2</sup> C CLK from Host
0	8	Touch Interrupt generated only when touch status is changed.
0	9	General Interrupts including touch interrupt (TINT) and external interrupts. They can be masked by the host MCU.
Р	6	Power (2.3V-5.5V)
Р	7	2.5V Power Input
Р	2	Ground
	I IO IO IO P P P	I 14 IO 12 I 11 O 8 O 9 P 6 P 7

#### FMA1125DC 16SOP Typical Application Circuit: Internal LDO



- The voltage range of VDDH can be from 2.5V to 5V.
- 2k¾ pull-up resistors are required for I<sup>2</sup>C communication.
- PA1 ~ PA6 can be configured as either touch input channels or DIO ports.
- I<sup>2</sup>C chip ID is fixed to 0x68.
- For LED dimming control through DIO ports, sink current circuit is mandatory as shown above.
- When PA ports are configured as DIO and used for LED dimming control, the circuit should be the same as DIO ports explained above.
- For External LDO connection, please refer to Case 1 and Case 2 in 24QFN's External LDO connections.

#### **Power Connection**

There are two methods to supply power to the FMA1125DC. One is to receive V25 core voltage from an internal LDO and the other is to receive core voltage from an external power supply. When using the internal LDO, the LDO should be turned on to Sleep mode, which causes slightly higher power consumption than using an external power supply for V25 core voltage.

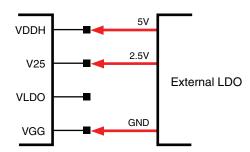
Note on case E below, if VPH receives 2.5V, the internal LDO cannot be used because VLDO cannot output 2.5V when VPH receives 2.5V from the external source.

#### Power Connection Example for 24QFN, 24SSOP and 24SOP

Case A.

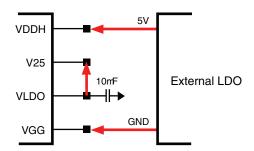
VDDH: External 5V

VLDO: External 2.5V (Internal LDO Off: Register Control)



Case B.

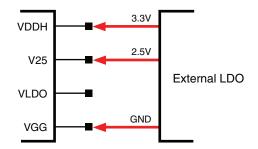
VDDH: External 5V VLDO: Internal LDO 2.5V



Case C.

VDDH: External 3.3V

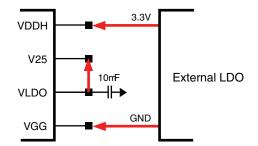
VLDO: External 2.5V (Internal LDO Off: Register Control)



Case D.

VDDH: External 3.3V

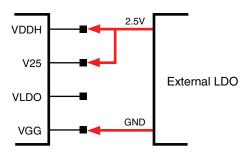
VLDO: Internal LDO 2.5V



Case E.

VDDH: External 2.5V

VLDO: External 2.5V (Internal LDO Off: Register Control)



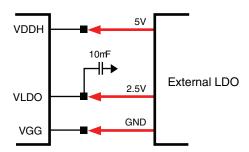
**Confidentia** 

#### Power Connection Example for 16QFN and 24SOP

Case A.

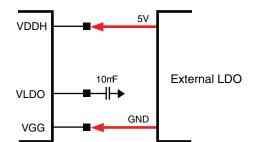
VDDH: External 5V

VLDO: External 2.5V (Internal LDO Off: Register Control)



Case B.

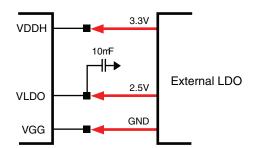
VDDH: External 5V VLDO: Internal LDO 2.5V



Case C.

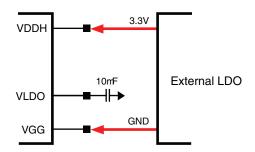
VDDH: External 3.3V

VLDO: External 2.5V (Internal LDO Off: Register Control)



Case D

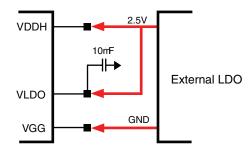
VDDH: External 3.3V VLDO: Internal LDO 2.5V



Case E.

VDDH: External 2.5V

VLDO: External 2.5V (Internal LDO Off: Register Control)



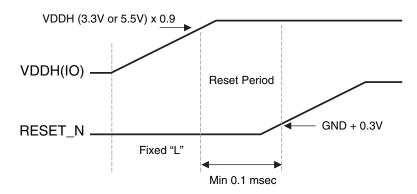
### **Power Sequence**

To initialize the FMA1125DC properly, please refer to the Power Sequence below when the power is given initially during boot-up.

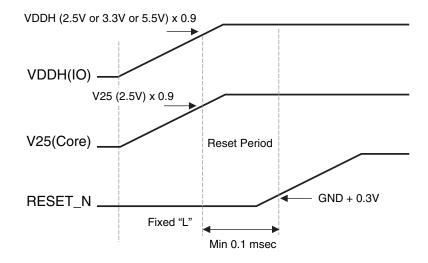
If the reset transition time during power on does not follow the time sequence below, the Internal LDO and oscillator would not operate normally.

The Power Sequence is based on the Power Connection type and is shown in the following example.

#### Power Connection Type is Case B or Case D



#### Power Connection Type is Case A, Case C, or Case E



### **Tuning System**

The tuning system helps the developer tune the target board with various parameters that determine the performance of the target touch board. The tuning system is positioned between the PC and the target touch board (Figure 7). It allows the developer to view all the necessary parameters for tuning and transfers the desired parameters to the FMA1125DC attached on the target touch board.

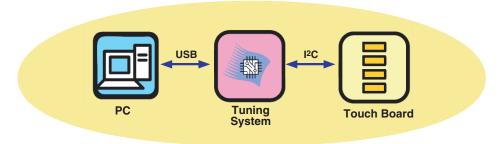


Figure 7: Conceptual Diagram for Tuning System

#### Hardware

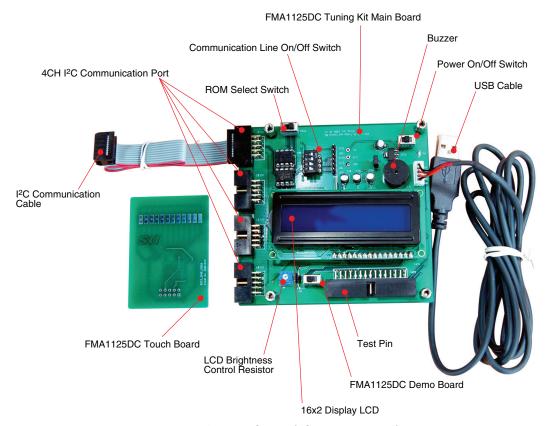


Figure 8: Tuning System (USB Interface Board)

Using this tuning system, the user can send commands to the MCU or receive touch data from the MCU through the USB interface. The MCU on the USB interface board controls the FMA1125DC on the target touch board via the I<sup>2</sup>C interface by reading/writing data to access internal registers in the FMA1125DC.

#### Software

The tuning software installed in the PC will display various parameters that the user can set and monitor. A typical tuning window is shown in Figure 9.

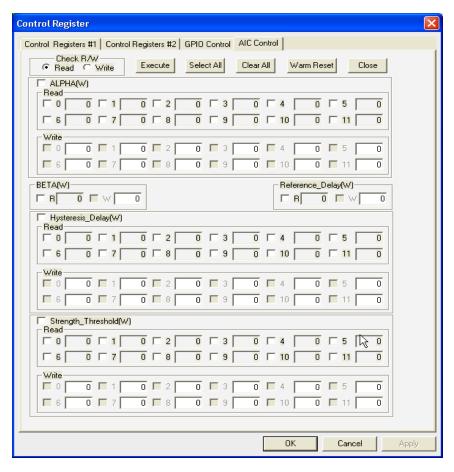
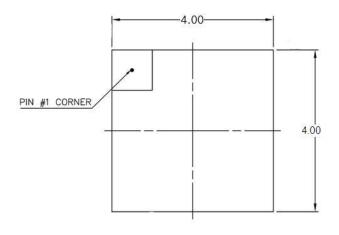


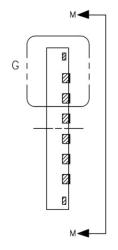
Figure 9: A Typical Parameter Window of Tuning System

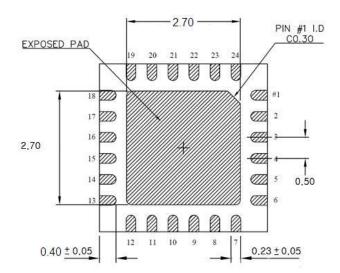
## FMA1125DC

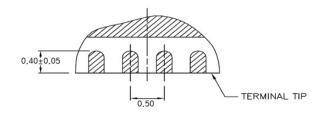
## **Package Dimensions**

### 24QFN

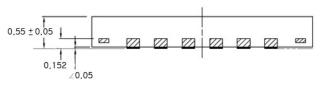






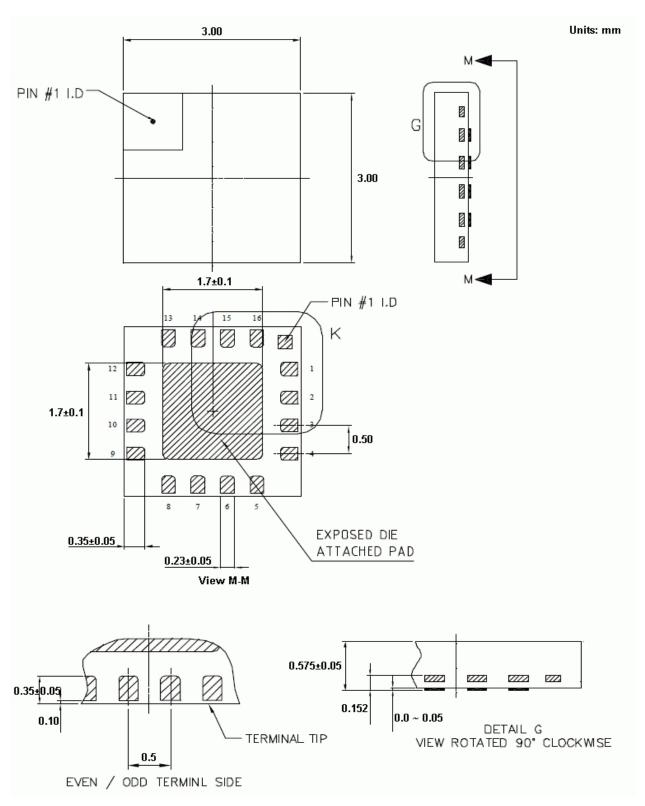


EVEN / ODD TERMINAL SIDE



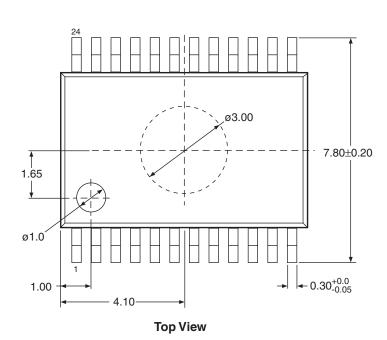
DETAIL G
VIEW ROTATED 90° CLOCKWISE

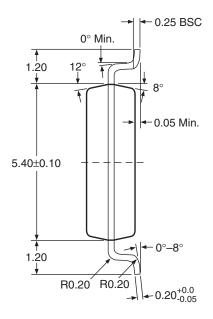
#### **16QFN**



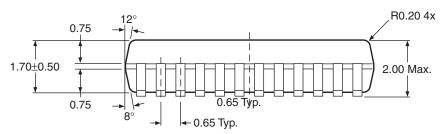
# FMA1125DC

#### **24SSOP**





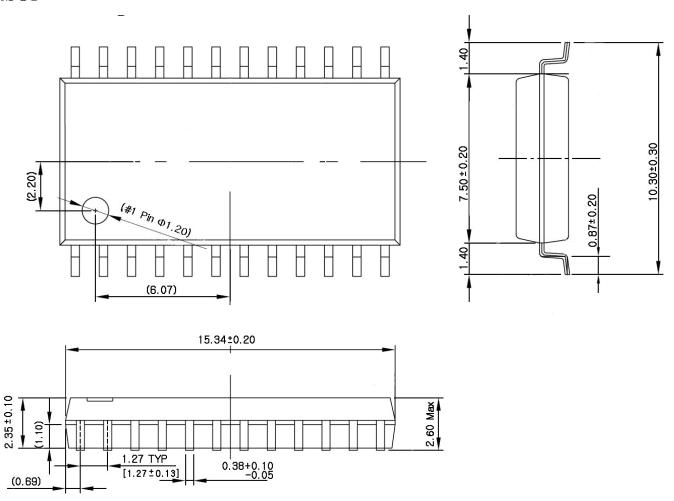
**End View** 



**Side View** 

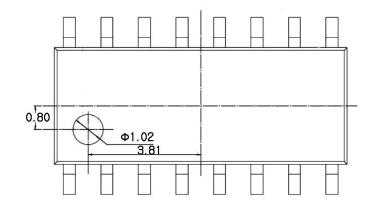
Units: mm

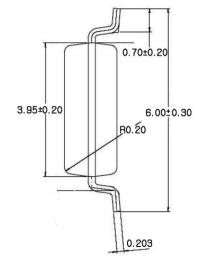
#### **24SOP**

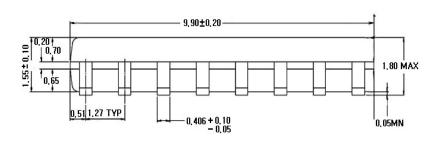


# FMA1125DC

#### **16SOP**







### **Revision History**

Date	Revision	Updates	
April 25, 2009	V1.0	First Release	

The FMA1125DC touch sensor controller is developed and owned by ATLab Inc., South Korea, and is distributed by Fujitsu Microelectronics America, Inc.

Corporate Headquarters
1250 East Arques Avenue, M/S 333, Sunnyvale, California 94085-5401
Tel: (800) 866-8608 Fax: (408) 737-5999
E-mail: inquiry@fma.fujitsu.com Web Site: http://us.fujitsu.com/micro

