AMIS-30585

S-FSK PLC Modem

General Description

The AMIS−30585 is a half duplex S−FSK modem and is dedicated for the data transmission on low− or medium−voltage power lines.

The device offers complete handling of the protocol layers from the physical up to the MAC. AMIS−30585 complies with the EN 50065 CENELEC, IEC 1334−4−32 and the IEC 1334−5−1 standards.

It operates from a single 3.3 V power supply and is interfaced to the power line by an external power driver and transformer. An internal PLL is locked to the mains frequency (50 Hz or 60 Hz) and is used to synchronize the data transmission at data rates of 300, 600 and 1200 baud for a 50 Hz mains frequency, corresponding to 3.6 or 12 data bits per half cycle of the mains frequency (50 Hz or 60 Hz).

Features

- Complies with IEC 1334−5−1 and IEC 1334−4−32
- Suited for 50 Hz or 60 Hz Mains
- Complete Modem for Data Communication on Power Line
- S−FSK Modulation
- Programmable Carrier in the Range of 9 kHz to 95 kHz
- Half Duplex up to 1440 bit/s
- Supports Chorus Transmission
- Programmable Configuration
- Internal ARM Microprocessor
- Serial Communication Interface (SCI) Port
- Low Power, 3 V Operation
- This is a Pb−Free Device*

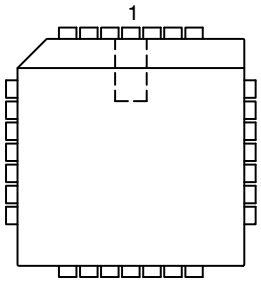
Applications

- IEC1334Utility PLC Modem
- Remote Meter Reading
- Utility Load Controls

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

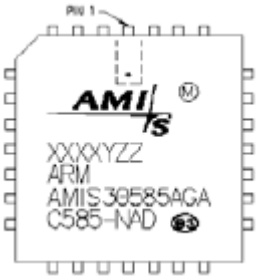
ON Semiconductor®

http://onsemi.com



PLCC 28
A SUFFIX
CASE 776AA

MARKING DIAGRAM



AMIS30585AGA = Specific Device Code
XXXX = Date Code
Y = Plant Identifier
ZZ = Traceability Code
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

December, 2008 − Rev. 2
Publication Order Number:
AMIS−30585/D

ORDERING INFORMATION

Product Name	Ordering Code (Tubes)	Package	Temperature Range
AMIS30585AGA	0C585−002−XTD	PLCC 28 452 G	−25°C to 70°C

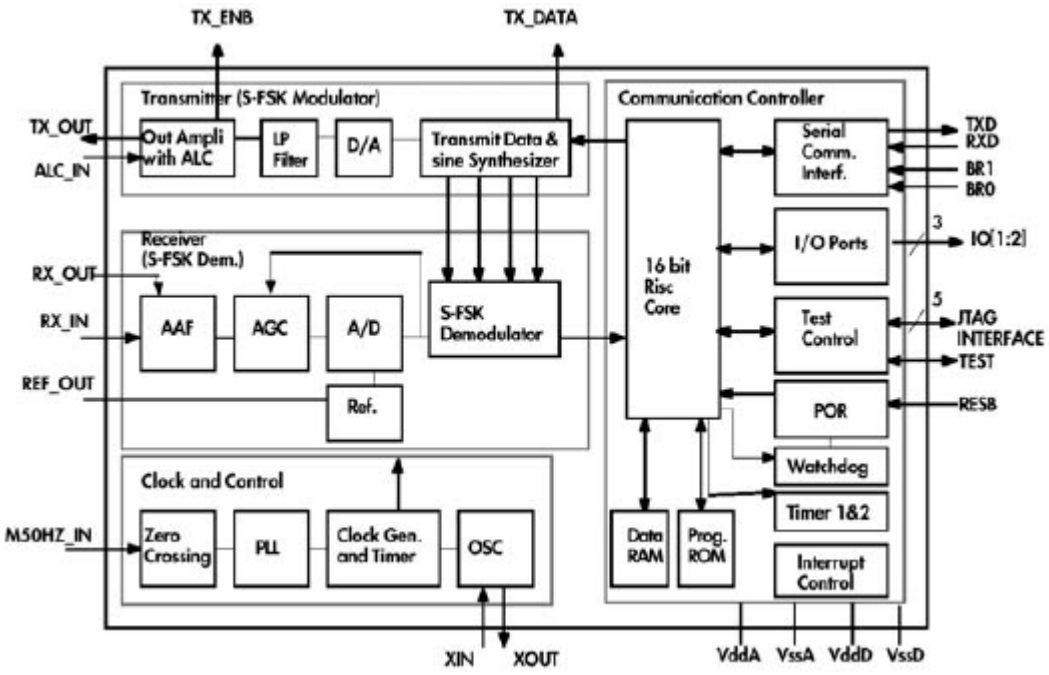


Figure 1. S−FSK Modem AMIS−30585 Block Diagram

Description

The AMIS−30585 is a single chip modem dedicated to power line carrier (PLC) communication in compliance to the European standard IEC 1334−5−1 and IEC 1334−4−32.

S−FSK is a modulation and demodulation technique that combines some of the advantages of a classical spread spectrum system (e.g. immunity against narrow band interferers) with the advantages of the classical FSK system (low complexity). The transmitter assigns the space frequency f_s to “data 0” and the mark frequency f_m to “data 1”. The difference between S−FSK and the classical FSK lies in the fact that f_s and f_m are now placed far from each other, making their transmission quality independent from each other (the strengths of the small interferences and the signal attenuation are both independent at the two frequencies). The frequency pairs supported by the AMIS−30585 are in the range of 9−95 kHz with a typical separation of 10 kHz.

The circuit is mostly digital. The conversion of the analog signal is performed at the front−end of the circuit. The processing of the signal and the handling of the protocol is digital. At the back−end side, the interface to the application is done through a serial interface. The digital processing of the signal is partitioned between hardwired blocks and a microprocessor block. The micro−processor is controlled by firmware. Where timing is most critical, the functions are implemented with dedicated hardware. For the functions where the timing is less critical, typically the higher level functions, the circuit makes use of the ARM 7TDMI microprocessor core.

The processor runs DSP algorithms and, at the same time, handles the communication protocol. The communication protocol, in this application, contains the MAC = Medium Access Control Layer. The program running on the microprocessor is stored into an on−board ROM. The working data necessary for the processing is stored in an internal RAM. For the back−end side, the link to the application hardware, a SCI is provided. The SCI is an easy to use serial interface, which allows communication between an external processor used for the application software and the AMIS−30585 modem. The SCI works on two wires: TXD and RXD. Baud rate is programmed by setting 2 bits (BR0, BR1).

Due to the handling of the low protocol layers in the circuit, the AMIS−30585 provides an innovative architectural split. Thanks to this, the user has the benefit of a higher level interface of the link to the PLC medium. Compared to an interface at the physical level, the AMIS−30585 allows faster development of applications. The user just needs to send the raw data to the AMIS−30585 and no longer has to take care of the protocol detail of the transmission over the specific medium. This last part represents usually 50 percent of the software development costs.

DETAILED BLOCKS DESCRIPTION

Receiver Path Description

The analog signal coming from the line−interface chip is low pass filtered in order to avoid aliasing during the conversion. Then the level of the signal is automatically adapted by an automatic gain control (AGC) block. This operation maximizes the dynamic range of the incoming signal. The signal is then converted to its digital representation using sigma delta modulation. From then on, the processing of the data is done in a digital way. By using dedicated hardware, a direct quadrature demodulation is performed. The signal demodulated in the base band is then low pass filtered to reduce the nose and reject the image spectrum.

Transmitter Path Description

For the generation of the tones, the direct digital synthesis of the sine wave frequencies is performed under the control of the microprocessor. After a signal conditioning step, a digital to analog conversion is performed. As for the receive path, a sigma delta modulation technique is used. In the analog domain, the signal is low pass filtered, in order to remove the high frequency quantization noise, and passed to the automatic level controller (ACL) block, where the level of the transmitted signal can be adjusted. The determination of the signal level is done through the sense circuitry.

Communication Controller

The communication channel is controlled by an embedded microcontroller. The processor uses the ARM reduced instruction set computer (RISC) architecture optimized for IO handling. For most of the instructions, the machine is able to perform one instruction per clock cycle. The microcontroller contains the necessary hardware to implement interrupt mechanisms, timers and is able to perform byte multiplication over one instruction cycle. The microcontroller is programmed to handle the physical layer (chip synchronization), the MAC. The program is stored in a masked ROM. The RAM contains the necessary space to store the working data. The back−end interface is done through the SPI block. This back−end is used for data transmission with the application hardware (concentrator, power meter, etc.) and for the definition of the modem configuration.

Clock and Control

According to the IEC standard, the frame data is transmitted at the zero crossing of the mains voltage. In order to recover the information at the zero crossing, a zero crossing detection of the mains is performed. A phase−locked loop (PLL) structure is used in order to allow a more reliable reconstruction of the synchronization. This PLL permits as well a safer implementation of the “repetition with credit” function (also known as chorus transmission). The clock generator makes use of a precise quartz oscillator master. The clock signals are then obtained by the use of a programmed division scheme. The support circuits are also contained in this block. The support circuits include the necessary blocks to supply the references voltages for the AD and DA converters, the biasing currents and power supply sense cells to generate the right power off and startup conditions.

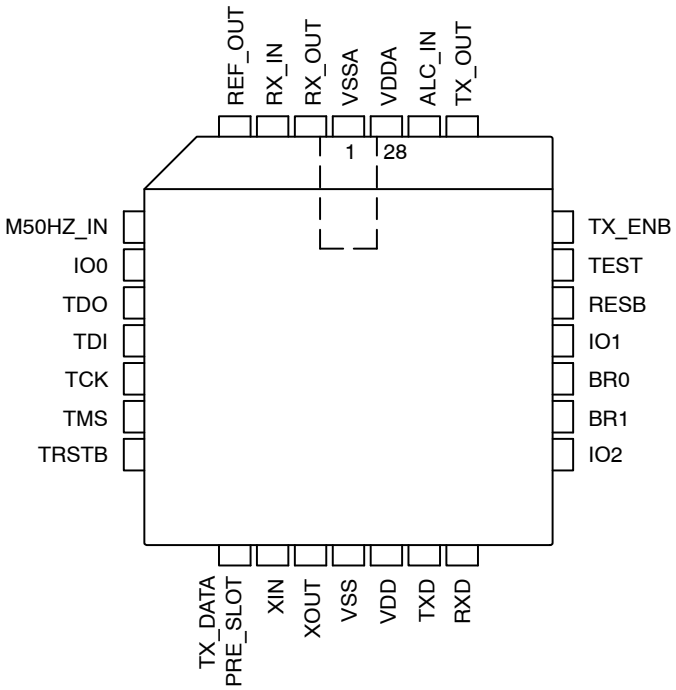


Figure 2. Pin−out of AMIS−30585

Table 1. AMIS−30585 PIN FUNCTIONS

No.	Name	I/O	Type	Description
1	VSSA		P	Analog ground
2	RX_OUT	Out	A	Output of input stage opamp
3	RX_IN	In	A	Positive input of input stage opamp
4	REF_OUT	Out	A	Reference output for stabilization
5	M50HZ_IN	In	A	50.60 Hz input
6	10O	In/Out	D, 5 V Safe	Programmable IO pin (open drain)
7	TDO	Out	D, 5 V Safe	Test data output
8	TDI	In	D, 5 V Safe	Test data output (internal pull down)
9	TCK	In	D, 5 V Safe	Test clock (internal pull down)
10	TMS	In	D, 5 V Safe	Test mode select (internal pull down)
11	TRSTB	In	D, 5 V Safe	Test reset bar (internal pull down, active low)
12	TX_DATA	Out	D, 5 V Safe	Data output corresponding to transmitted frequency
13	XIN	In	A	Xtal input (can be driven by an internal clock)
14	XOUT	Out	A	Xtal output (output floating when XIN driven by external clock)
15	VSS		P	Digital ground
16	VDD		P	3.3 V digital supply
17	TXD	Out	D, 5 V Safe	SCI transmit output (open drain)
18	RXD	In	D, 5 V Safe	SCI receive input (Schmitt trigger output)
19	IO2	In/Out	D, 5 V Safe	Programmable IO pin + interrupt (open drain)
20	BR1	In	D, 5 V Safe	SCI baud rate selection
21	BR0	In	D, 5 V Safe	SCI baud rate selection
22	IO1	In/Out	D, 5 V Safe	Programmable IO pin (open drain)
23	RESB	In	D, 5 V Safe	Master reset bar (Schmitt trigger input, active low)
24	TEST	In	D	Test enable (internal pull down)
25	TX_ENB	Out	D, 5 V Safe	TX enable bar (open drain)
26	TX_OUT	Out	A	Transmitter output
27	ALC_IN	In	A	Automatic level control input
28	VDDA		P	3.3 V analog supply

P: Power pin Out: Output signal
A: Analog pin In: Input signal
D: Digital pin In/Out: Bi−directional pin
5 V Safe: IO that support the presence of 5 V on bus line

Pin 1: VSSA

VSSA is the analog ground supply pin. It is strongly recommended putting a decoupling capacitance between this pin and the VDDA pin. This capacitance value is: 100 nF ±10 percent ceramic. Connection path of the capacitance to the VSSA and VDDA on the PCB should be kept as short as possible in order to minimize the serial resistance.

Pin 2: RX_OUT

RX_OUT is the output analog pin of the receiver low noise input op−amp. This op−amp is in a negative feedback configuration. To know how to use this pin, refer to the explanations given for pin RX_IN.

Pin 3: RX_IN

RX_IN is the positive analog input pin of the receiver low noise input op−amp. Together with the pins two and three, an active high pass filter is realized. This filter removes the main frequency (50 or 60 Hz) from the received signal. The filter characteristics are determined by external capacitors and resistors. Typical values are given in Table 2. For these values and after this filter, a typical attenuation of 80 dB at 50 or 60 Hz is obtained. Table 2 represents external components connection. The present construction supposes the presence of a previous formed with the coupling transformer and a parallel capacitance is placed on the mains. This last one performs a typical attenuation of 60 dB. The combined effect of the two filters decreases the voltage level of the main frequency well below the sensitivity of the AMIS−30585.

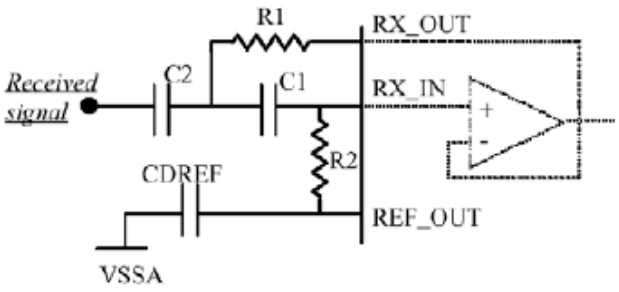


Figure 3. External Component Connection

The goal of the CDREF capacitance is to put the DC voltage of the received signal at the right level for the internal components. See also description of the pin REF_OUT.

Table 2. VALUE OF THE RESISTORS AND CAPACITORS

C1	560 pF
C2	560 pF
R1	82 KW
R2	39 KW
CDREF	1 mF

Pin 4: REF_OUT

REF_OUT is the analog output pin, which provides the voltage reference used by the A/D converter. This pin must be decoupled from the analog ground by a 1 mF ±10 percent ceramic capacitance (CDREF). This must be done as close as possible on the PCB. See Figure 4. It is not allowed to load this pin with other impedance load.

Pin 5: M50HZ_IN

M50HZ_IN is the mains frequency analog input pin − 50 or 60 Hz. This pin is used to detect the crossing of the zero voltage on one selected phase. This information is used, after filtering with the internal PLL, to synchronize frames with the mains frequency. In case of direct connection to the mains, the use of a series resistor of 1 MW is advised in order to limit the current flowing through the protection diodes.

Pin 6, 19 and 22: IO0, IO1 and IO2

IO0, IO1 and IO2 are general−purpose digital input and output pins. Only the IO2 pin is used – this is an input for the chip. All IOs support 5 V level on the bus (5 V safe IO).

When used as outputs, they must be able to deliver the 5 V on the bus if necessary. Outputs are open drain NMOS. The high level is created by opening the internal open drain MOS. The 5 V level is obtained by the use of an external pull−up resistance. Figure 4 gives a representation of a 5 V safe IO. A typical value for the pull−up resistance “RES” is 10 KW. With a larger value for “RES”, the current flowing through this resistance is reduced, hence the switch time from 0 V up to 5 V. IO2 pin is used as T_REQ signal, i.e. the transmission request. So this pin is used as an input pin for the chip in the normal working mode. This signal is used in order to initiate a local communication from the microcontroller to the AMIS−30585. The T_REQ signal is active when low. IO0 and IO1 are assigned to drive external LED. The embedded software defines pin activation.

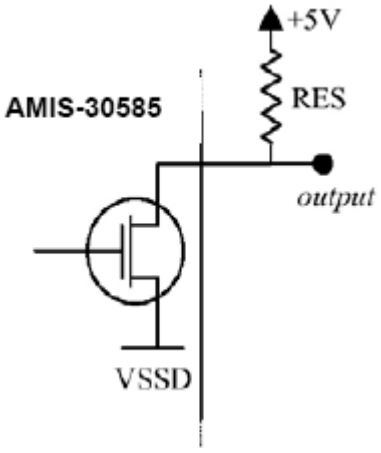


Figure 4. Representation of 5V Safe I/O

Pin 7, 8, 9, 10, and 11: TDO, TDI, TCK, TMS, and TRSTB

All these pins are part of the JTAG bus interface. It will be connected to the ARM ICE interface box. This provides an access to the embedded ARM processor. These pins are used during the debugging of the embedded software. Pin characteristics are in−line with the ARM JTAG interface specification. They will not be described here. Input pins (TDI, TCK, TMS, and TRSTB) contain internal pull−down resistance. TDO is an output. When not in use, the JTAG interface pins may be left floating.

Pin 12: TX_DATA

TX_DATA provides the digital output signal not modulated. It gives the logical level associated with the transmitted frequency. So, to transmit a frequency f_s, the TX_DATA logical state is 0 and is present on TX_DATA. To transmit a frequency f_m, the TX_DATA logical state is 1. This output pin is an open drain. An external pull−up resistance is needed to perform the voltage level associated with a logical one (as for the IOx pins).

Pin 13: XIN

XIN is the analog input pin of the oscillator. It is connected to the interval oscillator inverter gain stage. The clock signal can be created either internally with the external crystal and two capacitors or by connecting an external clock signal to XIN. For the internal generation case, the two external capacitors and crystal are placed as shown in Figure 5. For the external clock connection, the signal is connected to XIN and XOUT is left unused.

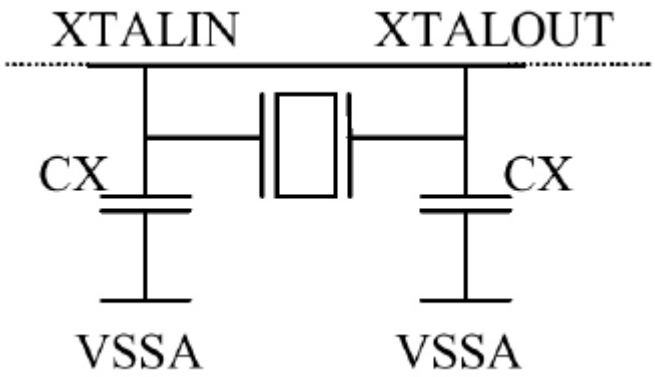


Figure 5. Placement of the Capacitors and Crystal with Clock Signal Generated Internally

The crystal is a classical parallel resonance crystal of 24 MHz. The values of the capacitors CX are given by the manufacturer of the crystal. Typical value is 30 pF. The crystal has to fulfill impedance characteristics specified in the AMIS−30585 data sheet. As an oscillator is sensitive and precise, it is advised to put the crystal as close as possible on the board.

Pin 14: XOUT

XOUT is the analog output pin of the oscillator. When the clock signal is provided from an external generator, this output must be floating. When working with a crystal, this pin cannot be used directly as clock output because no additional loading is allowed on the pin (limited voltage swing).

Pin 15: VSS

VSS is the digital ground supply pin. This pin must be decoupled from the digital supply by a 100 nF ±10 percent ceramic capacitor. It is advised to put this capacitance as close as possible on the PCB.

Pin 16: VDD

VDD is the 3.3 V digital supply pin. This pin must be connected to VSS by a decoupling capacitor (C_DEC) as explained for the pin 15.

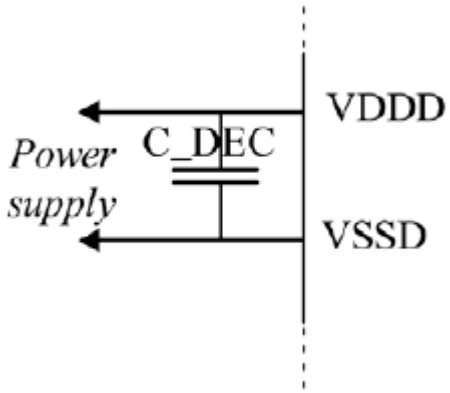


Figure 6. Placement of Decoupling Capacitor

Pin 17: TXD

TXD is the digital output of the asynchronous serial communication (SCI) unit. Only half−duplex transmission is supported. It is used to realize the communication between the AMIS−30585 and the application microcontroller. The TXD is an open drain IO (5 V safe). External pull−up resistances (typically 10 K) are necessary to generate the 5 V level. Refer to Figure 4 for the circuit schematic.

Pin 18: RXD

This is the digital input of the asynchronous SCI unit.

Only half−duplex transmission is supported. This pin supports a 5 V level. It is used to realize the communication between the AMIS−30585 and the application micro−controller. The RXD is a 5 V safe input.

Pin 19: IO2

IO0, IO1 and IO2 are general−purpose digital input and output pins. See Pin 6 for detailed explanation.

Pin 20, 21: BR1, BR0

BR0 and BR1 are digital input pins. They are used to select the baud rate (bits/second) of the SCI unit. The rate is defined according to Table 3. The values are taken into account after a reset, hardware or software. Modification of the baud rate during function is not possible. BR0 and BR1 are 5 V safe.

Table 3. BR1, BR0 BAUD RATES

BR1	BR0	SCI Baud Rate
0	0	4800
0	1	9600
1	0	19200
1	1	38400

Pin 22: IO1

IO0, IO1 and IO2 are general−purpose digital input and output pins. See Pin 6 for detailed explanation.

Pin 23: RESB

RESB is a digital input pin. It is used to perform a hardware reset of the AMIS−30585. This pin supports a 5 V voltage level. The reset is active when the signal is low (0 V).

Pin 24: TEST

TEST is a digital input pin. It is used to enable the test mode of the chip. Normal mode is activated when TEST signal is low (0 V). For normal operation, the TEST pin may be left unconnected. Thank to the internal pull−down, the signal is maintained to low (0 V). TEST pin is not 5 V safe.

Pin 25: TX_ENB

TX_ENB is a digital output pin. It is high when the transmitter is activated. The signal is available to turn on the line driver. TX_ENB is a 5 V safe with open drain output, hence a pull−up resistance is necessary to achieve the requested voltage level associated with a logical one. See also Figure 4 for reference.

Pin 26: TX_OUT

TX_OUT is the analog output pin of the transmitter. The provided signal is the S−FSK modulated frames. A filtering operation must be performed to reduce the second order harmonic distortion. For this purpose an active filter is realized. Figure 7 gives the representation of this filter.

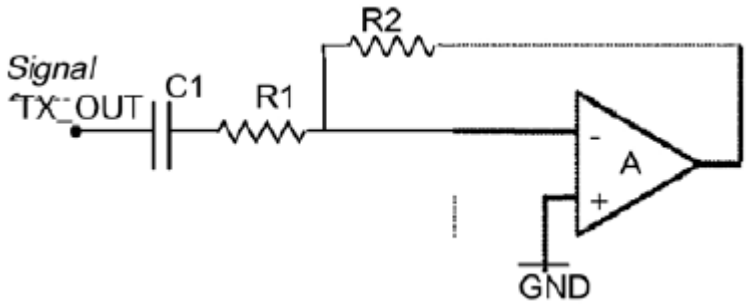


Figure 7. TX_OUT Filter

Pin 27: ALC_IN

ALC_IN is the automatic level control analog input pin. The signal is used to adjust the level of the transmitted signal. The signal level adaptation is based on the AC component. The DC level on the ALC_IN pin is fixed internally to 1.65 V. Comparing the peak voltage of the AC signal with two internal thresholds does the adaptation of the gain. Low threshold is fixed to 0.4 V. A value under this threshold will result in an increase of the gain. The high threshold is fixed to 0.6 V. A value over this threshold will result in a decrease of the gain. The pin must be decoupled from the sensed signal by a 1 mF capacitor. An application example is given in Figure 8. A serial capacitance is used to filter the DC components. The level adaptation is performed during the transmission of the first two bits of a new frame. Eight successive adaptations are performed.

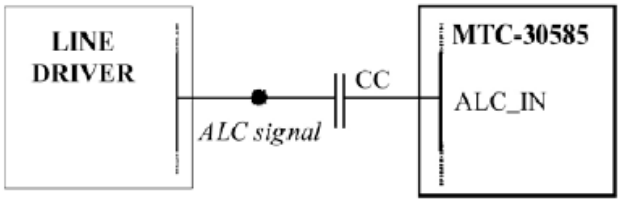


Figure 8. Connection to the Line Driver

Pin 28: VDDA

VDDA is the positive analog supply pin. Nominal voltage supply is 3.3 V. A decoupling capacitor (C_DEC) must be placed between this pin and the VSSA (see pin 1).

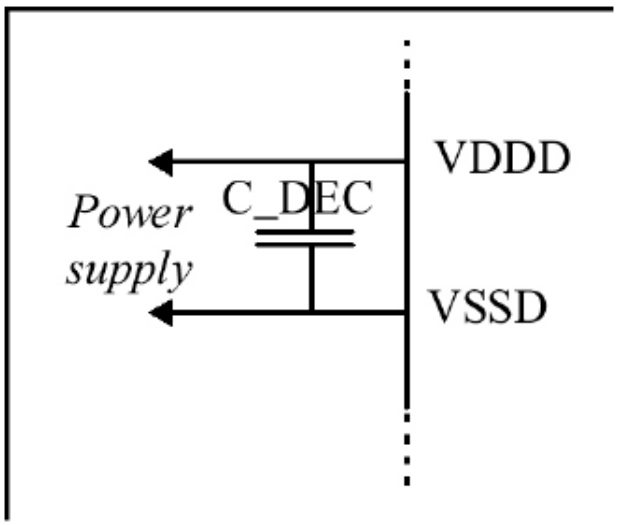


Figure 9. Placement of Decoupling Capacitor

NOTE: The user should take care about difference of ground voltages between different boards. Should ground voltages not be the same, the use of isolation devices is mandatory.

Operating Characteristics

Standard compliance: compliance to IEC 1334−5−1 (SFSK profile) and IEC 1334−4−32.

Main modem characteristics are given in Table 4.

Table 4. OPERATING CHARACTERISTICS

Parameter	Value	Unit
Positive supply voltage Negative supply voltage	3.0 to 3.6 −0.7 to + 0.3	V V
Max peak output level	1, 2	Vp
HD2	060	dB
HD3	−60	dB
ALC Steps	3	dB
ALC Range	(0...−21)	dB
Maximum input signal	1, 15	Vp
Input impedance	100	Kohm
Input sensitivity	0.4	mV
AGC steps	6	dB
AGC range	(0...+42)	dB
Maximum 50 Hz variation	0, 1	Hz/s
Data rate	300/360 (Note 7) 600/720 (Note 7) 1200/1440 (Note 7)	baud baud baud
Programmable carrier (Note 6)		
Frequency band		
Frequency minimum	9	kHz
Frequency maximum	95	kHz
Frequency deviation between pairs	>10	kHz
Dynamic range	40 (Note 1) 60 (Note 2) 80 (Note 3)	dB dB dB
Narrow band interfere BER (Note 4)	10E−5	
Impulsive noise BER (Note 5)	10E−5	

1. FER = 0 percent.
2. FER = 0.3 percent.
3. FER = 8.0 percent.
4. Signal between −60 dB and 0 dB interference signal level is 30 dB above signal level between 20 kHz and 95 kHz.
5. Input at −40 dB, duty cycle between 10 − 50 percent pulse noise frequency between 100 to 1000 Hz. BER: Bit error rate FER: Frame error rate (1 frame is 288 bits)
6. Carriers frequency is programmable by steps of 10 Hz.
7. 60 Hz mains frequency.

BACK−END INTERFACES

Serial Communication Interface (SCI)

The SCI allows asynchronous communication. It can communicate with a UART = Universal Asynchronous Receiver Transmitter, ACIA = Asynchronous Communication Interface Adapter and all other chips that employ standard asynchronous serial communication. The serial communication interface allows only half duplex communication.

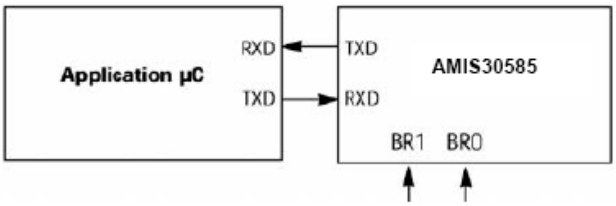


Figure 10. Connection to the Application Microcontroller

SCI Physical Layer Description

The following pins control the serial communication interface.

TXD: Transmit data output. It is the data output of the AMIS−30585 and the input of the base micro.

RXD: Receive data input. It is the data input of the AMIS−30585 and the output of the base micro.

BR0,BR1: Baud rate selection inputs. These pins are externally strapped to a value or controlled by the external base microcontroller.

Table 5. BR1, BR0 BAUD RATES

BR1	BR0	SCI Baud Rate
0	0	4800
0	1	9600
1	0	19200
1	1	38400

Typical External Components

The schematic showing the external components is shown in Figure 4 – a typical application.

Supply Decoupling

For correct functioning the VDDA and VSSA should be decoupled as close as possible on the PCB by a 100 nF ±10 percent ceramic decoupling capacitor CDA.

For correct functioning the VDD and VSS should be decoupled as close as possible on the PCB by a 100 nF ±10 percent ceramic decoupling capacitor CDD.

For correct functioning the REF_OUT and VSSA should be decoupled as close as possible on the PCB by a 1 µF ±10 percent ceramic decoupling capacitor CDREF.

50/60 Hz Suppression Circuit

A typical attenuation for 50 Hz of this filter is 80 dB. A mains coupling device has a typical attenuation of 60 dB. This brings a mains frequency of 220 V rms well below the sensitivity level. Typical values are shown in Table 6.

Oscillator

The oscillator works with a standard parallel resonance crystal of 24 MHz. XIN is the input to the oscillator inverter gain stage and XOUT is the output.

For correct functioning the following external circuit must be connected to the oscillator pins (Values of capacitors are indicative only and are given by the crystal manufacturer. For a crystal requiring a parallel capacitance of 20 pF CX must be around 30 pF.)

To guarantee startup the series loss resistance of the crystal must be smaller than 80 Ω.

The parasitic leakage resistance between XIN and XOUT must be higher than 1 MΩ. The parasitic leakage resistance between XIN and VSS must be higher than 1 MΩ.

When working with a crystal, XOUT cannot be used directly as a clock output because the voltage swing on this pin is limited.

Zero Crossing Detector

The pin M50HZ_IN can be used as a mains zero crossing detector input. If the mains are connected directly to this pin a resistance must be connected in series to limit the current through the protection diodes. Advisable is a series resistor of 1 MΩ (R50). The zero crossing detector output is logic zero when the input is lower than the falling threshold level and a logic one when the input is higher than the rising threshold level.

The falling edges of the output of the zero crossing detector are filtered by a period between 0.5 ms and 1 ms. Rising edges are not filtered.

5 V Safe Output

5 V safe pins are open drain output. The high level is detained by placing a pull up resistance between the output pin and the 5 V supply. Typical resistance value is 10 kΩ. (TXD, TXEN3, TX_DTATA)

Table 6. TYPICAL EXTERNAL COMPONENT VALUES

C11	560	pF
C12	560	pF
R11	82 K	Ω
R12	39 K	Ω
C20	1	μF

Configuration

Configuration is loaded through the SCI interface from the application controller.

- Mains frequency 50/60 Hz
- Master/slave/monitor/initialization configuration
- Baud rate selection 300/600/1200

Baud for 50 Hz mains

- Baud rate selection 360/720/1440

Baud for 60 Hz mains

- Carrier frequency programmation
- Carrier frequency spread

Configuration method and utilization are described in the AMIS−30585 data book, user interface documentation.

Application Example

A typical application example is given below. The example shows the AMIS−30585 with its companion devices. Namely the power line driver (AMIS−3058), the application controller and a meter device interface.

Between the modem chip and the line driver, an active bandpass filter is used to reduce the noise outside the transmission band. The filter is realized with external passive components.

From the line driver, the connection to the mains is done through a line transformer and a capacitive coupling.

From the application side, the interface between the modem and the application is done through the SCI. The link to the meter device will be done easily by using the meter device interface chip. This device is used to realize the physical interface between the controller and the standard S0 pulse (DIN 19234) generator output of the meter device.

C1 = C2 = 325 pF, R1 = 22.6 K, R2 = 2.2 K, R3 = 16.5 K, R4 = 1 K, R5 = 1.66 K.

Other values are given in the typical external components paragraph.

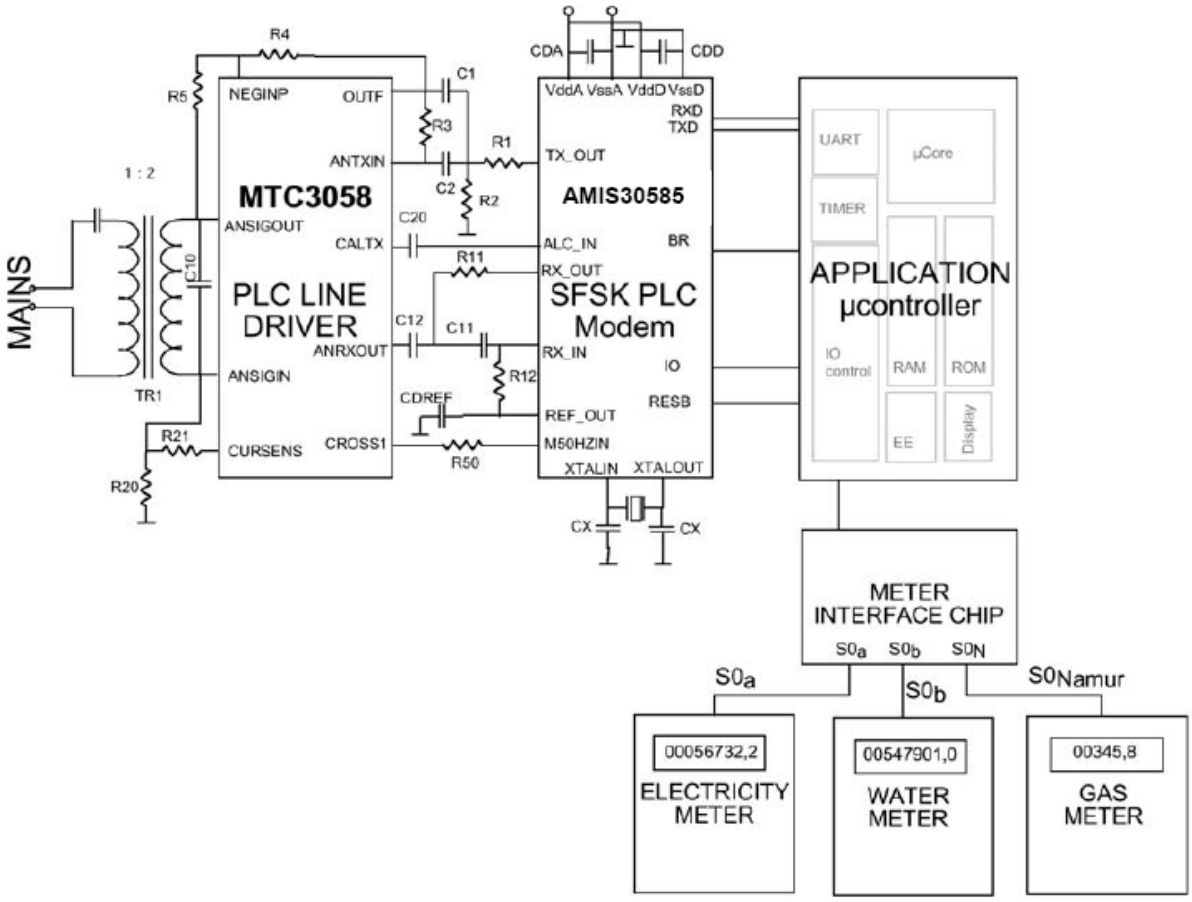


Figure 11. Typical Application for the AMIS−30585 S−FSK Modem

CIRCUIT PERFORMANCE

Nominal Conditions

Ambient temperature:	25°C
Power supply:	3.3 V
Mains frequency:	50 Hz
Crystal frequency fCLK:	24 MHz

Operating Ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device as described in Table 7 and for the reliability specifications as listed in the Block Description section. Functionality outside these limits is not implied.

Total cumulative dwell time outside the normal power supply voltage range or the ambient temperature under bias, must be less than 0.1 percent of the useful life as defined in the Block Description section.

Table 7. OPERATING RANGES

Parameter	Description	Condition	Min.	Max.	Unit
VDD	Power supply voltage range		3.0	3.6	V
T_{amb}	Ambient temperature		−25	70	°C

Oscillator: Pin XIN, XOUT

In production the actual oscillation of the oscillator and duty cycle will not be tested. The production test will be based on the static parameters and the inversion from XIN to XOUT in order to guarantee the functionality of the oscillator.

Table 8. OSCILLATOR

Parameter	Description	Condition	Min.	Max.	Unit
f_{CLK}	Crystal frequency	(Note 8)	24 MHz −100 ppm	24 MHz +100 ppm	
	Duty cycle with quartz connected	(Note 8)	30	70	%
$T_{startup}$	Start−up time	(Note 8)		50	Ms
CL_{XOUT}	Maximum Capacitive load on XOUT	XIN used as clock input		50	pF
VIL_{XOUT}	Low input threshold voltage	XIN used as clock input	−0.3 VDD		V
VIH_{XOUT}	High input threshold voltage	XIN used as clock input		0.7 vdd	V
VOL_{XOUT}	Low output voltage	XIN used as clock input, XOUT = 2 mA		0.3	V
VOH_{XOUT}	High input voltage	XIN used as clock input		VDD−0.3	V

8. For the design of the oscillator crystal parameters have been taken from the data sheet [8]. The series loss resistance for this type of crystal is maximum 50 W. However the oscillator cell has been designed with some margin for series loss resistance up to 80 W.

Table 9. ZERO CROSSING DETECTOR AND 50/60HZ PLL: Pin M50HZ_IN

Parameter	Description	Condition	Min.	Max.	Unit
Imaxp M50HZIN	Maximum peak input current		−20	20	mA
Imaxavg M50HZIN	Maximum average input current during 1 ms		−2	2	mA
V_{MAINS}	Mains voltage (ms) range	With protection resistor at M50HZIN	90	550	V
$VIRM_{50HZIN}$	Rising threshold level	(Note 9)		1.9	V
$VIFM_{50HZIN}$	Falling threshold level	(Note 9)	0.9		V
VHY_{50HZIN}	Hysteresis	(Note 9)	0.4		V
$Flock_{50Hz}$	Lock range for 50 Hz (Note 10)	MAINS_FREQ = 0 (50 Hz)	45	55	Hz
$Flock_{60Hz}$	Lock range for 60 Hz (Note 10)	MAINS_FREQ = 0 (60 Hz)	54	66	Hz
$Tlock_{50Hz}$	Lock time (Note 10)	MAINS_FREQ = 0 (50 Hz)		10	S
$Tlock_{60Hz}$	Lock time (Note 10)	MAINS_FREQ = 0 (60 Hz)		10	S
DF_{60Hz}	Frequency variation without going out of lock (Note 10)	MAINS_FREQ = 0 (50 Hz)		0.1	Hz/s
DF_{50Hz}	Frequency variation without going out of lock (Note 10)	MAINS_FREQ = 0 (60 Hz)		0.1	Hz/s
$Jitter_{CHIP\_CLK}$	Jitter of CHIP_CLK (Note 10)		−60	60	ms

9. Measured relative to VSS.
10. These parameters will not be measured in production since the performance is totally dependent of a digital circuit which will be guaranteed by the digital test patterns.

Transmitter External Parameters: Pin TX_OUT, ALC_IN, TX_ENB

To guarantee the transmitter external specifications the TX_CLK frequency must be 12 MHz # 100 ppm.

Table 10. TRANSMITTER EXTERNAL PARAMETERS

Parameter	Description	Condition	Min.	Max.	Unit
V_{TX_OUT}	Maximum peak output level	fTX_OUT = 50 kHz fTX_OUT = 95 kHz Level control at max. output	0.85 0.76	1.15 1.22	Vp
HD2	Second order harmonic distortion	fTX_OUT = 95 kHz Level control at max. output		−56	dB
HD3	Third order harmonic distortion	fTX_OUT = 95 kHz Level control at max. output		−58	dB
Df_{TX_OUT}	Frequency accuracy of the generated sine wave	(Notes 11 and 13)		30	Hz
CL_{TX_OUT}	Capacitive output load at pin TX_OUT	(Note 11)		20	pF
RL_{TX_OUT}	Resistive output load at pin TX_OUT		5		KΩ
Td_{TX_ENB}	Turn off delay of TX_ENB output	(Note 12)	0.25	0.5	ms

11. This parameter will not be tested in production.
12. This delay corresponds to the internal transmit path delay and will be defined during design.
13. Taking into account the resolution of the DDS and an accuracy of 100 ppm of the crystal.

Table 11. TRANSMITTER EXTERNAL PARAMETERS

Parameter	Description	Condition	Min.	Max.	Unit
ALC_{step}	Automatic level control attenuation step		2.9	3.1	dB
ALC_{range}	Maximum attenuation		20.3	21.7	dB
VTL_{ALC_IN}	Low threshold level on ALC_IN		−0.46	−0.36	V
VTH_{ALC_IN}	High threshold level on ALC_IN		−0.68	−0.54	V
$I_{LE\_ALC\_IN}$	Input leakage current of receiver input		−1	1	mA
$PSRR_{TX\_OUT}$	Power supply rejection ration of the transmitter section		10 (Note 14)	35 (Note 15)	dB

14. A sinusoidal signal of 10 kHz and 100 mV ptp is injected between VDDA and VSSA. The digital AD converter generates an idle pattern. The signal level at TX_OUT is measured to determine the parameter.
15. A sinusoidal signal of 50 Hz and 100 mV ptp is injected between VDDA and VSSA. The digital AD converter generates an idle pattern. The signal level at TX_OUT is measured to determine the parameter.

The LPF filter + amplifier must have a frequency characteristic between the limits listed below. The absolute output level depends on the operating condition. In production the measurement will be done for relative output levels where the 0 dB reference value is measured at 50 kHz with a signal amplitude of 100 mV.

Table 12. TRANSMITTER FREQUENCY CHARACTERISTICS

Frequency (kHx)	Min. (dB)	Max. (dB)
10	−0.5	0.5
95	−1.3	0.5
130	−4.5	−2.0
165		−3.0
330		−18.0
660		−36.0
1000		−50
2000		−50

Table 13. RECEIVER EXTERNAL PARAMETERS: Pin RX_IN, RX_OUT, REF_OUT

Parameter	Description	Condition	Min.	Max.	Unit
VOFFS_RX_IN	Input offset voltage 42 dB	AGC gain = 42 dB		5	mV
VOFFS_RX_IN	Input offset voltage 0 dB	AGC gain = 0 dB		50	mV
$V_{MAX\_RX\_IN}$	Max. peak input voltage (corresponding to 62.5% of the SD full scale)	AGC gain = 0 dB (Note 16)	0.85	1.15	Vp
NF_{RX_IN}	Input referred noise of the analog receiver path	AGC gain = 42 dB (Notes 16 and 17)		150	NV/#Hz
$I_{LE\_RX\_IN}$	Input leakage current of receiver input		−1	1	mA
IMax_REF_OUT	Max. current delivered by REF_OUT		−300	+300	mA
$PSRR_{LPF\_OUT}$	Power supply rejection ratio of the receiver input section	AGC gain = 42 dB	10 (Note 18) 35 (Note 19)		dB
AGC_{step}	AGC gain step		5.7	6.3	dB
AGC_{range}	AGC range		39.9	44.1	dB
V_{REF_OUT}	Analog ground reference output voltage		1.57	1.73	V
SN_{AD_OUT}	Signal to noise ratio at 62.5% of the SD full scale	(Notes 16 and 20)	54		dB
$V_{CLIP\_AGC\_IN}$	Clipping level at the output of the gain stage		1.15	1.65	Vp

16. Input at RX_IN, no other external components.
17. This parameter will be characterized on a limited number of prototypes and will not be tested in production.
18. A sinusoidal signal of 10 kHz and 100 mV ptp is injected between VDDA and VSSA. The signal level at the differential LPF_OUT and REF_OUT output is measured to determine the parameter.
19. A sinusoidal signal of 50 Hz and 100 mV ptp is injected between VDDA and VSSA. The signal level at the differential LPF_OUT output is measured to determine the parameter.
20. These parameters will be tested in production with an input signal of 95 kHz and 1 Vp by reading out the digital samples at the point AD_OUT with the default settings of T_RX_MOD[7], SDMOD_TYP, DEC_TYP, and COR_F_ENA. The AGC gain is switched to 0 dB.

The receive LPF filter + AGC + low noise amplifier must have a frequency characteristic between the limits listed below. The absolute output level depends on the operating condition. In production the measurement will be done for relative output levels where the 0 dB reference value is measured at 50 kHz with a signal amplitude of 100 mV.

Table 14. RECEIVER FREQUENCY CHARACTERISTICS

Frequency (kHx)	Min. (dB)	Max. (dB)
10	−0.5	0.5
95	−1.3	0.5
130	−4.5	−2.0
165		−3.0
330		−18.0
660		−36.0
1000		−50
2000		−50

Table 15. POWER−ON−RESET (POR)

Parameter	Description	Condition	Min.	Max.	Unit
VPOR	POR threshold		1.7	2.7	V
TRPOR	Power supply rise time	0 to 3 V	1		ms

Table 16. DIGITAL OUTPUTS: TDO, CLK_OUT

Parameter	Description	Condition	Min.	Max.	Unit
VOL	Low output voltage	IXOUT = 4 mA		0.4	V
VOH	High output voltage	IXOUT = −4 mA	0.85 VDD		V

Table 17. DIGITAL OUTPUTS WITH OPEN DRAIN: TX_ENB, TXD

Parameter	Description	Condition	Min.	Max.	Unit
VOL	Low output voltage	IXOUT = 4 mA		0.4	V

Table 18. DIGITAL INPUTS: BR0, BR1

Parameter	Description	Condition	Min.	Max.	Unit
VIL	Low input level			0.2 VDD	V
VIH	High input level		0.8 VDD		V
ILEAK	Input leakage current		−10	10	μA

Table 19. DIGITAL INPUTS WITH PULL DOWN: TDI, TMS, TCK, TRSTB, TEST

Parameter	Description	Condition	Min.	Max.	Unit
VIL	Low input level			0.2 VDD	V
VIH	High input level		0.8 VDD		V
RPU	Pull down resistor	(Note 21)	7	50	kΩ

21. Measured around a bias point of VDD/2.

Table 20. DIGITAL SCHMITT TRIGGER INPUTS: RXC, RESB

Parameter	Description	Condition	Min.	Max.	Unit
VT+	Rising threshold level			1.9	V
VT−	Falling threshold level		0.9		V
ILEAK	Input leakage current		−10	1−	uA

Table 21. DIGITAL INPUT/OUTPUTS OPEN DRAIN: IO0, IO1, IO2

Parameter	Description	Condition	Min.	Max.	Unit
VOL	Low output voltage	ICOUT = 4 mA		0.4	V
VIL	Low input level			0.2 VDD	V
VIH	High input level		0.8 VDD		V
ILEAK	Input leakage current		−10	10	μA

Table 22. CURRENT CONSUMPTION

Parameter	Description	Condition	Typ.	Max.	Unit
IRX	Current consumption during receive mode	Current through VDD and VDDA (Note 22)	60	80	mA
ITX	Current consumption during transmit mode	Current through VDD and VDDA (Note 22)	60	80	mA
IRESET	Current consumption when RESB = 0	Current through VDD and VDAA		4	mA

22. CLKARM is < 12 MHz, fCLK = 24 MHz.

Absolute Maximum Ratings and Storage Conditions

Absolute Maximum Ratings

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 23. POWER SUPPLY PINS VDD, VDDA, VSS, VSSA

Parameter	Description	Condition	Min.	Max.	Unit
VDDABXM	Absolute maximum digital power supply		VSS−0.3	3.9	V
VDDAABSM	Absolute maximum analog power supply		VSSA−0.3	3.9	V
VDD−VDDAABSM	Absolute maximum difference between digital and analog power supply		−0.3	0.3	V
VSS−VSSAABSM	Absolute maximum difference between digital and analog ground		−0.3	0.3	V

Table 24. NON 5 V SAFE PINS: TX_OUT, ALC_IN, RX_IN, RX_OUT, REF_OUT, M50HZ_IN, XIN, XOUT, TDO, TDI, TCK, TMS, TRSTB, TEST

Parameter	Description	Condition	Min.	Max.	Unit
VINABSM	Absolute maximum input for normal digital inputs and analog inputs		VSS*−0.3	VDD*+0.3	V
VOUTABSM	Absolute maximum voltage at any output pin		VSS*−0.3	VDD*+0.3	V

Table 25. 5 V SAFE PINS: TX_ENB, TXD, RXD, BR0, BR1, IO0, IO2, RESB

Parameter	Description	Condition	Min.	Max.	Unit
V5VSABSM	Absolute maximum input for digital 5 V safe inputs		VSS−0.3	6.0	V
VOUT5VABSM	Absolute maximum voltage at 5 V safe output pin		VSS−0.3	3.9	V

Marking and Delivery

Delivery of the production devices will be in:

- Tubes Y
- Trays N
- Tape on Reel N

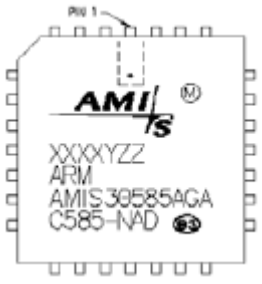
Marking

Bottom marking:

- AAAA Four letter code for country of assembly

Top marking:

- Logo AMIS logo
- XXXXYZZ Date code (XXXX), plant identifier (Y), traceability code
- Text ARM
- CUST.PART.NR AMIS30585AGA
- MMMM−MM C585−NAD



Storage Conditions

Storage conditions for packaged components before mounting for a maximum storage period of one year:

For through hole devices:

- Maximum temperature 40°C and maximum relative humidity 90 percent

For surface mount devices in dry bag:

- Maximum temperature 40°C and maximum relative humidity 90 percent

For surface mount devices not in dry bag:

- Maximum temperature 30°C and maximum relative humidity 60 percent (moisture sensitivity level two according to IPC/JEDEC standard J−STD−020A)

In case the storage conditions for surface mount devices are exceeded, a baking operation has to be performed before the devices can be mounted.

In case of dry bag delivery the storage details are summarized on a label attached to each dry bag.

The absolute maximum temperature ratings for storage of limited duration are −55°C and 150°C.

Product Acceptance

All products are tested by means of the production test program. In the program all parameters mentioned in the data sheet (and more parameters) are tested except:

- tsartup (= startup time of the oscillator)
- IMax_REF_OUT (= maximum current by REF_OUT)
- TRPOR (= power supply rise time)
- IRX (= current consumption during receive mode)
- ITX (= current consumption during transmit mode)

Lot conformance to specification in volume production is guaranteed by means of following quality conformance tests.

Table 26. QUALITY CONFORMANCE TESTS

QC Test	Conditions	AQL Level	Inspection Level
Electrical Functional and Parametric	To product data sheet	0.04	II
External Visual (Mechanical)	Physical damage o body or leads (e.g. bent leads)	0.15	II
External Visual (Cosmetic)	Correctness of marking; all other cosmetic defects	0.65	II

Each production lot will be accompanied with a certificate of conformance.

Quality and Reliability

A quality system with TS16949 certification is required.

External stress immunity:

- Electrostatic discharges (ESD): The device withstands 100 V standardized human body model (HBM) ESD pulses when tested according to MIL883C method 3015.5 (pin combination 2).
- Latch−up: Static latch−up protection level is 100 mA at 25°C when tested according to JEDEC No. 17.

The useful life:

- The useful life when used under moderate conditions is at least ten years.

Failure rate target for:

- Average outgoing quality (AOQ): 400ppm

Failure analysis down to the level of the failing sell is the responsibility of the customer.

Related Documents

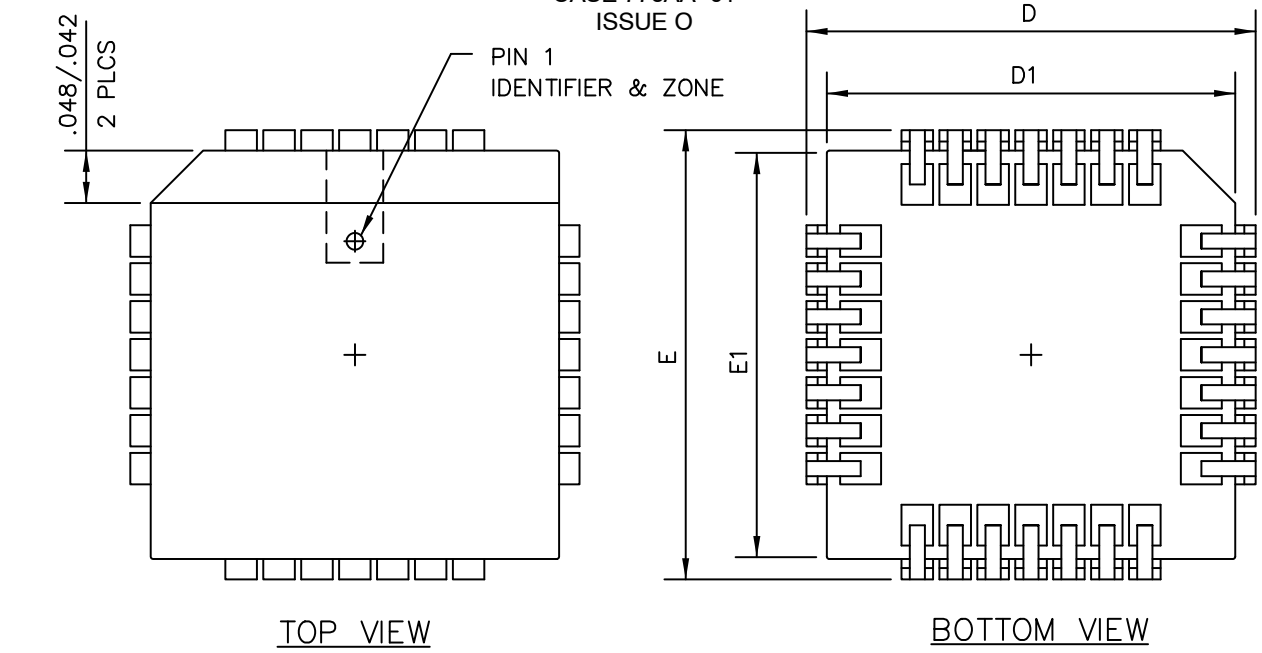
- AMIS−30585 Reference Manual
- IEC 1334−4−32: International Electro−technical Commission Distribution automation using distribution line carrier system data link layer – logical link control
- IEC 1334−5−1: International Electro−technical Commission Distribution automation using distribution line carrier system – the spread frequency shift keying (S−FSK) profile

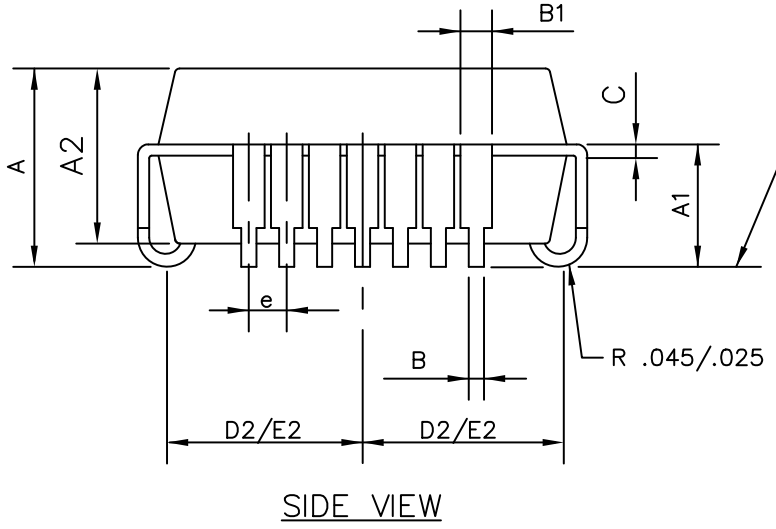
Company or Product Inquiries

For more information about ON Semiconductor's products or services visit our Web site at http://www.onsemi.com.

PACKAGE DIMENSIONS

PLCC 28 LEAD
CASE 776AA−01
ISSUE O





SYMBOL	MIN	NOM	MAX
A	0.165	0.172	0.180
A1	0.090	0.105	0.120
A2	0.148	0.152	0.156
B	0.013	0.017	0.021
B1	0.026	0.029	0.032
C	0.008	0.010	0.012
D	0.485	0.490	0.495
D1	0.450	0.453	0.456
D2	0.195	0.210	0.215
E	0.485	0.490	0.495
E1	0.450	0.453	0.456
E2	0.195	0.210	0.215
e	0.050 REF.		

ALL DIMENSIONS ARE IN INCHES.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

AMIS−30585/D