

# I<sup>2</sup>C BUS interface, general purpose I/O ports with condition watching function

## BU9929FV

ROHM's GPIO is a general-purpose IO that contains I<sup>2</sup>C BUS interface. It also contains monitoring function that conveys a change of the signal level in terminal to the host system via interrupt terminal or I<sup>2</sup>C BUS.

### ●Applications

Notebook PC, PC, VCR, TV etc. and other systems with I<sup>2</sup>C BUS.

### ●Features

- 1) I<sup>2</sup>C BUS interface
- 2) General purpose I/O port 16bits
- 3) State monitoring function to monitor all terminals
- 4) State detection signal serial output by I<sup>2</sup>C BUS master function
- 5) Output port of state detection signal
- 6) State detection ON/OFF setting input port during the default status
- 7) 32.768kHz clock input
- 8) Power supply voltage 3.3V / 5.0V

### ●Absolute maximum ratings (Ta=25°C)

| Parameter               | Symbol           | Limits                          | Unit |
|-------------------------|------------------|---------------------------------|------|
| Supply voltage          | V <sub>DD</sub>  | 7.0                             | V    |
| Power dissipation       | P <sub>d</sub>   | 640                             | mW   |
| Operating temperature   | T <sub>opr</sub> | -15 to +75                      | °C   |
| Storage temperature     | T <sub>sig</sub> | -55 to +125                     | °C   |
| Terminal supply voltage | V <sub>IN</sub>  | GND-0.5 to V <sub>DD</sub> +0.5 | V    |

\*Temperature derating : 6.4mW/°C over Ta=25°C

© Radiation resistance is not included in the design.

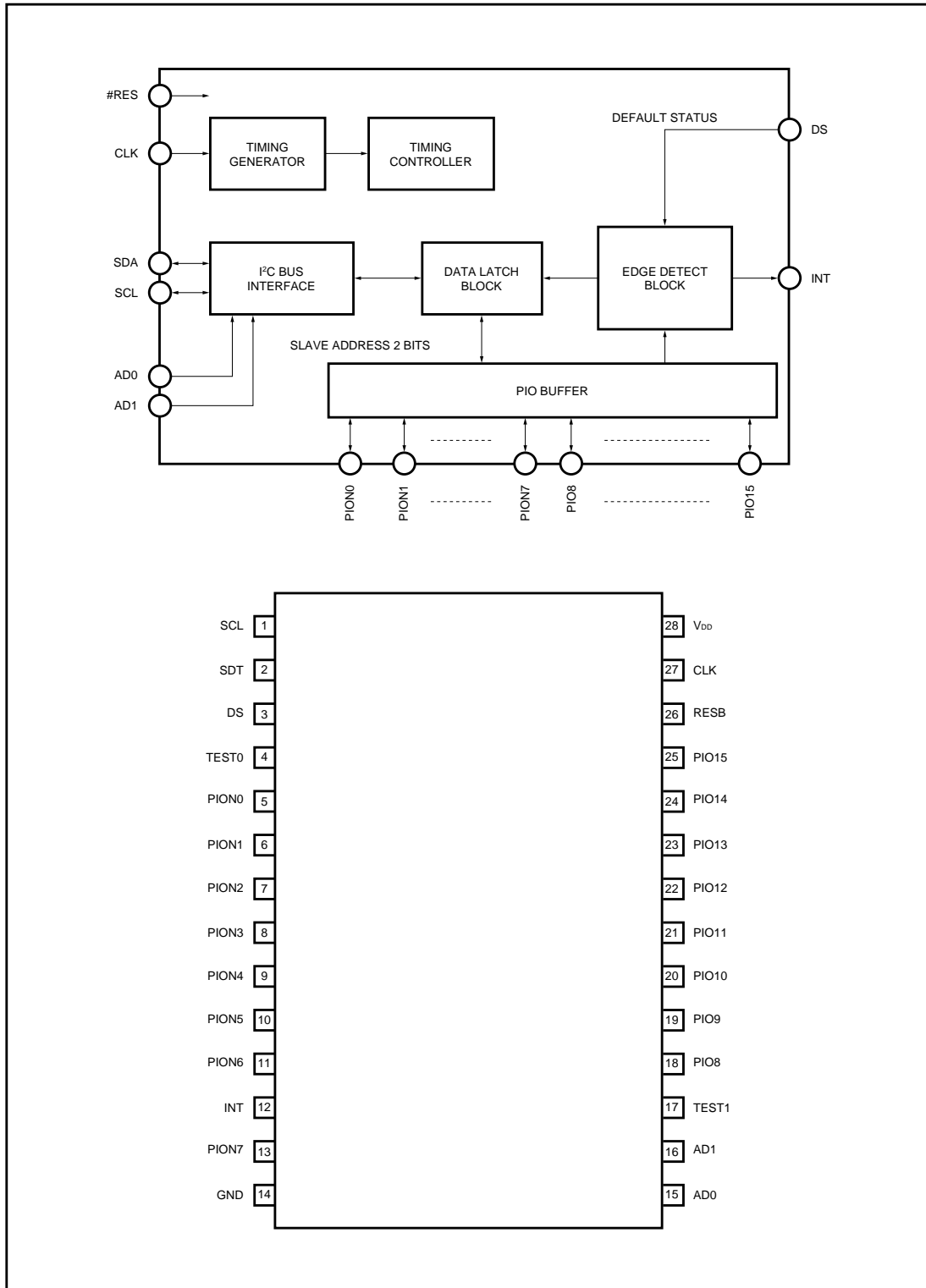
© Rohm CO., Ltd is a licensee of I<sup>2</sup>C BUS from Philips Semiconductors.

### ●Recommended operating conditions (Ta=25°C)

| Parameter                      | Min. | Typ. | Max. | Unit |
|--------------------------------|------|------|------|------|
| Operating supply voltage range | 3.0  | -    | 5.5  | V    |

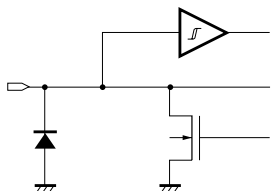
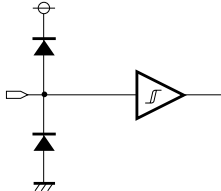
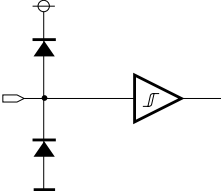
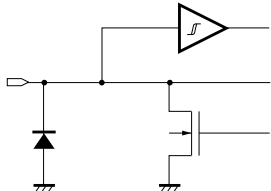
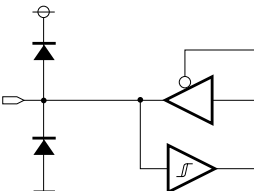
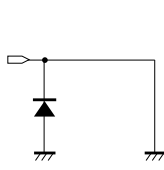
Multimedia ICs

●Block diagram

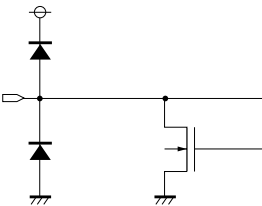
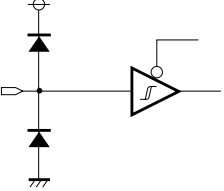
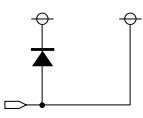
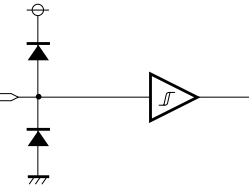
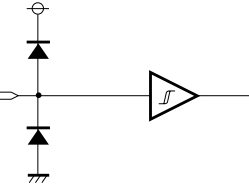
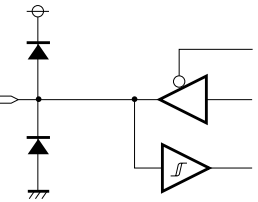


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●Pin description

| Pin. No | Pin. Name  | I/O circuit   | Pin Description   |
|---------|------------|---|---|
| 1<br>2  | SCL<br>SDT |    | I <sup>2</sup> C BUS Input/Output terminal  |
| 3       | DS         |    | To set condition detection mode at default state  |
| 26      | RES#       |    | Reset terminal<br>Reset condition by "L" input  |
| 5-11,13 | PION       |   | Nch open drain standard input/output terminal. Input at TTL level.<br>This waits for condition detection function of input.<br>Output will be Hi-Z at Shut Down mode.<br>5V input is possible when this IC is operated by 3.3V. |
| 18-25   | PIO        |  | Standard input/output terminal. Input at TTL level.<br>This waits for condition detection function of input. Output will be Hi-Z at Shut Down mode.   |
| 14      | GND        |  | GND terminal  |

## Multimedia ICs

| Pin. No  | Pin. Name       | I/O circuit   | Pin Description  |
|----------|-----------------|---|--|
| 12       | INT             |    | Output terminal for condition change detection.<br>Nch open drain output.  |
| 27       | CLK             |    | Clock input terminal.<br>32.768KHz should be put.<br>At Shut Down mode, clock supply into this IC will be shut down. |
| 28       | V <sub>DD</sub> |    | Power terminal.<br>3.3V/5.0V should be put in.   |
| 15<br>16 | AD0<br>AD1      |   | Input terminal for setting of I <sup>2</sup> C BUS<br>Slave address lower 2 bits.                                    |
| 4        | TEST0           |  | IC TEST Pin.<br>"L" Input required for normal operation.   |
| 17       | TEST1           |  | IC TEST Pin.<br>"L" Input required for normal operation.   |

## Multimedia ICs

●Electrical characteristics (Unless otherwise noted, V<sub>DD</sub>=5.0V, T<sub>a</sub>=25°C)

| Parameter                        | Symbol           | Min.                 | Typ.            | Max.                 | Unit | Conditions                       | Test Pin No.         |
|----------------------------------|------------------|----------------------|-----------------|----------------------|------|----------------------------------|----------------------|
| Circuit current (Normal)         | I <sub>DD</sub>  | –                    | 6.0             | 30                   | μA   | CLK=32.768Hz                     | 28                   |
| Circuit current (Shut down mode) | I <sub>DS</sub>  | –                    | 0.1             | 2.0                  | μA   | Shut Down Mode                   | 28                   |
| "H" Level input voltage 1        | V <sub>IH1</sub> | V <sub>DD</sub> ×0.7 | V <sub>DD</sub> | V <sub>DD</sub> +0.5 | V    |                                  | 1, 2                 |
| "L" Level input voltage 1        | V <sub>IL1</sub> | –0.5                 | 0.0             | V <sub>DD</sub> ×0.3 | V    |                                  | 1, 2                 |
| "H" Level input voltage 2        | V <sub>IH2</sub> | 2.5                  | V <sub>DD</sub> | V <sub>DD</sub> +0.5 | V    |                                  | 3, 4, 15-17          |
| "L" Level input voltage 2        | V <sub>IL2</sub> | –0.5                 | 0.0             | 0.8                  | V    |                                  | 3-5, 11, 13<br>15-27 |
| "H" Level input voltage 3        | V <sub>IH3</sub> | 2.5                  | V <sub>DD</sub> | 5.5                  | V    |                                  | 5-11, 13             |
| "H" Level input Current          | I <sub>IH</sub>  | 2.0                  | 0.0             | 1.0                  | μA   |                                  | 3-5, 11, 13<br>15-27 |
| "L" Level input Current          | I <sub>IL</sub>  | –1.0                 | 0.0             | –                    | μA   |                                  | 3-5, 11, 13<br>15-27 |
| "H" Level output voltage         | V <sub>SOH</sub> | 4.4                  | 4.8             | 5.0                  | V    | I <sub>OH</sub> =4mA             | 18-25                |
| "L" Level output voltage 1       | V <sub>SOL</sub> | 0.0                  | 0.2             | 0.6                  | V    | I <sub>OL</sub> =4mA             | 5-13, 18-25          |
| "L" Level output voltage 2       | V <sub>COL</sub> | 0.0                  | 0.2             | 0.6                  | V    | I <sub>OL</sub> =6mA             | 1, 2                 |
| I <sup>2</sup> C Fall time       | TFIC             | –                    | 100             | 250                  | ns   | I <sub>OL</sub> =6mA<br>CL=400pF | 1, 2                 |

Multimedia ICs

I<sup>2</sup>C BUS Interface characteristics (Unless otherwise noted, V<sub>DD</sub>=5.0V, Ta=25°C)

●Slave address

|     |   |   |   |   |    |     |     |
|-----|---|---|---|---|----|-----|-----|
| 0   | 1 | 1 | 1 | 1 | A1 | A0  | R/W |
| MSB |   |   |   |   |    | LSB |     |

A0 and A1 are set by input terminals of AD0 and AD1 as follows;

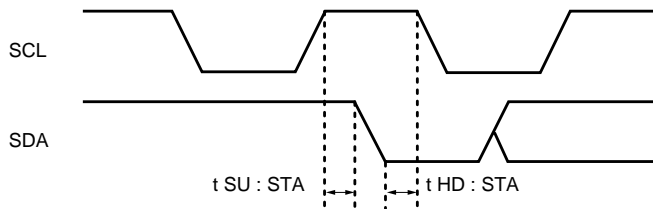
When AD0 / AD1=H, A0 / A1=1

When AD0 / AD1=L, A0 / A1=0

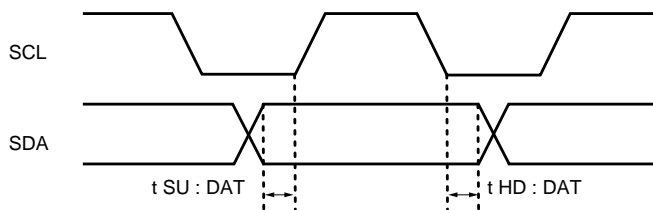
●Conforming to I<sup>2</sup>C BUS standard

| Parameter                   | Symbol     | Min. | Max. | Unit |
|-----------------------------|------------|------|------|------|
| SCL clock frequency         | f SCL      | 0    | 400  | kHz  |
| Start condition hold time   | t HD : STA | 0.6  | –    | μs   |
| Start condition set-up time | t SU : STA | 0.6  | –    | μs   |
| Data set-up time            | t SU : DAT | 100  | –    | ns   |
| Data hold time              | t HD : DAT | 0    | 0.9  | μs   |
| Stop condition set-up time  | t SU : STO | 0.6  | –    | μs   |

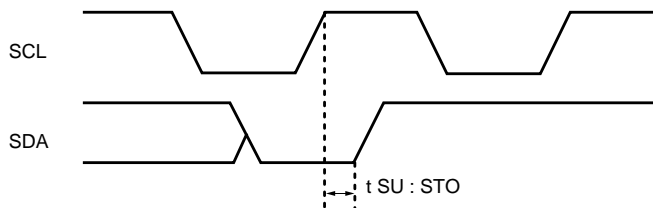
(Start Timing)



(Data Timing)



(Stop Timing)



## Multimedia ICs

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### 1. Data write mode

|    |               |           |   |              |   |               |   |              |   |    |
|----|---------------|-----------|---|--------------|---|---------------|---|--------------|---|----|
| St | SLAVE ADDRESS | $\bar{W}$ | A | COMMAND BYTE | A | WRITE DATA 1  | A | WRITE DATA 2 | A | Sp |
|    |               |           |   |              |   | PION7 – PION0 |   | PIO15 – PIO8 |   |    |

Command register : At reset, D0 to D7 are "0".

|         |         |          |        |        |          |          |        |
|---------|---------|----------|--------|--------|----------|----------|--------|
| D7      | D6      | D5       | D4     | D3     | D2       | D1       | D0     |
| SHT DWN | INT SEL | DOUT SEL | OUT ON | DIR ON | BYTE SEL | EDGE SEL | DET ON |

#### D7 : Shut Down mode

- 0 : Shut down mode off (Normal operation mode)
- 1 : Shut down mode on

#### D6 : INT output method choice

- 0 : LOW output
- 1 : Output of LOW pulse equivalent for one period of CLK

#### D5 : Detection result output choice

- 0 : Serial output. INT pin is also valid.
- 1 : Serial output (I<sup>2</sup>C MASTER function) off. Only INT pin is valid.

#### D4 : Output port writing set

- 0 : Writing invalid
- 1 : Writing valid. But, a port, which is indicated as input, is invalid.  
Following Write data 2byte-0 : "L" output, 1 : "H" output

#### D3 : I / O direction set

- 0 : Direction set invalid
- 1 : Direction set valid  
Following Write data 2byte-0 : input, 1 : output

#### D2 : Watching object input choice

- 0 : PION0 to PION7
- 1 : PION8 to PIO15

#### D1 : Change detection mode

- 0 : Falling edge
- 1 : Both rising and falling edge

#### D0 : Input port condition watching mode

- 0 : Invalid
- 1 : Valid

Multimedia ICs

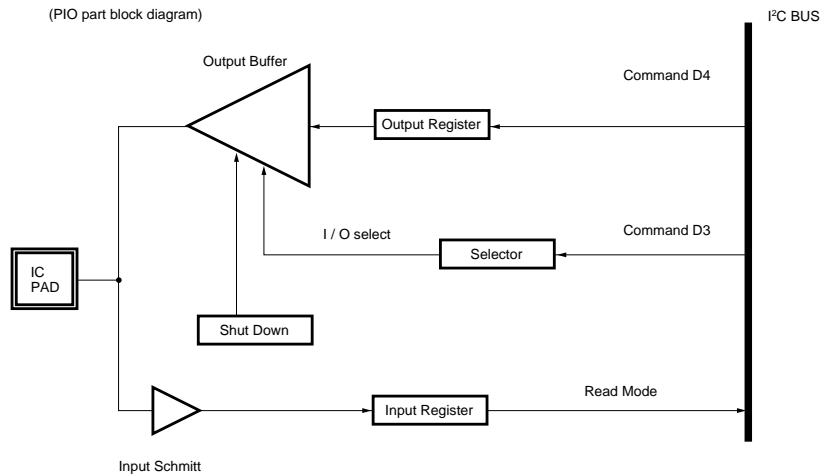
2. Data read mode

According to the following format, input/output value of PIO/PION pins can be read by I<sup>2</sup>C interface.

PIO data read

|    |               |   |   |               |   |              |           |    |
|----|---------------|---|---|---------------|---|--------------|-----------|----|
| St | SLAVE ADDRESS | R | A | READ DATA 1   | A | READ DATA 2  | $\bar{A}$ | Sp |
|    |               |   |   | PION7 – PION0 |   | PIO15 – PIO8 |           |    |

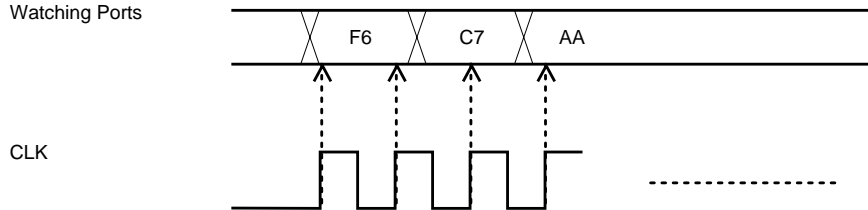
PIO part block diagram



Input Port sampling timing

As shown below, BU9929FV is sampling for Input Ports with the rising edges of CLK. Therefore it is necessary that Input Ports are keeping at least 1 CLK cycle, for their certain inputs.

Watching Ports





Multimedia ICs

3. Condition change detection result output mode

1) This IC becomes I<sup>2</sup>C master device, and the detection result is sent according to the following format;

2Byte Watching

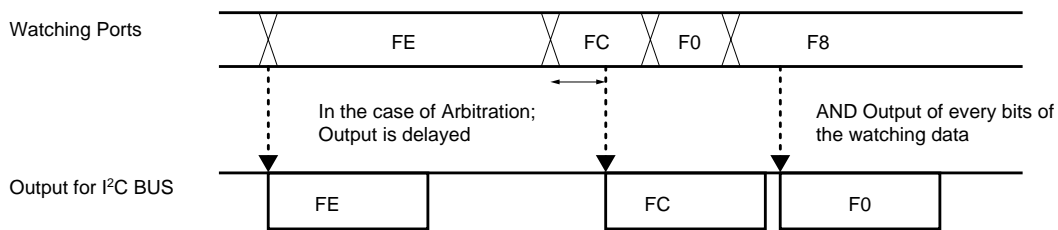
|    |   |   |   |   |   |   |   |           |   |                  |               |              |              |              |   |    |
|----|---|---|---|---|---|---|---|-----------|---|------------------|---------------|--------------|--------------|--------------|---|----|
| St | 0 | 0 | 0 | 1 | 0 | 0 | 0 | $\bar{W}$ | A | SLAVE ADDRESS +0 | A             | WRITE DATA 1 | A            | WRITE DATA 2 | A | Sp |
|    |   |   |   |   |   |   |   |           |   |                  | PION7 – PION0 |              | PIO15 – PIO8 |              |   |    |

1Byte Watching

|               |   |   |   |   |   |   |   |           |   |                  |   |              |   |    |
|---------------|---|---|---|---|---|---|---|-----------|---|------------------|---|--------------|---|----|
| St            | 0 | 0 | 0 | 1 | 0 | 0 | 0 | $\bar{W}$ | A | SLAVE ADDRESS +0 | A | WRITE DATA 1 | A | Sp |
| PION7 – PION0 |   |   |   |   |   |   |   |           |   |                  |   |              |   |    |

<DATA Keeping Operation>

In a case that there is a change in detection port during detection result transmission, then watching data is saved by the end of detection output, and it will be proceeded further after the detection output is finished. However, the output data in this case will be “AND” output of every bits of the watching data.



2) DS pin Description

By DS pin, valid/invalid of condition detection of the default condition (from RESET release to reception of the first I<sup>2</sup>C command) can be set.

<DS pic valid range>

In the range from RESET release to the first set of condition detection mode by I<sup>2</sup>C command, the set of this pin will be valid. After the set of condition detection mode by I<sup>2</sup>C command, this pin will be invalid, and the set by I<sup>2</sup>C commanded will be reflected.

<Pin setting>

DS pin= “H” : Input bit condition detection mode is valid.

But, 1 byte detection mode (only PION7-PION0 will be in condition detection)

DS pin=“L” : Input bit condition detection mode is invalid.

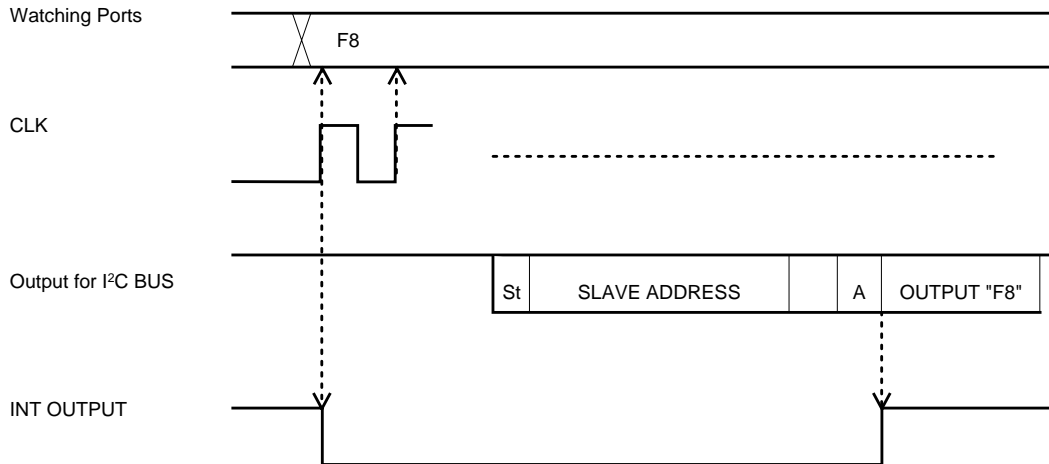
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3) INT pin specification

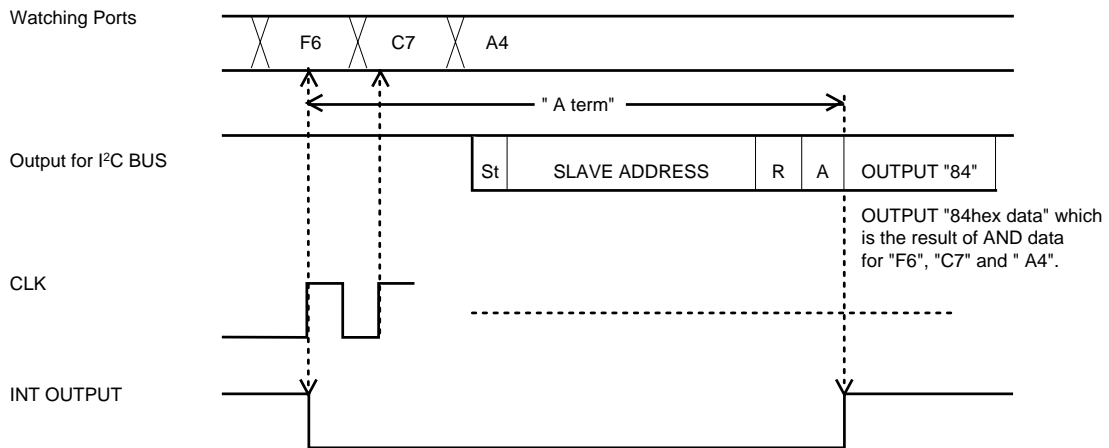
When condition watching mode, INT output pin works for reporting of detection of watching port.

(a) When command D6=0(including default time after RESET release)

INT pin falls when detection of watching port is received. And INT pin rises after ACK-output which is on the I<sup>2</sup>C Data read.



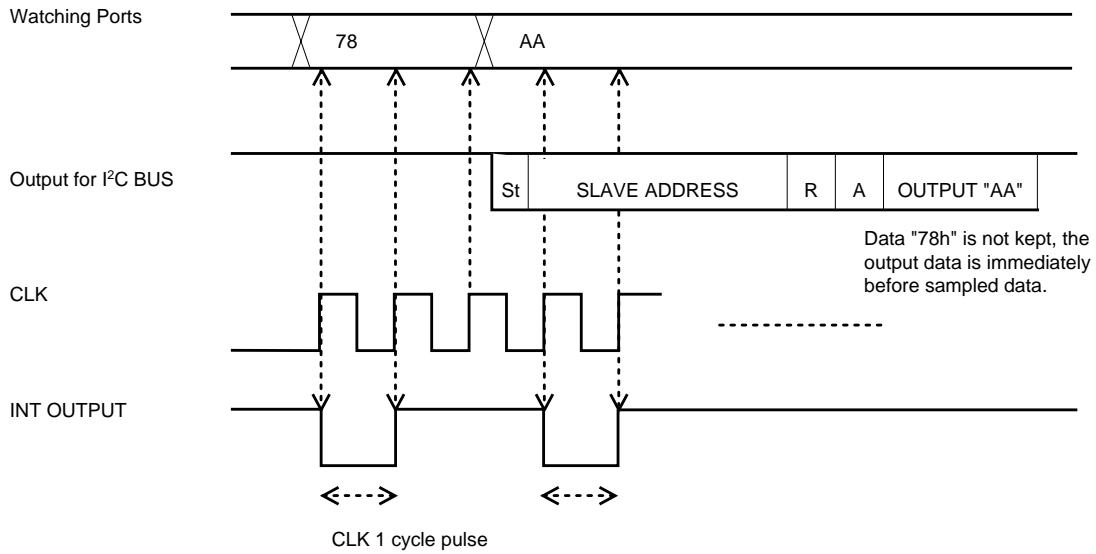
In the case that there is a change in detection ports once, and there are another changes before returning the ACK (as shown "A term"), then watching data is saved. And the output data in this case will be "AND" output of every bits of the watching data.



Multimedia ICs

(b) When command D6=1

INT pin outputs "1 clock cycle pulse" when detection of watching port is received. In the case that the output data is the data which is sampled immediately before the returning ACK.



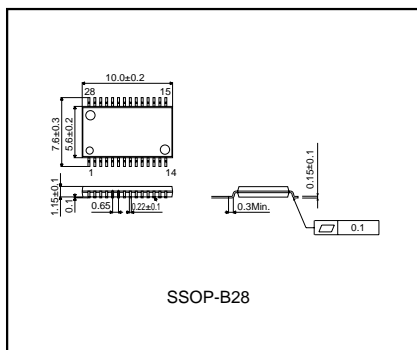
4. Shut down mode

By command D7=1, this IC can be set to Shut down mode, which can save current consumption. At Shut down mode, operation of CLK input pin will be stopped, and input of CLK into this IC can be shut down. Also, for every PIO/PION pins, pins under output condition will be saved as Hi-Z.

At Shut down mode, condition-watching function can not be used.

Contents of each register before shut down will be saved by the shut down release.

●External dimensions (Unit : mm)



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