

# SX1501/SX1502/SX1503

# 4/8/16 Channel Low Voltage GPIO with NINT and NRESET

### **GENERAL DESCRIPTION**

The SX1501, SX1502 and SX1503 are complete ultra low voltage General Purpose parallel Input/Output (GPIO) expanders ideal for low power handheld battery powered equipment. They allow easy serial expansion of I/O through a standard I<sup>2</sup>C interface. GPIO devices can provide additional control and monitoring when the microcontroller or chipset has insufficient I/O ports, or in systems where serial communication and control from a remote location is advantageous.

These devices can also act as a level shifter to connect a microcontroller running at one voltage level to a component running at a different voltage level. The core is operating as low as 1.2V while the I/O banks can operate between 1.2V and 5.5V independent of the core voltage and each other.

Each GPIO is programmable via 8-bit configuration registers. Data registers, direction registers, pull-up/pull-down registers, interrupt mask registers and interrupt registers allow the system master to program and configure 4 or 8 or 16-GPIOs using a standard 400kHz I<sup>2</sup>C interface.

The SX1501, SX1502 and SX1503 offer a unique fully programmable logic functions like a PLD to give more flexibility and reduce external logic gates used for standard applications.

The SX1501, SX1502 and SX1503 have the ability to generate mask-programmable interrupts based on falling/rising edge of any of its GPIO lines. A dedicated pin indicates to a host controller that a state change occurred in one or more of the GPIO lines.

The SX1501, SX1502 and SX1503 each come in a small QFN-UT-20/28 package as well as a TSSOP-20/28 package. All devices are rated from -40 $^{\circ}$  to +85 $^{\circ}$  temperature range.

### **ORDERING INFORMATION**

Part Number	I/O Channels	Package
SX1501I087TRT	4	QFN-UT-20
SX1502I087TRT	8	QFN-UT-20
SX1503I091TRT	16	QFN-UT-28
SX1501I088TRT <sup>(1)</sup>	4	TSSOP-20
SX1502I088TRT <sup>(1)</sup>	8	TSSOP-20
SX1503I089TRT <sup>(1)</sup>	16	TSSOP-28
SX1502EVK <sup>(2)</sup>	8	Evaluation Kit

<sup>(1)</sup>Future products

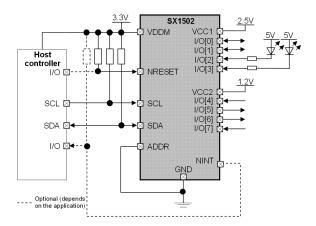
<sup>(2)</sup>SX1502I087TRT based, unique evaluation kit for the three parts.

#### **KEY PRODUCT FEATURES**

- 4/8/16 channel of I/Os
  - True bi-directional style I/O
  - Programmable Pull-up/Pull-down
  - Push/Pull outputs
- 1.2V to 5.5V independent operating voltage for all supply rails (VDDM, VCC1, VCC2)
- 5.5V compatible I/Os, up to 24mA output sink (no total sink current limit)
- Fully programmable logic functions (PLD)
- 400kHz 2-wire I<sup>2</sup>C compatible slave interface
- Open drain active low interrupt output (NINT)
   Bit maskable
  - Programmable edge sensitivity
- Power-On Reset and reset input (NRESET)
- Ultra low current consumption of typ. 1uA
- -40℃ to +85℃ operating temperature range
- Ultra-Thin 3x3mm QFN-UT-20 and TSSOP-20 packages (SX1501/SX1502)
- Ultra-Thin 4x4mm QFN-UT-28 and TSSOP-28 packages (SX1503)

#### **TYPICAL APPLICATIONS**

- Cell phones, PDAs, MP3 players
- Digital camera
- Portable multimedia player
- Notebooks
- GPS Units
- Industrial, ATE
- Any battery powered equipment



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#### **PIN DESCRIPTION** 1

#### SX1501 4-channel GPIO 1.1

Pin	Symbol	Туре	Description	
1	NRESET	DIO	Active low reset	
2	SDA	DIO	I <sup>2</sup> C serial data line	
3	NC1	-	Leave open, not connected	
4	SCL	DI	I <sup>2</sup> C serial clock line	
5	I/O[0]	DIO (*1)	I/O[0], at power-on configured as an input	
6	I/O[1]	DIO (*1)	I/O[1], at power-on configured as an input	
7	VCC1	Р	I/O supply voltage	
8	GND	Р	Ground Pin	
9	I/O[2]	DIO <sup>(*1)</sup>	I/O[2], at power-on configured as an input High sink I/O.	
10	I/O[3]	DIO <sup>(*1)</sup>	I/O[3], at power-on configured as an input High sink I/O.	
11	NINT	DO	Active low interrupt output	
12	ADDR	DI	Address input, connect to VDDM or GND	
13	NC2	-	Leave open, not connected	
14	VDDM	Р	Main supply voltage	
15	NC3	-	Leave open, not connected	
16	NC4	-	Leave open, not connected	
17	NC7	-	Connect to VCC1	
18	GND	Р	Ground Pin	
19	NC5	-	Leave open, not connected	
20	NC6	-	Leave open, not connected	

A: Analog D: Digital

I: Input O: Output

P: Power

(\*1) This pin is programmable through the I<sup>2</sup>C interface

#### Table 1 – SX1501 Pin Description

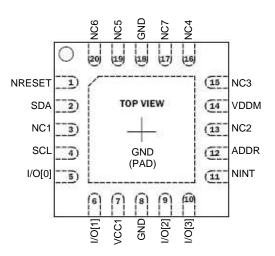


Figure 1 – SX1501 QFN-UT-20 Pinout



### 1.2 SX1502 8-channel GPIO

Pin	Symbol	Туре	Description	
1	NRESET	DIO	Active low reset	
2	SDA	DIO	I <sup>2</sup> C serial data line	
3	NC1	-	Leave open, not connected	
4	SCL	DI	I <sup>2</sup> C serial clock line	
5	I/O[0]	DIO (*1)	I/O[0], at power-on configured as an input	
6	I/O[1]	DIO (*1)	I/O[1], at power-on configured as an input	
7	VCC1	Р	Supply voltage for Bank A I/O[0-3]	
8	GND	Р	Ground Pin	
9	I/O[2]	DIO <sup>(*1)</sup>	I/O[2], at power-on configured as an input High sink I/O.	
10	I/O[3]	DIO <sup>(*1)</sup>	I/O[3], at power-on configured as an input High sink I/O.	
11	NINT	DO	Active low interrupt output	
12	ADDR	DI	Address input, connect to VDDM or GND	
13	NC2	-	Leave open, not connected	
14	VDDM	Р	Main supply voltage	
15	I/O[4]	DIO (*1)	I/O[4], at power-on configured as an input	
16	I/O[5]	DIO (*1)	I/O[5], at power-on configured as an input	
17	VCC2	Р	Supply voltage for Bank B I/O[4-7]	
18	GND	Р	Ground Pin	
19	I/O[6]	DIO <sup>(*1)</sup>	I/O[6], at power-on configured as an input	
20	I/O[7]	DIO <sup>(*1)</sup>	I/O[7], at power-on configured as an input	

A: Analog

D: Digital I: Input

O: Output

P: Power

(\*1) This pin is programmable through the I<sup>2</sup>C interface

Table 2 – SX1502 Pin Description

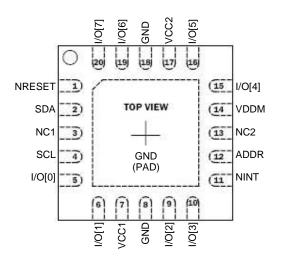


Figure 2 – SX1502 QFN-UT-20 Pinout



#### 1.3 SX1503 16-channel GPIO

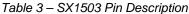
Pin	Symbol	Туре	Description	
1	GND	P	Ground Pin	
2	I/O[2]	DIO <sup>(*1)</sup>	I/O[2], at power-on configured as an input	
3	I/O[3]	DIO (~1)	I/O[3], at power-on configured as an input	
4	VCC1	P	I/O supply voltage for Bank A I/O[0-7]	
5	I/O[4]	DIO (*1)	I/O[4], at power-on configured as an input	
6	I/O[5]	DIO <sup>(*1)</sup>	I/O[5], at power-on configured as an input	
7	GND	Р	Ground Pin	
8	I/O[6]	DIO <sup>(*1)</sup>	I/O[6], at power-on configured as an input High sink I/O.	
9	I/O[7]	DIO <sup>(*1)</sup>	I/O[7], at power-on configured as an input High sink I/O.	
10	NINT	DO	Active low interrupt output	
11	NC	-	Leave open, not connected	
12	VDDM	Р	Main supply voltage	
13	I/O[8]	DIO <sup>(~1)</sup>	I/O[8], at power-on configured as an input	
14	I/O[9]	DIO (*1)	I/O[9], at power-on configured as an input	
15	GND	Р	Ground Pin	
16	I/O[10]	DIO <sup>(~1)</sup>	I/O[10], at power-on configured as an input	
17	I/O[11]	DIO (*1)	I/O[11], at power-on configured as an input	
18	VCC2	Р	I/O supply voltage for Bank B I/O[8-15]	
19	I/O[12]	DIO <sup>(*1)</sup>	I/O[12], at power-on configured as an input	
20	I/O[13]	DIO <sup>(~1)</sup>	I/O[13], at power-on configured as an input	
21	GND	Р	Ground Pin	
22	I/O[14]	DIO <sup>(*1)</sup>	I/O[14], at power-on configured as an input High sink I/O.	
23	I/O[15]	DIO <sup>(*1)</sup>	I/O[15], at power-on configured as an input High sink I/O.	
24	NRESET	DIO	Active low reset	
25	SDA	DIO	I <sup>2</sup> C serial data line	
26	SCL	DI	I <sup>2</sup> C serial clock line	
27	I/O[0]	DIO <sup>(~1)</sup>	I/O[0], at power-on configured as an input	
28	I/O[1]	DIO <sup>(*1)</sup>	I/O[1], at power-on configured as an input	

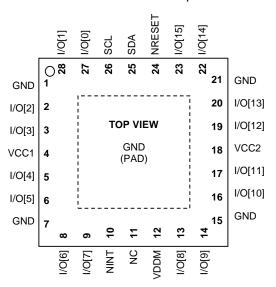
A: Analog D: Digital

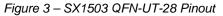
I: Input

O: Output P: Power

(\*1) This pin is programmable through the  $I^2C$  interface









### 2 ELECTRICAL CHARACTERISTICS

### 2.1 Absolute Maximum Ratings

Stress above the limits listed in the following table may cause permanent failure. Exposure to absolute ratings for extended time periods may affect device reliability. The limiting values are in accordance with the Absolute Maximum Rating System (IEC 134). All voltages are referenced to ground (GND).

Symbol	Description	Min	Max	Unit
<b>VDDM</b> <sub>max</sub>	Main supply voltage	- 0.4	6.0	V
VCC1,2 <sub>max</sub>	I/O banks supply voltage	- 0.4	6.0	V
V <sub>ESD HBM</sub>	Electrostatic handling HBM model <sup>(1)</sup>	-	1500	V
V <sub>ESD CDM</sub>	Electrostatic handling CDM model	-	300	V
V <sub>ESD MM</sub>	Electrostatic handling MM model	-	200	V
T <sub>A</sub>	Operating Ambient Temperature Range	-40	+85	ĉ
Tc	Junction Temperature Range	-40	+125	Ĉ
T <sub>STG</sub>	Storage Temperature Range	-55	+150	C
l <sub>lat</sub>	Latchup-free input pin current <sup>(2)</sup>	+/-100	-	mA

(1) Tested according to JESD22-A114A

(2) Static latch-up values are valid at maximum temperature according to JEDEC 78 specification Table 4 - Absolute Maximum Ratings

### 2.2 Electrical Specifications

Table below applies to default registers values (Boost Mode Off), unless otherwise specified. Typical values are given for  $T_A = +25$ °C, VDDM=VCC1=VCC2=3.3V.

Symbol	Description	Conditions	Min	Тур	Max	Unit
Supply						
VDDM	Main supply voltage	-	1.2	-	5.5	V
VCC1,2	I/O banks supply voltage	-	1.2	-	5.5	V
IDDM	Main supply current (I <sup>2</sup> C inactive)	-	-	1	5	μΑ
ICC1,2	I/O banks supply current <sup>(1)</sup>	VCC1,2 >= 2V	-	1	2	μA
1001,2	1/O banks supply current	VCC1,2 < 2V	-	0.5	1	μA
I/Os set a	as Input					
VIH	High level input voltage	-	0.7* VCC1,2	-	VCC1,2 +0.3	V
VIL	Low level input voltage	-	-0.4	-	0.3* VCC1,2	V
VHYS	Hysteresis of Schmitt trigger	-	-	0.1* VCC1,2	-	V
ILEAK	Input leakage current	Assuming no active pull-up/down	-1.5	-	1.5	μA
CI	Input capacitance	-	-	-	10	pF
I/Os set a	s Output					
VOH	High level output voltage	-	VCC1,2 - 0.3	-	VCC1,2	V
VOL	Low level output voltage	-	-0.4	-	0.3	V
ЮН	High level output source	VCC1,2 >= 2V	-	-	8	mΑ
1011	current	VCC1,2 < 2V	-	-	0.3 <sup>(2)</sup>	шл
	Low level output sink current	VCC1,2 >= 2V	-	-	24	mA
IOL	for the high sink I/Os	VCC1,2 < 2V	-	-	6 <sup>(2)</sup>	
102	Low level output sink current	VCC1,2 >= 2V	-	-	12	mΑ
	for the other I/Os.	VCC1,2 < 2V	-	-	6	
t <sub>PV</sub>	Output data valid timing	Cf. Figure 9	-	-	1.5	μs
NINT (Ou			1	1		
VOL	Low level output voltage	-	-	-	0.3	V
IOLM	Low level output sink current	VDDM >= 2V	-	-	12	mA
	·	VDDM < 2V	-	-	6	
t <sub>IV</sub>	Interrupt valid timing	From input data change	-	-	, i	μs



t_RInterrupt reset timingFrom Reginterrupt/Source clearing-2µVOLLow level output voltage0.3VVOLLow level output sink currentVDDM >= 2V0.3VVIL_MLow level output sink currentVDDM >= 2V6VIH_MRHigh level input voltage-0.7*-5.5VVIL_MLow level output sink currentVDDM >= 2V6VIN_SMHysterssis of Schmitt trigger0.4VDDMVDPORPower-On-Reset voltageCf. Figure 7-1.5µCIInput capacitance1.6µVDROPLWork-row-rout voltageCf. Figure 7-0.2-VVDROPLWork-row-rout voltageCf. Figure 7nVDROPLLow brow-rout voltageCf. Figure 7nnVDROPLLow brow-rout voltageCf. Figure 7nnVHMAHigh level input voltage1.6µVIL_MLow level input voltage1.5-1.5µVIL_MLow level input voltage0.3*VVDDM-VDDMVIL_MLow level input voltage0.4-0.3*VVIL_MLow level input	Cumhal	Description	Conditions	R/I in	Turn	May	1 1 1 1 1 1	
transmission       clearing       ·	Symbol	Description		Min	Тур	Max	Unit	
INRESET (input/Output)VOLLow level output voltage0.3VVOLLow level output sink currentVDDM >= 2V12VILMLow level input voltage-0.7*-6mVILMLow level input voltage-0.7*-6mVILMLow level input voltage0.40.3*VVHYSMHysteresis of Schmitt trigger0.1*VCIInput eakage current1.5µµCIInput eakage current1.6µµVDROPLDewr-On-Reset voltageCf. Figure 7-VDDM-VVDROPLDewr-On-Reset voltageCf. Figure 7nVDROPLLow brown-out voltageCf. Figure 7nnVDROPLLow brown-out voltageCf. Figure 7nnVDROPLLow brown-out voltageCf. Figure 7nnVDROPLLow brown-out voltageCf. Figure 70.2*-VDDM0.3*VVHrMaHigh level input voltage0.4*-0.3*V-0.3*VVILMLow level input voltage1.5*1.5*UVDDM-VDDM	t <sub>IR</sub>	Interrupt reset timing		-	-	2	μs	
IOL W IVHMRLow level output sink currentVDDM >= 2V12 mVIHMR W VHMR High level input voltage6mVIHMR W VHMS W VHYS Hysteresis of Schmitt trigger6mVILM VHMS W VDDMLow level input voltageVVDDM.VVDDM <td< td=""><td>NRESET</td><td>(Input/Output)</td><td>ÿ</td><td></td><td></td><td></td><td></td></td<>	NRESET	(Input/Output)	ÿ					
IDLmLow level output sink currentVDDM < 2V6MVIH_MRHigh level input voltage-0.7*-5.5VVIL_MLow level input voltage0.4-0.3*VVHYS_MHysteresis of Schmitt trigger0.1*VDDMVVINS_MHysteresis of Schmitt trigger1.0pfCIInput capacitance1.0pfVDROPHInput capacitance0.70.9VVDROPHLow brown-out voltageCf. Figure 77mVDROPHIngh forw-nout voltageCf. Figure 77mVDROPHLow brown-out voltageCf. Figure 77mVDROPHIngh fewel input voltage0.7*VDDMNNVHM_MAHigh level input voltage0.7*VDDMNVHM_MAHigh level input voltage0.1*VDDMNVHM_MAHout leapacitance1.5µCIInput capacitance1.5µCIInput capacitance0.3*VVHM_MAHigh level input voltage0.3*VVDLLow level output voltage0.3*VVOLLow level output voltage-	VOL	Low level output voltage	-	-	-		V	
VIHMAR IVILMAR VILMAR Low level input voltageVULMAR -VULMAR -VILAR VDDMVILAR -VILAR VDDMVILAR VDDMVILAR VDDMVILAR VDDMVILAR VDDMVILAR VDDMVILAR VDDMVILAR VDDMVILAR VDDMVILAR VDDMVILAR VDDMVILAR VDDMVILAR VDDMVILAR VDROPHInput leakage current voltage0.1* VDROPHVILAR VDROPHVILAR VDROPHVILAR VILAR High forwn-out voltageCI. Figure 7 CI. Figure 7 0.2 VIDAN-1 -VIIAR -VIIAR	101	Low level output sink current		-	-		mA	
VIEwa INTROHigh level input voltage-VDDM-5.5VVILM Low level input voltage0.4-0.1* VDDMVVHYSM LIEAKHysteresis of Schmitt trigger0.1* VDDMVVILM CIInput capacitance1.0pfVDROPH Liph brown-out voltageCf. Figure 70.7-0.9VVDROPL Low brown-out voltageCf. Figure 7-0.2-VVDROPH Low brown-out voltageCf. Figure 7-0.2-VVDROPH Low brown-out voltageCf. Figure 7-0.2-VVHMW High level input voltage-0.7*VDDM-+0.3VVILM Low level input voltage0.4-VDDM-VDDMVHYSM Hysteresis of Schmitt trigger1.0pSCL (Input) and SDA (Input/Output)1.0pSCL UDLM1.5-1.5µVOL Low level output voltage0.3VVVLMK MHigh level input voltage0.3VVOL Low Hystersis of Schmitt trigger0.3VVL Low + +tr0.3VVL Low + +tr0.3VVL Low + +tr	ICLM		VDDM < 2V	-	-	6	шл	
VILM         Low level input voltage         -         -0.4         -         VDDM         V           VHX6         Hysteresis of Schmitt trigger         -         -         0.1*         V         V           ILEAK         Input capacitance         -         -         1.5         -         1.5         µ           CI         Input capacitance         -         -         1.0         P           VDROPH         High town-out voltage         Cf. Figure 7         -         0.2         -         V           VDROPH         Low brown-out voltage         Cf. Figure 7         -         0.2         -         V           VBotest         Reset time         Cf. Figure 7         -         0.2         -         V           VBotest         Reset time         Cf. Figure 7         -         0.2         -         V           VHMa         High level input voltage         -         0.7*         VDDM         -         +0.3         N           VHLM         Low level input voltage         -         -         0.4         -         0.3*         V           VHMA         Hysteresis of Schmitt trigger         -         -         1.5         -         1.5	VIH <sub>MR</sub>	High level input voltage	-		-		V	
VHYsteresis of Schmitt ftigger         -         -         VDDM         -         V           ILEAK         Input leakage current         -         -         1.5         µ           CI         Input capacitance         -         -         1.5         µ           VDROPH         Enderstance         -         -         1.0         pV           VDROPH         Input capacitance         -         -         0.0         V           VDROPH         High brown-out voltage         Cf. Figure 7         -         0.2         -         V           VDROPH         Reset pulse from host uC         Cf. Figure 7         -         0.2         -         V           VILm         Reset pulse from host uC         Cf. Figure 7         -         0.2         -         V           VILm         Low level input voltage         -         0.7'         VDDM         -         0.3'         V           VILM         Low level input voltage         -         -         0.1         -         1.5         µ           CI         Input capacitance         -         -         1.5         µ         µ           Interface comples with slave F/S mode 1'C interface as described by Philips 1'C specifica	VIL <sub>M</sub>	Low level input voltage	-	-0.4	-		V	
ClInput capacitance10pfVPORPower-On-Reset voltageCf. Figure 70.7.0.9VVDROPHHigh brown-out voltageCf. Figure 7-VDDM-1.VVDROPHLow brown-out voltageCf. Figure 7-0.2VVBROPHLow brown-out voltageCf. Figure 7 <td< td=""><td><math>VHYS_M</math></td><td>Hysteresis of Schmitt trigger</td><td>-</td><td>-</td><td></td><td>-</td><td>V</td></td<>	$VHYS_M$	Hysteresis of Schmitt trigger	-	-		-	V	
VPOR VDROPH VDROPH High brown-out voltageCf. Figure 7 Cf. Figure 70.7 -0.9 V VDDM-1VDROPH Low brown-out voltageCf. Figure 7 Cf. Figure 7-0.2 V VDDM-1VDROPL Low brown-out voltageCf. Figure 7 Cf. Figure 7-0.2 V VDDMVBROPL Low brown-out voltageCf. Figure 7 Cf. Figure 77 mWHMA High level input voltage-0.7* -VDDM 0.3* -V VDDMVILM Low level input voltage0.4 VDDM VDDM -VHYSM Cl Input leakage current0.1* VDDMILEAK Input leakage current1.5 -1.5 -1.6 -1.0 pSCL (input) and SDA (input/Output)1.0 -pSCL (input) and SDA (input/Output)1.0 -pVOLLow level output voltage0.3 -VVOLLow level output voltage0.3 -VVOLLow level output voltage1.2 -VOLLow level output voltage1.2 -VOLLow level output voltage0.3* -VVILMLow level input voltage0.4 VILM </td <td></td> <td></td> <td>-</td> <td>-1.5</td> <td>-</td> <td></td> <td>μA</td>			-	-1.5	-		μA	
VDROPHHigh provm-out voltageCf. Figure 7-VDDM-1-VVDROPLLow brown-out voltageCf. Figure 7-0.2-VVErserReset timeCf. Figure 77mterserReset pulse from host uCCf. Figure 77mVILMAHigh level input voltage-0.7*-VDDM-+0.3VILMLow level input voltage0.40.3*VVILMLow level input voltage0.40.3*VILMLow level input voltage1.5-CIInput leakage current1.0pCIInput capacitance1.0pSCL(Input/Output)001.0pSCL(Input/Output)1.0pVOLLow level output voltage0.3VVOLLow level output voltage1.2VOLLow level output voltage0.3VVILMLow level input voltage0.4-0.3*VILMLow level output sink currentVDDM >= 2V1.2VDLMLow level output sink currentVDDM >= 2V1.2VILMLow level input voltage0.4-0			-	-	-		pF	
VDROPL Low brown-out voltageCf. Figure 7.0.2.V $I_{EQLSET}$ Reset pulse from host uCCf. Figure 7 $I_{EQLSET}$ Reset pulse from host uCCf. Figure 7 $MDR$ (Input)				0.7	-	0.9	-	
Itelser         Reset time         Cf. Figure 7         -         -         7         m           ADDR (Input)         Cf. Figure 7         300         -         -         n           ADDR (Input)         VIL <sub>MA</sub> High level input voltage         -         0.7*         VDDM           VIL <sub>MA</sub> Low level input voltage         -         0.7*         VDDM         +0.3         V           VIL <sub>MA</sub> Low level input voltage         -         0.4         0.3*         V         VDDM         +0.3         V           VHYSM         Hysteresis of Schmitt trigger         -         0.4         0.1*         VDDM         ·         V           Cl Input capacitance         -         -         1.5         -         1.5         .         1.5         .         1.5         .         1.5         .				-	VDDM-1	-		
Leuise ADDR (Input)       Reset pulse from host uC       Cf. Figure 7       300       -       -       ns         VIH <sub>MA</sub> High level input voltage       -       0.7*       VDDM       -       0.3*       V         VIH <sub>MA</sub> Low level input voltage       -       -0.4       -       VDDM       -       VDDM       V         VHYSM       Hysteresis of Schmitt trigger       -       -       0.1*       VDDM       -       VDDM       -       VDDM       -       VDDM       V         ILEAK       Input leakage current       -       -       1.5       µ       -       1.5       -       1.5       µ       -       1.5	VDROPL			-	0.2	-	V	
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ADDR (Input)VIHMAHigh level input voltage- $0.7^{*}$ VDDMVILMLow level input voltage- $-0.4$ $0.3^{*}$ VHYSMHysteresis of Schmitt trigger $0.1^{*}$ VDDMVHYSMHysteresis of Schmitt trigger $0.1^{*}$ VDDMVHYSMHysteresis of Schmitt trigger $1.5$ $V$ CIInput leakage current $1.5$ $V$ CIInput capacitance10 $p$ ScLGuite and SDA (input/Output) (**)Interface complex with slave F/S mode I*C interface as described by Philips I*C specification version 2.1dated January, 2000. Please refer to that document for more detailed I*C specifications. $V$ ScL $V$ $V$ $V$ $V$ Not $V$ $V$ $V$ Not $V$ $V$ $V$ VOLLow level output voltageVOLLow level output voltageVILMHigh level input voltage- $0.7^{*}$ VILMLow level input voltage- $0.4$ $0.3^{*}$ VILMLow level input voltage- $0.6$ - $t_{GOL}$ SCL clock frequency- $0.6$ - $t_{GOL}$ LOW period of the SCL clockVDDM >= 1.3V $0.6$ - $t_{HIGH}$ HIGH period of the SCL clockVDDM >= 1.3V $0.6$ - $t_{LOW}$ Data set-up time- $0.0^{(*)}$ $0.9$	t <sub>PULSE</sub>	Reset pulse from host uC	Cf. Figure 7	300	-	-	ns	
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VHYSMHysteresis or Schmitt triggerVDDM-NILLAKInput leakage current1.5-1.5µCIInput apacitance10pSCL (input) and SDA (input/Output) <sup>(3)</sup> Interface complies with slave F/S mode I <sup>2</sup> C interface as described by Philips I <sup>2</sup> C specification version 2.1dated January, 2000. Please refer to that document for more detailed I <sup>2</sup> C specifications.SDA0VOLLow + trIsubart + trVOLLow + trUDDM - 10.3VOLLow + trIsubart + trVDDM - 0.3VVOLLow + trLow + trUDDM - 0.3VVOLLow + etc12UDLM-0.3VVOLLow + etcVDDM - 0.3VDLLow + etcVDDM - 0.3VOLLow + etcVDDM - 0.3VDLLow + etcVDDM - 0.3VDLLow + etcVDDM - 0.3VDLLow + etcVDDM - 0.3VDLLow + etc<	VIL <sub>M</sub>	Low level input voltage	-	-0.4	-		V	
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SCL (Input) and SDA (Input/Output) (3)         Interface complex with slave F/S mode I <sup>2</sup> C interface as described by Philips I <sup>2</sup> C specification version 2.1 dated January, 2000. Please refer to that document for more detailed I <sup>2</sup> C specifications.         SDA         Implement of the second			-	-	-		pF	
Interface complies with slave F/S mode I'C interface as described by Philips I'C specification version 2.1 dated January, 2000. Please refer to that document for more detailed I'C specifications. SDA $t_{t_{t_{t_{t_{t_{t_{D},STA}}}}}}$ $t_{t_{t_{D},DAT}}$ $t_{t_{t_{t_{t_{t_{t}}}}}}$ $t_{t_{t_{t_{t_{t_{t}}}}}}$ $t_{t_{t_{t_{t_{t}}}}}$ $t_{t_{t_{t_{t}}}}$ $t_{t_{t_{t_{t}}}}$ $t_{t_{t_{t_{t}}}}$ $t_{t_{t_{t_{t}}}}$ $t_{t_{t_{t_{t}}}}$ $t_{t_{t_{t_{t}}}}$ $t_{t_{t_{t}}}$ $t_{t_{t_{t_{t}}}}$ $t_{t_{t_{t}}}$ $t_{t_{t_{t}}}$ $t_{t_{t_{t}}}$ $t_{t_{t_{t}}}$ $t_{t_{t_{t}}}$ $t_{t_{t_{t}}}$ $t_{t_{t_{t}}}$ $t_{t_{t_{t}}}$ $t_{t_{t_{t}}}$ $t_{t_{t}}$ $t_{t}$ $t_$	SCL (Inpu	ut) and SDA (Input/Output) (3)						
VOLLow level output voltage0.3VVOLLow level output voltage0.3VVDDM0.3VVOLLow level output voltage0.3VVDDM <= 2V0.3VVILMLow level output voltage0.3VVILMLow level output voltage <th colspan<="" td=""><td>Interface</td><td>complies with slave F/S mode</td><td></td><td></td><td></td><td>on version</td><td>2.1</td></th>	<td>Interface</td> <td>complies with slave F/S mode</td> <td></td> <td></td> <td></td> <td>on version</td> <td>2.1</td>	Interface	complies with slave F/S mode				on version	2.1
SCLVOLLow level output voltage0.3VIOL <sub>M</sub> Low level output sink currentVDDM >= 2V12VIH <sub>MR</sub> High level input voltage6VIL <sub>M</sub> Low level output sink currentVDDM <= 2V	SDA		\\)				_	
$\begin{array}{ c c c c c c } \hline VDDM & >= 2V & - & - & 12 \\ \hline VDDM & < 2V & - & - & 6 \\ \hline VIH_{MR} & High level input voltage & - & VDDM < 2V & - & - & 6 \\ \hline VIH_{MR} & High level input voltage & - & 0.7^* & - & 5.5 & V \\ \hline VIL_M & Low level input voltage & - & -0.4 & - & 0.3^* & V \\ \hline f_{SCL} & SCL clock frequency & - & 0 & - & 400 & kH \\ \hline t_{HD;STA} & Hold time (repeated) START & - & 0.6 & - & - & \mu \\ \hline t_{HGH} & HIGH period of the SCL clock & - & 1.3 & - & - & \mu \\ \hline t_{HIGH} & HIGH period of the SCL clock & - & 1.3 & - & - & \mu \\ \hline t_{HJCAT} & Set-up time for a repeated \\ \hline t_{HD;DAT} & Data hold time & - & 0^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set-up time & - & 100^{(6)} & - & - \\ \hline t_{SU:DAT} & Data set-up time & - & 100^{(6)} & - & - \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 00^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & - & 0.0^{(4)} & - & 0.9^{(5)} & \mu \\ \hline t_{SU:DAT} & Data set work implication & -$			t <sub>SU;STA</sub>	_/₩\	STO-	s	-	
IOLMLow level output sink currentVDDM < 2V6VIHMRHigh level input voltage- $0.7^*$ VDDM- $5.5$ VVILMLow level input voltage0.4- $0.3^*$ VDDMVfscLSCL clock frequency-0-400kHtHD;STAHold time (repeated) START condition-0.6 $\mu$ stLowLOW period of the SCL clock-1.3 $\mu$ stHIGHHIGH period of the SCL clockVDDM >= 1.3V0.6 $\mu$ stHIGHSet-up time for a repeated START condition-0.6 $\mu$ sturestaStart condition-0.6 $\mu$ sturesta-0.6 $\mu$ sturesta-0.6 $\mu$ sturesta-0.6 $\mu$ sturesta-0.6 <td>VOL</td> <td>Low level output voltage</td> <td></td> <td>-</td> <td>-</td> <td>0.3</td> <td>V</td>	VOL	Low level output voltage		-	-	0.3	V	
VIHMRHigh level input voltage-0VILMLow level input voltage-0.7* VDDM-5.5VVILMLow level input voltage0.4- $0.3^*$ VDDMVf_{SCL}SCL clock frequency-0-400kHt_HD;STAHold time (repeated) START condition-0.6 $\mu_S$ t_LOWLOW period of the SCL clock-1.3 $\mu_S$ t_HIGHHIGH period of the SCL clockVDDM >= 1.3V0.6 $\mu_S$ t_{SU;STASet-up time for a repeated START condition-0.6 $\mu_S$ t_HD:DATData hold time-0.6 $\mu_S$ t_HD:DATData set-up time-0.6 $\mu_S$ t_Rise time of both SDA and-0(4)-0.9(5) $\mu_S$	101	Low level output sink current		-	-		mΔ	
VIH_MRHigh level input voltage-VDDM-5.5VVIL_MLow level input voltage0.4- $0.3^*$ VDDMVf_{SCLSCL clock frequency-0-400kHt_{HD;STAHold time (repeated) START condition-0.6 $\mu$ st_{LOWLOW period of the SCL clock-1.3- $\mu$ st_{HIGHHIGH period of the SCL clockVDDM >= 1.3V0.6 $\mu$ st_{HIGHSet-up time for a repeated START condition-0.6 $\mu$ st_{HD;DATData hold time-0.6 $\mu$ st_{HD;DATData hold time-0.6 $\mu$ st_{U:DATData set-up time-100 <sup>(6)</sup> $\mu$ st_Rise time of both SDA and-20+0.1C. <sup>(7)</sup> -300ps	ICLM	Low level output sink current	VDDM < 2V		-	6	шл	
VILMLow level input voltage0.4-VDDMV $f_{SCL}$ SCL clock frequency-0-400kH $t_{HD;STA}$ Hold time (repeated) START condition-0.6 $\mu s$ $t_{LOW}$ LOW period of the SCL clock-1.3 $\mu s$ $t_{HIGH}$ HIGH period of the SCL clockVDDM >= 1.3V0.6 $\mu s$ $t_{HIGH}$ Set-up time for a repeated START condition-0.6 $\mu s$ $t_{HD;DAT}$ Data hold time-0.6 $\mu s$ $t_{HD;DAT}$ Data set-up time-0.6 $\mu s$ $t_{SU;STA}$ Strart condition-0.6 $\mu s$ $t_{HD;DAT}$ Data hold time-0.6 $\mu s$ $t_{SU;DAT}$ Data set-up time-100 <sup>(6)</sup> $t_{Rise time of both SDA and$ -20+0.1C. <sup>(7)</sup> -300ps	VIH <sub>MR</sub>	High level input voltage	-		-		V	
$t_{HD;STA}$ Hold time (repeated) START condition-0.6 $\mu_{S}$ $t_{LOW}$ LOW period of the SCL clock-1.3 $\mu_{S}$ $t_{HIGH}$ HIGH period of the SCL clockVDDM >= 1.3V0.6 $\mu_{S}$ $t_{HIGH}$ HIGH period of the SCL clockVDDM >= 1.3V0.6 $\mu_{S}$ $t_{SU;STA}$ Set-up time for a repeated START condition-0.6 $\mu_{S}$ $t_{HD;DAT}$ Data hold time-0.6 $\mu_{S}$ $t_{SU:DAT}$ Data set-up time-0.9(5) $\mu_{S}$ $t_{SU:DAT}$ Data set-up time-100(6) $t_{SU:DAT}$ Rise time of both SDA and-20+0.10(7)-300ns	VIL <sub>M</sub>	Low level input voltage	-	-0.4	-		V	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	f <sub>SCL</sub>		-	0	-	400	kHz	
t_{HIGH}HIGH period of the SCL clockVDDM >= 1.3V0.6 $t_{SU;STA}$ Set-up time for a repeated START condition-0.6 $\mu$ s $t_{HD;DAT}$ Data hold time-0.6 $\mu$ s $t_{SU;DAT}$ Data set-up time-0(4)-0.9(5) $\mu$ st_{SU;DAT}Data set-up time-100(6)tRise time of both SDA and-20+0.1C.(7)-300ns	t <sub>HD;STA</sub>	condition	-	0.6	-	-	μs	
tHIGHHIGH period of the SCL clockVDDM < 1.3V1 $\mu$ s $t_{SU;STA}$ Set-up time for a repeated START condition-0.6 $\mu$ s $t_{HD:DAT}$ Data hold time-0(4)-0.9(5) $\mu$ s $t_{SU:DAT}$ Data set-up time-100(6)tRise time of both SDA and-20+0.1C.(7)-300ns	t <sub>LOW</sub>	LOW period of the SCL clock	-	1.3	-	-	μs	
$t_{SU;STA}$ Set-up time for a repeated START condition-0.6 $\mu s$ $t_{HD:DAT}$ Data hold time- $0^{(4)}$ - $0.9^{(5)}$ $\mu s$ $t_{SU;DAT}$ Data set-up time- $100^{(6)}$ tRise time of both SDA and- $20+0.10^{(7)}$ - $300$ ns					-		μs	
$t_{HD:DAT}$ Data hold time- $0.9^{(4)}$ - $0.9^{(5)}$ $\mu s$ $t_{SU:DAT}$ Data set-up time- $100^{(6)}$ tRise time of both SDA and- $20+0.10^{(7)}$ - $300$ ns	t <sub>SU;STA</sub>		-	-			μs	
t     Rise time of both SDA and     20+0 1C. <sup>(7)</sup> 300     ns	tup:pat		-	0 <sup>(4)</sup>	-	0.9 <sup>(5)</sup>	μs	
t Rise time of both SDA and $20\pm0.10^{(7)}$ 300 ns			-	•	-	-	μ0	
	t <sub>r</sub>	Rise time of both SDA and SCL signals	-		-	300	ns	



Symbol	Description	Conditions	Min	Тур	Max	Unit		
t <sub>f</sub>	Fall time of both SDA and SCL signals	-	20+0.1C <sub>b</sub> <sup>(7)</sup>	-	300	ns		
t <sub>su;sto</sub>	Set-up time for STOP condition	-	0.6	-	-	μs		
t <sub>BUF</sub>	Bus free time between a STOP and START condition	-	1.3	-	-	μs		
Cb	Capacitive load for each bus line	-	-	-	400	pF		
V <sub>nL</sub>	Noise margin at the LOW level for each connected device (including hysteresis)	-	0.1*VDDM	-	-	v		
V <sub>nH</sub>	Noise margin at the HIGH level for each connected device (including hysteresis)	-	0.2*VDDM	-	-	V		
Miscellar	Miscellaneous							
RPULL	Programmable pull-up/down resistors for IO[0-7]	-	-	60	-	kΩ		
t <sub>PLD</sub>	PLD propagation delay	VCC1,2 & VDDM = 5V VCC1,2 & VDDM = 1.2V		-	25 500	ns		

(1) Assuming no load connected to outputs and inputs fixed to VCC1,2 or GND.

(2) Can be increased in RegAdvanced register. Please refer to §2.2.1 for more details.

(3) All values referred to VIH<sub>MR min</sub> and VIL<sub>M max</sub> levels.

(4) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to VIH<sub>MR min</sub>) to bridge the undefined region of the falling edge of SCL.

(5) The maximum t<sub>HD:DAT</sub> has only to be met if the device does not stretch the LOW period (t<sub>LOW</sub>) of the SCL signal.

(6) A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU;DAT} \ge 250$  ns must then be met.

This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{r max} + t_{SU;DAT} = 1000 + 250$ 

= 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

(7) C<sub>b</sub> = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed.

Table 5 – Electrical Specifications

#### 2.2.1 Increasing I/O Sink and Source Current Capabilities (Boost Mode)

When bit 1 of RegAdvanced register is set, max IOH and IOL spec when VCC1,2 is below VBOOST can be increased together with IDDM and ICC1.2 figures as described below.

IDDM	Low voltage boost threshold Main supply current (I <sup>2</sup> C inactive)		- / (VCC1,2 < VBOOST)	2.0	2.2	2.4	V
IDDM	Main supply current			-		2.4	V
				-	450		1
	(I <sup>2</sup> C inactive)	VDDM = 1.2V			150	250	μA
			/ (VCC1,2 < VBOOST)	-	25	50	uA
		SX1501/2	VCC1 = VBOOST	-	250	350	
ICC1	I/O bank A supply current	5/1501/2	VCC1 = 1.2V	-	100	200	
1001		SX1503	VCC1 = VBOOST	-	250	400	μA
		571505	VCC1 = 1.2V	-	100	200	
	I/O bank B supply current	SX1502	VCC2 = VBOOST	-	150	250	
ICC2		371302	VCC2 = 1.2V	-	50	150	μA
1002		SX1503         VCC2 = VBOOST           VCC2 = 1.2V	VCC2 = VBOOST	-	250	450	
			-	100	200		
/Os set as (	Output						
IOH	High level output source	VCC1	,2 >= VBOOST	-	-	8	mA
	current for all I/Os	VCC2	1,2 < VBOOST	-	-	4	mA
	Low level output sink current	VCC1,2 >= VBOOST		-	-	24	A
IOL -	for the high sink I/Os	VCC1,2 < VBOOST		-	-	12	mA
	Low level output sink current	VCC1	,2 >= VBOOST	-	-	12	<u>س</u> ۸
	for the other I/Os	VCC1,2 < VBOOST		-	-	6	mA
NINT, NRES	SET						
	Low level output sink current	VDD	M >= VBOOST	-	-	12	mA
IULM	for NINT, NRESET	VDD	M < VBOOST	-	-	6	

Table 6 – Electrical Specifications in Boost Mode

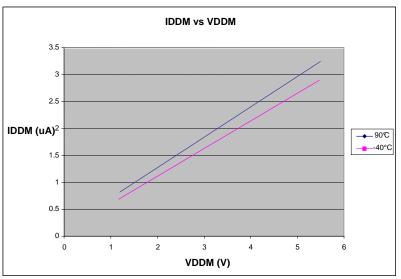
Important: RegAdvanced register doesn't affect any spec when VCC1 and VCC2 are above VBOOST.



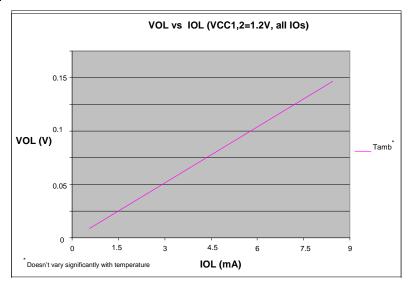
### **3 TYPICAL OPERATING CHARACTERISTICS**

Figures below apply to default registers values (Boost Mode Off), Tamb, unless otherwise specified.

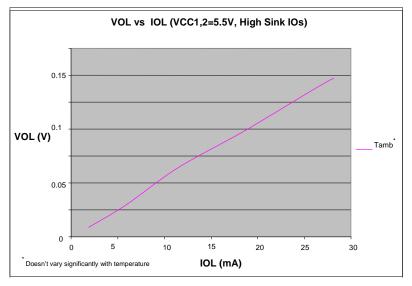
3.1 IDDM vs. VDDM



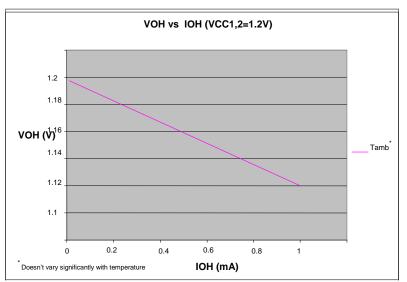
3.2 VOL vs. IOL

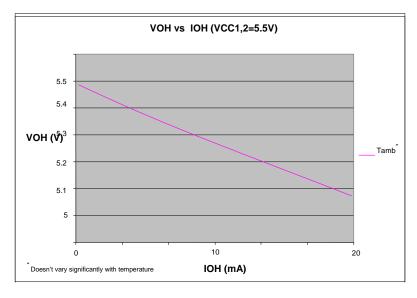






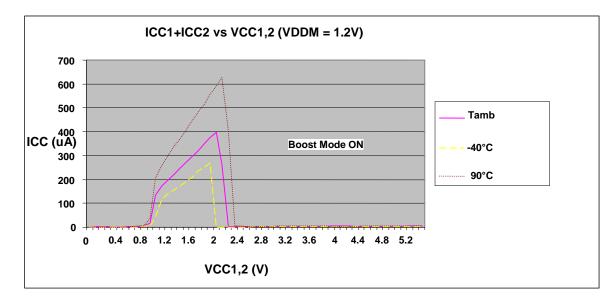
3.3 VOH vs. IOH

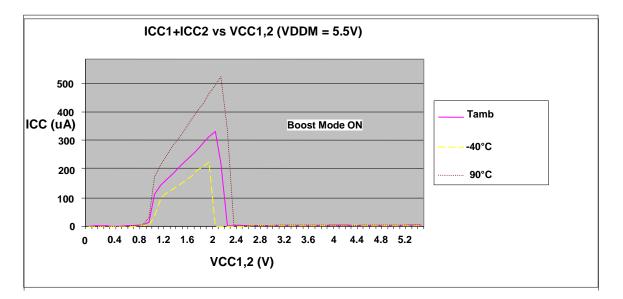






### 3.4 ICC1+ICC2 vs. VCC1,2 when Boost Mode is ON







### 4 BLOCK DETAILED DESCRIPTION

### 4.1 SX1501 4-channel GPIO

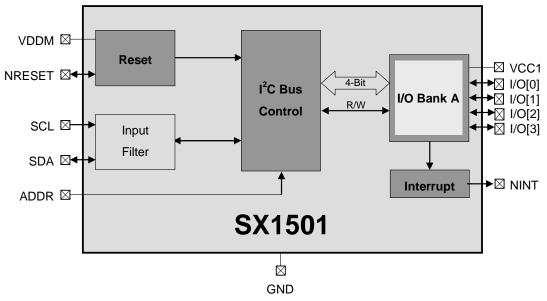


Figure 4 – 4-channel Low Voltage GPIO

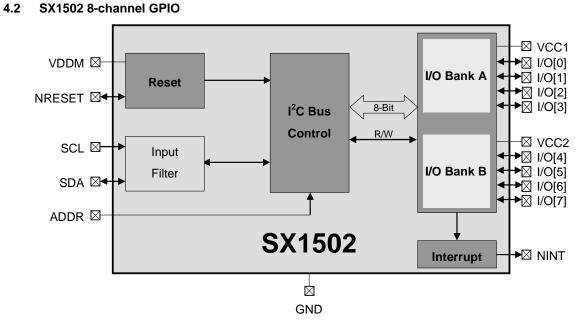
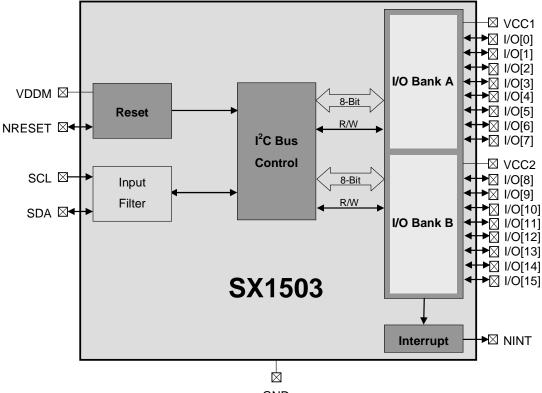


Figure 5 – 8-channel Low Voltage GPIO



### 4.3 SX1503 16-channel GPIO



GND

Figure 6 – 16-channel Low Voltage GPIO

### 4.4 Reset (NRESET)

The SX1501, SX1502 and SX1503 generate their own power on reset signal after a power supply is connected to the VDDM pin. The reset signal is made available for the user at the pin NRESET. The rising edge of the NRESET indicates that the startup sequence of the SX1501, SX1502 or SX1503 has finished. NRESET must be connected to VDDM (or greater) either directly, or via a resistor.

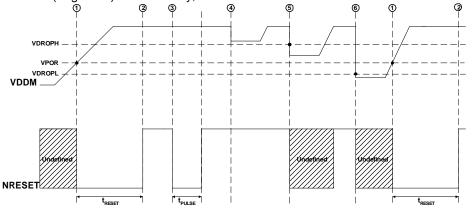


Figure 7 – Power-On / Brown-out Reset Conditions

- 1. Device behavior is undefined until VDDM rises above VPOR, at which point NRESET is driven to GND by the SX1501, SX1502 or SX1503.
- 2. After t<sub>RESET</sub>, NRESET is released (high-impedance) by the SX1501, SX1502 or SX1503 to allow it to be pulled high by an external resistor.
- 3. In operation, the SX1501, SX1502 and SX1503 may be reset at anytime by an external device driving NRESET low during t<sub>PULSE</sub>. Chip can be accessed normally again after NRESET rising edge.



- 4. During a brown-out event, if VDDM drops above VDROPH a reset will not occur.
- 5. During a brown-out event, if VDDM drops between VDROPH and VDROPL a reset may occur.
- 6. During a brown-out event, if VDDM drops below VDROPL a reset will occur next time VPOR is crossed.

Please note that a brown-out event is defined as a transient event on VDDM. If VDDM is attached to a battery, then the gradual decay of the battery voltage will not be interpreted as a brown-out event. Please also note that a sharp rise in VDDM (> 1V/us) may induce a circuit reset.

### 4.5 2-Wire Interface (I<sup>2</sup>C)

The SX1501, SX1502 and SX1503 2-wire interface (I<sup>2</sup>C compliant) operates only in slave mode. In this configuration, the device has one or two device addresses defined by ADDR pin.

Device	ADDR Pin	I <sup>2</sup> C Address	Description		
SX1501 &	0	0x2 <b>0</b> (010000 <b>0</b> )	First address of the 2-wire interface		
SX1502	1	0x21 (0100001)	Second address of the 2-wire interface		
SX1503		0x20 (0100000)	Fixed address of the 2-wire interface		
Table Z. O Mire Interface Address					

Table 7 - 2-Wire Interface Address

2 lines are used to exchange data between an external master host and the slave device:

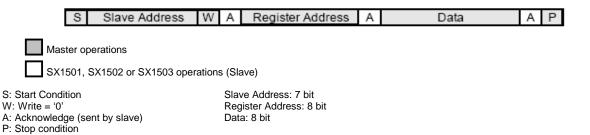
- SCL : Serial CLock
- SDA : Serial DAta

The SX1501, SX1502 and SX1503 are read-write slave-mode  $I^2C$  devices and comply with the Philips  $I^2C$  standard Version 2.1 dated January, 2000. The SX1501, SX1502 and SX1503 have respectively 12, 16, and 31 user-accessible internal 8-bit registers. The  $I^2C$  interface has been designed for program flexibility, in that once the slave address has been sent to the SX1501, SX1502 or SX1503 enabling it to be a slave transmitter/receiver, any register can be written or read independently of each other. While there is no auto increment/decrement capability in the SX1501 and SX1502  $I^2C$  logic, a tight software loop can be designed to access the next register independent of which register you begin accessing. SX1503 implements auto increment capability. The start and stop commands frame the data-packet and the repeat start condition is allowed if necessary.

Seven bit addressing is used and ten bit addressing is not allowed. Any general call address will be ignored by the SX1501, SX1502 and SX1503. The SX1501, SX1502 and SX1503 are not CBUS compatible and can operate in standard mode (100kbit/s) or fast mode (400kbit/s).

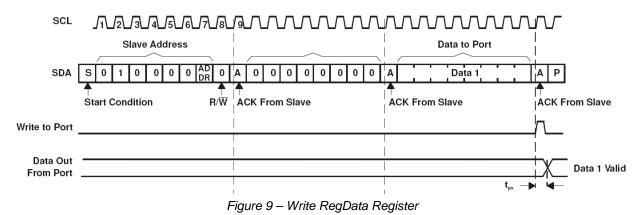
### <u>4.5.1</u> WRITE

The simplest format for an  $I^2C$  write is given below. After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The  $I^2C$  then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the appropriate 8 bit data byte. Once again the slave acknowledges and the master terminates the transfer with the stop condition [P].





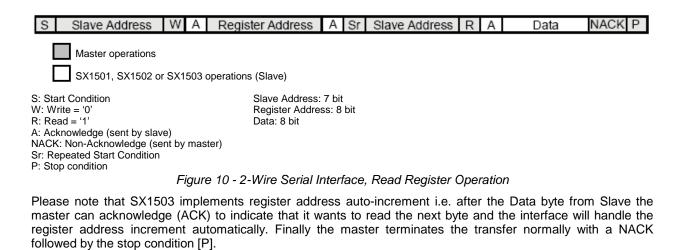




Please note that SX1503 implements register address auto-increment i.e. after the Data ACK from Slave the master can write further bytes and the interface will handle the register address increment automatically. Finally the master terminates the transfer normally the stop condition [P].

### 4.5.2 READ

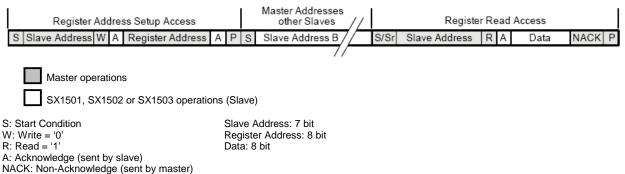
After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The  $I^2C$  then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the repeated start condition [Sr]. Once again, the slave address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge and the previously addressed 8 bit data byte; the master then sends a non-acknowledge (NACK). Finally, the master terminates the transfer with the stop condition [P].



4.5.3 READ - STOP separated format (SX1501 and SX1502 only)

When operating SX1501 or SX1502, stop-separated reads can also be used. This format allows a master to set up the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave address followed by a write command are sent after a start [S] condition. The slave then acknowledges it is being addressed, and the master responds with the 8-bit register address. The master sends a Stop or Restart condition and may then address another slave. After performing other tasks, the master can send a start or restart condition to the slave with a read command. The slave acknowledges this request and returns the data from the register location that had previously been set up.





Sr: Repeated Start Condition

P: Stop condition

Figure 11 - 2-Wire Serial Interface, Read – Stop Separated Mode Operation

### 4.6 Interrupt (NINT)

At start-up, the transition detection logic is reset, and NINT is released to a high-impedance state. The interrupt mask register is set to 0xFF, disabling the interrupt output for transitions on all I/O ports. The transition flags are cleared to indicate no data changes.

An interrupt NINT can be generated on any programmed combination of I/Os rising and/or falling edges through the RegInterruptMask and RegSense registers.

If needed, the I/Os which triggered the interrupt can then be identified by reading RegInterruptSource register.

When NINT is low (i.e. interrupt occurred), it can be reset back high (i.e. cleared) by writing 0xFF in RegInterruptSource (this will also clear corresponding bits in RegEventStatus register). SX1503 also allows the interrupt to be cleared automatically when reading RegData register (Cf. RegAdvanced)

Example: We want to detect rising edge of I/O[1] on SX1502 (NINT will go low).

- 1. We enable interrupt on I/O[1] in RegInterruptMask
- ⇒ RegInterruptMask ="XXXXXX0X"
- 2. We set edge sense for I/O[1] in RegSense
- ⇒ RegSenseLow ="XXXX**01**XX"

### 4.7 **Programmable Logic Functions (PLD)**

The SX1501, SX1502 and SX1503 offer a unique fully programmable logic functions like a PLD to give more flexibility and reduce external logic gates used for standard applications.

Since the whole truth table is fully programmable, the SX1501, SX1502, and SX1503 can implement combinatory functions ranging from the basic AND/OR gates to the most complicated ones with up to four 3-to1 PLDs or two 3-to-2 PLDs which can also be externally cascaded if needed.

In all cases, any IO not configured for PLD functionality retains its GPIO functionality while I/Os used by the PLD have their direction automatically set accordingly.

Please note that while RegDir corresponding bits are ignored for PLD operation they may still be set to input to access unused PLD inputs as normal GPI (PLD truth table can define some inputs to have no effect on PLD output) and/or generate interrupt based on any of the PLD inputs or outputs bits.

### <u>4.7.1</u> SX1501

The SX1501 I/Os can be configured to provide any combinational 2-to-1 logic function using I/O[0-2] whilst retaining GPIO capability on I/O[3] OR provide a combinational 3-to-1 decode function using all 4 I/O ports.

RegPLDMode	SX1501 I/Os					
1:0	3	2	1	0		
00	GPIO	GPIO	GPIO	GPIO		
01	GPIO	PLD OUT	PLD IN	PLD IN		
10	PLD OUT	PLD IN	PLD IN	PLD IN		

Table 8 – SX1501 PLD Modes Settings



### <u>4.7.2</u> SX1502

The SX1502 I/Os can be configured as per the SX1501, and can additionally be configured to provide a 2-to-1 logic function on I/O[4-6], 3-to-1 logic function on I/O[4-7], or 3-to-2 logic decode on I/O[0-4].

RegPL	DMode		SX1502 I/Os								
5:4	1:0	7	6	5	4	3	2	1	0		
00	00	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO		
00	01	GPIO	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN		
00	10	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN	PLD IN		
00	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN		
01	00	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO		
01	01	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN		
01	10	GPIO	PLD OUT	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN		
01	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN		
10	00	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO		
10	01	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN		
10	10	PLD OUT	PLD IN	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN		
10	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN		

Table 9 – SX1502 PLD Modes Settings

### <u>4.7.3</u> SX1503

Each of the two I/O banks of the SX1503 I/Os can be configured as per the SX1502.

RegPLD	ModeB		SX1503 I/Os							
5:4	1:0	15	14	13	12	11	10	9	8	
00	00	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	
00	01	GPIO	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN	
00	10	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN	PLD IN	
00	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	
01	00	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO	
01	01	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN	
01	10	GPIO	PLD OUT	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN	
01	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	
10	00	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO	
10	01	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN	
10	10	PLD OUT	PLD IN	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN	
10	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	

Table 10 – SX1503 PLD Modes Settings (Bank B)

RegPLD	OModeA	SX1503 I/Os							
5:4	1:0	7	6	5	4	3	2	1	0
00	00	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
00	01	GPIO	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN
00	10	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN	PLD IN
00	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN
01	00	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO
01	01	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN
01	10	GPIO	PLD OUT	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN
01	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN
10	00	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO
10	01	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN
10	10	PLD OUT	PLD IN	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN
10	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN

Table 11 – SX1503 PLD Modes Settings (Bank B)



### 4.7.4 Tutorial

The generic method described in this paragraph can be applied to any of the SX1501, SX1502 or SX1503. *Example: We want to implement an AND gate between I/O[0] and IO[1] on SX1502* 

- 1. Identify in the tables above the RegPLDMode setting to be programmed. What we need corresponds to the second line of the SX1502 PLD Table => RegPLDMode = "xx00xx01"
- 2. Fill corresponding RegPLDTableX with the wanted truth table. As mentioned in RegPLDMode description, using PLD 2-to-1 mode on I/0[0-2] implies to fill the truth table located in RegPLDTable0(3:0)

I/O[1]	I/O[0]	I/O[2]
0	0	(0)
0	1	0
1	0	0
1	1	1/

=> RegPLDTable0 = "xxxx(1000)"



### 5 CONFIGURATION REGISTERS

### 5.1 SX1501 4-channel GPIO

Address	Name	Description	Default
0x00	RegData	Data register	1111 1111
0x01	RegDir	Direction register	1111 1111
0x02	RegPullUp	Pull-up register	0000 0000
0x03	RegPullDown	Pull-down register	0000 0000
0x04	Reserved	Unused	XXXX XXXX
0x05	RegInterruptMask	Interrupt mask register	1111 1111
0x06	RegSenseHigh	Unused	XXXX XXXX
0x07	RegSenseLow	Sense register	0000 0000
0x08	RegInterruptSource	Interrupt source register	0000 0000
0x09	RegEventStatus	Event status register	0000 0000
0x10	RegPLDMode	PLD mode register	0000 0000
0x11	RegPLDTable0	PLD truth table 0	0000 0000
0x12	RegPLDTable1	Unused	XXXX XXXX
0x13	RegPLDTable2	PLD truth table 2	0000 0000
0x14	RegPLDTable3	Unused	XXXX XXXX
0x15	RegPLDTable4	Unused	XXXX XXXX
0xAB	RegAdvanced	Advanced settings register	0000 0000

Addr	Name	Default	Bits	Description			
			7:4	Reserved. Must be set to 1 (default value)			
0x00	RegData	0xFF	3:0	Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured.			
			7:4	Reserved. Must be set to 1 (default value)			
0x01	RegDir	0xFF	3:0	Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input			
			7:4	Reserved. Must be set to 0 (default value)			
0x02	RegPullUp	0x00	3:0	Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled			
			7:4	Reserved. Must be set to 0 (default value)			
0x03	RegPullDown	0x00	3:0	Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled			
0x04	Reserved	0xXX	7:0	Unused			
			7:4	Reserved. Must be set to 1 (default value)			
0x05	RegInterruptMask	0xFF	3:0	Configures which [input-configured] IO will trigger an in 0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt	terrupt on NINT pin		
0x06	RegSenseHigh	0xXX	7:0	Unused			
			7:6	Edge sensitivity of I/O[3]	00 : None		
0x07	RegSenseLow	0x00	5:4	Edge sensitivity of I/O[2]	01 : Rising		
0,101	nogodnoozon	0,000	3:2	Edge sensitivity of I/O[1]	10 : Falling		
			1:0	Edge sensitivity of I/O[0]	11 : Both		
			7:4	Reserved. Must be set to 0 (default value)			
0x08	RegInterruptSource	0x00	3:0	Interrupt source (from IOs set in RegInterruptMask) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event as configured in relevant RegSense register occured). Writing '1' clears the bit in RegInterruptSource and in RegEventStatus. When all bits are cleared, NINT signal goes back high.			
0x09		0x00	7:4	Reserved. Must be set to 0 (default value)			



Addr	Name	Default	Bits	Description			
	RegEventStatus		3:0	Event status of all IOs. 0 : No event has occured on this IO 1 : An event has occured on this IO (an edge as config register occured). Writing '1' clears the bit in RegEventStatus and in RegI	nterruptSource if relevant.		
			7:2	If the edge sensitivity of the IO is changed, the bit(s) will Reserved. Must be set to 0 (default value)	il be cleared automatically		
0x10	RegPLDMode	0x00	1:0	PLDMode 00 : PLD disabled – Normal GPIO mode for I/O[3:0] 01 : PLD 2-to-1 mode – I/O[2] is a decode of I/O[1:0] as defined in RegPLDTable0 10 : PLD 3-to-1 mode – I/O[3] is a decode of I/O[2:0] as defined in RegPLDTable2 11 : Not used			
			7:4	Reserved. Must be set to 0 (default value)			
		PLDTable0 0x00	3	Value to be output on I/O[2] when I/O[1:0] = 11			
0x11	0x11 RegPLDTable0		2	Value to be output on I/O[2] when I/O[1:0] = 10	Applies only when PLDMode is		
			1	Value to be output on I/O[2] when I/O[1:0] = 01	set to PLD 2-to-1 mode		
			0	Value to be output on I/O[2] when I/O[1:0] = 00			
0x12	RegPLDTable1	0xXX	7:0	Unused			
			7	Value to be output on I/O[3] when I/O[2:0] = 111			
			6	Value to be output on I/O[3] when I/O[2:0] = 110	_		
			5	Value to be output on I/O[3] when I/O[2:0] = 101			
0x13	RegPLDTable2	0x00	4	Value to be output on $I/O[3]$ when $I/O[2:0] = 100$	Applies only when PLDMode is set to PLD 3-to-1 mode		
			3	Value to be output on $I/O[3]$ when $I/O[2:0] = 011$	Set to FLD 3-to-1 mode		
			2	Value to be output on $I/O[3]$ when $I/O[2:0] = 010$	-		
			0	Value to be output on $I/O[3]$ when $I/O[2:0] = 001$ Value to be output on $I/O[3]$ when $I/O[2:0] = 000$			
0x14	RegPLDTable3	0xXX	7:0				
0x14 0x15	RegPLDTable4	0xXX 0xXX	7:0	Unused			
0.415	Regrieb rable4	0	7.0	Reserved. Must be set to 0 (default value)			
0xAB	RegAdvanced	0x00	1	Boost Mode (Cf. §2.2.1) 0: OFF 1: ON			
			0	Reserved. Must be set to 0 (default value)			

Table 13 – SX1501 Configuration Registers Description

### 5.2 SX1502 8-channel GPIO

Address	Name	Description	Default
0x00	RegData	Data register	1111 1111
0x01	RegDir	Direction register	1111 1111
0x02	RegPullUp	Pull-up register	0000 0000
0x03	RegPullDown	Pull-down register	0000 0000
0x04	Reserved	Unused	XXXX XXXX
0x05	RegInterruptMask	Interrupt mask register	1111 1111
0x06	RegSenseHigh	Sense register for I/O[7:4]	0000 0000
0x07	RegSenseLow	Sense register for I/O[3:0]	0000 0000
0x08	RegInterruptSource	Interrupt source register	0000 0000
0x09	RegEventStatus	Event status register	0000 0000
0x10	RegPLDMode	PLD mode register	0000 0000
0x11	RegPLDTable0	PLD truth table 0	0000 0000
0x12	RegPLDTable1	PLD truth table 1	0000 0000
0x13	RegPLDTable2	PLD truth table 2	0000 0000
0x14	RegPLDTable3	PLD truth table 3	0000 0000
0x15	RegPLDTable4	PLD truth table 4	0000 0000
0xAB	RegAdvanced	Advanced settings register	0000 0000

### Table 14 – SX1502 Configuration Registers Overview

Addr	Name	Default	Bits	Description
0x00	RegData	0xFF	7:0	Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured.
0x01	RegDir	0xFF	7:0	Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input



# ADVANCED COMMUNICATIONS & SENSING

Addr	Name	Default	Bits	Description			
0.00	Deepuillin	000	7.0	Enables the pull-up for each IO			
0x02	RegPullUp	0x00	7:0	0 : Pull-up is disabled 1 : Pull-up is enabled			
				Enables the pull-down for each IO			
0x03	RegPullDown	0x00	7:0	0 : Pull-down is disabled 1 : Pull-down is enabled			
0x04	Reserved	0xXX	7:0	Unused			
				Configures which [input-configured] IO will trigger an inf	errupt on NINT pin		
0x05	RegInterruptMask	0xFF	7:0	0 : An event on this IO will trigger an interrupt			
			7:6	1 : An event on this IO will NOT trigger an interrupt Edge sensitivity of I/O[7]	00 : None		
0x06	PagSansaHigh	0x00	5:4	Edge sensitivity of I/O[6]	01 : Rising		
0000	RegSenseHigh	0000	3:2	Edge sensitivity of I/O[5]	10 : Falling		
			1:0	Edge sensitivity of I/O[4]	11 : Both		
			7:6 5:4	Edge sensitivity of I/O[3]	00 : None 01 : Rising		
0x07	RegSenseLow	0x00	3:2	Edge sensitivity of I/O[2] Edge sensitivity of I/O[1]	10 : Falling		
			1:0	Edge sensitivity of I/O[0]	11 : Both		
				Interrupt source (from IOs set in RegInterruptMask)			
				0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event	as configured in relevant		
0x08	RegInterruptSource	0x00	7:0	RegSense register occured).			
				Writing 141 clears the hit is Destructure and is D			
				Writing '1' clears the bit in RegInterruptSource and in R When all bits are cleared, NINT signal goes back high.	egeventStatus		
-				Event status of all IOs.			
				0 : No event has occured on this IO 1 : An event has occured on this IO (an edge as config	red in relevant PagSanca		
0x09	RegEventStatus	0x00	7:0	register occured).	ared in relevant Regoense		
	-						
				Writing '1' clears the bit in RegEventStatus and in RegI If the edge sensitivity of the IO is changed, the bit(s) wi			
			7:6	Reserved. Must be set to 0 (default value)			
				PLDModeHigh (applies to I/O[7:4])			
			5:4	00 : PLD disabled – Normal GPIO mode for I/O[7:4] 01 : PLD 2-to-1 mode – I/O[6] is a decode of I/O[5:4] as	defined in ReaPI DTable()		
			0.4	10 : PLD 3-to-1 mode - I/O[7] is a decode of I/O[6:4] as			
0x10	Reg DI DMede	0x00	0.0	11 : Reserved			
0,10	RegPLDMode	0,000	3:2	Reserved. Must be set to 0 (default value) PLDModeLow (applies to I/O[3:0])			
				00 : PLD disabled – Normal GPIO mode for I/O[3:0]			
			1:0	01 : PLD 2-to-1 mode – I/O[2] is a decode of I/O[1:0] as 10 : PLD 3-to-1 mode – I/O[3] is a decode of I/O[2:0] as			
				11 : PLD 3-to-2 mode – I/O[4:3] are decode of I/O[2:0] as			
				and RegPLDTable4			
			7	Value to be output on $I/O[6]$ when $I/O[5:4] = 11$	Applies only when		
			<u>6</u> 5	Value to be output on $I/O[6]$ when $I/O[5:4] = 10$ Value to be output on $I/O[6]$ when $I/O[5:4] = 01$	PLDModeHigh is set to PLD 2-		
0:11	BogBI DTchico	0,000	4	Value to be output on I/O[6] when I/O[5:4] = 00 Value to be output on I/O[6] when I/O[5:4] = 00	to-1 mode		
0x11	RegPLDTable0	0x00	3	Value to be output on I/O[2] when I/O[1:0] = 11	Applies only when		
			2	Value to be output on $I/O[2]$ when $I/O[1:0] = 10$	PLDModeLow is set to PLD 2-		
			1 0	Value to be output on $I/O[2]$ when $I/O[1:0] = 01$ Value to be output on $I/O[2]$ when $I/O[1:0] = 00$	to-1 mode		
			7	Value to be output on $I/O[2]$ when $I/O[6:4] = 111$			
			6	Value to be output on $I/O[7]$ when $I/O[6:4] = 110$	]		
			5	Value to be output on $I/O[7]$ when $I/O[6:4] = 101$	Applies only when		
0x12	RegPLDTable1	0x00	4	Value to be output on $I/O[7]$ when $I/O[6:4] = 100$	PLDModeHigh is set to PLD 3-		
			3	Value to be output on I/O[7] when I/O[6:4] = 011 Value to be output on I/O[7] when I/O[6:4] = 010	to-1 mode		
			1	Value to be output on $I/O[7]$ when $I/O[6:4] = 001$	1		
			0	Value to be output on I/O[7] when I/O[6:4] = 000			
0x13	RegPLDTable2	0x00	7	Value to be output on $I/O[3]$ when $I/O[2:0] = 111$	Applies only when		
			6 5	Value to be output on $I/O[3]$ when $I/O[2:0] = 110$ Value to be output on $I/O[3]$ when $I/O[2:0] = 101$	PLDModeLow is set to PLD 3- to-1 mode		
			5 4	Value to be output on $I/O[3]$ when $I/O[2:0] = 101$ Value to be output on $I/O[3]$ when $I/O[2:0] = 100$	4		
			3	Value to be output on $I/O[3]$ when $I/O[2:0] = 001$	]		
			2	Value to be output on I/O[3] when I/O[2:0] = 010			
			1	Value to be output on I/O[3] when I/O[2:0] = 001			

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		0		Description	
		0	Value to be output on I/O[3] when I/O[2:0] = 000		
		7	Value to be output on I/O[4] when I/O[2:0] = 111		
		6	Value to be output on I/O[4] when I/O[2:0] = 110		
		5	Value to be output on I/O[4] when I/O[2:0] = 101	Applies only when	
RegPl DTable3	0×00	4	Value to be output on I/O[4] when I/O[2:0] = 100	Applies only when PLDModeLow is set to PLD 3-	
Regrediables	0,00	3	Value to be output on I/O[4] when I/O[2:0] = 011	to-2 mode	
		2	Value to be output on I/O[4] when I/O[2:0] = 010		
		1	Value to be output on I/O[4] when I/O[2:0] = 001		
		0	Value to be output on I/O[4] when I/O[2:0] = 000		
		7	Value to be output on I/O[3] when I/O[2:0] = 111		
		6	Value to be output on I/O[3] when I/O[2:0] = 110		
		5	Value to be output on I/O[3] when I/O[2:0] = 101		
PegPl DTable/	0×00	4	Value to be output on I/O[3] when I/O[2:0] = 100	Applies only when PLDModeLow is set to PLD 3-	
Kegr LD Table4	0,00	3	Value to be output on I/O[3] when I/O[2:0] = 011	to-2 mode	
		2	Value to be output on I/O[3] when I/O[2:0] = 010		
		1	Value to be output on I/O[3] when I/O[2:0] = 001		
		0	Value to be output on I/O[3] when I/O[2:0] = 000		
		7:2	Reserved. Must be set to 0 (default value)		
			Boost Mode (Cf. §2.2.1)		
RegAdvanced	0x00	1			
		0			
•	RegPLDTable3 RegPLDTable4 RegAdvanced	RegPLDTable4 0x00	RegPLD Table3         0x00         3         2         1           0         1         0         0         6         5         4         5         4         3         2         1         0         3         2         1         0         3         2         1         0         3         2         1         0         3         2         1         0         3         2         1         0         0         7:2         1         0         0         7:2         1         0         1         0         1         0         1         0         1         1         0         1         1         0         1         1         0         1	RegPLDTable3         0x00         3         Value to be output on I/O[4] when I/O[2:0] = 011           2         Value to be output on I/O[4] when I/O[2:0] = 010         1         2         Value to be output on I/O[4] when I/O[2:0] = 010           1         Value to be output on I/O[4] when I/O[2:0] = 001         0         Value to be output on I/O[4] when I/O[2:0] = 001           0         Value to be output on I/O[4] when I/O[2:0] = 000         7         Value to be output on I/O[3] when I/O[2:0] = 111           6         Value to be output on I/O[3] when I/O[2:0] = 110         5         Value to be output on I/O[3] when I/O[2:0] = 101           5         Value to be output on I/O[3] when I/O[2:0] = 101         2         Value to be output on I/O[3] when I/O[2:0] = 101           4         Value to be output on I/O[3] when I/O[2:0] = 011         2         Value to be output on I/O[3] when I/O[2:0] = 010           3         Value to be output on I/O[3] when I/O[2:0] = 011         2         Value to be output on I/O[3] when I/O[2:0] = 010           1         Value to be output on I/O[3] when I/O[2:0] = 001         0         Value to be output on I/O[3] when I/O[2:0] = 000           7:2         Reserved. Must be set to 0 (default value)         8005t Mode (Cf. §2.2.1)         0: OFF           1: ON         0: OFF         1: ON         0: OFF         1: ON	

Table 15 – SX1502 Configuration Registers Description

### 5.3 SX1503 16-channel GPIO

Address Name		Description	Default	
0x00	RegDataB	Data register for Bank B I/O[15:8]	1111 1111	
0x01	RegDataA	Data register for Bank A I/O[7:0]	1111 1111	
0x02	RegDirB	Direction register for Bank B I/O[15:8]	1111 1111	
0x03	RegDirA	Direction register for Bank A I/O[7:0]	1111 1111	
0x04	RegPullUpB	Pull-up register for Bank B I/O[15:8]	0000 0000	
0x05	RegPullUpA	Pull-up register for Bank A I/O[7:0]	0000 0000	
0x06	RegPullDownB	Pull-down register for Bank B I/O[15:8]	0000 0000	
0x07	RegPullDownA	Pull-down register for Bank A I/O[7:0]	0000 0000	
0x08	RegInterruptMaskB	Interrupt mask register for Bank B I/O[15:8]	1111 1111	
0x09	RegInterruptMaskA	Interrupt mask register for Bank A I/O[7:0]	1111 1111	
0x0A	RegSenseHighB	Sense register for I/O[15:12]	0000 0000	
0x0B	RegSenseHighA	Sense register for I/O[7:4]	0000 0000	
0x0C	RegSenseLowB	Sense register for I/O[11:8]	0000 0000	
0x0D	RegSenseLowA	Sense register for I/O[3:0]	0000 0000	
0x0E	RegInterruptSourceB	Interrupt source register for Bank B I/O[15:8]	0000 0000	
0x0F	RegInterruptSourceA	Interrupt source register for Bank A I/O[7:0]	0000 0000	
0x10	RegEventStatusB	Event status register for Bank B I/O[15:8]	0000 0000	
0x11	RegEventStatusA	Event status register for Bank A I/O[7:0]	0000 0000	
0x20	RegPLDModeB	PLD mode register for Bank B I/O[15:8]	0000 0000	
0x21	RegPLDModeA	PLD mode register for Bank A I/O[7:0]	0000 0000	
0x22	RegPLDTable0B	PLD truth table 0 for Bank B I/O[15:8]	0000 0000	
0x23	RegPLDTable0A	PLD truth table 0 for Bank A I/O[7:0]	0000 0000	
0x24	RegPLDTable1B	PLD truth table 1 for Bank B I/O[15:8]	0000 0000	
0x25	RegPLDTable1A	PLD truth table 1 for Bank A I/O[7:0]	0000 0000	
0x26	RegPLDTable2B	PLD truth table 2 for Bank B I/O[15:8]	0000 0000	
0x27	RegPLDTable2A	PLD truth table 2 for Bank A I/O[7:0]	0000 0000	
0x28	RegPLDTable3B	PLD truth table 3 for Bank B I/O[15:8]	0000 0000	
0x29	RegPLDTable3A	PLD truth table 3 for Bank A I/O[7:0]	0000 0000	
0x2A	RegPLDTable4B	PLD truth table 4 for Bank B I/O[15:8]	0000 0000	
0x2B	RegPLDTable4A	PLD truth table 4 for Bank A I/O[7:0]	0000 0000	
0xAD	RegAdvanced	Advanced settings register	0000 0000	

Table 16 - SX1503 Configuration Registers Overview

Addr	Name	Default	Bits	Description

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Addr	Name	Default	Bits	Description	
0x00	RegDataB	0xFF	7:0	Write: Data to be output to the output-configured IOs	n configured
				Read: Data seen at the IOs, independent of the direction configured. Write: Data to be output to the output-configured IOs	
0x01	RegDataA	0xFF	7:0	Read: Data seen at the IOs, independent of the direction	n configured.
				Configures direction for each IO.	
0x02	RegDirB	0xFF	7:0	0 : IO is configured as an output 1 : IO is configured as an input	
				Configures direction for each IO.	
0x03	RegDirA	0xFF	7:0	0 : IO is configured as an output	
				1 : IO is configured as an input	
0x04	RegPullUpB	0x00	7:0	Enables the pull-up for each IO 0 : Pull-up is disabled	
	3		-	1 : Pull-up is enabled	
0.05	DeerDuillin A	0.400	7.0	Enables the pull-up for each IO	
0x05	RegPullUpA	0x00	7:0	0 : Pull-up is disabled 1 : Pull-up is enabled	
				Enables the pull-down for each IO	
0x06	RegPullDownB	0x00	7:0	0 : Pull-down is disabled	
				1 : Pull-down is enabled Enables the pull-down for each IO	
0x07	RegPullDownA	0x00	7:0	0 : Pull-down is disabled	
		ļļ		1 : Pull-down is enabled	
0x08	RegInterruptMaskB	0xFF	7:0	Configures which [input-configured] IO will trigger an int 0 : An event on this IO will trigger an interrupt	errupt on NINT pin
0,00	Regimentuplinasko		7.0	1 : An event on this IO will NOT trigger an interrupt	
		0.55		Configures which [input-configured] IO will trigger an int	errupt on NINT pin
0x09	RegInterruptMaskA	0xFF	7:0	0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt	
			7:6	Edge sensitivity of I/O[15]	00 : None
0.00	DesCanaellishD	0.400	5:4	Edge sensitivity of I/O[14]	01 : Rising
0x0A	RegSenseHighB	0x00	3:2	Edge sensitivity of I/O[13]	10 : Falling
			1:0	Edge sensitivity of I/O[12]	11 : Both
			7:6	Edge sensitivity of I/O[7]	00 : None
0x0B	0x0B RegSenseHighA 0x00		5:4	Edge sensitivity of I/O[6]	01 : Rising 10 : Falling
			3:2 1:0	Edge sensitivity of I/O[5] Edge sensitivity of I/O[4]	11 : Both
			7:6	Edge sensitivity of I/O[11]	00 - Norse
0.00		0x00 5:4 3:2		Edge sensitivity of I/O[10]	00 : None 01 : Rising
0x0C	RegSenseLowB			Edge sensitivity of I/O[9]	10 : Falling
			1:0	Edge sensitivity of I/O[8]	11 : Both
			7:6	Edge sensitivity of I/O[3]	00 : None
0x0D	RegSenseLowA	0x00	5:4	Edge sensitivity of I/O[2]	01 : Rising 10 : Falling
			3:2 1:0	Edge sensitivity of I/O[1] Edge sensitivity of I/O[0]	11 : Both
			1.0	Interrupt source (from IOs set in RegInterruptMaskB)	
				0 : No interrupt has been triggered by this IO	
0,05	Poglatorrum Course D	0,000	7:0	1 : An interrupt has been triggered by this IO (an event a RegSense register occured).	as configured in relevant
0x0E	RegInterruptSourceB	0x00	7:0	Regoense register occurea).	
				Writing '1' clears the bit in RegInterruptSourceB and in I	
				When all bits of both RegInterruptSourceA/B are cleare	d, NINT signal goes back high.
				Interrupt source (from IOs set in RegInterruptMaskA) 0 : No interrupt has been triggered by this IO	
				1 : An interrupt has been triggered by this IO (an event	as configured in relevant
0x0F	RegInterruptSourceA	0x00	7:0	RegSense register occured).	
				Writing '1' clears the bit in RegInterruptSourceA and in RegEventStatusA When all bits of both RegInterruptSourceA/B are cleared, NINT signal goes back high.	
				Event status of all IOs.	a, i olgilai gooo buok nigit.
				0 : No event has occured on this IO	
0x10	RegEventStatusB	0x00	7:0	1 : An event has occured on this IO (an edge as configuregister occured).	ired in relevant RegSense
0,10		0,00	7.0		
				Writing '1' clears the bit in RegEventStatusB and in Reg	
				If the edge sensitivity of the IO is changed, the bit(s) wil	i de cleared automatically



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Addr	Name	Default	Bits	Description	
0x11	RegEventStatusA	0x00	7:0	Event status of all IOs. 0 : No event has occured on this IO 1 : An event has occured on this IO (an edge as configu register occured).	ured in relevant RegSense
				Writing '1' clears the bit in RegEventStatusA and in Reg If the edge sensitivity of the IO is changed, the bit(s) wi	
			7:6	Reserved. Must be set to 0 (default value) PLDModeHighB (applies to I/O[15:12])	
			5:4	00: PLD disabled – Normal GPIO mode for I/O[15:12] 01: PLD 2-to-1 mode – I/O[14] is a decode of I/O[13:12 10: PLD 3-to-1 mode – I/O[15] is a decode of I/O[14:12 11: Reserved	
0x20	RegPLDModeB	0x00	3:2	Reserved. Must be set to 0 (default value)	
			1:0	PLDModeLowB (applies to I/O[11:8]) 00: PLD disabled – Normal GPIO mode for I/O[11:8] 01: PLD 2-to-1 mode – I/O[10] is a decode of I/O[9:8] a 10: PLD 3-to-1 mode – I/O[11] is a decode of I/O[10:8] 11: PLD 3-to-2 mode – I/O[12:11] are decodes of I/O[1 RegPLDTable3B and RegPLDTable4B	as defined in RegPLDTable2B
			7:6	Reserved. Must be set to 0 (default value)	
			5:4	PLDModeHighA (applies to I/O[7:4]) 00 : PLD disabled – Normal GPIO mode for I/O[7:4] 01 : PLD 2-to-1 mode – I/O[6] is a decode of I/O[5:4] as 10 : PLD 3-to-1 mode – I/O[7] is a decode of I/O[6:4] as 11 : Reserved	
0x21	RegPLDModeA	0x00	3:2	Reserved. Must be set to 0 (default value)	
			1:0	PLDModeLowA (applies to I/O[3:0]) 00 : PLD disabled – Normal GPIO mode for I/O[3:0] 01 : PLD 2-to-1 mode – I/O[2] is a decode of I/O[1:0] as 10 : PLD 3-to-1 mode – I/O[3] is a decode of I/O[2:0] as 11 : PLD 3-to-2 mode – I/O[4:3] are decodes of I/O[2:0] and RegPLDTable4A	s defined in RegPLDTable2A
			7	Value to be output on I/O[14] when I/O[13:12] = 11	Applies only when
			6	Value to be output on $I/O[14]$ when $I/O[13:12] = 10$	Applies only when PLDModeHighB is set to PLD
			5 4	Value to be output on $I/O[14]$ when $I/O[13:12] = 01$	2-to-1 mode
0x22	RegPLDTable0B	0x00	3	Value to be output on $I/O[14]$ when $I/O[13:12] = 00$ Value to be output on $I/O[10]$ when $I/O[9:8] = 11$	
			2	Value to be output on I/O[10] when I/O[9:8] = 10	Applies only when
			1	Value to be output on I/O[10] when I/O[9:8] = 01	PLDModeLowB is set to PLD 2-to-1 mode
			0	Value to be output on $I/O[10]$ when $I/O[9:8] = 00$	
			7 6	Value to be output on $I/O[6]$ when $I/O[5:4] = 11$ Value to be output on $I/O[6]$ when $I/O[5:4] = 10$	Applies only when
			5	Value to be output on $I/O[6]$ when $I/O[5:4] = 10$ Value to be output on $I/O[6]$ when $I/O[5:4] = 01$	PLDModeHighA is set to PLD
0.22		0×00	4	Value to be output on $I/O[6]$ when $I/O[5:4] = 00$	2-to-1 mode
0x23	RegPLDTable0A	0x00	3	Value to be output on I/O[2] when I/O[1:0] = 11	Applies only when
			2	Value to be output on $I/O[2]$ when $I/O[1:0] = 10$	PLDModeLowA is set to PLD
			1	Value to be output on $I/O[2]$ when $I/O[1:0] = 01$ Value to be output on $I/O[2]$ when $I/O[1:0] = 00$	2-to-1 mode
			7	Value to be output on $I/O[15]$ when $I/O[14:12] = 111$	
			6	Value to be output on $I/O[15]$ when $I/O[14:12] = 110$	]
			5	Value to be output on $I/O[15]$ when $I/O[14:12] = 101$	Applies only when
0x24	RegPLDTable1B	0x00	4	Value to be output on $I/O[15]$ when $I/O[14:12] = 100$	PLDModeHighB is set to PLD
			3 2	Value to be output on $I/O[15]$ when $I/O[14:12] = 011$ Value to be output on $I/O[15]$ when $I/O[14:12] = 010$	3-to-1 mode
			1	Value to be output on $I/O[15]$ when $I/O[14.12] = 0.01$ Value to be output on $I/O[15]$ when $I/O[14.12] = 0.01$	-
			0	Value to be output on $I/O[15]$ when $I/O[14:12] = 000$	1
			7	Value to be output on I/O[7] when I/O[6:4] = 111	
			6	Value to be output on $I/O[7]$ when $I/O[6:4] = 110$	4
			5	Value to be output on $I/O[7]$ when $I/O[6:4] = 101$	Applies only when
0x25	RegPLDTable1A	0x00	4	Value to be output on $I/O[7]$ when $I/O[6:4] = 100$ Value to be output on $I/O[7]$ when $I/O[6:4] = 011$	PLDModeHighA is set to PLD
			2	Value to be output on $I/O[7]$ when $I/O[6:4] = 010$	3-to-1 mode
			1	Value to be output on I/O[7] when I/O[6:4] = 001	1
			0	Value to be output on I/O[7] when I/O[6:4] = 000	
0x26	RegPLDTable2B	0x00	7	Value to be output on $I/O[11]$ when $I/O[10:8] = 111$	Applies only when BLDModel owB is set to BLD
			6	Value to be output on I/O[11] when I/O[10:8] = 110	PLDModeLowB is set to PLD

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Addr	Name	Default	Bits	Description	
			5	Value to be output on I/O[11] when I/O[10:8] = 101	3-to-1 mode
			4	Value to be output on I/O[11] when I/O[10:8] = 100	
			3	Value to be output on I/O[11] when I/O[10:8] = 011	
			2	Value to be output on I/O[11] when I/O[10:8] = 010	
			1	Value to be output on I/O[11] when I/O[10:8] = 001	
			0	Value to be output on I/O[11] when I/O[10:8] = 000	
			7	Value to be output on I/O[3] when I/O[2:0] = 111	
			6	Value to be output on I/O[3] when I/O[2:0] = 110	
			5	Value to be output on I/O[3] when I/O[2:0] = 101	
0x27	RegPLDTable2A	0x00	4	Value to be output on I/O[3] when I/O[2:0] = 100	Applies only when PLDModeLowA is set to PLD
0721	Regrediableza	0,00	3	Value to be output on I/O[3] when I/O[2:0] = 011	3-to-1 mode
			2	Value to be output on I/O[3] when I/O[2:0] = 010	
			1	Value to be output on I/O[3] when I/O[2:0] = 001	
			0	Value to be output on I/O[3] when I/O[2:0] = 000	
			7	Value to be output on I/O[11] when I/O[10:8] = 111	
			6	Value to be output on I/O[11] when I/O[10:8] = 110	
			5	Value to be output on I/O[11] when I/O[10:8] = 101	Annling anti-united
0x28	RegPLDTable3B	0x00	4	Value to be output on I/O[11] when I/O[10:8] = 100	<ul> <li>Applies only when</li> <li>PLDModeLowB is set to PLD</li> </ul>
0,20	Regi ED Tablead	0,00	3	Value to be output on I/O[11] when I/O[10:8] = 011	3-to-2 mode
			2	Value to be output on I/O[11] when I/O[10:8] = 010	
			1	Value to be output on I/O[11] when I/O[10:8] = 001	
			0	Value to be output on I/O[11] when I/O[10:8] = 000	
			7	Value to be output on I/O[3] when I/O[2:0] = 111	
			6	Value to be output on I/O[3] when I/O[2:0] = 110	
		<b>e3A</b> 0x00	5	Value to be output on I/O[3] when I/O[2:0] = 101	Applies only when PLDModeLowA is set to PLD 3-to-2 mode
0x29	0x29 RegPLDTable3A		4	Value to be output on I/O[3] when I/O[2:0] = 100	
			3	Value to be output on I/O[3] when I/O[2:0] = 011	
			2	Value to be output on I/O[3] when I/O[2:0] = 010	_
			1	Value to be output on I/O[3] when I/O[2:0] = 001	_
			0	Value to be output on $I/O[3]$ when $I/O[2:0] = 000$	
			7	Value to be output on $I/O[12]$ when $I/O[10:8] = 111$	_
			6	Value to be output on $I/O[12]$ when $I/O[10:8] = 110$	_
			5	Value to be output on $I/O[12]$ when $I/O[10:8] = 101$	Applies only when
0x2A	RegPLDTable4B	0x00	4	Value to be output on $I/O[12]$ when $I/O[10:8] = 100$	PLDModeLowB is set to PLD
			3	Value to be output on $I/O[12]$ when $I/O[10:8] = 011$	3-to-2 mode
			2	Value to be output on $I/O[12]$ when $I/O[10:8] = 010$	4
			1	Value to be output on $I/O[12]$ when $I/O[10:8] = 001$	4
		-	0 7	Value to be output on $I/O[12]$ when $I/O[10:8] = 000$	
				Value to be output on $I/O[4]$ when $I/O[2:0] = 111$	-1
			<u>6</u> 5	Value to be output on $I/O[4]$ when $I/O[2:0] = 110$ Value to be output on $I/O[4]$ when $I/O[2:0] = 101$	-1
			5 4	Value to be output on $I/O[4]$ when $I/O[2:0] = 101$ Value to be output on $I/O[4]$ when $I/O[2:0] = 100$	Applies only when
0x2B	RegPLDTable4A	0x00	3	Value to be output on $I/O[4]$ when $I/O[2:0] = 100$ Value to be output on $I/O[4]$ when $I/O[2:0] = 011$	PLDModeLowA is set to PLD
			2	Value to be output on $I/O[4]$ when $I/O[2:0] = 010$	3-to-2 mode
			1	Value to be output on $I/O[4]$ when $I/O[2:0] = 010$	4
			0	Value to be output on $I/O[4]$ when $I/O[2:0] = 000$	1
		1 1	7:3	Reserved. Must be set to 0 (default value)	
0xAD	RegAdvanced	0x00	2	Autoclear NINT on RegData read (Cf. §4.6) 0: OFF.RegInterruptSource must be manually cleared 1: ON.RegInterruptSource is automatically cleared whe Boost Mode (Cf. §2.2.1)	
			1	0: OFF 1: ON	
			0	Reserved. Must be set to 0 (default value)	

Table 17 – SX1503 Configuration Registers Description



### 6 **APPLICATION INFORMATION**

6.1 Typical Application Circuit

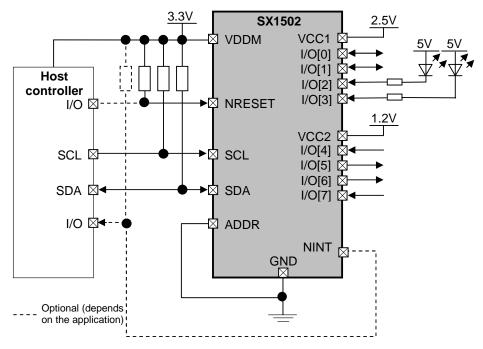
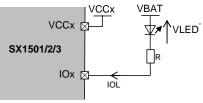


Figure 12 - Typical Application Schematic

### 6.2 Typical LED Operation

Typical LED operation is described below. The LED is usually connected to a high voltage (VBAT) to take advantage of the high sink current of the I/O and to accommodate high LED threshold voltages (VLED).



LED colour/technology dependent

Figure 13 – Typical LED Operation

Important:

- VCCx must exceed VBAT-VLED (VCCx = VBAT is recommended) else the LED will never be completely OFF
- R must be calculated for IOL not to exceed its max spec (Cf. Table 5)

6.2.1	LED ON/OFF	Control

	RegDir[x]	RegData[x]
LED ON	"0" (Output)	" <b>0</b> "
LED OFF		"1"

Table 18 – LED ON/OFF Control



### 6.2.2 LED Intensity Control

When the max IOL spec is not enough it is possible to drive simultaneously multiple I/Os connected together hence increasing the total sink capability.

Example: on an SX1502, by driving an LED with both IO[2] and IO[3] one can sink up to 24+24 =48mA.

Driving an LED with multiple I/Os can also be used to implement more intensity steps for the LED. Example: with two I/Os capable of sinking each 24mA the LED can sink a total of 0mA (no I/O set to "0"), 24mA (one I/O set to "0") or 48mA (both I/Os set to "0") => 3 LED intensity steps ( 4 steps with 3 I/Os, 5 steps with 4 I/Os, etc)

### 6.3 Keypad Implementation

SX1501, SX1502, and SX1503 can be used to implement keypad applications up to 8x8 matrix (i.e. 64 keys)

Example: We want to implement a 4x4matrix keypad on SX1502

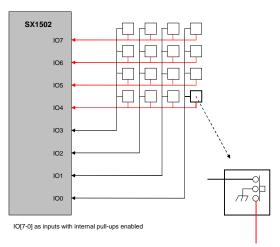


Figure 14 – 4x4 keypad connection to SX1502

- 1. Set all I/Os as inputs with internal pull-up (RegDir = 0xFF, RegPullUp = 0xFF)
- Set NINT to be triggered on any IO's failing edge (RegInterruptMask = 0x00, RegSenseHigh = 0xAA, RegSenseLow = 0xAA)
- 3. When NINT goes low read RegData (or RegInterruptSource) to know the X:Y coordinates of the button which has been pressed.
- 4. Clear NINT (RegInterruptSource = 0xFF, can be done automatically on SX1503 depending on RegAdvanced setting)
- 5. Restart from point 3

### 6.4 Level Shifter Implementation Hints

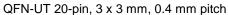
Because of their I/O banks with independent supply voltages between 1.2V and 5.5V, the SX1502 and SX1503 can be easily used to perform level shifting of signals from one I/O bank to an other (uC reads I/O from one I/O bank and sends it back to the other I/O bank)

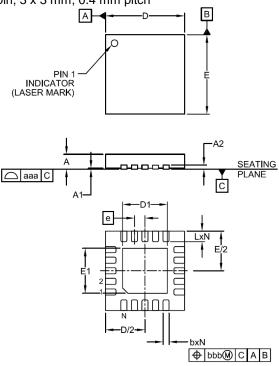
This can save significant BOM cost in a final application where only a few slow signals need to be level-shifted.



### 7 PACKAGING INFORMATION

### 7.1 QFN-UT 20-pin Outline Drawing





	DIMENSIONS							
DIM	1	NCHE	s	MILLIMETERS				
DIN	MIN	NOM	MAX	MIN	NOM	MAX		
Α	.020	-	.024	0.50	-	0.60		
A1	.000	-	.002	0.00	-	0.05		
A2		(.006)			(0.152)			
q	.006	.008	.010	0.15	0.20	0.25		
D	.114	.118	.122	2.90	3.00	3.10		
D1	.061	.067	.071	1.55	1.70	1.80		
Е	.114	.118	.122	2.90	3.00	3.10		
E1	.061	.067	.071	1.55	1.70	1.80		
е		016 BS	С	0	.40 BS	c S		
Г	.012	.016	.020	0.30	0.40	0.50		
Ν		20			20			
aaa	.003				0.08			
bbb		.004			0.10			

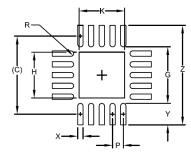
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES),

- 2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
- 3. DAP IS 1.90 x 1.90mm.

Figure 15 - Packaging Information – QFN-UT 20-pin Outline Drawing

### 7.2 QFN-UT 20-pin Land Pattern

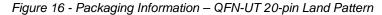


	DIMENSIONS						
DIM	INCHES	MILLIMETERS					
С	(.114)	(2.90)					
G	.083	2.10					
Н	.067	1.70					
K	.067	1.70					
Р	.016	0.40					
R	.004	0.10					
Х	.008	0.20					
Y	.031	0.80					
Z	.146	3.70					

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

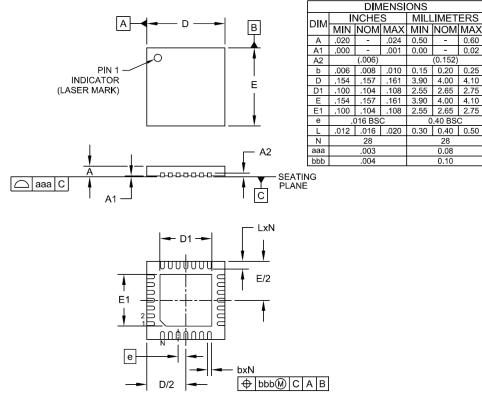
- 2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
- 3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.





### 7.3 QFN-UT 28-pin Outline Drawing

QFN-UT 28-pin, 4 x 4 mm, 0.4 mm pitch



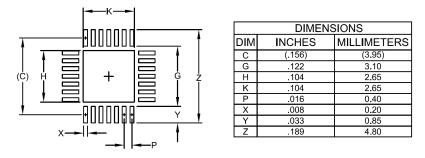
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 17 - Packaging Information – QFN-UT 28-pin Outline Drawing

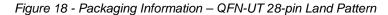
### 7.4 QFN-UT 28-pin Land Pattern



NOTES:

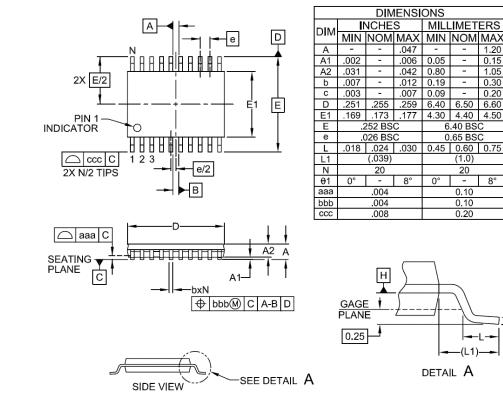
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

- 2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
- THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
   SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.





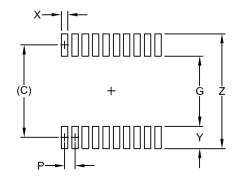
### 7.5 TSSOP 20-pin Outline Drawing



NOTES:

- 1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
- 2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
- 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 4. REFERENCE JEDEC STD MO-153, VARIATION AC. Figure 19 - Packaging Information – TSSOP 20-pin Outline Drawing

### 7.6 TSSOP 20-pin Land Pattern



	DIMENSIONS						
DIM	INCHES	MILLIMETERS					
С	(.222)	(5.65)					
G	.161	4.10					
Р	.026	0.65					
Х	.016	0.40					
Y	.061	1.55					
Ζ	.283	7.20					

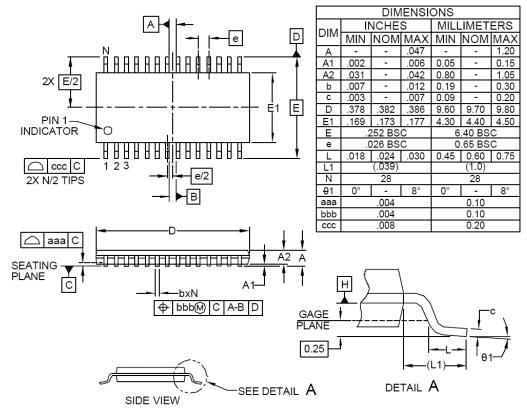
NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.





### 7.7 TSSOP 28-pin Outline Drawing

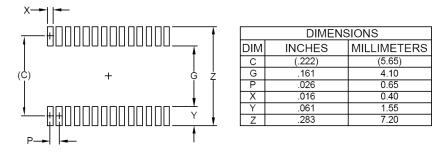


NOTES:

- 1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
- 2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
- 3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 4. REFERENCE JEDEC STD MO-153, VARIATION AE.

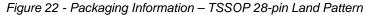
```
Figure 21 - Packaging Information – TSSOP 28-pin Outline Drawing
```

### 7.8 TSSOP 28-pin Land Pattern



NOTES

 THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.





### 8 SOLDERING PROFILE

The soldering reflow profile for the SX1501, SX1502 and SX1503 is described in the standard IPC/JEDEC J-STD-020C. For detailed information please go to <a href="http://www.jedec.org/download/search/jstd020c.pdf">http://www.jedec.org/download/search/jstd020c.pdf</a>

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts <sub>max</sub> to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts <sub>min</sub> ) – Temperature Max (Ts <sub>max</sub> ) – Time (ts <sub>min</sub> to ts <sub>max</sub> )	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T <sub>L</sub> ) – Time (t <sub>L</sub> )	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

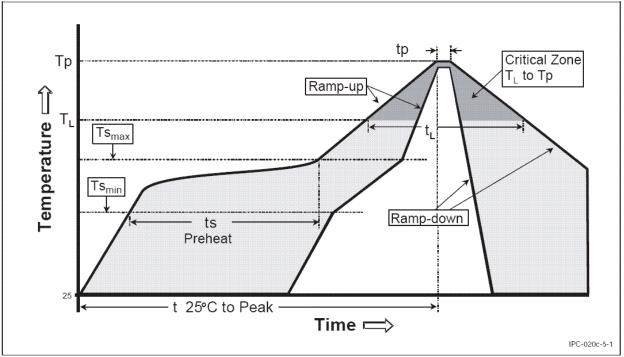


Figure 23 - Classification Reflow Profile (IPC/JEDEC J-STD-020C)



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### **Contact Information**

Semtech Corporation Advanced Communications and Sensing Products Division 200 Flynn Road, Camarillo, CA 93012 Phone: (805) 498-2111 Fax: (805) 498-3804