National Semiconductor

January 1995

MF8 4th-Order Switched Capacitor Bandpass Filter

General Description

The MF8 consists of two second-order bandpass filter stages and an inverting operational amplifier. The two filter stages are identical and may be used as two tracking second-order bandpass filters, or cascaded to form a single fourth-order bandpass filter. The center frequency is controlled by an external clock for optimal accuracy, and may be set anywhere between 0.1 Hz and 20 kHz. The ratio of clock frequency to center frequency is programmable to 100:1 or 50:1. Two inputs are available for TTL or CMOS clock signals. The TTL input will accept logic levels referenced to either the negative power supply pin or the ground pin, allowing operation on single or split power supplies. The CMOS input is a Schmitt inverter which can be made to self-oscillate using an external resistor and capacitor.

By using the uncommitted amplifier and resistors for negative feedback, any all-pole (Butterworth, Chebyshev, etc.) filter can be formed. This requires only three resistors for a fourth-order bandpass filter. Q of the second-order stages may be programmed to any of 31 different values by the five "Q logic" pins. The available Q values span a range from 0.5 through 90. Overall filter bandwidth is programmed by connecting the appropriate Q logic pins to either V^+ or V^-. Filters with order higher than four can be built by cascading MF8s.

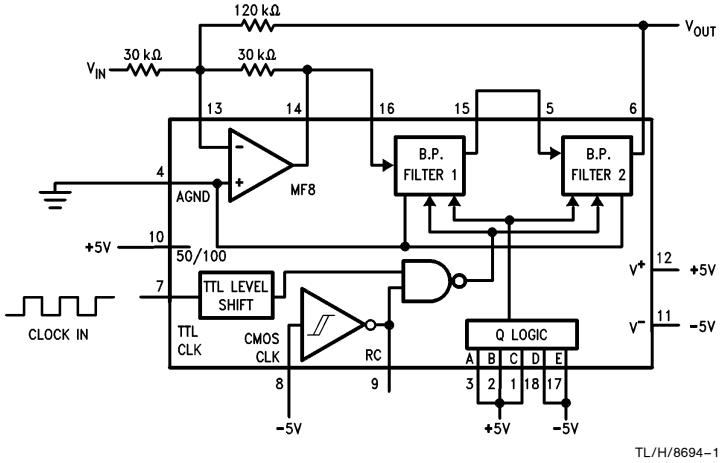
Features

- Center frequency set by external clock
- Q set by five-bit digital word
- Uncommitted inverting op amp
- 4th-order all-pole filters using only three external resistors
- Cascadable for higher-order filters
- Bandwidth, response characteristic, and center frequency independently programmable
- Separate TTL and CMOS clock inputs
- 18 pin 0.3″ wide package

Key Specifications

- Center frequency range 0.1 Hz to 20 kHz
- Q range 0.5 to 90
- Supply voltage range 9V to 14V (±4.5V to ±7V)
- Center frequency accuracy 1% over full temperature range

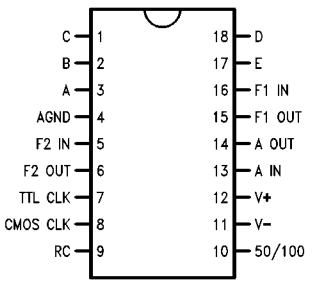
Typical Application & Connection Diagrams



TL/H/8694–1

Fourth-Order Butterworth Bandpass Filter

Dual-In-Line Package



TL/H/8694–2

Top View

Order Number MF8CCJ or MF8CCN
See NS Package Number J18A or N18A

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_S = V^+ - V^-$)	−0.3V to +15V
Voltage at any Input (Note 2)	V^- −0.3V to V^+ +0.3V
Input Current at any Input Pin (Note 2)	±1 mA
Output Short-Circuit Current (Note 7)	±1 mA
Power Dissipation (Note 3)	500 mW
Storage Temperature	−65°C to +150°C
Soldering Information:	
J Package: 10 sec.	260°C
N Package: 10 sec.	300°C
SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

ESD rating is to be determined.

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
MF8CCN	$0°C \le T_A \le +70°C$
MF8CCJ	$-40°C \le T_A \le +85°C$
Supply Voltage ($V_S = V^+ - V^-$)	+9V to +14V
$f_{CLK} \times Q$ Range	
for 10 Hz $\le f_{CLK} \le$ 250 kHz	any Q
for 250 kHz $\le f_{CLK} \le$ 1 MHz	$f_{CLK} \times Q \le$ 5 MHz

Filter Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V^- = -5V$, $C_{LOAD} =$ 50 pF and $R_{LOAD} = 50\ k\Omega$ on filter output unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter (Notes 4, 5)	Conditions	MF8CCN			MF8CCJ			Units
			Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	
H_o	Gain at f_o	$f_{CLK} = 250$ kHz 100:1 ABCDE = 11100	6.02 ±.05	6.02 ±0.2		6.02 ±0.05	6.02 ±0.2		dB
Q	Q		3.92 ±2%	3.92 ±10%		3.92 ±2%	3.92 ±10%		
R	f_{CLK}/f_o		99.2 ±0.3%	99.2 ±1%		99.2 ±0.3%	99.2 ±1%		
H_o	Gain at f_o	$f_{CLK} = 250$ kHz 100:1 ABCDE = 10011	6.02 ±0.2	6.02 ±0.5		6.02 ±0.2	6.02 ±0.5		dB
Q	Q		15.5 ±3%	15.5 ±12%		15.5 ±3%	15.5 ±12%		
R	f_{CLK}/f_o		99.7 ±0.3%	99.7 ±1%		99.7 ±0.3%	99.7±1%		
H_o	Gain at f_o	$f_{CLK} = 250$ kHz 50:1 ABCDE = 00001	5.85 ±0.4	5.85 ±1		5.85 ±0.4	5.85 ±1		dB
Q	Q		55 ±5%	55 ±14%		55 ±5%	55 ±14%		
R	f_{CLK}/f_o		49.9 ±0.2%	49.9 ±1%		49.9 ±0.2%	49.9 ±1%		
H_o	Gain at f_o	$V_S = \pm5V$ ±5% $f_{CLK} \le 250$ kHz	6.02 ±0.5		**6.02 ±1.5**	6.02 ±0.5		**6.02 ±1.5**	dB
$\Delta Q/Q_{TH}$	Q Deviation from Theoretical (See Table I)	$V_S = \pm5V$ ±5% $f_{CLK} \le 250$ kHz, Q > 1	±5%		**±15%**	±5%		**±15%**	
		$f_{CLK} \le 100$ kHz, 1 < Q < 57	±2%		**±6%**	±2%		**±6%**	
$\Delta R/R_{TH}$	f_{CLK}/f_o Deviation from Theoretical (See Table I)	$V_S = \pm5V$ ±5% $f_{CLK} \le 250$ kHz	±0.3%		**±1%**	±0.3%		**±1%**	
Q	Q	$f_{CLK} = 250$ kHz, 50:1 ABCDE = 00110	10.6 ±2%		**10.6 ±10%**	10.6 ±2%	**10.6 ±10%**		
	Dynamic Range (Note 6)	ABCDE = 11100	86			86			dB
		ABCDE = 10011	80			80			dB
		ABCDE = 00001	75			75			dB
	Clock Feedthrough	Filter and Op Amp $f_{CLK} \le 250$ kHz							
		Q ≤ 1	80			80			mV
		Q > 1	40			40			mV
I_S	Maximum Supply Current	$f_{CLK} = 250$ kHz, no loads on outputs	9	12	**12**	9	**13**		mA
V_{OS}	Maximum Filter Output Offset Voltage	$f_{CLK} = 250$ kHz, Q = 4							
		50:1	±40	±120		±40	±120		mV
		100:1	±80	±240		±80	±240		mV
V_{OUT}	Minimum Filter Output Swing	$R_{LOAD} = 5\ k\Omega$ (Note 6)	±4.1	±3.8	**±3.8**	±4.1	**±3.6**		V

Op Amp Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V^- = -5V$ and no load on the Op Amp output unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	MF8CCN			MF8CCJ			Units
			Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	
V_{OS}	Maximum Input Offset Voltage		±8	±20		±8	±20		mV
I_B	Maximum Input Bias Current		10			10			pA
V_{OUT}	Minimum Output Voltage Swing	$R_{LOAD} = 5\ k\Omega$	±3.5			±3.5			V
A_{VOL}	Open Loop Gain		80			80			dB
GBW	Gain Bandwidth Product		1.8			1.8			MHz
SR	Slew Rate		10			10			V/μs

Logic Input and Output Characteristics

The following specifications apply for $V^+ = +10V$ and $V^- = 0V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions	MF8CCN			MF8CCJ			Units
				Typical (Note 9)	Tested Limit (Note 10	Design Limit (Note 11)	Typical (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	
V_T^+	Positive Threshold Voltage on pin 8	Min	$V_S = V^+ - V^-$ referred to $V^- = 0V$ (Note 8)	$0.7V_S$	$0.58V_S$		$0.7V_S$	$0.58V_S$		V
		Max		$0.7V_S$	$0.89V_S$		$0.7V_S$	$0.89V_S$		V
V_T^-	Negative Threshold Voltage on pin 8	Min	$V_S = V^+ - V^-$ referred to $V^- = 0V$ (Note 8)	$0.35V_S$	$0.11V_S$		$0.35V_S$	$0.11V_S$		V
		Max		$0.35V_S$	$0.47V_S$		$0.35V_S$	$0.47V_S$		V
V_{OH}	Output Voltage on pin 9 (Note 12)	Min High	$I_O = -10\ \mu A$		9.0	**9.0**		**9.0**		V
V_{OL}		Max Low	$I_O = +10\ \mu A$		1.0	**1.0**		**1.0**		V
I_{OH}	Output Current on pin 9	Min Source	Pin 9 tied to V^-	6.0	3.0		6.0	3.0		mA
I_{OL}		Min Sink	Pin 9 tied to V^+	5.0	2.5		5.0	2.5		mA
V_{IH}	Input Voltage on pins: 1, 2, 3, 10, 17, & 18 (Note 12)	Min High		7.0		**9.0**	7.0	**9.0**		V
V_{IL}		Max Low		3.0		**1.0**	3.0	**1.0**		V
I_{IN}	Input Current on pins: 1, 2, 3, 7, 8, 10, 17, & 18				10	**10**		**10**		μA
V_{IH}	Input Voltage on pin 7	Min High	$V^+ = +10V$, $V^- = 0V$ or $V^+ = +5V$, $V^- = -5V$		2.0	**2.0**		**2.0**		V
V_{IL}		Max Low			0.8	**0.8**		**0.8**		V

Note 1: Absolute Maximum Raings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: When the applied voltage at any pin falls outside the power supply voltages ($V_{IN} < V^-$ or $V_{IN} > V^+$), the absolute value of current at that pin should be limited to 1 mA or less.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, Θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF8CCN when board mounted is 50°C/W. For the MF8CCJ, this number increases to 65°C/W.

Note 4: The center frequency of each 2nd-order filter section is defined as the frequency where the phase shift through the filter is zero.

Note 5: Q is defined as the measured center frequency divided by the measured bandwidth, where the bandwidth is the difference between the two frequencies where the gain is 3 dB less than the gain measured at the center frequency.

Note 6: Dynamic range is defined as the ratio of the tested minimum output swing of 2.69 Vrms (±3.8V peak-to-peak) to the wideband noise over a 20 kHz bandwidth. For Qs of 1 or less the dynamic range and output swing will degrade because the gain at an internal node is 2/Q. Keeping the input signal level below 1.23xQ Vrms will avoid distortion in this case.

Note 7: If it is possible for a signal output (pin 6, 14, or 15) to be shorted to V^+, V^- or ground, add a series resistor to limit output current.

Note 8: If V^- is anything other than 0V then the value of V^- should be added to the values given in the table. For example for $V^+ = +5V$ and $V^- = -5V$ the typical $V_T^+ = 0.7\ (10V) + (-5V) = +2V$.

Note 9: Typicals are at 25°C and represent the most likely parametric norm.

Note 10: Tested Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Design Limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 12: These logic levels have been referenced to V^-. The logic levels will shift accordingly for split supplies.

Pin Descriptions

Q Logic Inputs A, B, C, D, E (3, 2, 1, 18, 17): These inputs program the Qs of the two 2nd-order bandpass filter stages. Logic "1" is V^+ and logic "0" is V^-.

AGND (4): This is the analog and digital ground pin and should be connected to the system ground for split supply operation or biased to mid-supply for single supply operation. For best filter performance, the ground line should be "clean".

V^+ (12), V^- (11): These are the positive and negative power supply inputs. Decoupling the power supply pins with 0.1 μF or larger capacitors is highly recommended.

F1 IN (16), F2 IN (5): These are the inputs to the bandpass filter stages. To minimize gain error the source impedance should be less than 2 kΩ. Input signals should be referenced to AGND.

F1 OUT (15), F2 OUT (6): These are the outputs of the bandpass filter stages.

A IN (13): This is the inverting input to the uncommitted operational amplifier. The non-inverting input is internally connected to AGND.

A OUT (14): This is the output of the uncommitted operational amplifier.

50/100 (10): This pin sets the ratio of the clock frequency to the bandpass center frequency. Connecting this pin to V^+ sets the ratio to 100:1. Connecting it to V^- sets the ratio to 50:1.

TTL CLK (7): This is the TTL-level clock input pin. There are two logic threshold levels, so the MF8 can be operated on either single-ended or split supplies with the logic input referred to either V^- or AGND. When this pin is not used (or when CMOS logic levels are used), it should be connected to either V^+ or V^-.

CMOS CLK (8): This pin is the input to a CMOS Schmitt inverter. Clock signals with CMOS logic levels may be applied to this input. If the TTL input is used this pin should be connected to V^-.

RC (9): This pin allows the MF8 to generate its own clock signal. To do this, connect an external resistor between the RC pin and the CMOS Clock input, and an external capacitor from the CMOS Clock input to AGND. The TTL Clock input should be connected to V^- or V^+. When the MF8 is driven from an external clock, the RC pin should be left open.

1.0 Application Information

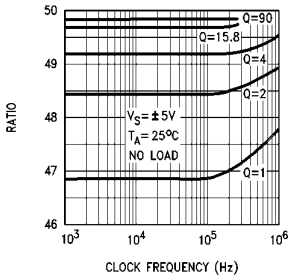
1.1 INTRODUCTION

A simplified block diagram for the MF8 is shown in *Figure 1*. The analog signal path components are two identical 2nd-order bandpass filters and an operational amplifier. Each filter has a fixed voltage gain of 2. The filters' cutoff frequency is proportional to the clock frequency, which may be applied to the chip from an external source or generated internally with the aid of an external resistor and capacitor. The proportionality constant f_{CLK}/f_0 can be set to either 50 or 100 depending on the logic level on pin 10. The "Q" of the two filters can have any of 31 values ranging from 0.5 to 90 and is set by the logic levels on pins 1, 2, 3, 17, and 18. Table I shows the available values of Q and the logic levels required to obtain them. The operational amplifier's non-inverting input is internally grounded, so it may be used only for inverting applications.

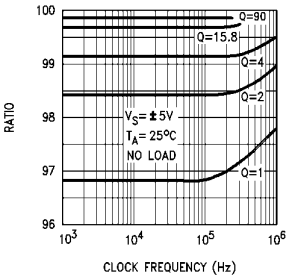
The components in the analog signal path can be interconnected in several ways, three of which are illustrated in *Figures 2a, 2b* and *2c.* The two second-order filter sections can be used as separate filters whose center frequencies track very closely as in *Figure 2a*. Each filter section has a high input impedance and low output impedance. The op amp may be used for gain scaling or other inverting functions. If sharper cutoff slopes are desired, the two filter sections may be cascaded as in *Figure 2b*. Again, the op amp is uncommitted. The circuit in *Figure 2c* uses both filter sections with the op amp and three resistors to build a "multiple feedback loop" filter. This configuration offers the greatest flexibility for fourth-order bandpass designs. Virtually any fourth-order all pole response shape (Butterworth, Chebyshev) can be obtained with a wide range of bandwidths, simply by proper choice of resistor values and Q. The three connection schemes in *Figure 2* will be discussed in more detail in Sections 1.4 and 1.5.

Typical Performance Characteristics

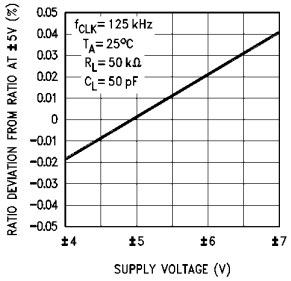
f_{CLK}/f_o Ratio vs Clock Frequency—50:1 Mode



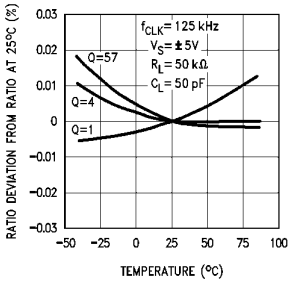
f_{CLK}/f_o Ratio vs Clock Frequency—100:1 Mode



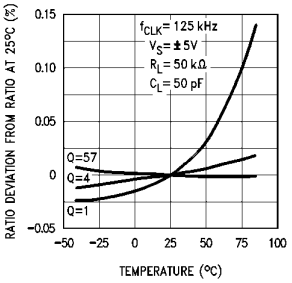
f_{CLK}/f_o Ratio vs Supply Voltage—50:1 and 100:1 Mode



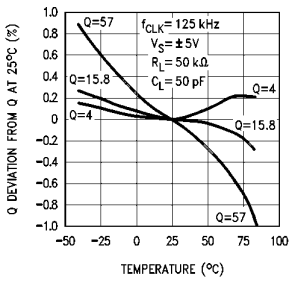
f_{CLK}/f_o Ratio vs Temperature—100:1 Mode



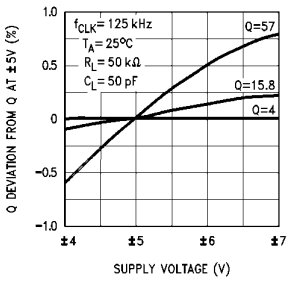
f_{CLK}/f_o Ratio vs Temperature—50:1 Mode



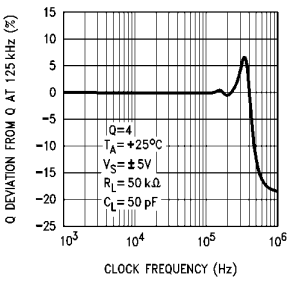
Q vs Temperature—50:1 and 100:1



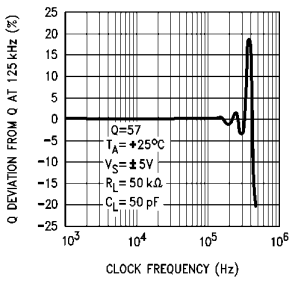
Q vs Supply Voltage—50:1 and 100:1



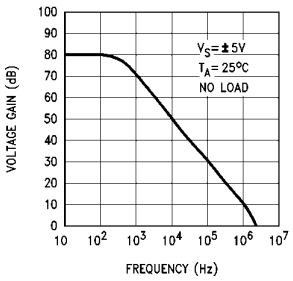
Q vs Clock Frequency—50:1 and 100:1



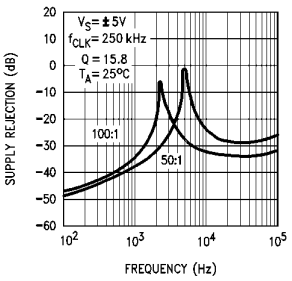
Q vs Clock Frequency—50:1 and 100:1



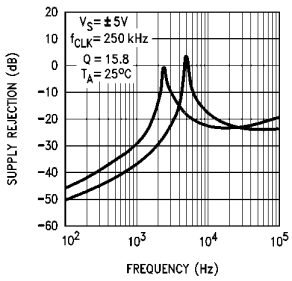
Op Amp—Open Loop Frequency Response



Positive Power Supply Rejection



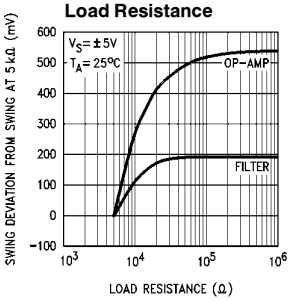
Negative Power Supply Rejection



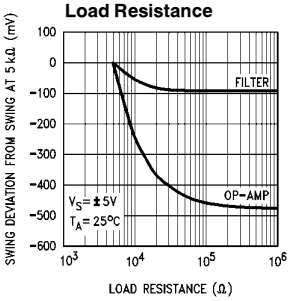
TL/H/8694–24

Typical Performance Characteristics (Continued)

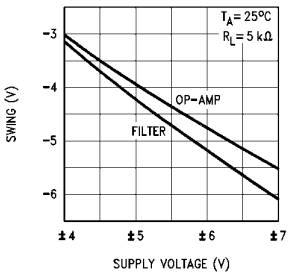
Positive Swing vs Load Resistance



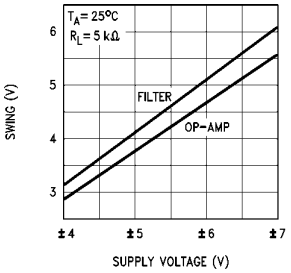
Negative Swing vs Load Resistance



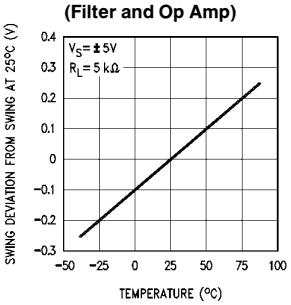
Negative Swing vs Supply Voltage



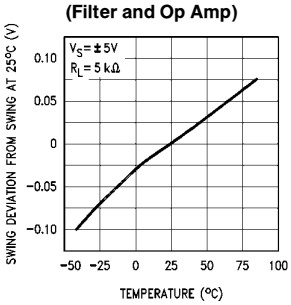
Positive Swing vs Supply Voltage



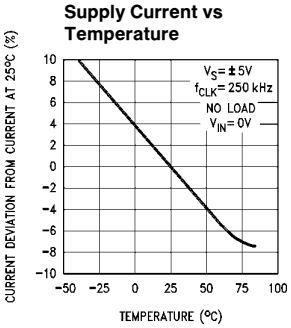
Negative Swing vs Temperature (Filter and Op Amp)



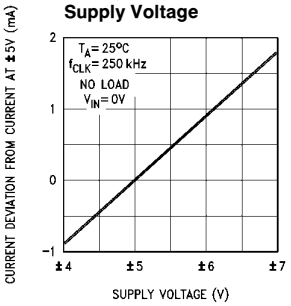
Positive Swing vs Temperature (Filter and Op Amp)



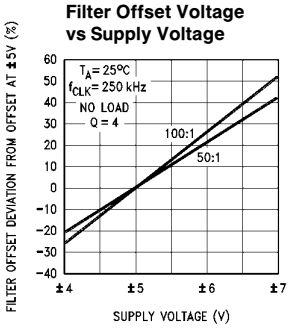
Supply Current vs Temperature



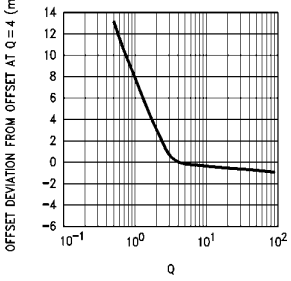
Supply Current vs Supply Voltage



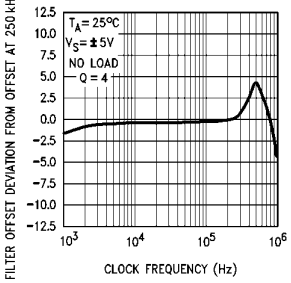
Filter Offset Voltage vs Supply Voltage



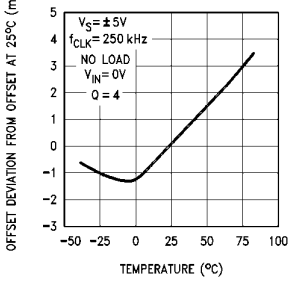
Filter Offset Voltage vs Q—50:1 and 100:1



Filter Offset Voltage vs Clock Frequency—50:1 and 100:1

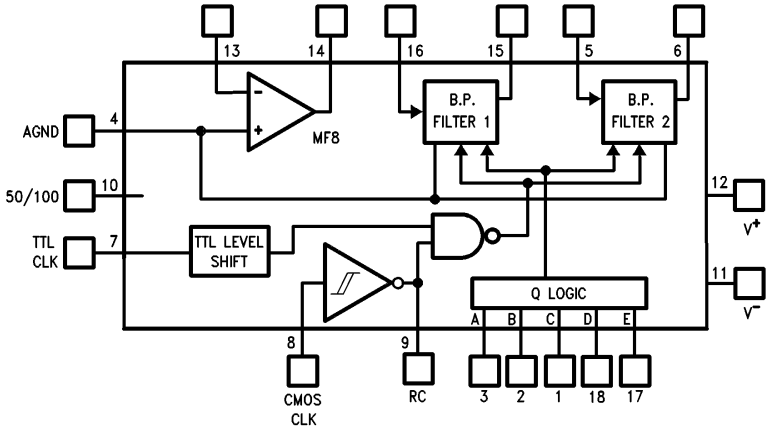


Filter Offset Voltage vs Temperature—50:1 and 100:1



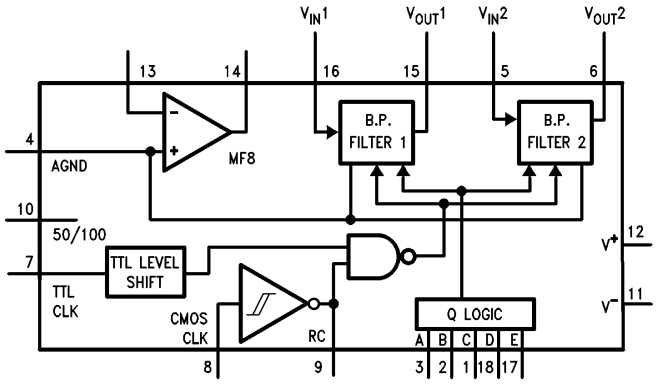
TL/H/8694–25

1.0 Application Information (Continued)



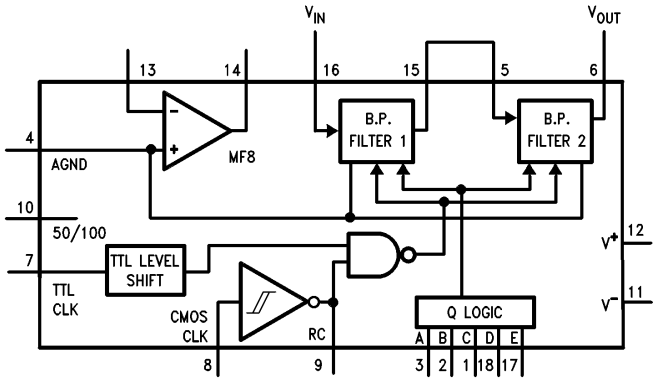
TL/H/8694–3

FIGURE 1. Simplified Block Diagram of the MF8



TL/H/8694–4

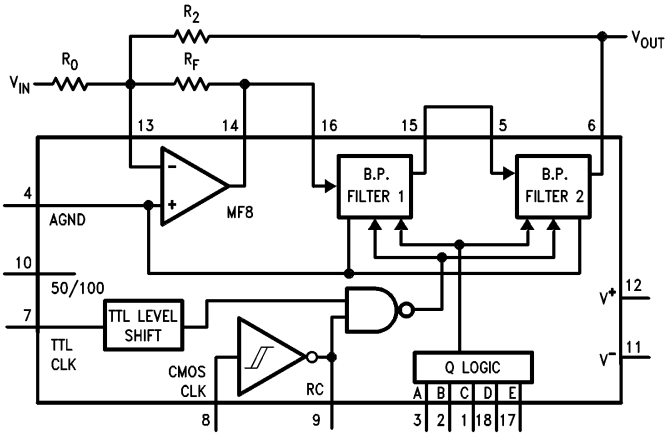
FIGURE 2a. Separate Second-Order "Tracking" Filters



TL/H/8694–5

FIGURE 2b. Fourth-Order Bandpass Made by Cascading Two Second-Order Stages

1.0 Application Information (Continued)



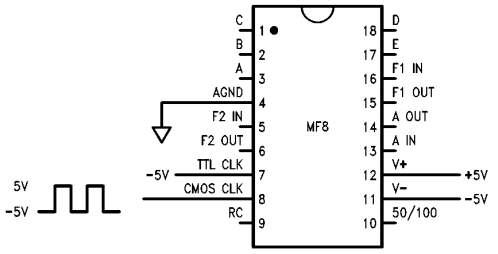
TL/H/8694–6

FIGURE 2c. Multiple Feedback Loop Connection

1.2 CLOCKS

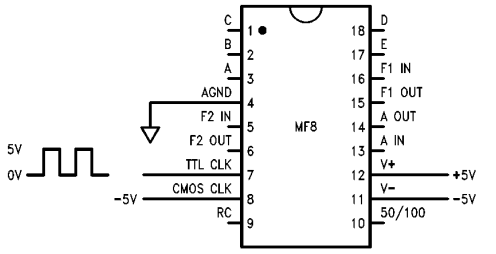
The MF8 has two clock input pins, one for CMOS logic levels and the other for TTL levels. The TTL (pin 7) input automatically adjusts its switching threshold to enable operation on either single or split power supplies. When this input is used, the CMOS logic input should be connected to pin 11(V^-). The CMOS Schmitt trigger input at pin 8 accepts CMOS logic levels. When it is used, the TTL input should be connected to either pin 11 (V^-) or pin 12 (V^+). The basic clock hookups for single and split supply operation are shown in *Figures 3* and *4*.

Clock signals derived from a crystal-controlled oscillator are recommended when maximum center frequency accuracy is desired, but in less critical applications the MF8 can generate its own clock signal as in *Figures 3c* and *4c*. An external resistor and capacitor determine the oscillation frequency. Tolerance of these components and part-to-part variations in Schmitt-trigger logic thresholds limit the accuracy of the RC clock frequency. In the self-clocked mode the TTL Clock input should be connected to either pin 11 or pin 12.



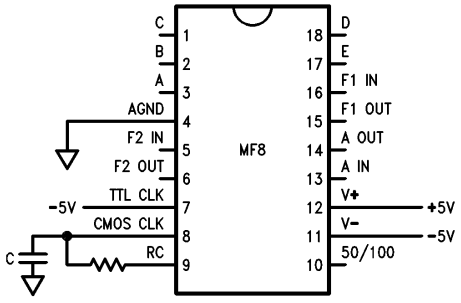
TL/H/8694–7

(a) MF8 Driven with CMOS Logic Level Clock



TL/H/8694–8

(b) MF8 Driven with TTL Logic Level Clock



$$f_{CLK} = \frac{1}{RC \ln\left|\left(\frac{V_S - V_{T-}}{V_S - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right|}$$

Typically for $V_S^* = 10V$

$$f_{CLK} = \frac{1}{1.69\ RC}$$

$^*V_S = V^+ - V^-$

TL/H/8694–9

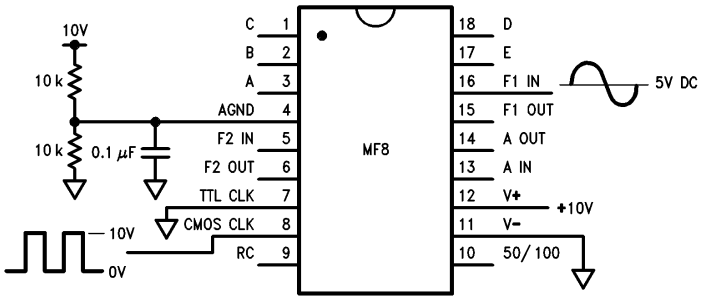
(c) MF8 Driven with Schmitt Trigger Oscillator

FIGURE 3. Dual Supply Operation

1.0 Application Information (Continued)

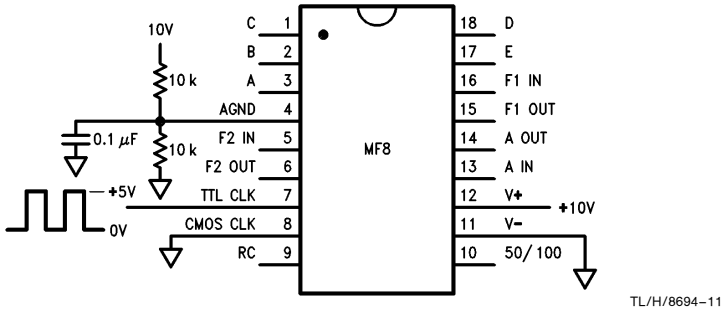
1.3 POWER SUPPLIES AND ANALOG GROUND

The MF8 can be operated from single or dual-polarity power supplies. For dual-supply operation, the analog ground (pin 4) should be connected to system ground. When single supplies are used, pin 4 should be biased to $V^+/2$ as in *Figures 3* and *4*. The input signal should either be capacitively coupled to the filter input or biased to $V^+/2$. It is strongly recommended that each power supply pin be bypassed to ground with at least a 0.1 μF ceramic capacitor. In single supply applications, with V^- connected to ground, V^+ and AGND should be bypassed to system ground.



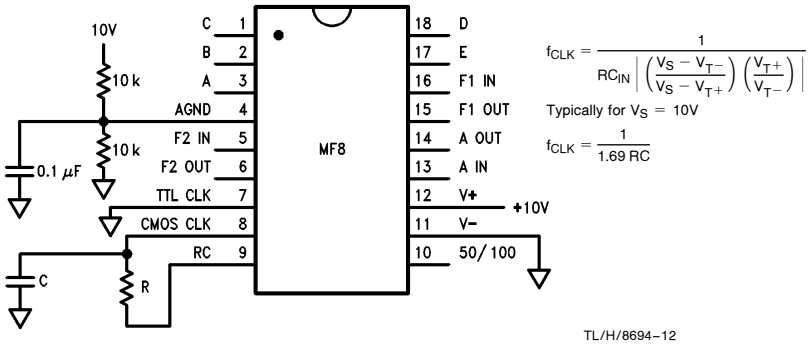
TL/H/8694–10

(a) MF8 Driven with CMOS Logic Level Clock



TL/H/8694–11

(b) MF8 Driven with TTL Logic Clock



TL/H/8694–12

(c) MF8 Driven with the Schmitt Trigger Oscillator

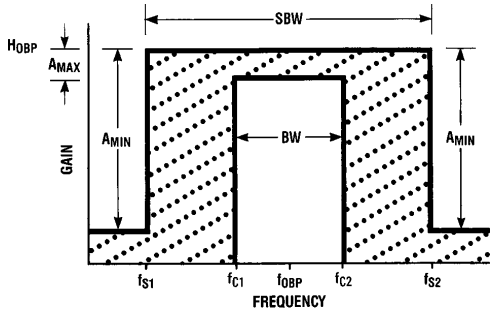
FIGURE 4. Single supply operation. The AGND pin must be biased to mid-supply. The input signal should be dc biased to mid-supply or capacitor-coupled to the input pin.

1.0 Application Information (Continued)

1.4 MULTIPLE FEEDBACK LOOP CONFIGURATION

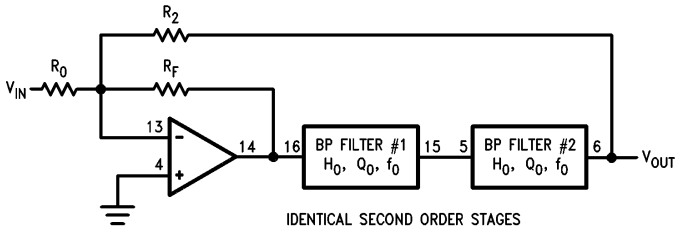
The multi-loop approach to building bandpass filters is highly flexible and stable, yet uses few external components. *Figure 5* shows the MF8's internal operational amplifier and two second-order filter stages with three external resistors in a fourth-order multiple feedback configuration. Higher-order filters may be built by adding more second-order sections and feedback resistors as in *Figure 6*. The filter's response is determined by the clock frequency, the clock-to-center-frequency ratio, the ratios of the feedback resistor values, and the Qs of the second-order filter sections. The design procedure for multiple feedback filters can be broken down into a few simple steps:

1) Determine the characteristics of the desired filter. This will depend on the requirements of the particular application. For a given application, the required bandpass response can be shown graphically as in *Figure 7*, which shows the limits for the filter response. *Figure 7* also makes use of several parameters that must be known in order to design a filter. These parameters are defined below in terms of *Figure 7*.



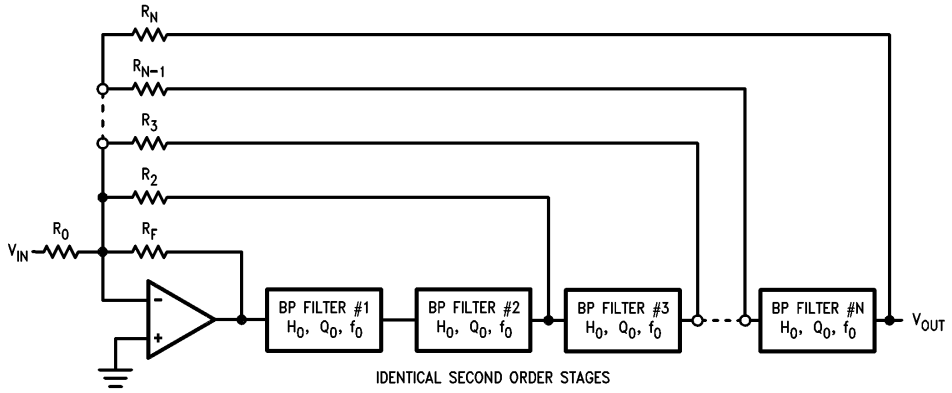
TL/H/8694–15

FIGURE 7. Graphical representation of the amplitude response specifications for a bandpass filter. The filter's response should fall within the shaded area.



TL/H/8694–13

FIGURE 5. General fourth-order multiple-feedback bandpass filter circuit. MF8 pin numbers are shown.



TL/H/8694–14

FIGURE 6. By adding more second-order filter stages and feedback resistors, higher order multiple-feedback filters may be built.

1.0 Application Information (Continued)

f_{C1} and f_{C2}: The filter's lower and upper cutoff frequencies. These define the filter's passband.

f_{S1} and f_{S2}: The boundaries of the filter's stopband.

BW: The filter's bandwidth. $BW = f_{C2} - f_{C1}$.

SBW: The width of the filter's stopband. $SBW = f_{S2} - f_{S1}$.

f_0: The center frequency of the filter. f_0 is equal to the geometric mean of f_{C1} and f_{C2}: $f_0 = \sqrt{f_{C1} f_{C2}}$. f_0 is also equal to the geometric mean of f_{S1} and f_{S2}.

H_{0BP}: The nominal passband gain of the bandpass filter. This is normally taken to be the gain at f_0.

f_0/BW: The ratio of the center frequency to the bandwidth. For second-order filters, this quantity is also known as "Q".

SBW/BW: The ratio of stopband width to bandwidth. This quantity is also called "Omega" and may be represented by the symbol "Ω".

A_{max}: The maximum allowable gain variation within the filter passband. This will depend on the system requirements, but typically ranges from a fraction of a dB to 3 dB.

A_{min}: The minimum allowable attenuation in the stopband. Again, the required value will depend on system constraints.

2). Choose a Butterworth or Chebyshev response characteristic. Butterworth bandpass filters are monotonic on either side of the center frequency, while Chebyshev filters will have "ripple" in the passband, but generally faster attenuation outside the passband. Chebyshev filters are specified according to the amount of ripple (in dB) within the passband.

3) Determine the filter order necessary to meet the response requirements defined above. This may be done with the aid of the nomographs in *Figures 8* and *9* for Butterworth and Chebyshev filters. To use the nomographs, draw a line through the desired values on the A_{MAX}/A_{MIN} scales to the left side of the graph. Draw a horizontal line to the right of this point and mark its intersection with the vertical line corresponding to the required ratio SBW/BW. The required filter order will be equal to the number of the curve falling on or just above the intersection of the two lines. This is illustrated in *Figure 10* for a Chebyshev filter with 1 dB ripple, 30 dB minimum attenuation in the stopband, and $SBW/BW = 3$. From the *Figure,* the required filter order is 6.

4) The design tables in section 2.0 can now be used to find the component values that will yield the desired response for filters of order 4 through 12. The "K_n" give the ratios of resistors "R_n" to R_F, and K_Q is Q divided by f_0/BW.

As an example of the Tables' use, consider a fourth-order Chebyshev filter with 0.5 dB ripple and $f_0/BW = 6$. Begin by choosing a convenient value for R_F, such as 100 kΩ. From the "0.5 dB Chebyshev" filter table, $K_0 = R_0/R_F = 1.3405$. This gives $R_0 = R_F \times 1.345 = 134.05k$. In a similar manner, R_2 is found to equal 201.61k. Q is found using the column labeled K_Q. This gives $Q = K_Q \times f_0/BW = 8.4174$.

Table I shows the available Q values; the nearest value is 8.5, which is programmed by tying pins 1, 2, 3, and 18 to V^+ and pin 17 to V^-.

Note that the resistor values obtained from the tables are normalized for center frequency gain $H_{OBP} = 1$. For different gains, simply divide R_0 by the desired gain.

5) Choose the clock-to-center-frequency ratio. This will nominally be 100:1 when pin 10 is connected to pin 12(V^+) and 50:1 when pin 10 is connected to pin 11(V^-). 100:1 generally gives a response curve nearer the ideal and fewer (if any) problems with aliasing, while 50:1 allows operation over the highest octave of center frequencies (10 kHz to 20 kHz). Supply the MF8 with a clock signal of the appropriate frequency to either the TTL or CMOS input, depending on the available clock logic levels.

TABLE I. Q and Clock-to-Center-Frequency Ratio Versus Logic Levels on "Q-set" Pins

	50:1 mode		100:1 mode	
ABCDE	**F_{CLK}/F_o**	**Q**	**F_{CLK}/F_o**	**Q**
10000	43.7	0.45	94.0	0.47
11000	45.8	0.71	95.8	0.73
01000	46.8	0.96	96.8	0.98
10100	48.4	2.0	98.4	2.0
00100	48.7	2.5	98.7	2.5
01100	48.9	3.0	98.9	3.0
11100	49.2	4.0	99.2	4.0
01010	49.3	5.0	99.3	5.0
10010	49.4	5.7	99.4	5.7
10110	49.4	6.4	99.4	6.4
00010	49.5	7.6	99.5	7.6
11110	49.6	8.5	99.6	8.5
00110	49.6	10.6	99.6	10.6
11001	49.6	11.7	99.6	11.7
11010	49.7	12.5	99.7	12.5
11101	49.7	13.6	99.7	13.6
01001	49.7	14.7	99.7	14.7
10011	49.7	15.8	99.7	15.8
10101	49.7	16.5	99.7	16.5
01110	49.7	17	99.7	17
10001	49.8	19	99.8	19
10111	49.8	22	99.8	22
11011	49.8	27	99.8	27
11111	49.8	30	99.8	30
00101	49.8	33	99.8	33
01011	49.8	40	99.8	40
00111	49.8	44	99.8	44
00001	49.9	57	99.9	57
01101	49.9	68	99.9	68
00011	49.9	79	99.9	79
01111	49.9	90	99.9	90

1.0 Application Information (Continued)

Higher-order filters are designed in a similar manner. An eighth-order Chebyshev with 0.1 dB ripple, center frequency equal to 1 kHz, and 100 Hz bandwidth, for example, could be built as in *Figure 11* with the following component values:

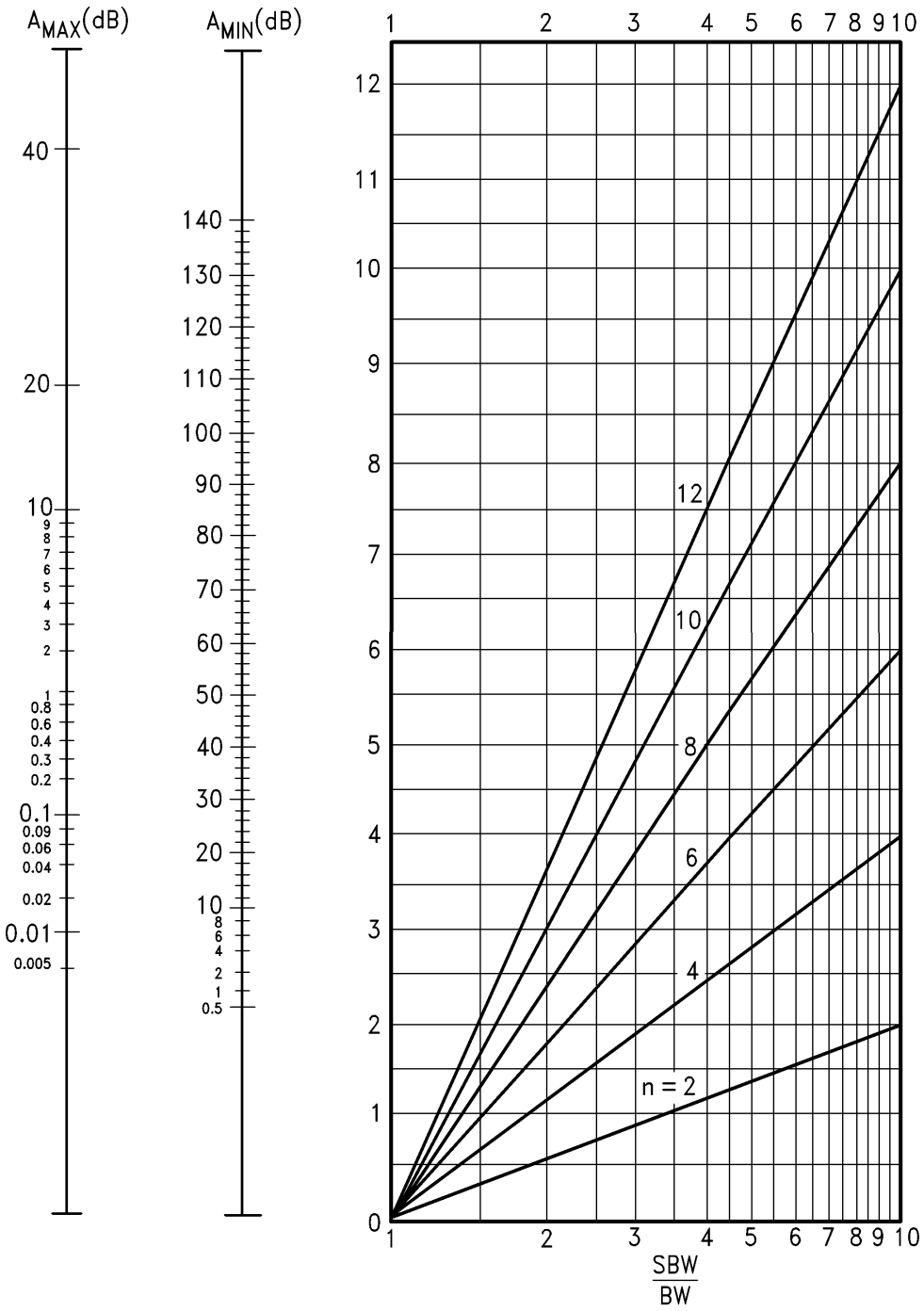
$R_0 = 79.86k$
$R_F = 100k$
$R_2 = 57.82k$
$R_3 = 188.08k$
$R_4 = 203.42k$

Pins 1, 3, 17 and 18 high, pin 2 low. For 100:1 clock-to-center-frequency ratio, pin 10 is tied to V^+ and the clock frequency is 100 kHz. For 50:1 clock-to-center-frequency ratio, pin 10 is tied to V^- and the clock frequency is 50 kHz.

When building filters of order 4 or higher, best performance will always be realized when the filter blocks are cascaded in numerical order: Filter 1 (pins 16 and 15) should always precede Filter 2 (pins 5 and 6). If a second MF8 is used, Filter 2 of the first MF8 should precede Filter 1 of the second MF8, and so on.

Dynamic Considerations

Some filter response characteristics will result in high gain at certain internal nodes, particularly at the op amp output. This can cause clipping in intermediate stages even when no clipping is evident at the filter output. The consequences are significant distortion and degradation of the overall transfer function. The likelihood of clipping at the op amp output becomes greater as R_F/R_0 increases. As the design tables show, R_F/R_0 increases with increasing filter order and increasing ripple. It is good practice to keep out-of-band input signal levels small enough that the first stage can't overload.



TL/H/8694–16

FIGURE 8. Butterworth Bandpass Filter Design Nomograph

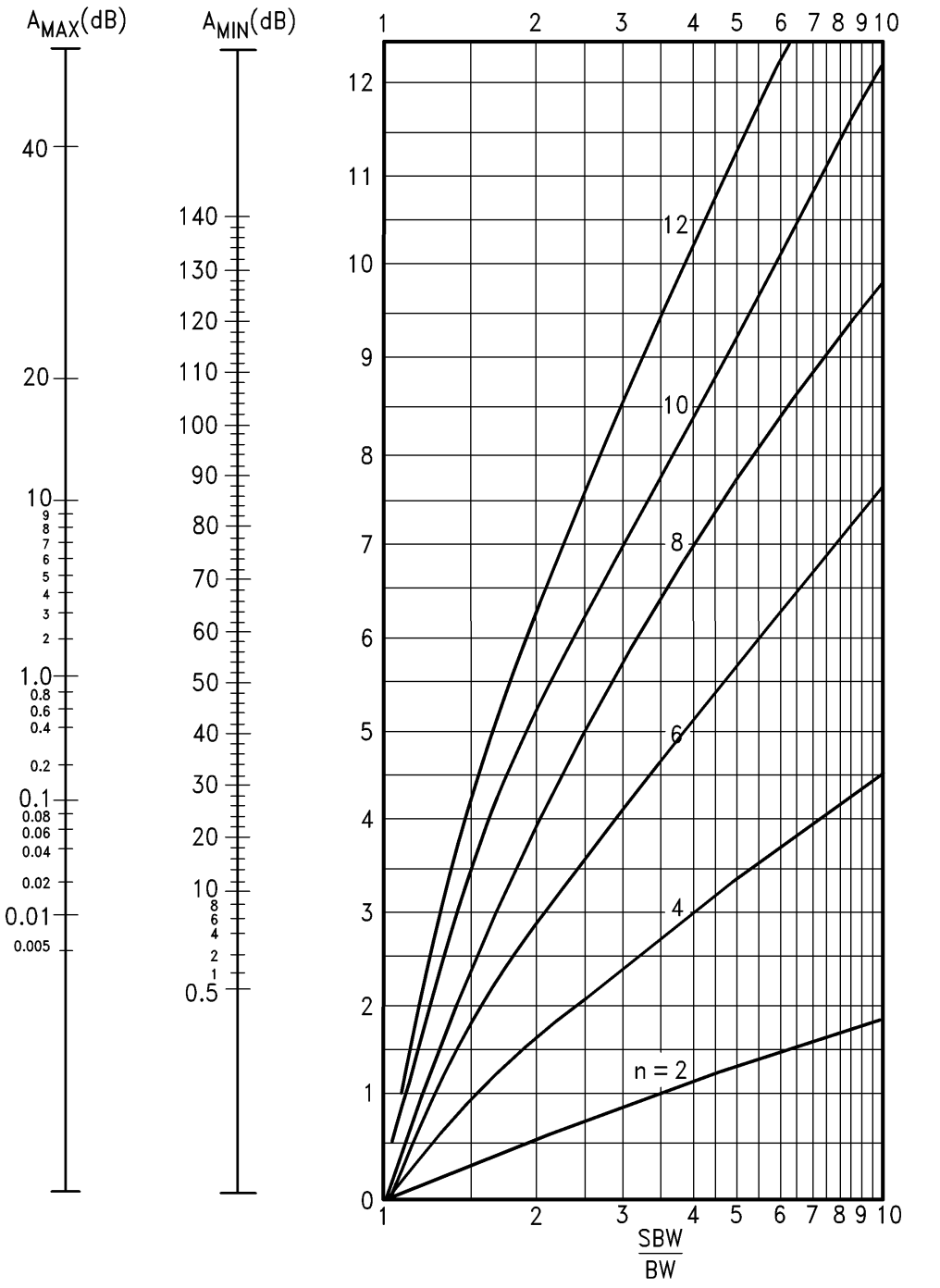


FIGURE 9. Chebyshev Bandpass Filter Design Nomograph

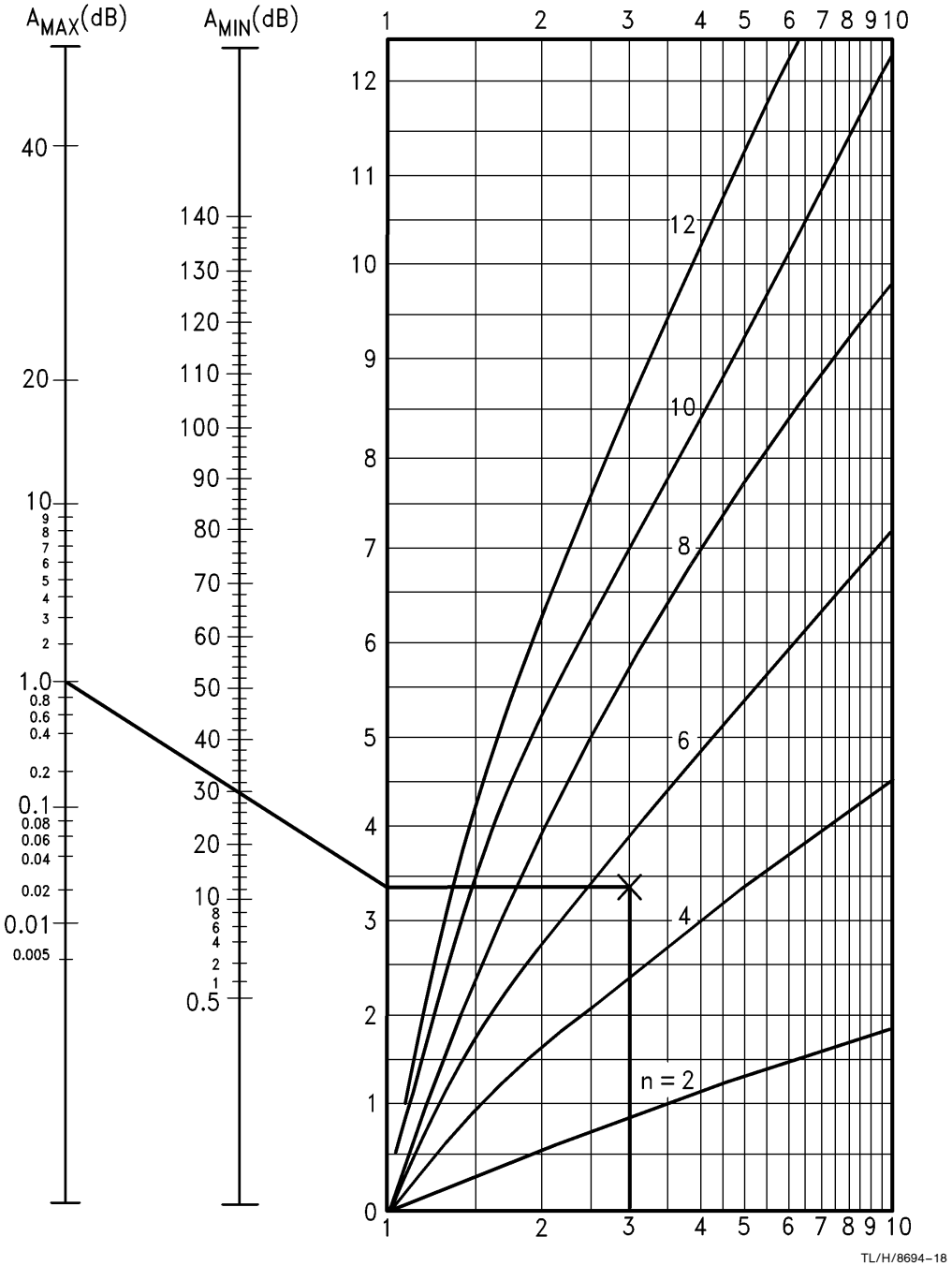
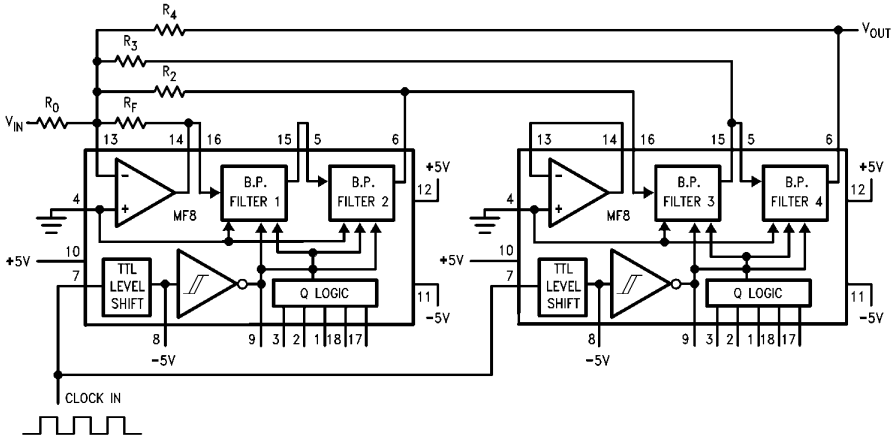


FIGURE 10. Example of Chebyshev Bandpass Nomograph Use.

$A_{max} = 1$ dB, $A_{min} = 30$ dB, and $\frac{SBW}{BW} = 3$, resulting in $n = 6$.

1.0 Application Information (Continued)



TL/H/8694–19

FIGURE 11. Eighth-Order multiple-feedback bandpass filter using two MF8s. The circuit shown accepts a TTL-level clock signal and has a clock-to-center-frequency ratio of 100:1.

1.5 TRACKING AND CASCADED SECOND-ORDER BANDPASS FILTERS

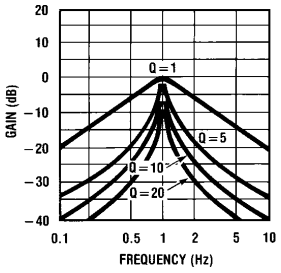
The individual second-order bandpass stages may be used as ''stand-alone'' filters without adding external feedback resistors. The clock frequency and Q logic voltages set the center frequency and bandwidth of both second-order bandpass filters, so the two filters will have equivalent responses. Thus, they may be used as separate ''tracking'' filters for two different signal sources as in *Figure 2a*, or cascaded as in *Figure 2b*. For individual or cascaded second-order bandpass filters, the −3 dB bandwidth and the amplitude response are given by the following two equations:

$$BW(-3) = \frac{f_0}{Q}\sqrt{2^{(1/N)} - 1} \qquad (1)$$

$$H(s) = \left[2 \times \frac{\frac{w_0}{Q}s}{s^2 + \frac{w_0}{Q}s + w_0^2} \right]^N \qquad (2)$$

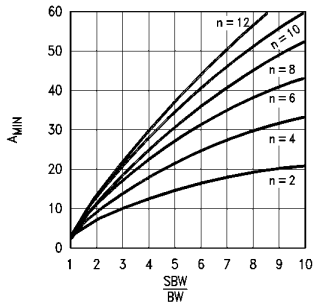
where

BW(−3) = the −3 dB bandwidth of the overall filter



TL/H/8694–20

FIGURE 12. H(s) For second-order bandpass filters with various values of Q. H_o normalized in each case to 0 dB.



TL/H/8694–21

FIGURE 13. Design Nomograph for Cascaded Identical Second-Order Bandpass Filters

Q = the Q of each second order bandpass stage

f_0 = the center frequency of the filter in Hertz

w_0 = $2\pi f_0$ = the center frequency of the filter in radians per second

N = the number of cascaded second-order stages = $\frac{n}{2}$

H(s) = the overall filter transfer function

H(s) for a second order bandpass filter is plotted in *Figure 12*. Curves are shown for several different values of Q. Center frequency is normalized to 1 Hz and center-frequency gain is normalized to 0 dB.

To find the necessary order n for cascaded second-order bandpass filters using the nomograph in *Figure 13*, first determine the −3 dB bandwidth BW(−3), stopband width SBW, and minimum stopband attenuation A_{min}. Draw a vertical line up from SBW/BW(−3), and a horizontal line across from A_{min}. The required order is shown on the curve just above the point of intersection of the two lines. Remember that each second-order filter section will have a center frequency gain of 2, so the overall gain of a cascaded filter will be 2^N.

Cascading filters in this way may provide acceptable performance when minimum external parts count is very impor-

1.0 Application Information (Continued)

tant, but much greater flexibility and better performance will be obtained by using the feedback techniques described in 1.4.

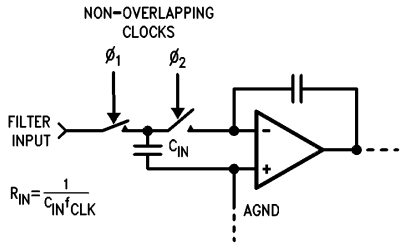
1.6 INPUT IMPEDANCE

The input to each filter block is a switched-capacitor circuit as shown in *Figure 14*. During the first half of a clock cycle, the input capacitor charges to the input voltage V_{in}, and during the second half-cycle, its charge is transferred to a feedback capacitor. The input impedance approximates a resistor of value

$$R_{in} \cong \frac{1}{C_{in} f_{CLK}}.$$

C_{in} depends on the value of Q selected by the Q logic pins, and varies from about 1 pF to about 5 pF. For a worst-case calculation of R_{in}, assume $C_{in} = 5$ pF. Thus,

$$R_{in}(\min) \cong \frac{1}{5 \times 10^{-12} f_{CLK}}$$



TL/H/8694–22

FIGURE 14. Simplified MF8 Input Stage

At the maximum clock frequency of 1 MHz, this gives $R_{in} \cong 200$k. Note that R_{in} increases as f_{CLK} decreases, so the input impedance should never be less than this number. Source impedance should be low enough that the gain isn't significantly affected.

1.7 OUTPUT DRIVE

The filter outputs can typically drive a 5 kΩ load resistor to over ±4V peak-to-peak. Load resistors smaller than 5 kΩ should not be used. The operational amplifier can drive the minimum recommended load resistance of 5 kΩ to at least ±3.5V.

1.8 SAMPLED-DATA SYSTEM CONSIDERATIONS

Aliasing

The MF8 is a sampled-data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF8's sampling frequency is the same as its clock frequency). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled-data system, it will be ''reflected'' to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2 + 10$ Hz will cause the system to respond as though the input frequency was $f_s/2 - 10$ Hz. This phenomenon is known as ''aliasing''. Aliasing can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter (a simple passive RC network will generally suffice) ahead of the MF8 to attenuate unwanted high-frequency signals. However, since the clock frequency is much greater than the center frequency, this will usually not be necessary.

Output Steps

Another characteristic of sampled-data circuits is that the output voltage changes only once every clock cycle, resulting in a discontinuous output signal (*Figure 15*). The ''steps'' are smaller when the clock-to-center-frequency ratio is 100:1 than when the ratio is 50:1.

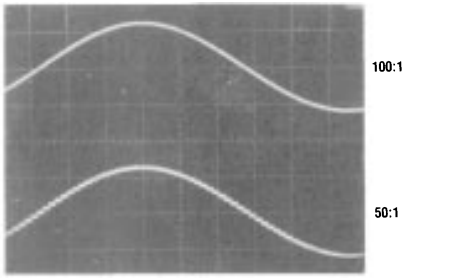
Clock Frequency Limitations

The performance characteristics of a switched-capacitor filter depend on the switching (clock) frequency. At very low clock frequencies (below 10 Hz), the internal capacitors begin to discharge slightly between clock cycles. This is due to very small parasitic leakage currents. At very low clock frequencies, the time between clock cycles is relatively long, allowing the capacitors to discharge enough to affect the filters' output offset voltage and gain. This effect becomes stronger at elevated operating temperatures.

At higher clock frequencies, performance deviations are primarily due to the reduced time available for the internal integrating op amps to settle. For this reason, the clock waveform's duty cycle should be as close as possible to 50%, especially at higher frequencies. Filter Q shows more variation from the nominal values at higher frequencies, as indicated in the typical performance curves. This is the reason for the different maximum limits on Q accuracy at $f_{CLK} = 250$ kHz and $f_{CLK} = 100$ kHz in the table of performance specifications.

Center Frequency Accuracy

Ideally, the ratio f_{CLK}/f_0 should be precisely 100 or 50, depending on the logic voltage on pin 10. However, as Table I shows, this ratio will change slightly depending on the Q selected. As the table shows, the largest errors occur at the lowest values of Q.



TL/H/8694–23

FIGURE 15. Output Waveform of MF8 Showing Sampling Steps

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters

BUTTERWORTH RIPPLE 3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	2.0000	4.0000					1.4142
6	2.3704	2.6667	9.1429				1.5000
8	2.9142	2.0000	5.8284	14.3145			1.5307
10	3.6340	1.6000	4.4112	6.9094	27.2014		1.5451
*12	4.5635	1.3333	3.5800	4.3198	11.5043	49.0673	1.5529

CHEBYSHEV RIPPLE 0.01 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.9041	3.6339					0.4489
6	1.8277	1.8450	6.6170				0.9438
8	1.4856	0.9919	3.1209	5.0414			1.4257
*10	1.0171	0.5740	1.7484	1.2943	4.8814		1.8908

CHEBYSHEV RIPPLE 0.02 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.8644	3.4922					0.5393
6	1.7024	1.6787	6.0772				1.0849
8	1.2893	0.8707	2.7661	4.0779			1.6106
*10	0.8163	0.4934	1.5155	0.9879	3.7119		2.1179

CHEBYSHEV RIPPLE 0.03 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.8341	3.3871					0.6016
6	1.6183	1.5713	5.7231				1.1808
8	1.1688	0.7977	2.5491	3.5270			1.7362
*10	0.7034	0.4467	1.3786	0.8252	3.0938		2.2724

CHEBYSHEV RIPPLE 0.04 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.8085	3.3009					0.6508
6	1.5535	1.4908	5.4548				1.2560
8	1.0814	0.7454	2.3919	3.1471			1.8348
*10	0.6264	0.4139	1.2818	0.7181	2.6883		2.3940

CHEBYSHEV RIPPLE 0.05 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7860	3.2268					0.6923
6	1.5002	1.4260	5.2373				1.3191
8	1.0129	0.7046	2.2685	2.8609			1.9175
*10	0.5686	0.3888	1.2072	0.6402	2.3938		2.4961

CHEBYSHEV RIPPLE 0.06 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7657	3.1612					0.7285
6	1.4548	1.3717	5.0536				1.3741
8	0.9566	0.6713	2.1670	2.6336			1.9897
*10	0.5230	0.3685	1.1467	0.5800	2.1666		2.5852

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE .07 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7471	3.1020					0.7609
6	1.4150	1.3249	4.8943				1.4232
8	0.9089	0.6431	2.0808	2.4466			2.0543
*10	0.4856	0.3516	1.0959	0.5316	1.9842		2.6649

CHEBYSHEV RIPPLE .08 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7298	3.0478					0.7905
6	1.3795	1.2837	4.7534				1.4679
8	0.8675	0.6187	2.0060	2.2887			2.1130

CHEBYSHEV RIPPLE .09 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.7136	2.9978					0.8177
6	1.3475	1.2469	4.6271				1.5090
8	0.8311	0.5973	1.9400	2.1529			2.1671

CHEBYSHEV RIPPLE 0.1 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.6983	2.9512					0.8430
6	1.3183	1.2137	4.5125				1.5473
8	0.7986	0.5782	1.8809	2.0343			2.2176

CHEBYSHEV RIPPLE 0.2 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.5757	2.5998					1.0378
6	1.1128	0.9894	3.7271				1.8413
8	0.5891	0.4551	1.4954	1.3309			2.6057

CHEBYSHEV RIPPLE 0.3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.4833	2.3575					1.1804
6	0.9835	0.8560	3.2501				2.0568
*8	0.4732	0.3861	1.2760	0.9885			2.8914

CHEBYSHEV RIPPLE 0.4 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.4067	2.1698					1.2988
6	0.8888	0.7618	2.9088				2.2363
*8	0.3956	0.3391	1.1250	0.7792			3.1299

CHEBYSHEV RIPPLE 0.5 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.3405	2.0161					1.4029
6	0.8143	0.6897	2.6447				2.3944
*8	0.3389	0.3040	1.0114	0.6365			3.3406

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE 0.6 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.2816	1.8857					1.4975
6	0.7530	0.6316	2.4305				2.5385
*8	0.2952	0.2762	0.9212	0.5326			3.5329

CHEBYSHEV RIPPLE 0.7 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.2283	1.7727					1.5852
6	0.7012	0.5834	2.2515				2.6724
*8	0.2601	0.2535	0.8471	0.4535			3.7119

CHEBYSHEV RIPPLE 0.8 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.1797	1.6731					1.6678
6	0.6564	0.5424	2.0983				2.7989
*8	0.2314	0.2344	0.7846	0.3913			3.8811

CHEBYSHEV RIPPLE 0.9 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.1347	1.5841					1.7464
6	0.6171	0.5068	1.9650				2.9194
*8	0.2073	0.2181	0.7309	0.3413			4.0426

CHEBYSHEV RIPPLE 1.0 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.0930	1.5039					1.8219
6	0.5822	0.4756	1.8475				3.0354
*8	0.1869	0.2038	0.6840	0.3002			4.1981

CHEBYSHEV RIPPLE 1.1 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.0539	1.4310					1.8949
6	0.5509	0.4479	1.7428				3.1476
*8	0.1693	0.1913	0.6426	0.2660			4.3487

CHEBYSHEV RIPPLE 1.2 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	1.0173	1.3643					1.9657
6	0.5226	0.4231	1.6487				3.2567
*8	0.1540	0.1801	0.6056	0.2372			4.4952

CHEBYSHEV RIPPLE 1.3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.9828	1.3029					2.0348
6	0.4969	0.4006	1.5634				3.3633
*8	0.1406	0.1701	0.5724	0.2125			4.6385

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE 1.4 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.9501	1.2461					2.1024
6	0.4733	0.3803	1.4857				3.4678

CHEBYSHEV RIPPLE 1.5 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.9192	1.1934					2.1688
6	0.4515	0.3616	1.4145				3.5705

CHEBYSHEV RIPPLE 1.6 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8897	1.1443					2.2341
6	0.4315	0.3445	1.3490				3.6717

CHEBYSHEV RIPPLE 1.7 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8617	1.0983					2.2986
6	0.4128	0.3287	1.2883				3.7717

CHEBYSHEV RIPPLE 1.8 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8350	1.0553					2.3624
6	0.3955	0.3141	1.2321				3.8706

CHEBYSHEV RIPPLE 1.9 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.8095	1.0148					2.4255
6	0.3793	0.3005	1.1797				3.9687

CHEBYSHEV RIPPLE 2.0 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7850	0.9767					2.4881
6	0.3641	0.2878	1.1308				4.0660

CHEBYSHEV RIPPLE 2.1 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7616	0.9407					2.5503
6	0.3498	0.2759	1.0850				4.1628

CHEBYSHEV RIPPLE 2.2 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7391	0.9067					2.6122
6	0.3364	0.2648	1.0420				4.2591

2.0 Design Tables for Multiple Feedback Loop Bandpass Filters (Continued)

CHEBYSHEV RIPPLE 2.3 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.7176	0.8744					2.6737
6	0.3237	0.2544	1.0016				4.3550

CHEBYSHEV RIPPLE 2.4 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6968	0.8438					2.7350
6	0.3118	0.2446	0.9635				4.4507

CHEBYSHEV RIPPLE 2.5 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6769	0.8148					2.7962
6	0.3005	0.2353	0.9275				4.5462

CHEBYSHEV RIPPLE 2.6 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6577	0.7871					2.8573
6	0.2897	0.2265	0.8935				4.6415

CHEBYSHEV RIPPLE 2.7 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6392	0.7607					2.9183
6	0.2796	0.2182	0.8612				4.7368

CHEBYSHEV RIPPLE 2.8 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6213	0.7356					2.9792
6	0.2699	0.2104	0.8306				4.8322

CHEBYSHEV RIPPLE 2.9 dB

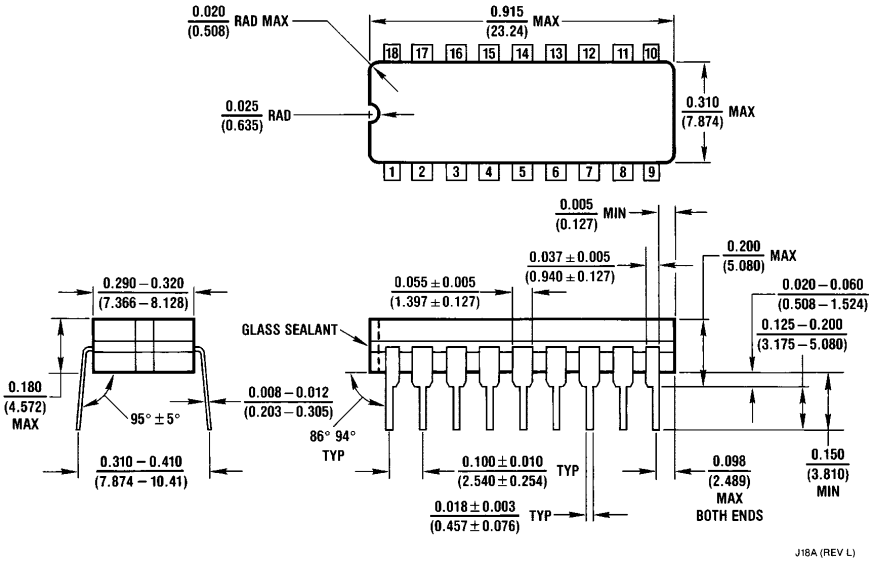
Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.6041	0.7116					3.0402
6	0.2607	0.2029	0.8016				4.9276

CHEBYSHEV RIPPLE 3.0 dB

Order	K_0	K_2	K_3	K_4	K_5	K_6	K_Q
4	0.5875	0.6886					3.1013
6	0.2519	0.1959	0.7739				5.0231

Note: Multiple feedback loop filters of higher order than those specified in the tables will oscillate due to phase shift at the output of the summing amplifier. This phase shift is not the fault of the MF8; it is inherent in this type of multiple feedback loop topology. In addition, all filters marked with an asterisk (*) will be unstable for $Q \leq 1$, due to phase shifts caused by the MF8's switched-capacitor design approach.

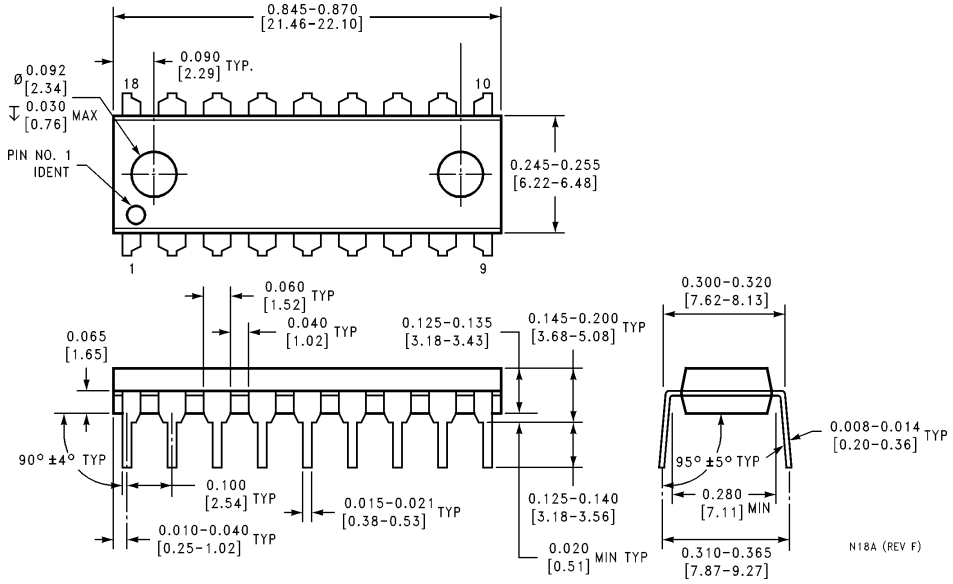
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MF8CCJ
NS Package Number J18A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 108778



Molded Dual-In-Line Package (N)
Order Number MF8CCN
NS Package Number N18A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408