National Semiconductor

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MF4 4th Order Switched Capacitor Butterworth Lowpass Filter

General Description

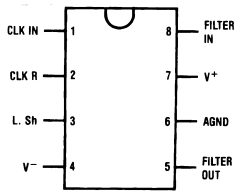
The MF4 is a versatile, easy to use, precision 4th order Butterworth low-pass filter. Switched-capacitor techniques eliminate external component requirements and allow a clock-tunable cutoff frequency. The ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50 to 1. A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control an external TTL or CMOS logic compatible clock can be applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF4 sections together for higher order filtering.

Features

- Low Cost
- Easy to use
- 8-pin mini-DIP or 14-pin wide-body S.O.
- No external components
- 5V to 14V supply voltage
- Cutoff frequency range of 0.1 Hz to 20 kHz
- Cutoff frequency accuracy of ± 0.3% typical
- Cutoff frequency set by external clock
- Separate TTL and CMOS/Schmitt-trigger clock inputs

Connection Diagram

Dual-In-Line Package



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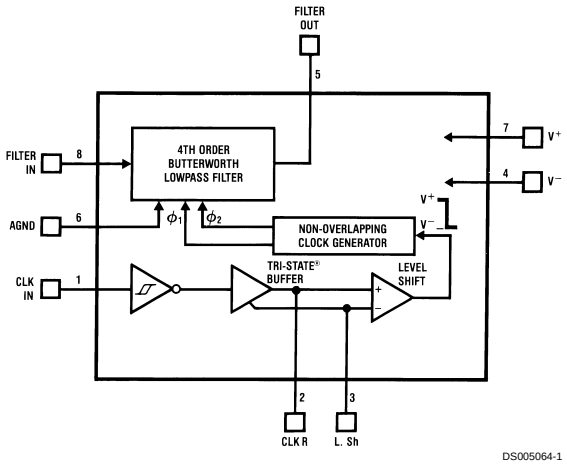
Order Number MF4CN-50
See NS Package Number N08E

Block Diagram



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Block Diagram (Continued)

Pin Descriptions

Pin #	Pin Name	Function
1	CLK IN	A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self clocking Schmitt-trigger oscillator (see section 1.1).
2	CLK R	A TTL logic level clock input when in split supply operation (±2.5V to ±7V) with L. Sh tied to system ground. This pin becomes a low impedance output when L. Sh is tied to V^-. Also used in conjunction with the CLK IN pin for a self clocking Schmitt-trigger oscillator (see section 1.1). The TTL input signal must not exceed the supply voltages by more than 0.2V.
3	L. Sh	Level shift pin; selects the logic threshold levels for the clock. When tied to V^- it enables an internal tri-state buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output. When the voltage level at this input exceeds 25% ($V^+ - V^-$) + V^- the internal tri-state buffer is disabled allowing the CLK R pin to become the clock input for the internal clock level-shift stage. The CLK R threshold level is now 2V above the voltage on the L. Sh pin. The CLK R pin will be compatible with TTL logic levels when the MF4 is operated on split supplies with the L. Sh pin connected to system ground.
5	FILTER OUT	The output of the low-pass filter. It will typically sink 0.9 mA and source 3 mA and swing to within 1V of each supply rail.
6	AGND	The analog ground pin. This pin sets the DC bias level for the filter section and must be tied to the system ground for split supply operation or to mid-supply for single supply operation (see section 1.2). When tied to mid-supply this pin should be well bypassed.
7, 4	V^+, V^-	The positive and negative supply pins. The total power supply range is 5V to 14V. Decoupling these pins with 0.1 µF capacitors is highly recommended.
8	FILTER IN	The input to the low-pass filter. To minimize gain errors the source impedance that drives this input should be less than 2K (see section 1.3 of the Application Hints). For single supply operation the input signal must be biased to mid-supply or AC coupled through a capacitor.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V^+–V^-)	14V
Voltage At Any Pin	V^+ + 0.2V
	V^- − 0.2V
Input Current at Any Pin (Note 14)	5 mA
Package Input Current (Note 14)	20 mA
Power Dissipation (Note 15)	500 mW
Storage Temperature	150˚C
ESD Susceptibility (Note 13)	800 V
Soldering Information (10 sec.)	260˚C

Operating Ratings (Note 2)

Temperature Range	$T_{min} \le T_A \le T_{max}$
MF4CN-50	0˚C≤ T_A≤ 70˚C
Supply Voltage (V^+–V^-)	5V to 14V

Filter Electrical Characteristics

The following specifications apply for $f_{CLK} \le 250$ kHz (Note 5) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25$˚C.

Parameter		Conditions	Typical (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Unit
V^+ = +5V, V^- = −5V						
f_c, Cutoff Frequency Range (Note 3)	Min				0.1	Hz
	Max				20k	
Supply Current		f_{clk} = 250 kHz	2.5	3.5	**3.5**	mA
Maximum Clock Feedthrough (Peak-to-Peak)	Filter Output	V_{in} = 0V	25			mV
H_o, DC Gain		$R_{source} \le 2$ kΩ	0.0	±0.15	**±0.15**	dB
f_{clk}/f_c, Clock to Cutoff Frequency Ratio			49.96 ±0.3%	49.96 ±1%		
f_{clk}/f_c Temperature Coefficient			±15			ppm/˚C
Stopband Attenuation (Min)		at 2 f_c	−25.0	−24.0	**−24.0**	dB
DC Offset Voltage			−200			mV
Minimum Output Swing		R_L = 10 kΩ	+4.0 −4.5	+3.5 −4.0	**+3.5** **−4.0**	V V
Output Short Circuit Current (Note 8)	Source		50			mA
	Sink		1.5			mA
Dynamic Range (Note 4)			80			dB
Additional Magnitude Response Test Points (Note 6) f_{clk} = 250 kHz		f = 6000 Hz		−7.57 ±0.47	**−7.57** **±0.47**	dB
		f = 4500 Hz		−1.44 ±0.12	**−1.44** **±0.12**	
		f = 3000 Hz				dB
		f = 2250 Hz				
V^+ = +2.5V, V^- = −2.5V						
f_c Cutoff Frequency Range (Note 3)	min				0.1	Hz
	max				10k	
Supply Current		f_{clk} = 250 kHz	1.5	2.25	**2.25**	mA
Maximum Clock Feedthrough (Peak-to-Peak)	Filter Output	V_{in} = 0V	15			mV
H_o, DC Gain		$R_{source} \le 2$ kΩ	0.0	±0.15	**±0.15**	dB
f_{clk}/f_c, Clock to Cutoff Frequency Ratio			50.07 ±0.3%	50.07 ±1.0%		
f_{CLK}/f_C Temperature Coefficient			±25			ppm/˚C

Filter Electrical Characteristics (Continued)

The following specifications apply for $f_{CLK} \leq 250$ kHz (Note 5) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$.

Parameter		Conditions	Typical (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Unit
$V^+ = +2.5V$, $V^- = -2.5V$						
Stopband Attenuation (Min)		at 2 f_c	−25.0	−24.0	**−24.0**	dB
DC Offset Voltage			−150			mV
Minimum Output Swing		R_L = 10 kΩ	+1.5	+1.0	**+1.0**	V
			−2.2	−1.7	**−1.7**	V
Output Short Circuit Current (Note 8)	Source		28			mA
	Sink		0.5			mA
Dynamic Range (Note 4)			78			dB
Additional Magnitude Response Test Points (Note 6) (f_c = 5 kHz)		f_{clk} = 250 kHz				
		f = 6000 Hz		−7.57	**−7.57**	dB
				±0.47	**±0.47**	
Magnitude at (f_c = 2.5 kHz) Magnitude		f = 4500 Hz		−1.46	**−1.46**	dB
				±0.12	**±0.12**	
		f = 3000 Hz				dB
		f = 2250 Hz				

Logic Input-Output Characteristics

The following specifications apply for $V^- = 0V$ (Note 7) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$.

Parameter		Conditions		Typical (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Unit
SCHMITT TRIGGER							
V_T+, Positive Going Threshold Voltage	Min	$V^+ = 10V$		7.0	6.1	**6.1**	V
	Max					**8.9**	
	Min	$V^+ = 5V$		3.5	3.1	**3.1**	V
	Max				4.4	**4.4**	
V_T-, Negative Going Threshold Voltage	Min	$V^+ = 10V$		3.0	1.3	**1.3**	V
	Max				3.8	**3.8**	
	Min	$V^+ = 5V$		1.5	0.6	**0.6**	V
	Max				1.9	**1.9**	
Hysteresis (V_{T+}–V_{T-})	Min	$V^+ = 10V$		4.0	2.3	**2.3**	V
	Max				7.6	**7.6**	
	Min	$V^+ = 5V$		2.0	1.2	**1.2**	V
	Max				3.8	**3.8**	
Minimum Logical “1” Output Voltage (pin 2)		I_O = −10 µA	$V^+ = 10V$		9.0	**9.0**	V
			$V^+ = 5V$		4.5	**4.5**	V
Maximum Logical “0” Output Voltage (pin 2)		I_O = 10 µA	$V^+ = 10V$		1.0	**1.0**	V
			$V^+ = 5V$		0.5	**0.5**	V
Minimum Output Source Current (pin 2)		CLK R Shorted to Ground	$V^+ = 10V$	6.0	3.0	**3.0**	mA
			$V^+ = 5V$	1.5	0.75	**0.75**	mA
Maximum Output Sink Current (pin 2)		CLK R Shorted to V^+	$V^+ = 10V$	5.0	2.5	**2.5**	mA
			$V^+ = 5V$	1.3	0.65	**0.65**	mA

Logic Input-Output Characteristics (Continued)

The following specifications apply for V^- = 0V (Note 7) unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$.

Parameter	Conditions	Typical (Note 10)	Tested Limit (Note 11)	Design Limit (Note 12)	Unit
TTL CLOCK INPUT, CLK R PIN (Note 9)					
Maximum V_{IL}, Logical "0" Input Voltage		0.8			V
Minimum V_{IH}, Logical "1" Input Voltage		2.0			V
Maximum Leakage Current at CLK R Pin	L. Sh Pin at Mid-Supply	2.0			µA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. AC and DC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are with respect to GND.

Note 3: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 4: For ±5V supplies the dynamic range is referenced to 2.82 Vrms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 280 µVrms for the MF4-50. For ±2.5V supplies the dynamic range is referenced to 1.06 Vrms (1.5V peak) where the wideband noise over a 20 kHz bandwidth is typically 130 µVrms.

Note 5: The specifications for the MF4 have been given for a clock frequency (f_{CLK}) of 250 kHz or less. Above the clock frequency the cutoff frequency begins to deviate from the specified error band of ±0.6% but the filter still maintains its magnitude characteristics. See Application Hints.

Note 6: Besides checking the cutoff frequency (f_c) and the stopband attenuation at 2 f_c, two additional frequencies are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB.

Note 7: For simplicity all the logic levels have been referenced to V^- = 0V (except for the TTL input logic levels). The logic levels will scale accordingly for ±5V and ±2.5V supplies.

Note 8: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage and then shorting that output to the positive supply. These are worst case conditions.

Note 9: The MF4 is operating with symmetrical split supplies and L. Sh is tied to ground.

Note 10: Typicals are at 25°C and represent most likely parametric norm.

Note 11: Guaranteed to National's Average Outgoing Quality Level (AOQL).

Note 12: Guaranteed, but not 100% production tested. These limits are not used to determine outgoing quality levels.

Note 13: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

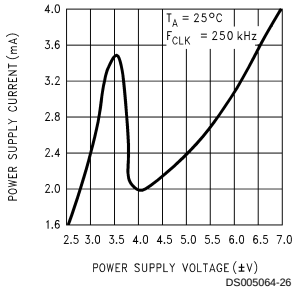
Note 14: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 15: Thermal Resistance

θ_{JA} (Junction to Ambient) N Package: 105°C/W.

Typical Performance Characteristics

Power Supply Current vs Power Supply Voltage



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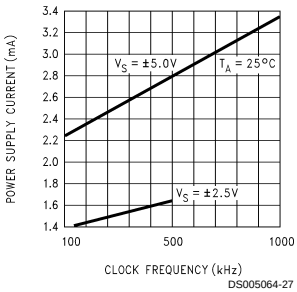
Power Supply Current vs Clock Frequency



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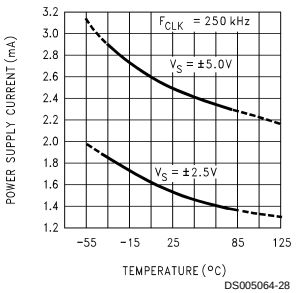
Power Supply Current vs Temperature



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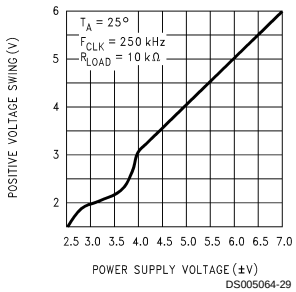
Positive Voltage Swing vs Power Supply Voltage



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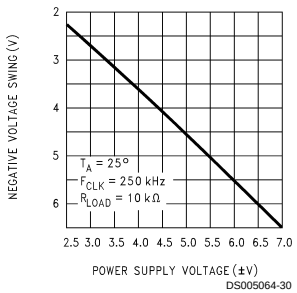
Negative Voltage Swing vs Power Supply Voltage



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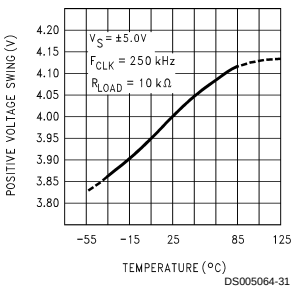
Positive Voltage Swing vs Temperature



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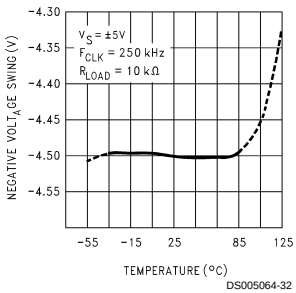
Negative Voltage Swing vs Temperature



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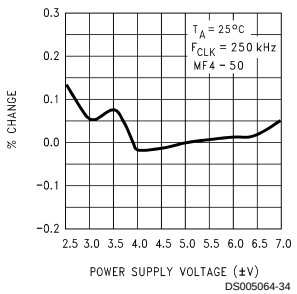
f_{CLK}/f_c Deviation vs Power Supply Voltage



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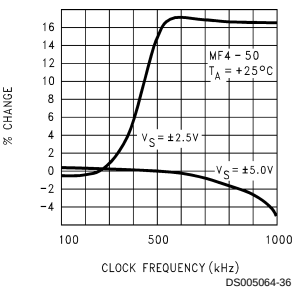
f_{CLK}/f_c Deviation vs Clock Frequency



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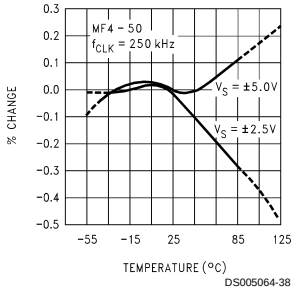
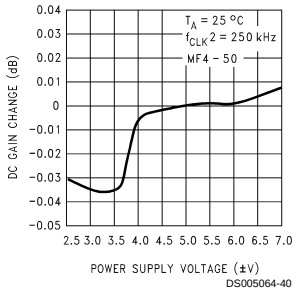
Typical Performance Characteristics (Continued)

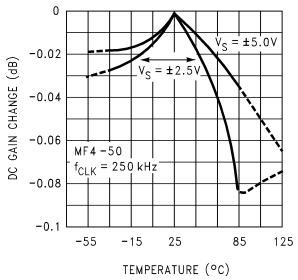
f_{CLK}/f_c Deviation vs Temperature



DC Gain Deviation vs Power Supply Voltage



DC Gain Deviation vs Temperature



1.0 MF4 Application Hints

The MF4 is a non-inverting unity gain low-pass fourth-order Butterworth switched-capacitor filter. The switched-capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio of the clock frequency supplied to the filter. Internal integrator time constants set the filter's cutoff frequency. The resistive element of these integrators is actually a capacitor which is "switched" at the clock frequency (for a detailed discussion see Input Impedance Section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock-to-cutoff-frequency ratio ($f_{CLK}f_c$) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock-to-cutoff-frequency ratio the closer this approximation is to the theoretical Butterworth response. The MF4 is available in f_{CLK}/f_c ratios of 50:1 (MF4-50).

1.1 CLOCK INPUTS

The MF4 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. Pin 3 is connected to V^- which makes Pin 2 a low impedance output. The oscillator's frequency is nominally

$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]} \quad (1)$$

which, is typically

$$f_{CLK} \cong \frac{1}{1.69\,RC} \quad (2)$$

for V_{CC} = 10V.

Note that f_{CLK} is dependent on the buffer's threshold levels as well as the resistor/capacitor tolerance (see *Figure 1*). Schmitt-trigger threshold voltage levels can change significantly causing the R/C oscillator's frequency to vary greatly from part to part.

Where accurate cutoff frequency is required, an external clock can be used to drive the CLK R input of the MF4. This input is TTL logic level compatible and also presents a very light load to the external clock source (~2 µA). With split supplies and the level shift (L. Sh) tied to system ground, the logic level is about 2V. (See the Pin Description for L. Sh).

1.2 POWER SUPPLY

The MF4 can be powered from a single supply or split supplies. The split supply mode shown in *Figures 2, 3* is the most flexible and easiest to implement. Supply voltages of ±5V to ±7V enable the use of TTL or CMOS clock logic levels. *Figure 4* shows AGND resistor-biased to $V^+/2$ for single supply operation. In this mode only CMOS clock logic levels can be used, and input signals should be capacitor-coupled or biased near mid-supply.

1.3 INPUT IMPEDANCE

The MF4 low-pass filter input (FILTER IN) is not a high impedance buffer input. This input is a switched-capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the filter's input can be seen in *Figure 5*. The input capacitor charges to V_{in} during the first half of the clock period; during the second half the charge is transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore $Q = C_{in}V_{in}$, and since current is defined as the flow of charge per unit time, the average input current becomes

$$I_{in} = Q/T$$

(where T equals one clock period) or

$$I_{in} = \frac{C_{in}V_{in}}{T} = C_{in}V_{in}f_{CLK}$$

The equivalent input resistor (R_{in}) then can be expressed as

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{C_{in}f_{CLK}}$$

The input capacitor is 2 pF, so

$$R_{in} = \frac{5 \times 10^{11}}{f_{CLK}} = \frac{5 \times 10^{11}}{f_c \times 50} = \frac{1 \times 10^{10}}{f_c}$$

The higher the clock-to-cutoff-frequency ratio, the greater equivalent input resistance for a given clock frequency.

This input resistance will form a voltage divider with the source impedance (R_{source}). Since R_{in} is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to load the input signal which would appear as an overall decrease in gain to the output of the filter. Since the filter's ideal gain is unity, the overall gain is given by:

1.0 MF4 Application Hints (Continued)

$$A_v = \frac{R_{in}}{R_{in} + R_{source}}$$

If the MF were set up for a cutoff frequency of 10 kHz the input impedance would be:

$$R_{in} = \frac{1 \times 10^{10}}{10\ kHz} = 1\ M\Omega$$

In this example with a source impedance of 10K the overall gain, if the MF4 had an ideal gain of 1 or 0 dB, would be:

$$A_v = \frac{1\ M\Omega}{10\ k\Omega + 1\ M\Omega} = 0.99009 \text{ or } -0.086\ dB$$

Since the maximum overall gain error for the MF4 is ±0.15 dB with $R_s \leq 2\ k\Omega$ the actual gain error for this case would be +0.06 dB to −0.24 dB.

1.4 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency (f_c) has a lower limit due to leakage currents through the internal switches draining the charge stored on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error, for example:

$$f_{CLK} = 100\ Hz,\ I_{leakage} = 1\ pA,\ C = 1\ pF$$

$$V = \frac{1\ pA}{1\ pF\ (100\ Hz)} = 10\ mV$$

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors limit the filter's accuracy at high clock frequencies. The amplitude characteristic on ±5V supplies will typically stay flat until f_{CLK} exceeds 750 kHz and then peak at about 0.5 dB at the corner frequency with a 1 MHz clock. As supply voltage drops to ± 2.5V, a shift in the f_{CLK}/f_c ratio occurs which will become noticeable when the clock frequency exceeds 250 kHz. The response of the MF4 is still a good approximation of the ideal Butterworth low-pass characteristic shown in *Figures 6, 7*.

2.0 Designing With The MF4

Given any low-pass filter specification, two equations will come in handy in trying to determine whether the MF4 will do the job. The first equation determines the order of the low-pass filter required to meet a given response specification:

$$n = \frac{\log\left[(10^{0.1A_{min}} - 1)/(10^{0.1A_{max}} - 1)\right]}{2\log(f_s/f_b)} \quad (3)$$

where n is the order of the filter, A_{min} is the minimum stopband attenuation (in dB) desired at frequency f_s, and A_{max} is the passband ripple or attenuation (in dB) at cutoff frequency f_b. If the result of this equation is greater than 4, more than a single MF4 is required.

The attenuation at any frequency can be found by the following equation:

$$\text{Attn}(f) = 10\log\left[1 + (10^{0.1A_{max}} - 1)(f/f_b)^{2n}\right]\ dB \quad (4)$$

where n = 4 for the MF4.

2.1 A LOW-PASS DESIGN EXAMPLE

Suppose the amplitude response specification in *Figure 8* is given. Can the MF4 be used? The order of the Butterworth approximation will have to be determined using *Equation (1)*:

$$A_{min} = 18\ dB,\ A_{max} = 1.0\ dB,\ f_s = 2\ kHz, \text{ and } f_b = 1\ kHz$$

$$n = \frac{\log\left[(10^{1.8} - 1)/(10^{0.1} - 1)\right]}{2\log(2)} = 3.95$$

Since n can only take on integer values, n = 4. Therefore the MF4 can be used. In general, if n is 4 or less a single MF4 stage can be utilized.

Likewise, the attenuation at f_s can be found using *Equation (4)* with the above values and n = 4:

Attn (2 kHz) = 10 log [1 + $10^{0.1}$ − 1) (2 kHz/1 kHz)^8] = 18.28 dB

This result also meets the design specification given in *Figure 8* again verifying that a single MF4 section will be adequate.

Since the MF4's cutoff frequency (f_c), which corresponds to a gain attenuation of −3.01 dB, was not specified in this example, it needs to be calculated. Solving *Equation (4)* where $f = f_c$ as follows:

$$f_c = f_b\left[\frac{(10^{0.1(3.01\ dB)} - 1}{(10^{0.1A_{max}} - 1)}\right]^{1/(2n)}$$

$$= 1\ kHz\left[\frac{10^{0.301} - 1}{10^{0.1} - 1}\right]^{1/8}$$

$$= 1.184\ kHz$$

where $f_c = f_{CLK}/50$. To implement this example for the MF4-50 the clock frequency will have to be set to f_{CLK} = 50(1.184 kHz) = 59.2 kHz, or for the MF4-100, f_{CLK} = 100 (1.184 kHz) = 118.4 kHz.

2.2 CASCADING MF4s

When a steeper stopband attenuation rate is required, two MF4s can be cascaded (*Figure 9*) yielding an 8th order slope of 48 dB per octave. Because the MF4 is a Butterworth filter and therefore has no ripple in its passband when MF4s are cascaded, the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1V/V. The resulting response is shown in *Figure 10*, *Figure 11*.

In determining whether the cascaded MF4s will yield a filter that will meet a particular amplitude response specification, as above, *Equations (5), (6)* can be used, shown below.

$$n = \frac{\log\left[(10^{0.05A_{min}} - 1)/(10.^{0.05A_{max}} - 1)\right]}{2\log(f_s/f_c)} \quad (5)$$

$$\text{Attn}(f) = 10\log\left[1 + (10^{0.05A_{max}} - 1)(f/f_c)^2\right]\ dB \quad (6)$$

where n = 4 (the order of each filter).

Equation (5) will determine whether the order of the filter is adequate ($n \leq 4$) while *Equation (6)* can determine the actual stopband attenuation and cutoff frequency (f_c) necessary to obtain the desired frequency response. The design procedure would be identical to the one shown in section 2.0.

2.0 Designing With The MF4

(Continued)

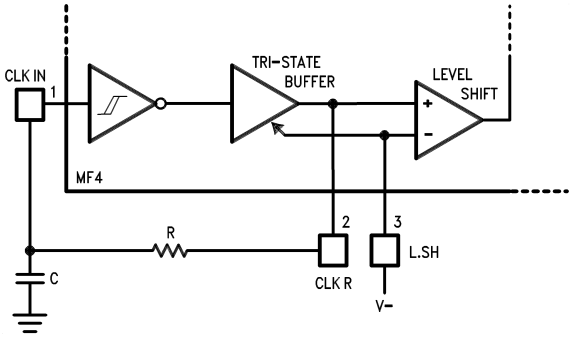
2.3 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The MF4 will respond favorably to an instantaneous change in clock frequency. If the control signal in *Figure 12* is low the MF4-50 has a 100 kHz clock making f_c = 2 kHz; when this signal goes high the clock frequency changes to 50 kHz yielding f_c = 1 kHz. As the Figure illustrates, the output signal changes quickly and smoothly in response to a sudden change in clock frequency.

The step response of the MF4 in *Figure 13* is dependent on f_c. The MF4 responds as a classical fourth-order Butterworth low-pass filter.

2.4 ALIASING CONSIDERATIONS

Aliasing effects have to be considered when input signal frequencies exceed half the sampling rate. For the MF4 this equals half the clock frequency (f_{CLK}). When the input signal contains a component at a frequency higher than half the clock frequency $f_{CLK}/2$, as in *Figure 14a*, that component will be "reflected" about $f_{CLK}/2$ into the frequency range below $f_{CLK}/2$, as in *Figure 14b*. If this component is within the passband of the filter and of large enough amplitude it can cause problems. Therefore, if frequency components in the input signal exceed $f_{CLK}2$ they must be attenuated before being applied to the MF4 input. The necessary amount of attenuation will vary depending on system requirements. In critical applications the signal components above $f_{CLK}/2$ will have to be attenuated at least to the filter's residual noise level.

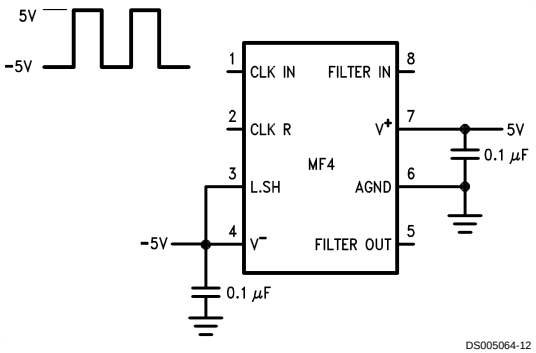


$$f = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

$$f \cong \frac{1}{1.69\ RC}$$

(V_{CC} = 10V)

FIGURE 1. Schmitt Trigger R/C Oscillator



$V_{IH} \geq 0.8\ V_{cc}$
$V_{IL} \leq 0.2\ V_{cc}$
$V_{cc} = V^+ - V^-$

FIGURE 2. Split Supply Operation with CMOS Level Clock

2.0 Designing With The MF4 (Continued)

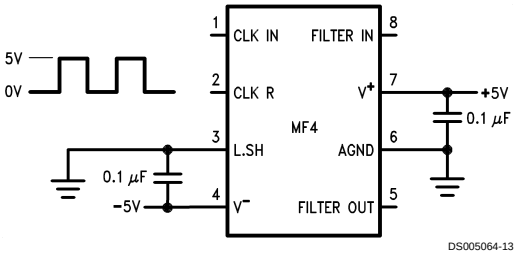


FIGURE 3. Split Supply Operation with TTL Level Clock

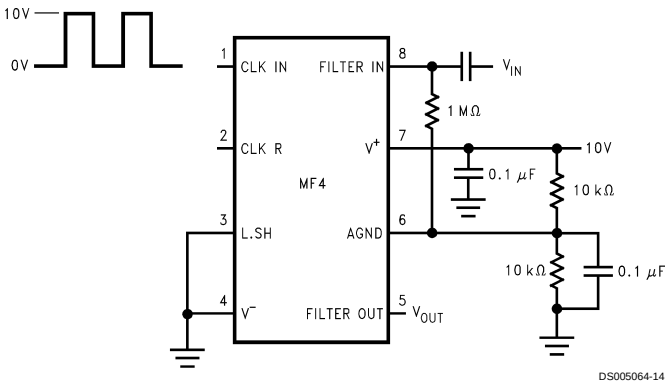
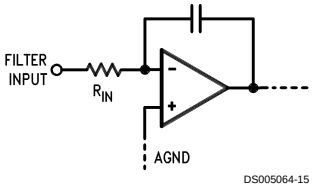
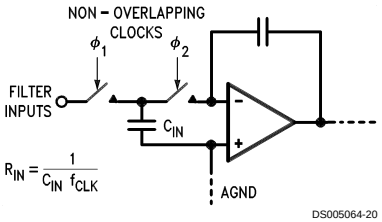


FIGURE 4. Single Supply Operation. ANGD Resistor Biased to $V^+/2$



a) Equivalent Circuit for MF4 Filter Input



b) Actual Circuit for MF4 Filter Input

FIGURE 5. MF4 Filter Input

2.0 Designing With The MF4 (Continued)

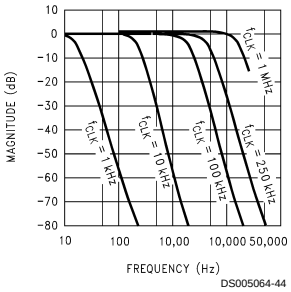


FIGURE 6. MF4-50 Amplitude Response with ±5V Supplies

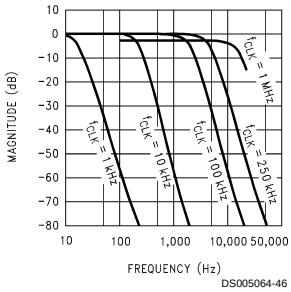


FIGURE 7. MF4-50 Amplitude Response with ±2.5V Supplies

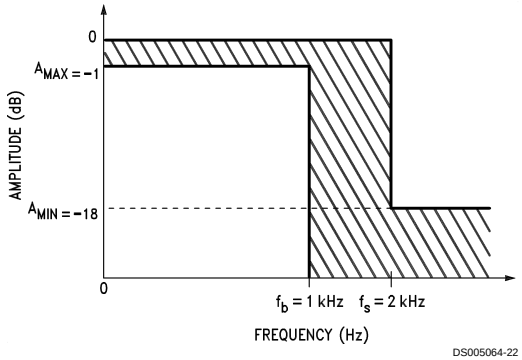


FIGURE 8. Design Example Magnitude Response Specification where the Response of the Filter Design must fall within the shaded area of the specification

2.0 Designing With The MF4 (Continued)

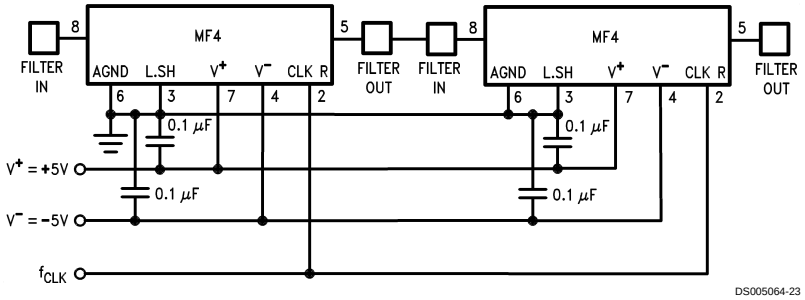


FIGURE 9. Cascading Two MF4s

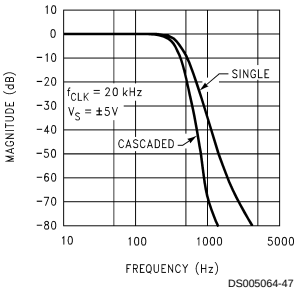


FIGURE 10. One MF4-50 vs Two MF4-50s Cascaded

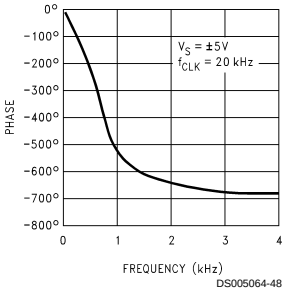


FIGURE 11. Phase Response of Two Cascaded MF4-50s

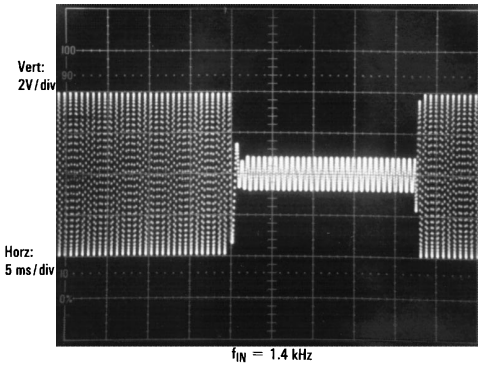


FIGURE 12. MF4-50 Abrupt Clock Frequency Change

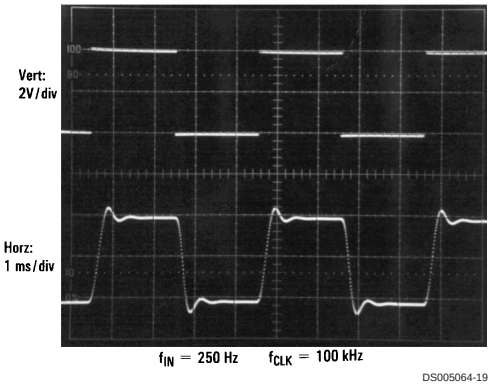
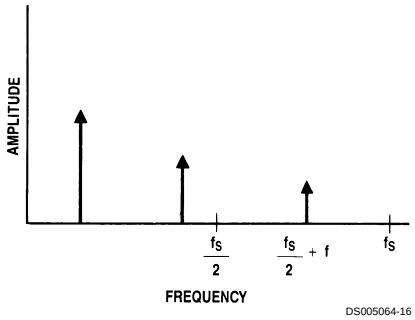
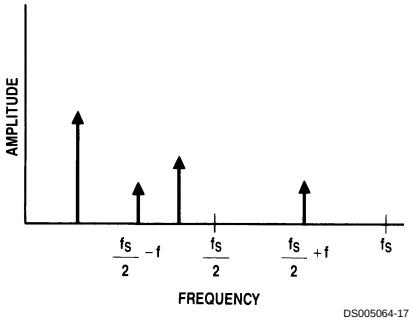


FIGURE 13. MF4-50 Input Step Response

2.0 Designing With The MF4 (Continued)



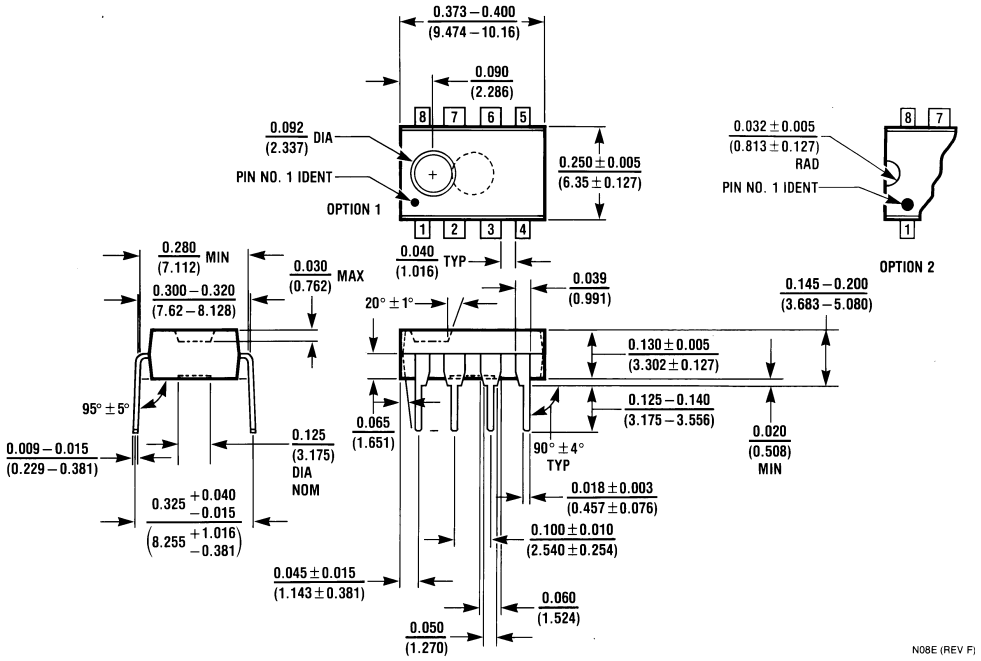
(a) input signal spectrum



(b) Output signal spectrum. Note that the input signal at $f_c/2 + f$ causes an output signal to appear at $f_c/2 - f$.

FIGURE 14. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the MF4, $f_s = f_{CLK}$.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number MF4CN-50
NS Package Number N08E

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