

## Decimating Digital Filter

The HSP43220 Decimating Digital Filter is a linear phase low pass decimation filter which is optimized for filtering narrow band signals in a broad spectrum of a signal processing applications. The HSP43220 offers a single chip solution to signal processing applications which have historically required several boards of ICs. This reduction in component count results in faster development times as well as reduction of hardware costs.

The HSP43220 is implemented as a two stage filter structure. As seen in the block diagram, the first stage is a high order decimation filter (HDF) which utilizes an efficient sample rate reduction technique to obtain decimation up to 1024 through a coarse low-pass filtering process. The HDF provides up to 96dB aliasing rejection in the signal pass band. The second stage consists of a finite impulse response (FIR) decimation filter structured as a transversal FIR filter with up to 512 symmetric taps which can implement filters with sharp transition regions. The FIR can perform further decimation by up to 16 if required while preserving the 96dB aliasing attenuation obtained by the HDF. The combined total decimation capability is 16,384.

The HSP43220 accepts 16-bit parallel data in 2's complement format at sampling rates up to 33MSPS. It provides a 16-bit microprocessor compatible interface to simplify the task of programming and three-state outputs to allow the connection of several ICs to a common bus. The HSP43220 also provides the capability to bypass either the HDF or the FIR for additional flexibility.

## Features

- Single Chip Narrow Band Filter with up to 96dB Attenuation
- DC to 33MHz Clock Rate
- 16-Bit 2's Complement Input
- 20-Bit Coefficients in FIR
- 24-Bit Extended Precision Output
- Programmable Decimation up to a Maximum of 16,384
- Standard 16-Bit Microprocessor Interface
- Filter Design Software Available DECIMATE™
- Up to 512 Taps
- Pb-Free Available (RoHS compliant)

## Applications

- Very Narrow Band Filters
- Zoom Spectral Analysis
- Channelized Receivers
- Large Sample Rate Converter

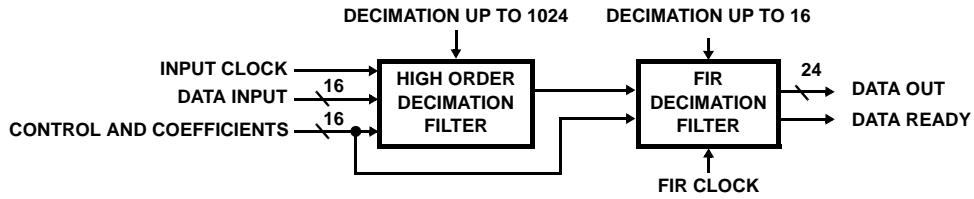
## Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HSP43220JC-25	HSP43220JC-25	0 to +70	84 Ld PLCC	N84.1.15
HSP43220JC-25Z	HSP43220JC-25Z	0 to +70	84 Ld PLCC (Pb-free)	N84.1.15
HSP43220JC-33	HSP43220JC-33	0 to +70	84 Ld PLCC	N84.1.15
HSP43220JC-33Z	HSP43220JC-33Z	0 to +70	84 Ld PLCC (Pb-free)	N84.1.15

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

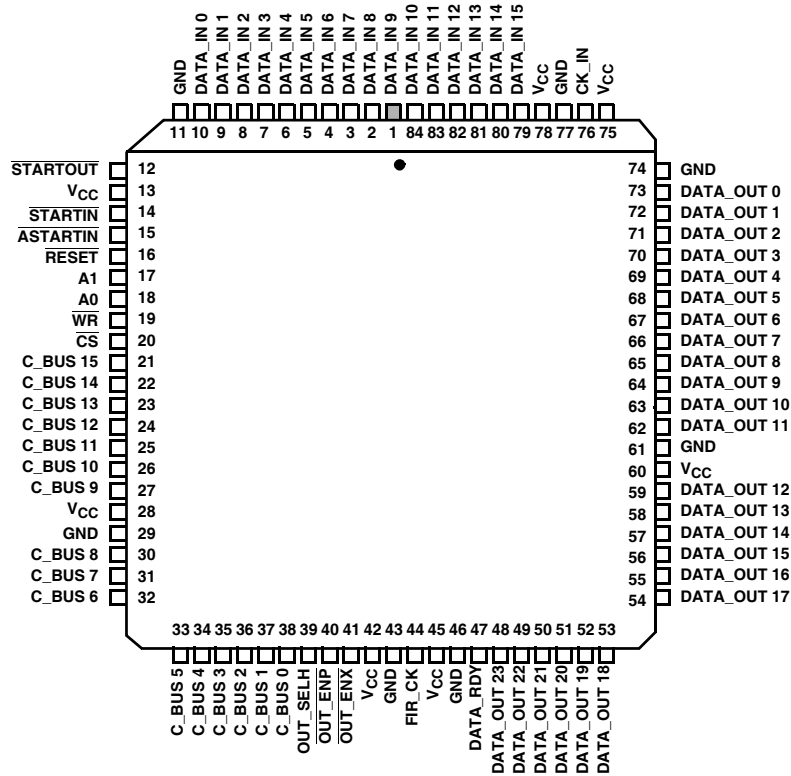
NOTE: DECIMATE Software Development Tool (This software tool may be downloaded from our internet site: [www.intersil.com](http://www.intersil.com))

**Block Diagram**



**Pinout**

HSP43220  
84 PLASTIC LEADED CHIP CARRIER (PLCC)  
TOP VIEW



**Pin Description**

NAME	TYPE	DESCRIPTION
V <sub>CC</sub>		The +5V power supply pins.
GND		The device ground.
CK_IN	I	Input Sample Clock. Operations in the HDF are synchronous with the rising edge of this clock signal. The maximum clock frequency is 33MHz. CK_IN is synchronous with FIR_CK and thus the two clocks may be tied together if required, or CK_IN can be divided down from FIR_CK. CK_IN is a CMOS level signal.
FIR_CK	I	Input Clock for the FIR Filter. This clock must be synchronous with CK_IN. Operations in the FIR are synchronous with the rising edge of this clock signal. The maximum clock frequency is 33MHz. FIR_CK is a CMOS level signal.

**Pin Description (Continued)**

NAME	TYPE	DESCRIPTION
DATA_IN0-15	I	Input Data Bus. This bus is used to provide the 16-bit input data to the HSP43220. The data must be provided in a synchronous fashion, and is latched on the rising edge of the CK_IN signal. The data bus is in 2's complement fractional format. Bit 15 is the MSB.
C_BUS0-15	I	Control Input Bus. This input bus is used to load all the filter parameters. The pins $\overline{WR}$ , $\overline{CS}$ and A0, A1 are used to select the destination of the data on the Control bus and write the Control bus data into the appropriate register as selected by A0 and A1
DATA_OUT0-23	O	Output Data Bus. This 24-Bit output port is used to provide the filtered result in 2's complement format. The upper 8 bits of the output, DATA_OUT16-23 will provide extension or growth bits depending on the state of OUT_SELH and whether the FIR has been put in bypass mode. Output bits DATA_OUT0-15 will provide bits 20 through 2-15 when the FIR is not bypassed and will provide the bits 2-16 through 2-31 when the FIR is in bypass mode.
DATA_RDY	O	An active high output strobe that is synchronous with FIR_CK that indicates that the result of the just completed FIR cycle is available on the data bus.
$\overline{RESET}$	I	$\overline{RESET}$ is an asynchronous signal which requires that the input clocks CK_IN and FIR_CK are active when $\overline{RESET}$ is asserted. $\overline{RESET}$ disables the clock divider and clears all of the internal data registers in the HDF. The FIR filter data path is not initialized. The control register bits that are cleared are F_BYP, H_STAGES, and H_DRATE. The F_DIS bit is set. In order to guarantee consistent operation of the part, the user must reset the DDF after power-up.
$\overline{WR}$	I	Write Strobe. $\overline{WR}$ is used for loading the internal registers of the HSP43220. When $\overline{CS}$ and $\overline{WR}$ are asserted, the rising edge of $\overline{WR}$ will latch the C_BUS0-15 data into the register specified by A0 and A1.
$\overline{CS}$	I	Chip Select. The Chip Select input enables loading of the internal registers. When $\overline{CS}$ and $\overline{WR}$ are low, the A0 and A1 address lines are decoded to determine the destination of the data on C_BUS0-15. The rising edge of $\overline{WR}$ then loads the appropriate register as specified by A0 and A1.
A0, A1	I	Control Register Address. These lines are decoded to determine which control register is the destination for the data on C_BUS0-15. Register loading is controlled by the A0 and A1, $\overline{WR}$ and $\overline{CS}$ inputs.
$\overline{ASTARTIN}$	I	$\overline{ASTARTIN}$ is an asynchronous signal which is sampled on the rising edge of CK_IN. It is used to put the DDF in operational mode. $\overline{ASTARTIN}$ is internally synchronized to CK_IN and is used to generate $\overline{STARTOUT}$ .
$\overline{STARTOUT}$	O	$\overline{STARTOUT}$ is a pulse generated from the internally synchronized version of $\overline{ASTARTIN}$ . It is provided as an output for use in multi-chip configurations to synchronously start multiple HSP43220's. The width of $\overline{STARTOUT}$ is equal to the period of CK_IN.
$\overline{STARTIN}$	I	$\overline{STARTIN}$ is a Synchronous Input. A high to low transition of this signal is required to start the part. $\overline{STARTIN}$ is sampled on the rising edge of CK_IN. This synchronous signal can be used to start single or multiple HSP43220's.
OUT_SELH	I	Output Select. The OUT_SELH input controls which bits are provided at output pins DATA_OUT16-23. A HIGH on this control line selects bits 28 through 21 from the accumulator output. A LOW on this control line selects bits 2-16 through 2-23 from the accumulator output. Processing is not interrupted by this pin.
$\overline{OUT\_ENP}$	I	Output Enable. The $\overline{OUT\_ENP}$ input controls the state of the lower 16 bits of the output data bus, DATA_OUT0-15. A LOW on this control line enables the lower 16 bits of the output bus. When $\overline{OUT\_ENP}$ is HIGH, the output drivers are in the high impedance state. Processing is not interrupted by this pin.
$\overline{OUT\_ENX}$	I	Output Enable. The $\overline{OUT\_ENX}$ input controls the state of the upper 8 bits of the output data bus, DATA_OUT16-23. A LOW on this control line enables the upper 8 bits of the output bus. When $\overline{OUT\_ENX}$ is HIGH, the output drivers are in the high impedance state. Processing is not interrupted by this pin.

**The HDF**

The first filter section is called the High Order Decimation Filter (HDF) and is optimized to perform decimation by large factors. It implements a low pass filter using only adders and delay elements instead of a large number of multiplier/ accumulators that would be required using a standard FIR filter.

The HDF is divided into 4 sections: the HDF filter section, the clock divider, the control register logic and the start logic (Figure 1).

**Data Shifter**

After being latched into the Input Register the data enters the Data Shifter. The data is positioned at the output of the shifter to prevent errors due to overflow occurring at the output of the HDF. The number of bits to shift is controlled by H\_GROWTH.

### Integrator Section

The data from the shifter goes to the Integrator section. This is a cascade of 5 integrator (or accumulator) stages, which implement a low pass filter. Each accumulator is implemented as an adder followed by a register in the feed forward path. The integrator is clocked by the sample clock, CK\_IN as shown in Figure 2. The bit width of each integrator stage goes from 66 bits at the first integrator down to 26 bits at the output of the fifth integrator. Bit truncation is performed at each integrator stage because the data in the integrator stages is being accumulated and thus is growing, therefore the lower bits become insignificant, and can be truncated without losing significant data.

There are three signals that control the integrator section; they are H\_STAGES, H\_BYP and RESET. In Figure 2 these control signals have been decoded and are labelled INT\_EN1 - INT\_EN5. The order of the filter is loaded via the

control bus and is called H\_STAGES. H\_STAGES is decoded to provide the enables for each integrator stage. When a given integrator stage is selected, the feedback path is enabled and the integrator accumulates the current data sample with the previous sum. The integrator section can be put in bypass mode by the H\_BYP bit. When H\_BYP or RESET is asserted, the feedback paths in all integrator stages are cleared.

### Decimation Register

The output of the Integrator section is latched into the Decimation Register by CK\_DEC. The output of the Decimation register is cleared when RESET is asserted. The HDF decimation rate = H\_DRATE + 1, which is defined as H\_DEC for convenience.

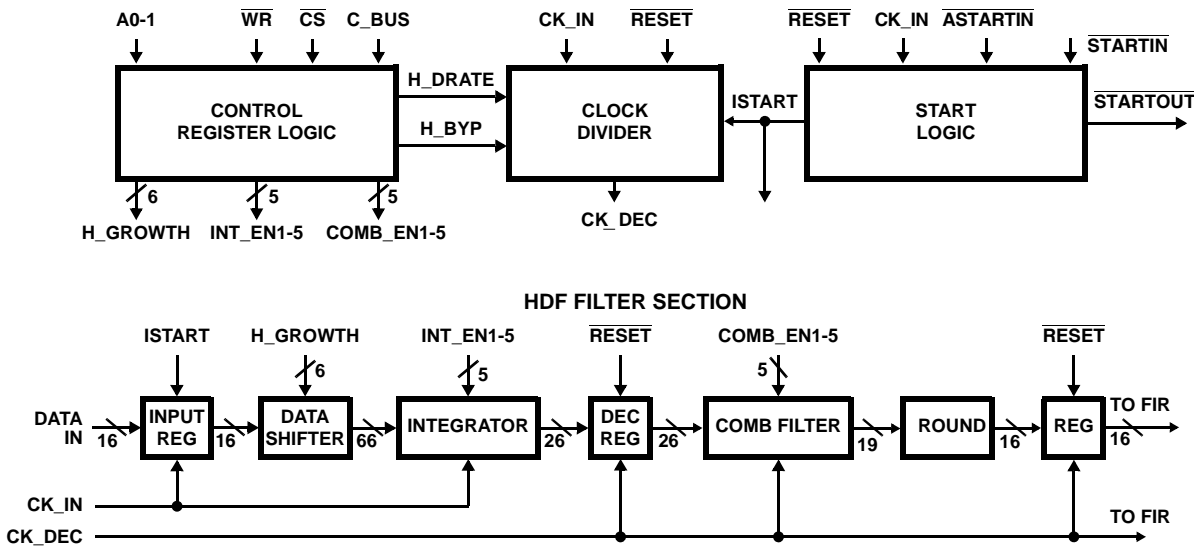


FIGURE 1. HIGH ORDER DECIMATION FILTER FIGURE

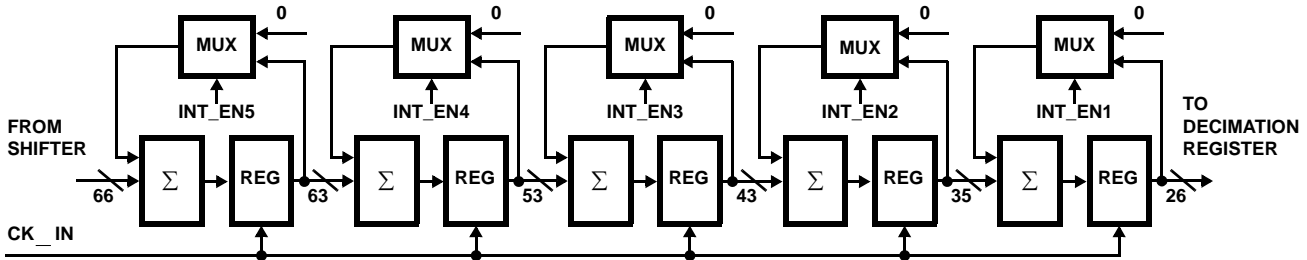


FIGURE 2. INTEGRATOR

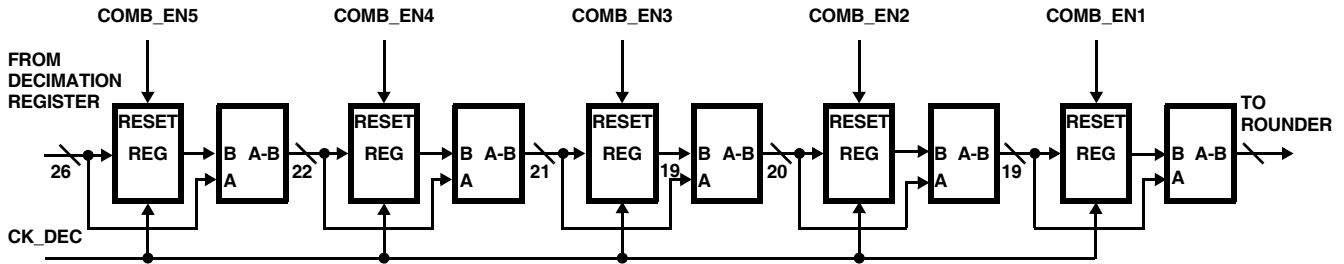


FIGURE 3. COMB FILTER

**Comb Filter Section**

The output of the Decimation Register is passed to the Comb Filter Section. The Comb section consists of 5 cascaded Comb filters or differentiators. Each Comb filter section calculates the difference between the current and previous integrator output. Each Comb filter consists of a register which is clocked by CK\_DEC, followed by an subtractor, where the subtractor calculates the difference between the input and output of the register. Bit truncations are done at each stage as shown in Figure 3. The first stage bit width is 26 bits and the output of the fifth stage is 19 bits.

There are three signals that control the Comb Filter; H\_STAGES, H\_BYP and RESET. In Figure 3 these control signals are decoded as COMB\_EN1 - COMB\_EN5. The order of the Comb filter is controlled by H\_STAGES, which is programmed over the control bus. H\_BYP is used to put the comb section in bypass mode. RESET causes the register output in each Comb stage to be cleared. The H\_BYP and RESET control pins, when asserted force the output of all registers to zero so data is passed through the subtractor unaltered. When the H\_STAGES control bits enable a given stage the output of the register is subtracted from the input.

It is important to note that the Comb filter section has a speed limitation. The Input sampling rate divided by the decimation factor in the HDF (CK\_IN/HDEC) should not exceed 4MHz. Violating this condition causes the output of the filter to be incorrect. When the HDF is put in bypass mode this limitation does not apply. Equation 2 describes the relationship between F\_TAPS, F\_DRATE, H\_DRATE, CK\_IN and FIR\_CK.

**Rounder**

The filter accuracy is limited by the 16-bit data input. To maintain the maximum accuracy, the output of the comb is rounded to 16 bits.

The Rounder performs a symmetric round of the 19-bit output of the last Comb stage. Symmetric rounding is done to prevent the synthesis of a 0Hz spectral component by the rounding process and thus causing a reduction in spurious free dynamic range. Saturation logic is also provided to prevent roll over from the largest positive value to the most negative value after rounding. The output of the last comb

filter stage in the HDF section has a 16-bit integer portion with a 3-bit fractional part in 2's complement format.

The rounding algorithm is as follows:

POSITIVE NUMBERS	
Fractional Portion $\geq$ to 0.5	Round-Up
Fractional Portion $<$ 0.5	Truncate
NEGATIVE NUMBERS	
Fractional Portion $\leq$ 0.5	Round-Up
Fractional Portion $>$ 0.5	Truncate

The output of the rounder is latched into the HDF output register with CK\_DEC. CK\_DEC is generated by the Clock Divider section. The output of the register is cleared when RESET is asserted.

**Clock Divider and Control Logic**

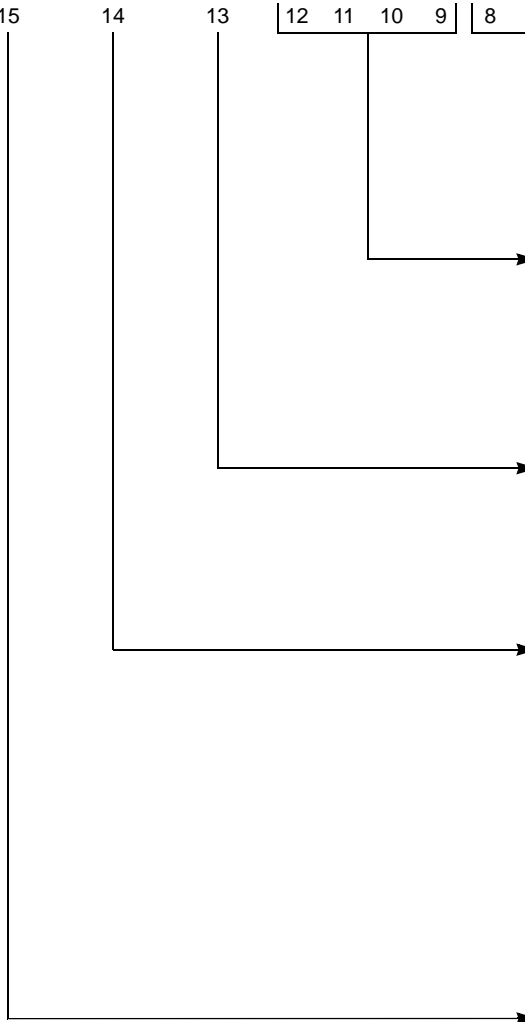
The clock divider divides CK\_IN by the decimation factor HDEC to produce CK\_DEC. CK\_DEC clocks the Decimation Register, Comb Filter section, HDF output register. In the FIR filter CK\_DEC is used to indicate that a new data sample is available for processing. The clock generator is cleared by RESET and is not enabled until the DDF is started by an internal start signal (see "Start Logic" on page 9).

The Control Register Logic enables the updating of the Control registers which contain all of the filter parameter data. When WR and CS are asserted, the control register addressed by bits A0 and A1 is loaded with the data on the C\_BUS.

**DDF Control Registers**

F\_Register (A1 = 0, A0 = 0)

F_OAD	F_BYP	F_ESYM	F_DRATE				F_TAPS								
FA0	FB0	ES0	D3	D2	D1	D0	T8	T7	T6	T5	T4	T3	T2	T1	T0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0



**F\_TAPS**

Bits T0-T8 are used to specify the number of FIR filter taps. The number entered is one less than the number of taps required. For example, to specify a 511 tap filter F\_TAPS would be programmed to 510. The minimum number of FIR taps = 3 (F\_TAPS = 2).

**F\_DRATE**

Bits D0-D3 are used to specify the amount of FIR decimation. The number entered is one less than the decimation required. For example, to specify decimation of 16, F\_DRATE would be programmed to 15. For no FIR decimation, F\_DRATE would be set equal to 0. FDRATE +1 is defined as FDEC.

**F\_ESYM**

Bit ES0 is used to select the FIR symmetry. F\_ESYM is set equal to one to select even symmetry and set equal to zero to select odd symmetry. When F\_ESYM is one, data is added in the pre-adder; when it is zero, data is subtracted. Normally set to one.

**F\_BYP**

FB0 is used to select FIR bypass mode. FIR bypass mode is selected by setting F\_BYP = 1. When FIR bypass mode is selected, the FIR is internally set up for a 3 tap even symmetric filter, no decimation (F\_DRATE = 0) and F\_OAD is set equal to one to zero one side of the preadder. In FIR bypass mode all FIR filter parameters, except F\_CLA, are ignored, including the contents of the FIR coefficient RAM. In FIR bypass mode the output data is brought output on the lower 16 bits of the output bus DATA\_OUT 0-15. To disable FIR bypass mode, F\_BYP is set equal to zero. When F\_BYP is returned to zero, the coefficients must be reloaded.

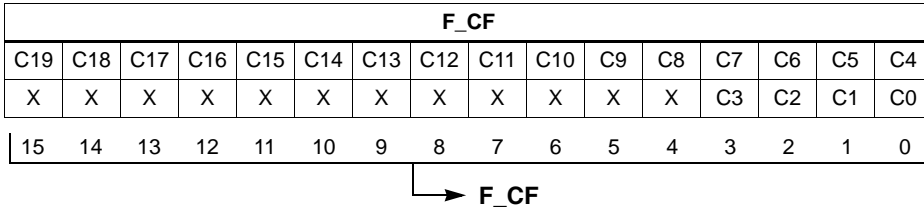
**F\_OAD**

Bit FA0 is used to select the zero the preadder mode. This mode zeros one of the inputs to the pre-adder. Zero preadder mode is selected by setting F\_OAD equal to one. This feature is useful when implementing arbitrary phase filters or can be used to verify the filter coefficients. To disable the Zero Preadder mode F\_OAD is set equal to zero.

FIGURE 4.

**DDF Control Registers** (Continued)

FC\_Register (A1 = 0, A0 = 1)



Bits C0-C19 represent the coefficient data, where C19 is the MSB. Two writes are required to write each coefficient which is 2's complement fractional format. The first write loads C19 through C4; C3 through C0 are loaded on the second write cycle. As the coefficients are written into this register they are formatted into a 20-bit coefficient and written into the Coefficient RAM sequentially starting with address location zero. The coefficients must be loaded sequentially, with the center tap being the last coefficient to be loaded. See "Coefficient RAM" on page 10.

**FIGURE 5.**

**DDF Control Registers** (Continued)

H\_Register 1 (A1 = 1, A0 = 0)

RESERVED			F_DIS	F_CLA	H_BYB	H_DRATE									
			FD0	FC0	HB0	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

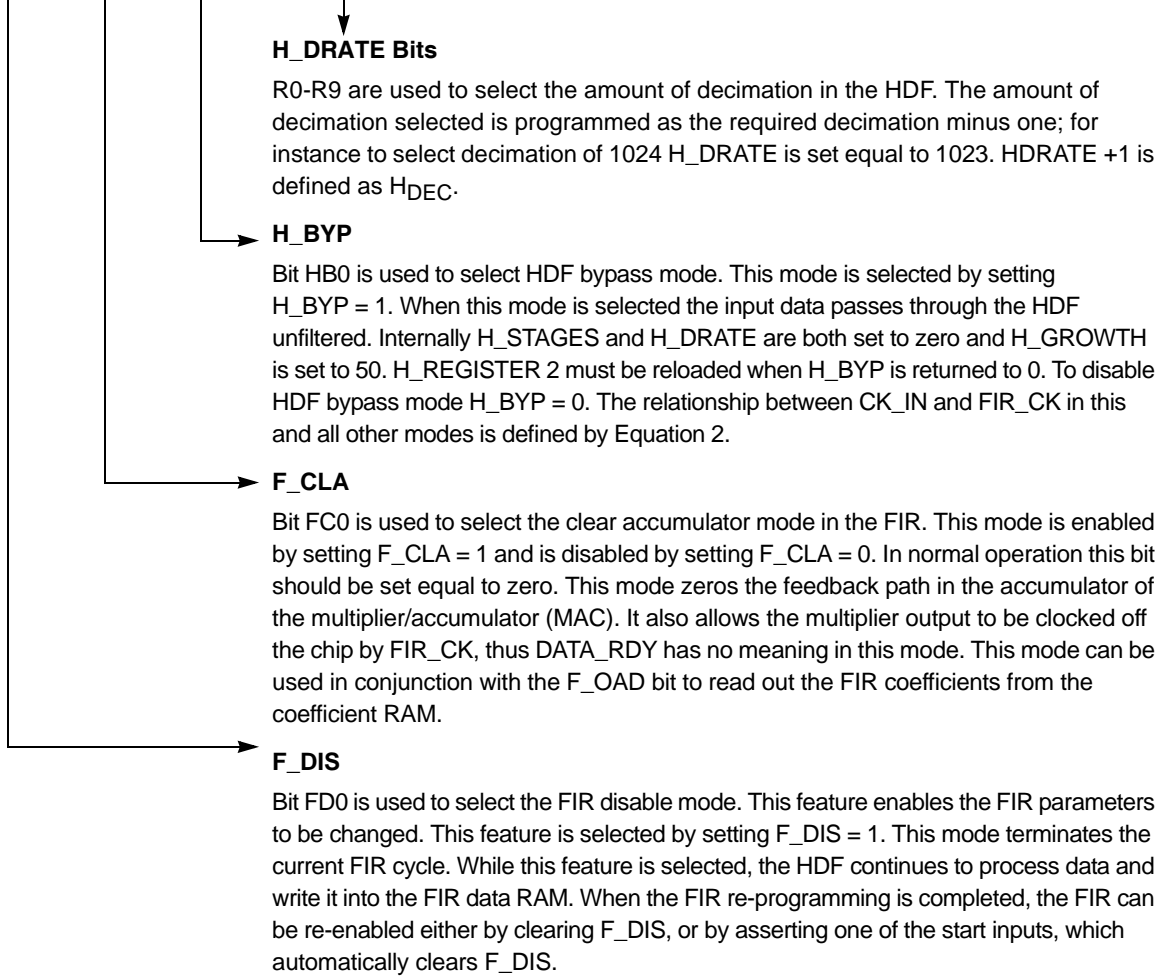


FIGURE 6.



**DDF Control Registers** (Continued)

H\_Register 2 (A1 = 1, A0 = 1)

RESERVED					H_GROWTH						H_STAGES				
					G5	G4	G3	G2	G1	G0	N2	N1	N0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**H\_STAGES**

Bits N0-N2 are used to select the number of stages or order of the HDF filter. The number that is programmed in is equal to the required number of stages. For a 5th order filter, H\_STAGES would be set equal to 5.

**H\_GROWTH**

Bits G0-G5 are used to select the proper amount of growth bits. H\_GROWTH is calculated using Equation 1:

$$H\_GROWTH = 50 - \text{CEILING}\{H\_STAGES \times \log(H\_DEC) / \log(2)\} \tag{EQ. 1}$$

where the CEILING { } means use the next largest integer of the result of the value in brackets and log is the log to the base 10.

The value of H\_GROWTH represents the position of the LSB on the output of the data shifter.

FIGURE 7.

**Start Logic**

The Start Logic generates a start signal that is used internally to synchronously start the DDF. If  $\overline{ASTARTIN}$  is asserted ( $\overline{STARTIN}$  must be tied high) the Start Logic synchronizes it to CK\_IN by double latching the signal and generating the signal  $\overline{STARTOUT}$ , which is shown in Figure 8. The  $\overline{STARTOUT}$  signal is then used to synchronously start other DDFs in a multi-chip configuration (the  $\overline{STARTOUT}$  signal of the first DDF would be tied to the  $\overline{STARTIN}$  of the second DDF). The NAND gate shown in Figure 8 then passes this synchronized signal to be used on-chip to provide a synchronous start. Once started, the chip requires a  $\overline{RESET}$  to halt operation.

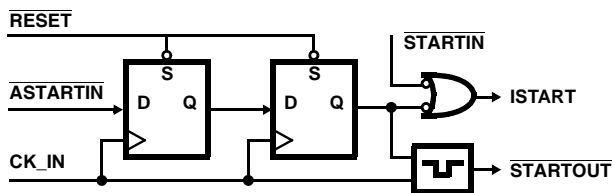


FIGURE 8. START LOGIC

When  $\overline{STARTIN}$  is asserted ( $\overline{ASTARTIN}$  must be tied high) the NAND gate passes  $\overline{STARTIN}$  which is used to provide the internal start,  $\overline{ISTART}$ , for the DDF. When  $\overline{RESET}$  is asserted the internal start signal is held inactive, thus it is necessary to

assert either  $\overline{ASTARTIN}$  or  $\overline{STARTIN}$  in order to start the DDF. The timing of the first valid DATA\_IN with respect to  $\overline{START\_IN}$  is shown in the Timing Waveforms.

In using  $\overline{ASTARTIN}$  or  $\overline{STARTIN}$  a high to low transition must be detected by the rising edge of CK\_IN, therefore these signals must have been high for more than one CK\_IN cycle and then taken low.

**The FIR Section**

The second filter in the top level block diagram is a Finite Impulse Response (FIR) filter which performs the final shaping of the signal spectrum and suppresses the aliasing components in the transition band of the HDF. This enables the DDF to implement filters with narrow pass bands and sharp transition bands.

The FIR is implemented in a transversal structure using a single multiplier/accumulator (MAC) and RAM for storage of the data and filter coefficients as shown in Figure 9. The FIR can implement up to 512 symmetric taps and decimation up to 16.

The FIR is divided into 2 sections: the FIR filter section and the FIR control logic.

**Coefficient RAM**

The Coefficient RAM stores the coefficients for the current FIR filter being implemented. The coefficients are loaded into the Coefficient RAM over the control bus (C\_BUS). The coefficients are written into the Coefficient RAM sequentially, starting at location zero. It is only necessary to write one half of the coefficients when symmetric filters are being implemented, where the last coefficient to be written in is the center tap.

The coefficients are loaded into address 01 in two writes. The first write loads the upper 16 bits of the 20-bit coefficient, C4 through C19. The second write loads the lower 4 bits of the coefficient, C0 through C3, where C19 is the MSB. The two 16-bit writes are then formatted into the 20-bit coefficient that is then loaded into the Coefficient RAM starting at RAM address location zero, where the coefficient at this location is the outer tap (or the first coefficient value).

To reload coefficients, the Coefficient RAM Address pointer must be reset to location zero so that the coefficients will be loaded in the order the FIR filter expects. There are two methods that can be used to reset the Coefficient RAM address pointer. The first is to assert  $\overline{\text{RESET}}$ , which automatically resets the pointer, but also clears the HDF and alters some of the control register bits. ( $\overline{\text{RESET}}$  does not change any of the coefficient values.) The second method is to set the F\_DIS bit in control register H\_REGISTER1. This control bit allows any of the FIR control register bits to be re-programmed, but does not automatically modify any control registers. When the programming is completed, the FIR is re-started by clearing the F\_DIS bit or by asserting one of the start inputs (ASTARTIN or STARTIN). The F\_DIS bit allows the filter parameters to be changed more quickly and is thus the recommended reprogramming method.

**Data RAM**

The Data RAM stores the data needed for the filter calculation. The format of the data is:

$$2^0 \cdot 2^{-1} 2^{-2} 2^{-3} 2^{-4} 2^{-5} 2^{-6} 2^{-7} 2^{-8} 2^{-9} 2^{-10} 2^{-11} 2^{-12} 2^{-13} 2^{-14} 2^{-15}$$

where the sign bit is in the  $2^0$  location.

The 16-bit output of the HDF Output Register is written into the Data Ram on the rising edge of CK\_DEC.

$\overline{\text{RESET}}$  initializes the write pointer to the data RAM. After a  $\overline{\text{RESET}}$  occurs, the output of the FIR will not be valid until the number of new data samples written to the Data RAM equals TAPS.

The filter always operates on the most current sample and the taps-1 previous samples. Thus if the F\_DIS bit is set, data continues to be written into the data RAM coming from the HDF section. When the FIR is enabled again the filter will be operating on the most current data samples and thus another transient response will not occur.

The maximum throughput of the FIR filter is limited by the use of a single Multiplier/Accumulator (MAC). The data output from the HDF being clocked into the FIR filter by CK\_DEC must not be at a rate that causes an erroneous result being calculated because data is being overwritten.

Equation 2 describes the relationship between, FIR\_CK, CK\_DEC, the number of taps that can be implemented in the FIR, the decimation rate in the HDF and the decimation rate in the FIR. (In the Design Considerations section of the "Operational Section" on page 12 there is a chart that shows the tradeoffs between these parameters.)

$$\text{FIR\_CK} \geq \frac{\text{CK\_IN}[(\text{TAPS}/2) + 4 + \text{F\_DEC}]}{\text{H\_DEC} \text{ F\_DEC}} \quad (\text{EQ. 2})$$

This equation expresses the minimum FIR\_CK. The minimum FIR\_CK is the smallest integer multiple of CK\_IN that satisfies Equation 1. In addition, the TSK specification must be met (see AC Electrical Specifications). F\_DEC is the decimation rate in the FIR (F\_DEC = F\_DRATE + 1), where TAPS = the number of taps in the FIR for even length filters and equals the number of taps+1 for odd length filters.

Solving Equation 3 for the maximum number of taps:

$$\text{TAPS} = 2 \left( \frac{\text{FIR\_CK} \text{ H\_DEC} \text{ F\_DEC}}{\text{CK\_IN}} - \text{F\_DEC} - 4 \right) \quad (\text{EQ. 3})$$

In using this equation, it must be kept in mind that CK\_IN/H\_DEC must be less than or equal to 4MHz (unless the HDF is in bypass mode in which case this limitation in the HDF does not apply). In the "Operational Section" on page 12 under the Design Considerations, there is a table that shows the trade-offs of these parameters. In addition, Intersil provides a software package called DECIMATE™ which designs the DDF filter from System specifications.

The registered outputs of the data RAM are added or subtracted in the 17-bit pre-adder. The F\_OAD control bit allows zeros to be input into one side of the pre-adder. This provides the capability to implement non-symmetric filters.

The selection of adding the register outputs for an even symmetric filter or for subtracting the register outputs for odd symmetric filter is provided by the control bit F\_ESYM, which is programmed over the control bus. When subtraction is selected, the new data is subtracted from the old data. The 17-bit output of the adder forms one input of the multiplier/accumulator.

A control bit F\_CLA provides the capability to clear the feedback path in the accumulator such that multiplier output will not be accumulated, but will instead flow directly to the output register. The bit weightings of the data and coefficients as they are processed in the FIR is shown as follows.

$$\begin{aligned} \text{Input Data (from HDF)} & \quad 2^0 \cdot 2^{-1} \dots 2^{-15} \\ \text{Pre-adder Output} & \quad 2^1 2^0 \cdot 2^{-1} \dots 2^{-15} \\ \text{Coefficient} & \quad 2^0 \cdot 2^{-1} \dots 2^{-19} \\ \text{Accumulator} & \quad 2^8 \dots 2^0 \cdot 2^1 \dots 2^{-34} \end{aligned}$$

**FIR Output**

The 40 most significant bits of the accumulator are latched into the output register. The lower 3 bits are not brought to the output. The 40 bits out of the output register are selected to be output by a pair of multiplexers. This register is clocked by FIR\_CK (see Figure 9).

There are two multiplexers that route 24 of the 40 output bits from the output register to the output pins. The first multiplexer selects the output register bits that will be routed to output pins DATA\_OUT16-23 and the second multiplexer selects the output register bits that will be routed to output pins DATA\_OUT0-15.

The multiplexers are controlled by the control signal F\_BYP and the OUT\_SELH pin. F\_BYP and OUT\_SELH both

control the first multiplexer that selects the upper 8 bits of the output bus, DATA\_OUT16-23. F\_BYP controls the second multiplexer that selects the lower 16 bits of the output bus, DATA\_OUT0-15. The output formatter is shown in detail in Figure 10.

**FIR Control Logic**

The DATA\_RDY strobe indicates that new data is available on the output of the FIR. The rising edge of DATA\_RDY can be used to load the output data into an external register or RAM.

**Data Format**

The DDF maintains 16 bits of accuracy in both the HDF and FIR filter stages. The data formats and bit weightings are shown in Figure 11.

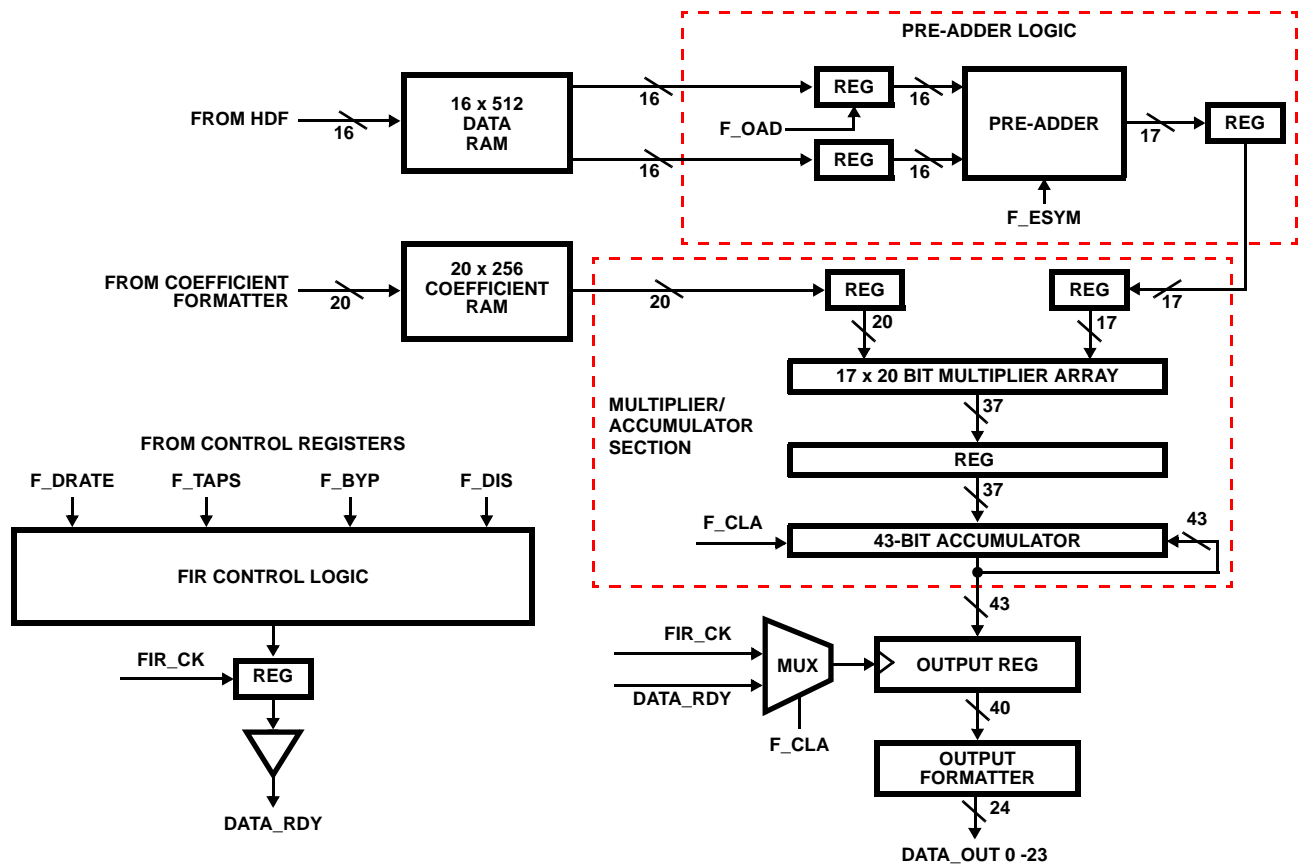


FIGURE 9. FIR FILTER

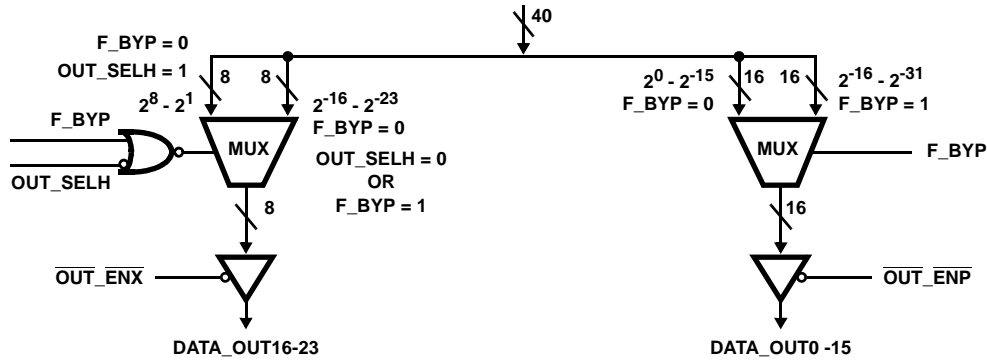


FIGURE 10. FIR OUTPUT FORMATTER

**INPUT DATA FORMAT**

Fractional Two's Complement Input

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$	$2^{-4}$	$2^{-5}$	$2^{-6}$	$2^{-7}$	$2^{-8}$	$2^{-9}$	$2^{-10}$	$2^{-11}$	$2^{-12}$	$2^{-13}$	$2^{-14}$	$2^{-15}$

**FIR COEFFICIENT FORMAT**

Fractional Two's Complement Input

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$	$2^{-4}$	$2^{-5}$	$2^{-6}$	$2^{-7}$	$2^{-8}$	$2^{-9}$	$2^{-10}$	$2^{-11}$	$2^{-12}$	$2^{-13}$	$2^{-14}$	$2^{-15}$	$2^{-16}$	$2^{-17}$	$2^{-18}$	$2^{-19}$

**OUTPUT DATA FORMAT**

Fractional Two's Complement Output

FOR: **OUT\_SELH = 1, F\_BYP = 0**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$2^{-8}$	$2^{-7}$	$2^{-6}$	$2^{-5}$	$2^{-4}$	$2^{-3}$	$2^{-2}$	$2^{-1}$	$2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$	$2^{-4}$	$2^{-5}$	$2^{-6}$	$2^{-7}$	$2^{-8}$	$2^{-9}$	$2^{-10}$	$2^{-11}$	$2^{-12}$	$2^{-13}$	$2^{-14}$	$2^{-15}$

FOR: **OUT\_SELH = 0, F\_BYP = 0**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	23	22	21	20	19	18	17	16
$2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$	$2^{-4}$	$2^{-5}$	$2^{-6}$	$2^{-7}$	$2^{-8}$	$2^{-9}$	$2^{-10}$	$2^{-11}$	$2^{-12}$	$2^{-13}$	$2^{-14}$	$2^{-15}$	$2^{-16}$	$2^{-17}$	$2^{-18}$	$2^{-19}$	$2^{-20}$	$2^{-21}$	$2^{-22}$	$2^{-23}$

FOR: **OUT\_SELH = X, F\_BYP = 1**

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$2^{-16}$	$2^{-17}$	$2^{-18}$	$2^{-19}$	$2^{-20}$	$2^{-21}$	$2^{-22}$	$2^{-23}$	$2^{-16}$	$2^{-17}$	$2^{-18}$	$2^{-19}$	$2^{-20}$	$2^{-21}$	$2^{-22}$	$2^{-23}$	$2^{-24}$	$2^{-25}$	$2^{-26}$	$2^{-27}$	$2^{-28}$	$2^{-29}$	$2^{-30}$	$2^{-31}$

FIGURE 11.

**Operational Section**

**Start Configurations**

The scenario to put the DDF into operational mode is: reset the DDF by asserting the  $\overline{\text{RESET}}$  input, configure the DDF over the control bus, and apply a start signal, either by  $\overline{\text{ASTARTIN}}$  or  $\overline{\text{STARTIN}}$ . Until the DDF is put in operational mode with a start pulse, the DDF ignores all data inputs.

To use the asynchronous start, an asynchronous active low pulse is applied to the  $\overline{\text{ASTARTIN}}$  input.  $\overline{\text{ASTARTIN}}$  is internally synchronized to the sample clock,  $\text{CK\_IN}$ , and generates  $\overline{\text{STARTOUT}}$ . This signal is also used internally

when the asynchronous mode is selected. It puts the DDF in operational mode and allows the DDF to begin accepting data. When the  $\overline{\text{ASTARTIN}}$  input is being used, the  $\overline{\text{STARTIN}}$  input must be tied high to ensure proper operation.

To start the DDF synchronously, the  $\overline{\text{STARTIN}}$  is asserted with a active low pulse that has been externally synchronized to  $\text{CK\_IN}$ . Internally the DDF then uses this start pulse to put the DDF in operate mode and start accepting data inputs. When  $\overline{\text{STARTIN}}$  is used to start the DDF the  $\overline{\text{ASTARTIN}}$  input must be tied high to prevent false starts.

**Multi-Chip Start Configurations**

Since there are two methods to start-up the DDF, there are also two configurations that can be used to start-up multiple chips.

The first method is shown in Figure 12. The timing of the  $\overline{\text{STARTOUT}}$  circuitry starts the second DDF on the same clock as the first. If more DDFs are also to be started synchronously,  $\overline{\text{STARTOUT}}$  is connected to their  $\overline{\text{STARTIN}}$ 's.

The second method to start-up DDFs in a multiple chip configuration is to use the synchronous start scenario.

The  $\overline{\text{STARTIN}}$  input is wired to all the chips in the chain, and is asserted by a active low synchronous pulse that has been externally synchronized to  $\text{CK\_IN}$ . In this way all DDFs are synchronously started. The  $\overline{\text{ASTARTIN}}$  input on all the chips is tied high to prevent false starts. The  $\overline{\text{STARTOUT}}$  outputs are all left unconnected. This configuration is illustrated in Figure 13.

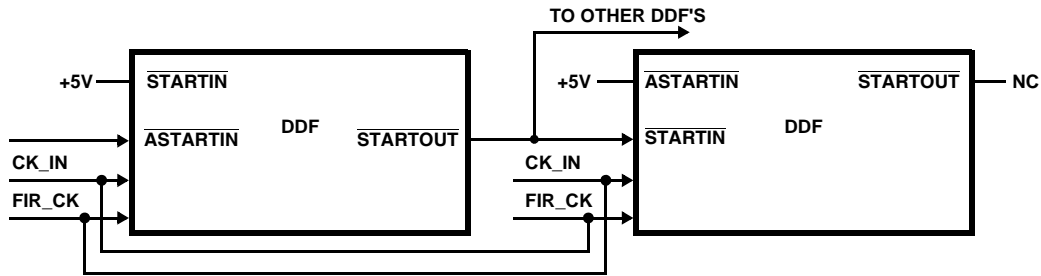


FIGURE 12. ASYNCHRONOUS START-UP

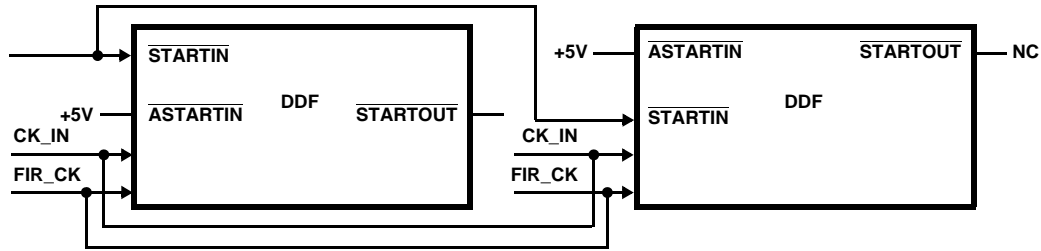


FIGURE 13. SYNCHRONOUS START-UP

**Chip Set Application**

The HSP43220 is ideally suited for narrow band filtering in Communications, Instrumentation and Signal Processing applications. The HSP43220 provides a fully integrated solution to high order decimation filtering.

The combination of the HSP43220 and the HSP45116 (which is a NCOM Numerically Controlled Oscillator/ Modulator) provides a complete solution to digital receivers. The diagram in Figure 14 illustrates this concept.

The HSP45116 down converts the signal of interest to baseband, generating a real component and an imaginary component. A HSP43220 then performs low pass filtering and reduces the sampling rate of each of the signals.

The system scenario for the use of the DDF involves a narrow band signal that has been over-sampled. The signal is over-sampled in order to capture a wide frequency band containing many narrow band signals. The NCOM is "tuned" to the frequency of the signal of interest and performs a complex down conversion to baseband of this signal, which results in a complex signal centered at baseband. A pair of DDFs then low pass filters the NCOM output, extracting the signal of interest.

**Design Trade-Off Considerations**

Equation 2 in the Functional Description section expresses the relationship between the number of TAPS which can be implemented in the FIR as a function of  $\text{CK\_IN}$ ,  $\text{FIR\_CK}$ ,  $H_{\text{DEC}}$ ,  $F_{\text{DEC}}$ . Table 1 provides a tradeoff of these parameters. For a given speed grade and the ratio of the clocks, and assuming minimum decimation in the HDF, the number of FIR taps that can be implemented is given in Equation 2.

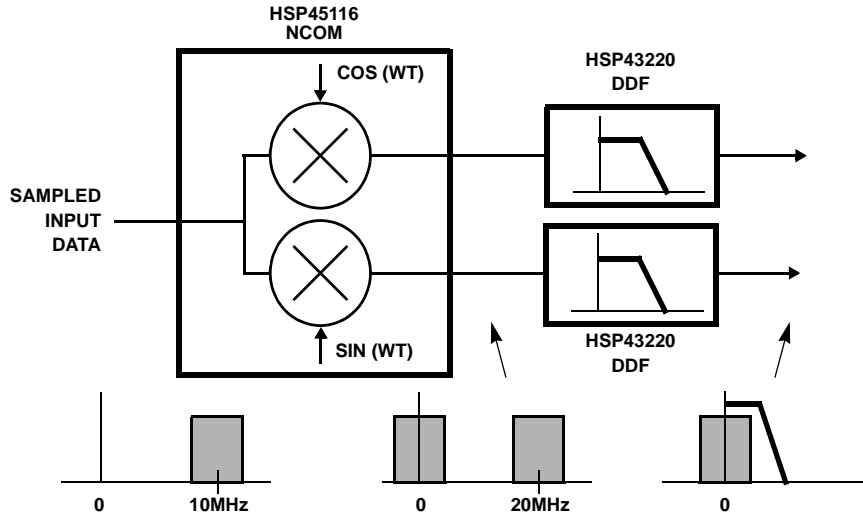


FIGURE 14. DIGITAL CHANNELIZER

TABLE 1. DESIGN TRADE OFF FOR MINIMUM H<sub>DEC</sub>

SPEED GRADE (MHz)	FIR_CK / CK_IN	MIN H <sub>DEC</sub>	TAPS				
			F <sub>DEC</sub> = 1	F <sub>DEC</sub> = 2	F <sub>DEC</sub> = 4	F <sub>DEC</sub> = 8	F <sub>DEC</sub> = 16
33	1	9	8	24	56	120	248
25.6	1	7	4	16	40	88	184
15	1	4	(Note)	4	16	40	88
33	2	5	10	28	64	136	280
25.6	2	4	6	20	48	104	216
15	2	2	(Note)	4	16	40	88
33	4	3	14	36	80	168	344
25.6	4	2	6	20	48	104	216
15	4	1	(Note)	4	16	40	88
33	8	2	22	52	112	232	472
25.6	8	1	6	20	48	104	216
15	8	1	6	20	48	104	216

NOTE: Filter not realizable.

## **DECIMATE**

Intersil provides a development system which assists the design engineer to utilizing this filter. The DECIMATE software package provides the user with both filter design and simulation environments for filter evaluation and design. These tools are integrated within one standard DSP CAD environment, The Athena Group's Monarch Professional DSP Software package.

The software package is designed specifically for the DDF. It provides all the filter design software for this proprietary architecture. It provides a user-friendly menu driven interface to allow the user to input system level filter requirements. It provides the frequency response curves and a data flow simulation of the specified filter design (Figure 15). It also creates all the information necessary to program the DDF, including a PROM file for programming the control registers.

This software package runs on an IBM™ PC™, XT™, AT™, PS/2™ computer or 100% compatible with the following configuration:

640k RAM

5.25" or 3.5" Floppy drive

hard disk

math co-processor

MS/PC-DOS 2.0 or higher

CGA, MCGA, EGA, VGA and

Hercules graphics adapters

For more information, see the description of DECIMATE in "DECIMATE" on page 15.

HSP43220 DDF FILTER SPECIFICATION

```

Filter File      : vectors\example.DDF
Input Sample Rate: 33 MHz   Design Mode      : AUTO
Output Rate     : 100 kHz  Generate Report  : YES
Passband        : 20 kHz   Display Response : LOG
Transition Band  : 7.5 kHz  Save Freq Responses: YES
Passband Atten  : 0.5 dB   Save FIR Response  : YES
Stopband Atten  : 80 dB
    
```

FIR Type : PRECOMP

```

HDF Order      : 4      FIR Input Rate : 300 kHz
HDF Decimation : 110   FIR Clock (min) : 33 MHz
HDF Scale Factor : 0.54542  FIR Order      : 135
                                   FIR Decimation     : 3
    
```

(C) Harris Semiconductor 1990

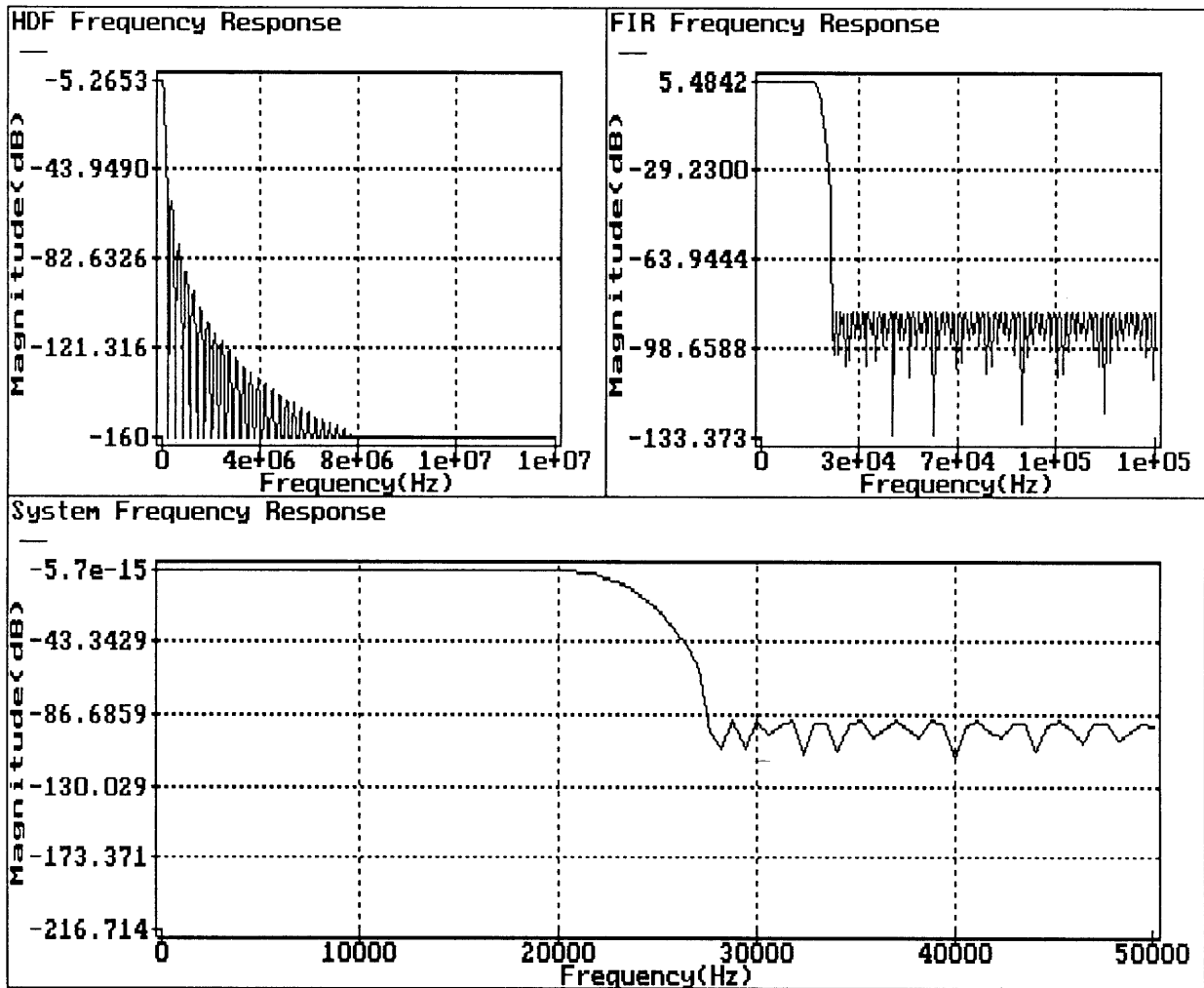


FIGURE 15. DECIMATE DESIGN MODULE SCREENS



# HSP43220

## Absolute Maximum Ratings $T_A = +25^\circ\text{C}$

Supply Voltage . . . . . +6.0V  
 Input, Output or I/O Voltage Applied . . . . . GND -0.5V to  $V_{CC} +0.5V$   
 ESD Classification . . . . . Class 1

## Operating Conditions

Temperature Range . . . . .  $0^\circ\text{C}$  to  $+70^\circ\text{C}$   
 Voltage Range . . . . . +4.75V to +5.25V

## Thermal Information

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  ( $^\circ\text{C}/\text{W}$ )  
 PLCC Package . . . . . 35  
 Maximum Storage Temperature Range . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Maximum Junction Temperature  
 PLCC Package . . . . .  $+150^\circ\text{C}$   
 Pb-Free Reflow Profile . . . . . see link below  
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

## Die Characteristics

Component Count . . . . . 193,000 Transistors

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTE:

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

**DC Electrical Specifications** Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	$V_{IH}$	$V_{CC} = 5.25V$	2.0	-	V
Logical Zero Input Voltage	$V_{IL}$	$V_{CC} = 4.75V$	-	0.8	V
High Level Clock Input	$V_{IHC}$	$V_{CC} = 5.25V$	3.0	-	V
Low Level Clock Input	$V_{ILC}$	$V_{CC} = 4.75V$	-	0.8	V
Output HIGH Voltage	$V_{OH}$	$I_{OH} = -400\mu\text{A}$ , $V_{CC} = 4.75V$	2.6	-	V
Output LOW Voltage	$V_{OL}$	$I_{OL} = +2.0\text{mA}$ , $V_{CC} = 4.75V$	-	0.4	V
Input Leakage Current	$I_I$	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$	-10	10	$\mu\text{A}$
I/O Leakage Current	$I_O$	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 5.25V$	-10	10	$\mu\text{A}$
Standby Power Supply Current	$I_{CCSB}$	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.25V$ , (Note 3)	-	500	$\mu\text{A}$
Operating Power Supply Current	$I_{CCOP}$	$f = 15\text{MHz}$ , $V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$ , (Notes 2, 4)	-	120	mA

## Capacitance $T_A = +25^\circ\text{C}$ , (Note 3)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input Capacitance	$C_{IN}$	FREQ = 1MHz, $V_{CC} = \text{Open}$ , All measurements are referenced to device ground	-	12	pF
Output Capacitance	$C_O$		-	10	pF

### NOTES:

- Power supply current is proportional to operating frequency. Typical rating for  $I_{CCOP}$  is 8mA/MHz.
- Not tested, but characterized at initial design and at major process/design changes.
- Output load per test load circuit with switch open and  $C_L = 40\text{pF}$ .

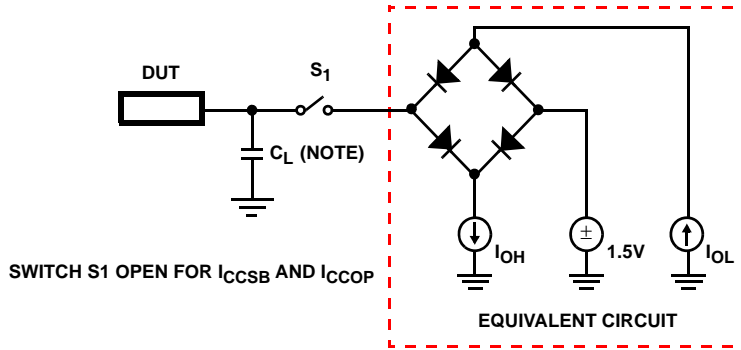
**AC Electrical Specifications**  $V_{CC} = +4.75V$  to  $+5.25V$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$  (Note 7). Parameters with MIN and/or MAX limits are 100% tested at  $+25^{\circ}C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	NOTES	-15		-25		-33		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
Input Clock Frequency	$F_{CK}$		0	15	0	25.6	0	33	MHz
FIR Clock Frequency	$F_{FIR}$		0	15	0	25.6	0	33	MHz
Input Clock Period	$t_{CK}$		66	-	39	-	30	-	ns
FIR Clock Period	$t_{FIR}$		66	-	39	-	30	-	ns
Clock Pulse Width Low	$t_{SPWL}$		26	-	16	-	13	-	ns
Clock Pulse Width High	$t_{SPWH}$		26	-	16	-	13	-	ns
Clock Skew Between FIR_CK and CK_IN	$t_{SK}$		0	$t_{FIR} - 25$	0	$t_{FIR} - 15$	0	$t_{FIR} - 15$	ns
CK_IN Pulse Width Low	$t_{CH1L}$	(Notes 5, 8)	29	-	19	-	19	-	ns
CK_IN Pulse Width High	$t_{CH1H}$	(Notes 5, 8)	29	-	19	-	19	-	ns
CK_IN Setup to FIR_CK	$t_{CIS}$	(Notes 5, 8)	27	-	17	-	17	-	ns
CK_IN Hold from FIR_CK	$t_{CIH}$	(Notes 5, 8)	2	-	2	-	2	-	ns
RESET Pulse Width Low	$t_{RSPW}$		$4t_{CK}$	-	$4t_{CK}$	-	$4t_{CK}$	-	ns
Recovery Time on RESET	$t_{RTRS}$		$8t_{CK}$	-	$8t_{CK}$	-	$8t_{CK}$	-	ns
ASTARTIN Pulse Width Low	$t_{AST}$		$t_{CK} + 10$	-	$t_{CK} + 10$	-	$t_{CK} + 10$	-	ns
STARTOUT Delay from CK_IN	$t_{STOD}$		-	35	-	20	-	18	ns
STARTIN Setup to CK_IN	$t_{STIC}$		25	-	15	-	10	-	ns
Setup Time on DATA_IN	$t_{SET}$		20	-	15	-	14	-	ns
Hold Time on All inputs	$t_{HOLD}$		0	-	0	-	0	-	ns
Write Pulse Width Low	$t_{WL}$		26	-	15	-	12	-	ns
Write Pulse Width High	$t_{WH}$		26	-	20	-	18	-	ns
Setup Time on Address Bus Before the Rising Edge of Write	$t_{STADD}$		26	-	20	-	20	-	ns
Setup Time On-chip Select Before the Rising Edge of Write	$t_{STCS}$		26	-	20	-	20	-	ns
Setup Time on Control Bus Before the Rising Edge of Write	$t_{STCB}$		26	-	20	-	20	-	ns
DATA_RDY Pulse Width Low	$t_{DRPWL}$		$2t_{FIR} - 20$	-	$2t_{FIR} - 10$	-	$2t_{FIR} - 10$	-	ns
DATA_OUT Delay Relative to FIR_CK	$t_{FIRDV}$		-	50	-	35	-	28	ns
DATA_RDY Valid Delay Relative to FIR_CK	$t_{FIRDR}$		-	35	-	25	-	20	ns
DATA_OUT Delay Relative to OUT_SELH	$t_{OUT}$		-	25	-	20	-	20	ns
Output Enable to Data Out Valid	$t_{OEV}$	(Note 6)	-	15	-	15	-	15	ns
Output Disable to Data Out Three-State	$t_{OEZ}$	(Note 5)	-	15	-	15	-	15	ns
Output Rise, Output Fall Times	$t_r, t_f$	from 0.8V to 2V, (Note 5)	-	8	-	8	-	6	ns

NOTES:

- Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
- Transition is measured at  $\pm 200mV$  from steady state voltage with loading as specified in test load circuit with and  $C_L = 40pF$ .
- AC Testing is performed as follows: Input levels (CLK Input) 4.0V and 0V, Input levels (all other Inputs) 0V and 3.0V, Timing reference levels (CLK) = 2.0V, (Others) = 1.5V, Output load per test load circuit and  $C_L = 40pF$ .
- Applies only when  $H\_BYP = 1$  or  $H\_DRATE = 0$ .

AC Test Load Circuit



NOTE: Test head capacitance.

Timing Waveforms

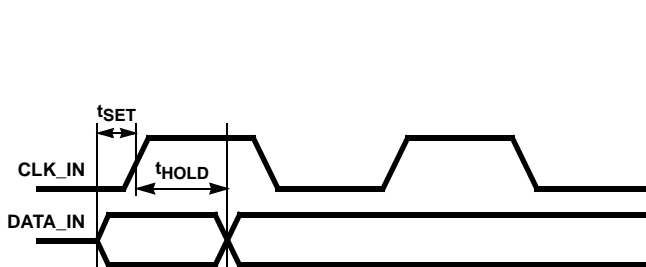


FIGURE 16A.

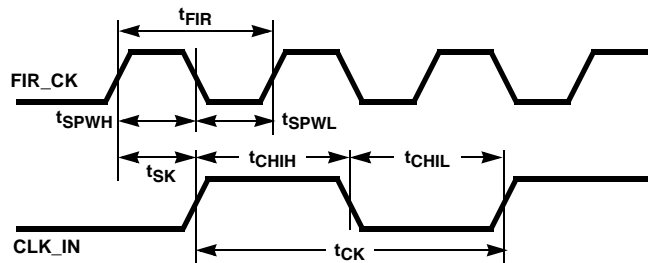


FIGURE 16B.

FIGURE 16. INPUT TIMING

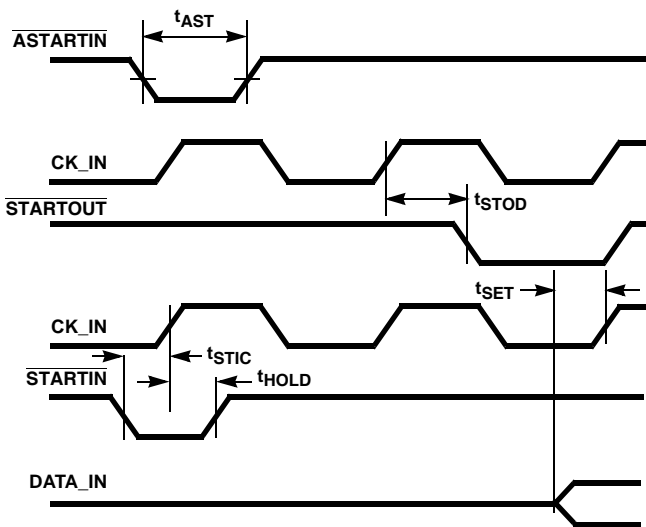


FIGURE 17A.

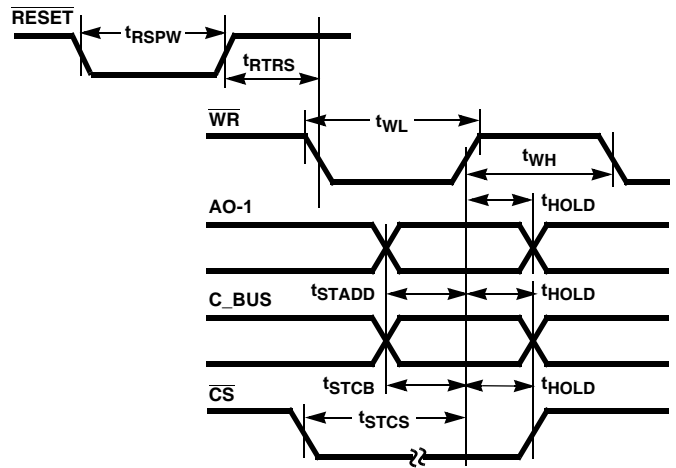


FIGURE 17B.

FIGURE 17. START TIMING

Timing Waveforms (Continued)

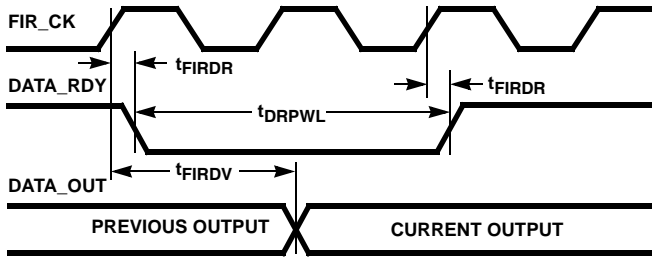


FIGURE 18A.

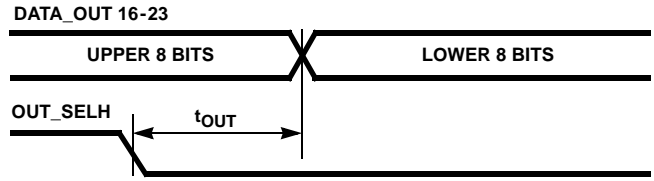


FIGURE 18B.

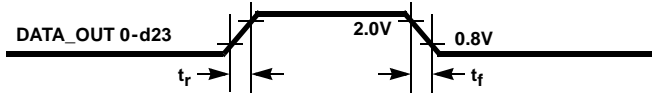


FIGURE 18C.

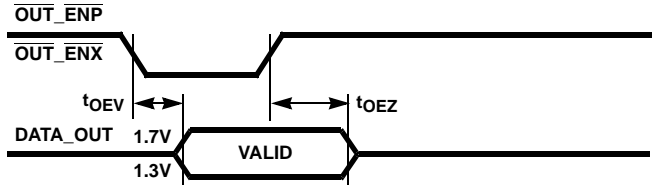


FIGURE 18D.

FIGURE 18.

