

General Description

The MAX3349E ±15kV ESD-protected, USB transceiver provides a full-speed USB interface to a lower voltage microprocessor or ASIC. The device supports enumeration, suspend, and VBUS detection. A special UART multiplexing mode routes external UART signals (Rx and Tx) to D+ and D-, allowing the use of a shared connector to reduce cost and part count for mobile devices.

The UART interface allows mobile devices such as PDAs, cellular phones, and digital cameras to use either UART or USB signaling through the same connector. The MAX3349E features a separate UART voltage supply input to support legacy devices using +2.75V signaling. The MAX3349E supports a maximum UART baud rate of 921kbaud.

Upon connection to a USB host, the MAX3349E enters USB mode and provides a full-speed USB 2.0 compliant interface through VP, VM, RCV, and OE. The MAX3349E features internal series termination resistors on D+ and D-, and an internal $1.5k\Omega$ pullup resistor to D+ to allow the device to logically connect and disconnect from the USB while plugged in. A suspend mode is provided for low-power operation. D+ and D- are protected from electrostatic discharge (ESD) up to ±15kV.

The MAX3349E is available in 16-pin TQFN (4mm x 4mm) and 16-bump UCSP™ (2mm x 2mm) packages, and is specified over the -40°C to +85°C extended temperature range.

Applications

Cell Phones

PDAs

Digital Cameras

MP3 Players

Features

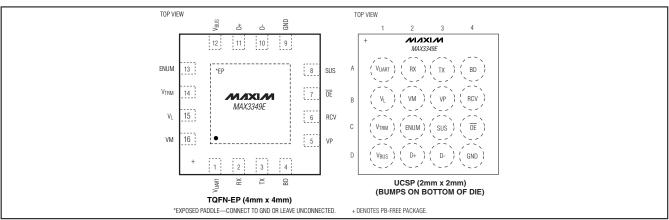
- ±15kV ESD HBM Protection on D+ and D-
- **♦ UART Mode Routes External UART Signals to** D+/D-
- ♦ Internal Linear Regulator Allows Direct Powering from the USB Cable
- Separate Voltage Input for UART Transmitter/Receiver (VUART)
- ♦ Internal 1.5kΩ Pullup Resistor on D+ Controlled by Enumerate Input
- ♦ Internal Series Termination Resistors on D+ and D-
- ♦ Complies with USB Specification Revision 2.0, **Full-Speed 12Mbps Operation**
- ♦ Built-In Level Shifting Down to +1.4V, Ensuring Compatibility with Low-Voltage ASICs
- ♦ VBUS Detection
- **♦ Combined VP and VM Inputs/Outputs**
- ♦ No Power-Supply Sequencing Required
- ♦ Available in 16-Bump UCSP (2mm x 2mm) **Package**

Ordering Information

PART	PIN-PACKAGE	PACKAGE CODE
MAX3349EEBE-T	16 UCSP	B16-1
MAX3349EETE*	16 TQFN	T1644-4

Note: All devices specified for the -40°C to +85°C extended temperature range.

Pin Configurations



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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

^{*}Future product—contact factory for availability.

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
VUART, VL, VBUS, D+, D0.3V to +6V
V _{TRM} 0.3V to (V _{BUS} + 0.3V)
VP, VM, SUS, RX, TX, ENUM, RCV, \overline{OE} , BD, -0.3V to (V _L + 0.3V)
Short Circuit Current (D+ and D-)±150mA
Maximum Continuous Current (all other pins)±15mA
Continuous Power Dissipation ($T_A = +70^{\circ}C$)
16-Bump UCSP (derate 8.2mW/°C above +70°C)659.5mW
16-Pin 4mm x 4mm TQFN (derate 25.0mW/°C
above +70°C)2000mW

Operating Temperature Range40°C to +8	5°C
Junction Temperature+15	0°C
Storage Temperature Range65°C to +15	0°C
Lead Temperature (soldering, 10s)+30	0°C
Bump Temperature (soldering, reflow)+23	5°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{BUS} = +4.0V \text{ to } +5.5V, V_{UART} = +2.7V \text{ to } +3.3V, V_{L} = +1.40V \text{ to } +2.75V, T_{A} = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } V_{BUS} = +5V, V_{L} = +1.8V, V_{UART} = +2.75V \text{ (UART Mode)}, \text{ and } T_{A} = +25^{\circ}\text{C.)} \text{ (Note 1)}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY INPUTS/OUTPUTS (VBU	S, VUART, VTRM,	V _L)				
V _{BUS} Input Range	V _{BUS}	USB mode	4.0		5.5	V
V _L Input Range	VL		1.40		2.75	V
V _{UART} Input Range	Vuart	UART mode	2.7		3.3	V
Regulated Supply-Voltage Output	V_{TRM}	Internal regulator, USB mode	3.0		3.6	V
Operating V _{BUS} Supply Current	I _{BUS}	Full-speed transmitting/receiving at 12Mbps, C _L = 50pF on D+ and D-			10	mA
Operating V _{UART} Supply Current	Ivuart	UART transmitting/receiving at 921kbaud, C _L = 200pF			2.5	mA
Static VUART Supply Current	IVUART(STATIC)	UART mode		3.5	5	μΑ
Operating V _L Supply Current	lvL	Full-speed transmitting/receiving at 12Mbps, C _L = 50pF on D+ and D-			6	mA
Full-Speed Idle and SE0 Supply Current	IVBUS(IDLE)	Full-speed idle, $V_{D+} > +2.7V$, $V_{D-} < +0.3V$		290	400	μΑ
Current		SE0: $V_{D+} < +0.3V$, $V_{D-} < +0.3V$		340	450	
Static V _L Supply Current	I _{VL(STATIC)}	Full-speed idle, SE0, suspend mode, or static UART mode		2	10	μΑ
Sharing Mode V _L Supply Current	IvL(OFF)	V _{BUS} and V _{UART} not present		2	5	μΑ
USB Suspend V _{BUS} Supply Current	lvbus(sus)	VM, VP unconnected; OE = 1, SUS = 1		38	65	μA
V _{BUS} DETECTION (BD)						
USB Power-Supply Detection Threshold	V _{TH_VBUS}		0.4 x V _L		0.9 x VL	V
USB Power-Supply Detection Hysteresis	VHYS_VBUS			40		mV
V _L Power-Supply Detection Threshold	V _{TH_V} L			0.7		V

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ELECTRICAL CHARACTERISTICS (continued)

 $(V_{BUS} = +4.0V \text{ to } +5.5V, \ V_{UART} = +2.7V \text{ to } +3.3V, \ V_{L} = +1.40V \text{ to } +2.75V, \ T_{A} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \ \text{unless otherwise noted.}$ Typical values are at $V_{BUS} = +5V, \ V_{L} = +1.8V, \ V_{UART} = +2.75V \ (UART\ Mode), \ \text{and}$ Transfer for the transfer of the transfer o

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{UART} Power-Supply Detection Threshold	VTH_UART		0.4 x V _L	0.65 x V _L	0.9 x VL	V
DIGITAL INPUTS/OUTPUTS (VP,	VM, RCV, SUS, (OE, RX, TX, ENUM, BD)				ı
Input Voltage Low	VIL				0.3 x VL	V
Input Voltage High	VIH		0.7 x V _L			V
Output Voltage Low	VoL	$I_{OL} = +2mA, V_L > 1.65V$ $I_{OL} = +1mA, V_L < 1.65V$			0.4	٧
Output Voltage High	VOH	$I_{OH} = +2mA, V_L > 1.65V$ $I_{OH} = +1mA, V_L < 1.65V$	V _L - 0.4			V
Input Leakage Current	ILKG		-1		+1	μΑ
ANALOG INPUTS/OUTPUTS (D+,	D- in USB Mode	e)	•			
Differential Input Sensitivity	V _{ID}	V _{D+} - V _{D-}	0.2			V
Differential Common-Mode Voltage	V _{CM}	Includes V _{ID} range	0.8		2.5	V
Single-Ended Input Low Voltage	VILSE				0.8	V
Single-Ended Input High Voltage	VIHSE		2.0			V
USB Output Voltage Low	Vusb_old	$R_L = 1.5k\Omega$ connected to +3.6V			0.3	V
USB Output Voltage High	Vusb_ohd	$R_L = 15k\Omega$ connected to GND	2.8		3.6	V
Off-State Leakage Current	l _{LZ}		-1		+1	μA
Driver Output Impedance	Z_{DRV}	Steady-state drive	28		43	Ω
Transceiver Capacitance	CIND	Measured from D+/D- to GND		20		pF
Input Impedance	Z _{IN}	Driver off	1			ΜΩ
D+ Internal Pullup Resistor	R _{PU}	ENUM = 1	1425	1500	1575	Ω
ANALOG INPUTS/OUTPUTS (D+,	D- in UART Mod	de)				
Input Voltage High	Vuart_ih	UART mode, +2.70 < V _{UART} < +2.85V	2.0			V
Input Voltage Low	Vuart_il	UART mode, +2.70V < V _{UART} < +2.85V			0.8	V
Output Voltage High	Vuart_oh	UART mode, +2.70V < VUART < +2.85V UART_OH = -2mA	2.2			V
Output Voltage Low	Vuart_ol	UART mode, +2.70V < VUART < +2.85V UART_OL = +2mA			0.4	V



ELECTRICAL CHARACTERISTICS (continued)

 $(V_{BUS} = +4.0V \text{ to } +5.5V, V_{UART} = +2.7V \text{ to } +3.3V, V_{L} = +1.40V \text{ to } +2.75V, T_{A} = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted.}$ Typical values are at $V_{BUS} = +5V, V_{L} = +1.8V, V_{UART} = +2.75V \text{ (UART Mode)}, \text{ and } T_{A} = +25^{\circ}C.)$ (Note 1)

ESD PROTECTION (D+, D-)								
Human Body Model		(Figures 9 and 10)	±15	kV				
IEC 61000-4-2 Air-Gap Discharge			±8	kV				
IEC 61000-4-2 Contact Discharge			±8	kV				

TIMING CHARACTERISTICS

 $(V_{BUS} = +4.0V \text{ to } +5.5V, V_{UART} = +2.7V \text{ to } +3.3V, V_L = +1.4V \text{ to } +2.75V, T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted. Typical values are at $V_{BUS} = +5V, V_L = +1.8V, V_{UART} = +2.75V \text{ (UART Mode)}$, and $T_A = +25^{\circ}\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		TYP	MAX	UNITS	
USB DRIVER CHARACTERISTICS	S (C _L = 50pF)						
Rise Time	tFR	10% to 90% of Vusb_OHD - Vusb_OLD (Figures 1 and 7)			20	ns	
Fall Time	tFF	90% to 10% of Vusb_OHD - Vusb_OLD (Figures 1 and 7)	4		20	ns	
Rise/Fall Time Matching	tFR/tFF	Excluding the first transition from idle state (Note 2) (Figures 1 and 7)	90		110	%	
Output Signal Crossover Voltage	VCRS_F	Excluding the first transition from idle state (Note 2) (Figure 2)	1.3		2.0	V	
		V _L > +1.65V (Figures 2 and 7)		22.5			
Driver Presenting Delay	tplh_drv	+1.4V < V _L < +1.65V (Figures 2 and 7)			25	ns	
Driver Propagation Delay	tphl_drv	V _L > +1.65V (Figures 2 and 7)			22.5		
		+1.4V < V _L < +1.65V (Figures 2 and 7)			25		
Driver Disable Delay	tphz_drv	High-to-off transition (Figures 3 and 6)			25	ns	
Driver Disable Delay	tplz_drv	Low-to-off transition (Figures 3 and 6)			25	113	
Driver Enable Delay	tpzh_drv	Off-to-high transition (Figures 3 and 7)			25	ns	
Driver Erlable Delay	tpzl_drv	Off-to-low transition (Figures 3 and 7)			25	115	
USB RECEIVER CHARACTERIST	ICS (C _L = 15pF	-)					
	tour pov	V _L > +1.65V (Figures 4 and 8)			25		
Differential Receiver Propagation	tPLH_RCV	+1.4V < V _L < +1.65V (Figures 4 and 8)			30		
Delay	tour pov	V _L > +1.65V (Figures 4 and 8)			25	ns	
	tphl_RCV	1.4V < V _L < +1.65V (Figures 4 and 8)			30		
	tou u or	V _L > +1.65V (Figures 4 and 8)			28		
Single-Ended Receiver	tplh_se	+1.4V < V _L < +1.65V (Figures 4 and 8)			35	_	
Propagation Delay	tour ec	V _L > +1.65V (Figures 4 and 8)			28	28 ns	
	tphl_se	+1.4V < V _L < +1.65V (Figures 4 and 8)		35			

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TIMING CHARACTERISTICS (continued)

 $(V_{BUS} = +4.0V \text{ to } +5.5V, V_{UART} = +2.7V \text{ to } +3.3V, V_{L} = +1.4V \text{ to } +2.75V, T_{A} = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } V_{BUS} = +5V, V_{L} = +1.8V, V_{UART} = +2.75V \text{ (UART Mode), and } T_{A} = +25^{\circ}\text{C.)} \text{ (Note 1)}$

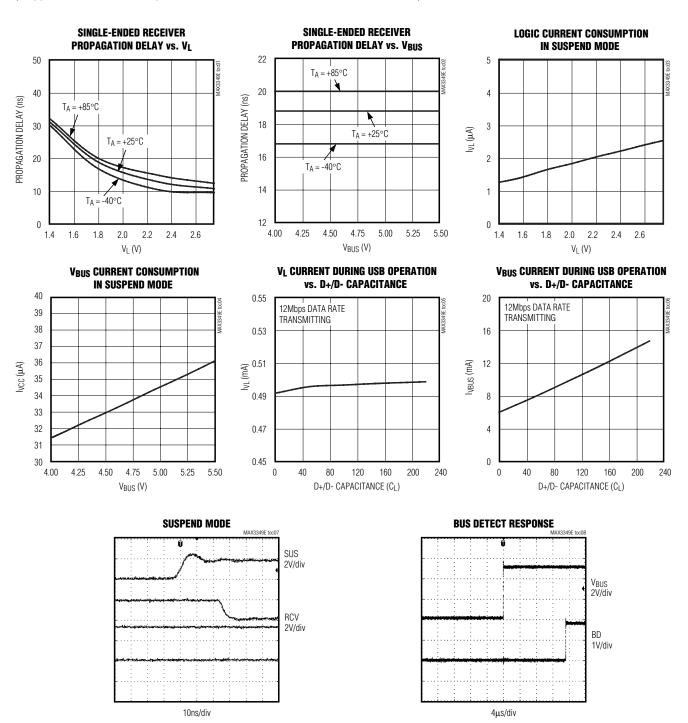
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS		
		High-to-off transition, V _L > +1.65V (Figure 5)			10			
Single-Ended Receiver Disable	tPHZ_SE	High-to-off transition, +1.4V < V _L < +1.65V (Figure 5)			12			
Delay	to. = o=	Low-to-off transition, V _L > +1.65V (Figure 5)			10	ns		
	^t PLZ_SE	Low-to-off transition, +1.4V < V _L < +1.65V (Figure 5)			12			
	t==== 05	Off-to-high transition, V _L > +1.65V (Figure 5)			20	ns		
Single-Ended Receiver Enable	tpzh_se	Off-to-high transition, +1.4V < V _L < +1.65 (Figure 5)			20			
Delay		Off-to-low transition, V _L > +1.65V (Figure 5)			20			
	^t PZL_SE	Off-to-low transition, +1.4V < V _L < +1.65V (Figure 5)			20			
UART DRIVER CHARACTERISTIC	CS (C _L = 200pF)						
Rise Time (D-)	tfr_tuart	10% to 90% of VOHD - VOLD (Figure 13)		60	200	ns		
Fall Time (D-)	tff_tuart	90% to 10% of VOHD - VOLD (Figure 13)		60	200	ns		
Driver Propagation Delay	tplh_tuart	(Figure 13)		70	200	no		
Driver i Topagation Delay	tphl_tuart	(Figure 13)	70 200		200	ns		
UART RECEIVER CHARACTERIS	UART RECEIVER CHARACTERISTICS (C _L = 15pF)							
Receiver (Rx) Propagation Delay	tplh_ruart	(Figure 14)	gure 14)		60	ns		
Thoseiver (Tix) Tropagation Delay	tphl_ruart	(Figure 14)			60	110		
Receiver (Rx) Rise/Fall Time	tfr_ruart	(Figure 14)			45	ns		
Thousand (Tix) Histori all Tille	tff_ruart	(Figure 14)			45	110		

Note 1: Parameters are 100% production tested at $T_A = +25$ °C, unless otherwise noted. Limits over temperature are guaranteed by design.

Note 2: Guaranteed by design, not production tested.

Typical Operating Characteristics

 $(V_{BUS} = +5V, V_{L} = +3.3V, V_{UART} = +2.75V, T_{A} = +25^{\circ}C, unless otherwise noted.)$



Pin Description

PIN UCSP TQFN		TVDE		FUNCTION			
		TYPE	NAME	FUNCTION			
A1	1	POWER	VUART	UART Supply Voltage. V_{UART} powers the internal UART transmitter and receiver. Connect a regulated voltage between +2.7V and +3.3V to V_{UART} . Bypass V_{UART} to GND with a 0.1 μ F ceramic capacitor.			
A2	2	OUTPUT	RX	UART Receive Output. In UART mode, RX is a level-shifted output that expresses the logic state of D+.			
А3	3	INPUT	TX	UART Transmit Input. In UART mode, D- follows the logic state on TX.			
A4	4	OUTPUT	BD	USB Detect Output. When V_{BUS} exceeds the V_{TH-BUS} threshold, BD is logic-high to indicate that the MAX3349E is connected to a USB host. The MAX3349E operates in USB mode when BD is logic-high, and operates in UART mode when BD is logic-low.			
B1	15	POWER	VL	Digital Logic Supply. Connect a +1.4V to +2.75V supply to V_L . Bypass V_L to GND with a $0.1\mu F$ or larger ceramic capacitor.			
B2	16	I/O	VM	Receiver Output/Driver Input. VM functions as a receiver output when $\overline{OE} = V_L$. VM follows the logic state of D- when receiving. VM functions as a driver input when $\overline{OE} = GND$ (Tables 2 and 3).			
В3	5	I/O	VP	Receiver Output/Driver Input. VP functions as a receiver output when $\overline{OE} = V_L$. VP follows the logic state of D+ when receiving. VP functions as a driver input when \overline{OE} = GND (Tables 2 and 3).			
B4	6	OUTPUT	RCV	Differential Receiver Output. In USB mode, RCV is the output of the USB differential receiver (Table 3).			
C1	14	POWER	VTRM	Internal Regulator Output. V_{TRM} provides a regulated +3.3V output. Bypass V_{TRM} to GND with a 1µF ceramic capacitor. V_{TRM} draws power from V_{BUS} . Do not power external circuitry from V_{TRM} .			
C2	13	INPUT	ENUM	Enumerate Input. Drive ENUM to V _L to connect the internal $1.5k\Omega$ resistor from D+ to V _{TRM} (when V _{BUS} is present). Drive ENUM to GND to disconnect the internal $1.5k\Omega$ pullup resistor. ENUM has no effect when the device is in UART mode.			
C3	8	INPUT	SUS	Suspend Input. Drive SUS low for normal operation. Drive SUS high to force the MAX3349E into suspend mode.			
C4	7	INPUT	ŌĒ	Output Enable. Drive \overline{OE} low to set VP/VM to transmitter inputs in USB mode. Drive \overline{OE} high to set VP/VM to receiver outputs in USB mode. \overline{OE} has no effect when the device is in UART mode.			
D1	12	POWER	V _{BUS}	USB Supply Voltage. V _{BUS} provides power to the internal linear regulator when in USB mode. Bypass V _{BUS} to GND with a 0.1µF ceramic capacitor.			
D2	11	I/O	D+	USB Differential Data Input/Output. Connect D+ directly to the USB connector.			
D3	10	I/O	D-	USB Differential Data Input/Output. Connect D- directly to the USB connector.			
D4	9	POWER	GND	Ground			
_	EP	_	EP	Exposed Paddle. Connect exposed paddle to GND.			



Timing Diagrams

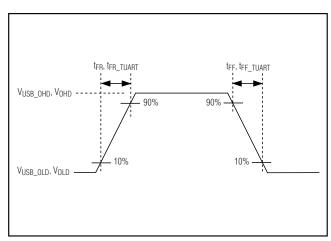


Figure 1. Rise and Fall Times

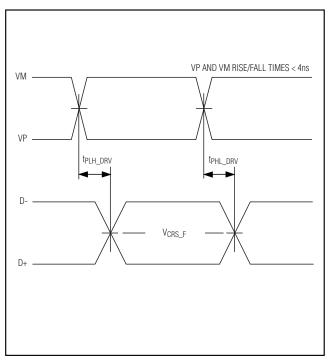


Figure 2. Timing of VP and VM to D+ and D-

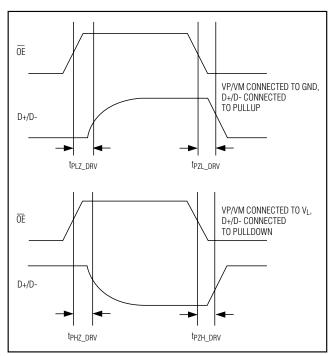


Figure 3. Driver Enable and Disable Timing

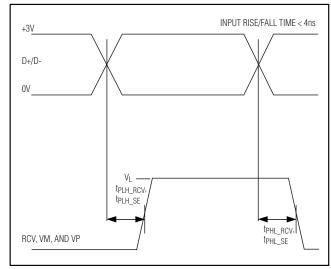


Figure 4. D+/D- Timing to VP, VM, and RCV

Timing Diagrams (continued)

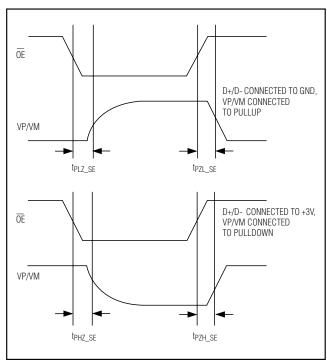


Figure 5. Receiver Enable and Disable Timing

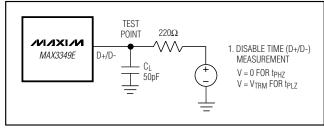


Figure 6. Test Circuit for Disable Time

Detailed Description

The MAX3349E \pm 15kV ESD-protected, USB transceiver provides a full-speed USB interface to a microprocessor or ASIC. The device supports enumeration, suspend, and V_{BUS} detection. A special UART multiplexing mode routes external UART signals (Rx and Tx) to D+ and D-, allowing the use of a shared connector to reduce cost and part count for mobile devices.

The UART interface allows mobile devices such as PDAs, cellular phones, and digital cameras to use either UART or USB signaling through the same connector. The MAX3349E features a separate UART voltage supply input. The

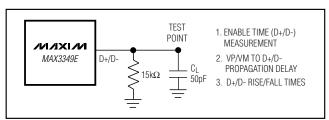


Figure 7. Test Circuit for Enable Time, Transmitter Propagation Delay, and Transmitter Rise/Fall Time

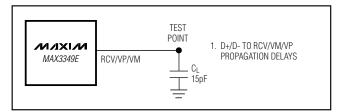


Figure 8. Test Circuit for Receiver Propagation Delay

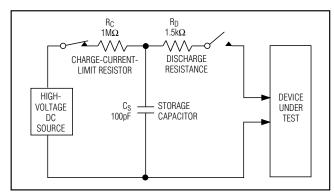


Figure 9. Human Body ESD Test Model

MAX3349E supports a maximum UART baud rate of 921kbaud.

Upon connection to a USB host, the MAX3349E enters USB mode and provides a full-speed USB 2.0 compliant interface through VP, VM, RCV, and $\overline{\text{OE}}.$ The MAX3349E features internal series resistors on D+ and D-, and an internal 1.5k Ω pullup resistor to D+ to allow the device to logically connect and disconnect from the USB bus while plugged in. A suspend mode is provided for low-power operation. D+ and D- are protected from electrostatic discharge (ESD) up to $\pm 15 \text{kV}$. To ensure full $\pm 15 \text{kV}$ ESD protection, bypass VBUS to GND

Timing Diagrams (continued)

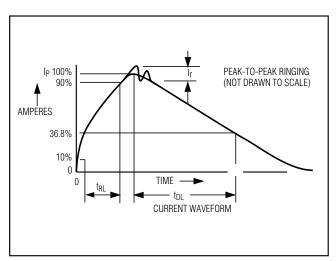


Figure 10. Human Body Model Current Waveform

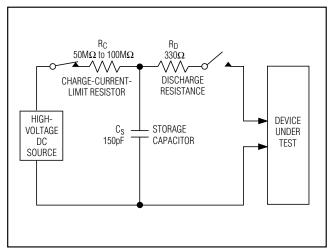


Figure 11. IEC61000-4-2 ESD Contact Discharge Test Model

with a $0.1\mu F$ ceramic capacitor as close to the device as possible.

Operating Modes

The MAX3349E operates in either USB mode or UART mode, depending on the presence or absence of VBUS. Bus detect output BD is logic-high when a voltage higher than $V_{TH-VBUS}$ is applied to V_{BUS} , and logic-low otherwise. The MAX3349E operates in USB

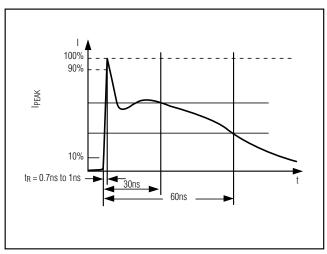


Figure 12. IEC 61000-4-2 Contact Discharge Model Current Waveform

mode when BD is logic-high, and UART mode when BD is logic-low.

USB Mode

In USB mode, the MAX3349E implements a full-speed (12Mbps) USB interface on D+ and D-, with enumerate and suspend functions. A differential USB receiver presents the USB state as a logic-level output RCV (Table 3a). VP/VM are outputs of single-ended USB receivers when $\overline{\text{OE}}$ is logic-high, allowing detection of single-ended 0 (SE0) events. When $\overline{\text{OE}}$ is logic-low, VP and VM serve as inputs to the USB transmitter. Drive suspend input SUS logic-high to force the MAX3349E into a low-power operating mode and disable the differential USB receiver (Table 3b).

UART Mode

The MAX3349E operates in UART mode when BD is logic-low (V_{BUS} not present). The Rx signal is the output of a single-ended receiver on D+, and the Tx input is driven out on D-. Signaling voltage thresholds for D+ and D- are determined by V_{UART} , an externally applied voltage between +2.7V and +3.3V.

Power-Supply Configurations

V_L Logic Supply

In both USB and UART modes, the control interface is powered from V_L. The MAX3349E operates with logic-side voltage (V_L) as low as +1.4V, providing level shifting for lower voltage ASICs and microcontrollers.

Table 1. Power-Supply Configuration

V _{BUS} (V)	V _{TRM} (V)	V _L (V)	V _{UART} (V)	CONFIGURATION
+4.0 to +5.5	+3.0 to +3.6 Output	+1.4 to +2.75	GND, Unconnected, or +2.7V to +3.3V	USB Mode
+4.0 to +5.5	+3.0 to +3.6 Output	GND or Unconnected	GND, Unconnected, or +2.7V to +3.3V	Disable Mode
GND or Unconnected	High Impedance	+1.4 to +2.75	+2.7V to +3.3V	UART Mode

Table 2. USB Transmit Truth Table $(\overline{OE} = 0)$

INPUTS			OUTPUTS
VP VM		D+	D-
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Table 3a. USB Receive Truth Table ($\overline{OE} = 1$, SUS = 0)

INP	UTS	OUTPUTS			
D+ D-		VP	VM	RCV	
0	0	0	0	RCV*	
0	1	0	1	0	
1	0	1	0	1	
1	1	1	1	Х	

^{* =} Last State

X = Undefined

USB Mode

The MAX3349E is in USB mode when V_{BUS} is greater than V_{TH-BUS} and the bus detect output (BD) is logichigh. In USB mode, power for the MAX3349E is derived from V_{BUS}, typically provided through the USB connector. An internal linear regulator generates the required +3.3V V_{TRM} voltage from V_{BUS}. V_{TRM} powers the internal USB transceiver circuitry and the D+ enumeration resistor. Bypass V_{TRM} to GND with a 1µF ceramic capacitor as close to the device as possible. Do not power external circuitry from V_{TRM}.

Disable Mode

Connect V_{BUS} to a system power supply and leave V_L unconnected or connect to ground to enter disable mode. In disable mode, D+ and D- are high impedance, and withstand external signals up to +5.5V. \overline{OE} , SUS, and control signals are ignored.

Table 3b. USB Receive Truth Table ($\overline{OE} = 1$, SUS = 1)

INP	UTS	OUTPUTS									
D+	D-	VP	VM	RCV							
0	0	0	0	0							
0	1	0	1	0							
1	0	1	0	0							
1	1	1	1	0							

UART Mode

Connect V_L and V_{UART} to system power supplies, and leave V_{BUS} unconnected or below V_{TH-BUS} to operate the MAX3349E in UART mode. The MAX3349E supports V_{UART} from +2.7V to +3.3V (see Table 1).

USB Control Signals

OE

OE controls the direction of communication for USB mode. When OE is logic-low, VP and VM operate as logic inputs, and D+/D- are outputs. When OE is logic-high, VP and VM operate as logic outputs, and D+/D- are inputs. RCV is the output of the differential USB receiver connected to D+/D-, and is not affected by the OE logic level.

ENUM

Drive ENUM logic-high to enable the internal 1.5k Ω pullup resistor from D+ to V_{TRM}. Drive ENUM logic-low to disable the internal pullup resistor and logically disconnect the MAX3349E from the USB.

SUS

Operate the MAX3349E in low-power USB suspend mode by driving SUS logic-high. In suspend mode, the USB differential receiver is turned off and V_{BUS} consumes 38µA (typ) of supply current. The single-ended VP and VM receivers remain active to detect a SE0 state on USB bus lines D+ and D-. The USB transmitter



remains enabled in suspend mode to allow transmission of a remote wake-up on D+ and D-.

D+ and D-

D+ and D- are either USB signals or UART signals, depending on the operating mode. In USB mode, D+/D- serve as receiver inputs when $\overline{\text{OE}}$ is logic-high and transmitter outputs when $\overline{\text{OE}}$ is logic-low. Internal series resistors are provided on D+ and D- to allow a direct interface with a USB connector. In UART mode, D+ is an input and D- is an output. UART signals on Tx are presented on D-, and signals on D+ are presented on Rx. The UART signaling levels for D+/D- are determined by VUART. Logic thresholds for Rx and Tx are determined by VL. D+ and D- are ESD protected to $\pm 15 \text{kV}$ HBM.

RCV

RCV is the output of the differential USB receiver. RCV is a logic 1 for D+ high and D- low. RCV is a logic 0 for D+ low and D- high. RCV retains the last valid logic state when D+ and D- are both low (SE0). RCV is driven logic-low when SUS is high. See Tables 3a and 3b.

BD

The bus-detect (BD) output is asserted logic-high when a voltage greater than V_{TH-BUS} is presented on V_{BUS}. This is typically the case when the MAX3349E is connected to a powered USB. BD is logic-low when V_{BUS} is unconnected.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. Additional ESD-protection structures guard D+ and D- against damage from ESD events up to ±15kV. The ESD structures arrest ESD events in all operating modes: normal operation, suspend mode, and when the device is unpowered.

Several ESD testing standards exist for gauging the robustness of ESD structures. The ESD protection of the MAX3349E is characterized to the following standards:

- ±15kV Human Body Model (HBM)
- ±8kV Air-Gap Discharge per IEC 61000-4-2
- ±8kV Contact Discharge per IEC 61000-4-2

Human Body Model

Figure 9 shows the model used to simulate an ESD event resulting from contact with the human body. The model consists of a 100pF storage capacitor that is charged to a high voltage, then discharged through a $1.5 \mathrm{k}\Omega$ resistor. Figure 10 shows the current waveform

when the storage capacitor is discharged into a low impedance.

IEC 61000-4-2 Contact Discharge

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2 due to lower series resistance. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is typically lower than that measured using the Human Body Model. Figure 11 shows the IEC 61000-4-2 model. The Contact Discharge method connects the probe to the device before the probe is charged. Figure 12 shows the current waveform for the IEC 61000-4-2 Contact Discharge Model.

ESD Test Conditions

ESD performance depends on a variety of conditions. Please contact Maxim for a reliability report documenting test setup, methodology, and results.

_Applications Information

Data Transfer in USB Mode

Transmitting Data to the USB

To transmit data to the USB, operate the MAX3349E in USB mode (see the *Operating Modes* section), and drive $\overline{\text{OE}}$ low. The MAX3349E transmits data to the USB differentially on D+ and D-. VP and VM serve as differential input signals to the driver. When VP and VM are both driven low, a single-ended zero (SE0) is output on D+/D-.

Receiving Data from the USB

To receive data from the USB, operate the MAX3349E in USB mode (see the *Operating Modes* section.) Drive $\overline{\text{OE}}$ high and SUS low. Differential data received at D+/D- appears as a logic signal at RCV. VP and VM are the outputs of single-ended receivers on D+ and D-.

Data Transfer in UART Mode

In UART mode, D+ is an input and D- is an output. UART signals on Tx are presented on D-, and signals on D+ are presented on Rx. The UART signaling levels for D+/D- are determined by VUART. The voltage thresholds for Rx and Tx are determined by VL. The voltage thresholds for D+ and D- are determined by VUART.

Power-Supply Decoupling

Bypass VBUS, VL, and VUART to ground with 0.1 μF ceramic capacitors. Additionally, bypass VTRM to

_Timing Diagrams

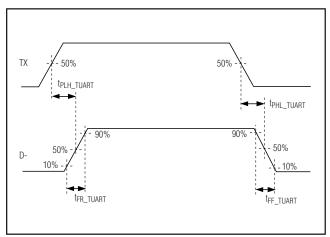


Figure 13. UART Transmitter Timing

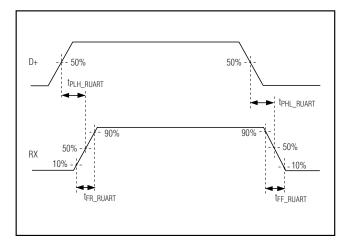


Figure 14. UART Receiver Timing

ground with a $1\mu F$ ceramic capacitor. Place all bypass capacitors as close as possible to the device .

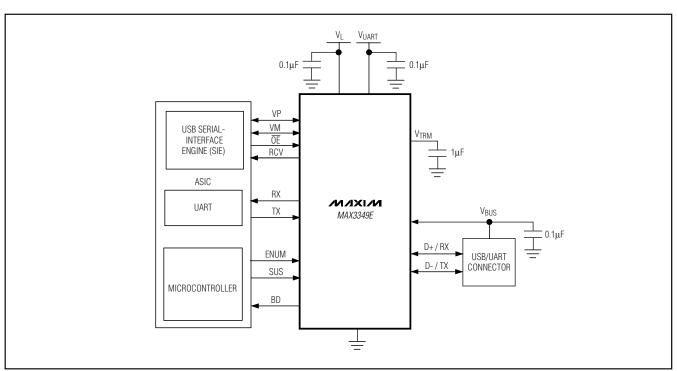
Power Sequencing

There are no power-sequencing requirements for V_{L} , V_{UART} , and V_{BUS} .

UCSP Application Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit-board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note *UCSP- A Wafer-Level Chip-Scale Package* available on Maxim's website at www.maxim-ic.com/ucsp.

Typical Operating Circuit



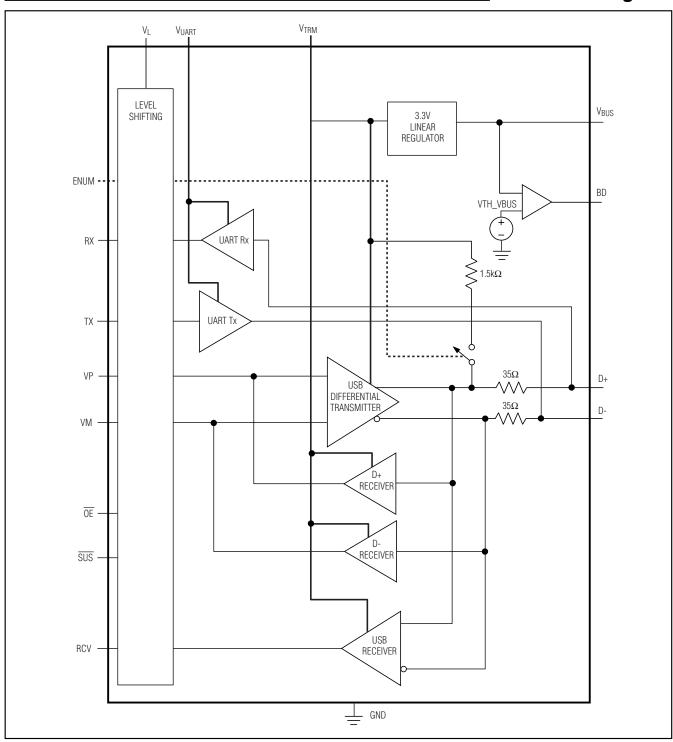
Chip Information

PROCESS: BICMOS

EXPOSED PADDLE: Connect to ground or leave unconnected.

WIXKN _____

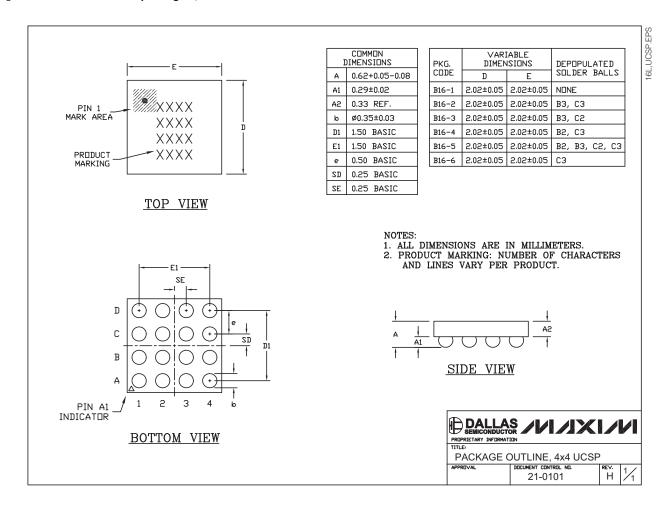
Functional Diagram



MIXIM

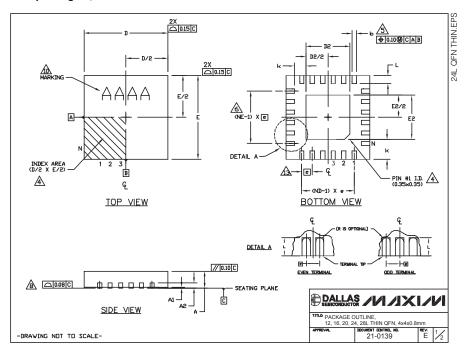
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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