

DS3650 Quad Differential Line Receivers

General Description

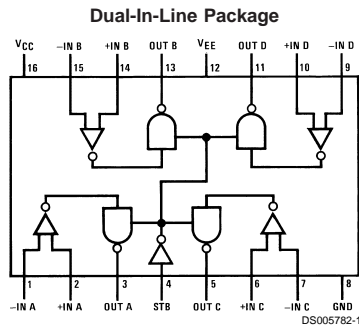
The DS3650 is TTL compatible quad high speed circuits intended primarily for line receiver applications. Switching speeds have been enhanced over conventional line receivers by the use of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bussed organizations.

The DS3650 has active pull-up outputs and offers a TRI-STATE strobe.

Features

- High speed
- TTL compatible
- Input sensitivity: ± 25 mV
- TRI-STATE outputs for high speed busses
- Standard supply voltages: ± 5 V
- Pin and function compatible with MC3450

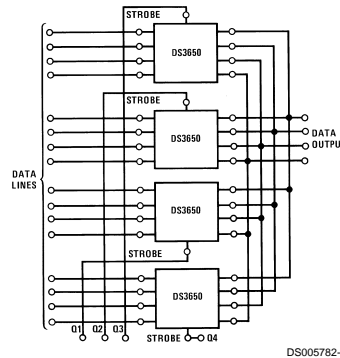
Connection Diagram



Top View

Order Number DS3650M or DS3650N
See NS Package Number M16A or N16A
For Complete Military 883 Specifications,
see RETS Data Sheet.

Wired "OR" Data Selecting Using TRI-STATE Logic



Input	Strobe	Output
		DS3650
$V_D \geq 25$ mV	L	H
	H	Open
-25 mV $\leq V_{ID} \leq 25$ mV	L	X
	H	Open
$V_{ID} \leq -25$ mV	L	L
	H	Open

L = Low Logic State Open = TRI-STATE
H = High Logic State X = Indeterminate State

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltages	
V_{CC}	+7.0 V_{DC}
V_{EE}	-7.0 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	$\pm 6.0 V_{DC}$
Common-Mode Input Voltage Range, V_{ICR}	$\pm 5.0 V_{DC}$
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation (Note 1) at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW

SO Package

1051 mW

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V_{DC}
Supply Voltage, V_{EE}	-4.75	-5.25	V_{DC}
Operating Temperature, T_A	0	+70	°C
Output Load Current, I_{OL}		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	-5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	-3.0	+3.0	V_{DC}
Input Voltage Range Input to GND, V_{IR}	-5.0	+3.0	V_{DC}

Note 1: Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.8 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Electrical Characteristics (Notes 3, 4)

($V_{CC} = 5.0 V_{DC}$, $V_{EE} = -5.0 V_{DC}$, $\text{Min} \leq T_A \leq \text{Max}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
V_{IS}	Input Sensitivity, (Note 6) (Common-Mode Voltage Range = $-3V \leq V_{IN} \leq 3V$)	$\text{Min} \leq V_{CC} \leq \text{Max}$ $\text{Min} \geq V_{EE} \geq \text{Max}$			± 25.0	mV	
$I_{IH(I)}$	High Level Input Current to Receiver Input	(Figure 5)			75	μA	
$I_{IL(I)}$	Low Level Input Current to Receiver Input	(Figure 6)			-10	μA	
$I_{IH(S)}$	High Level Input Current to Strobe Input	(Figure 3)			$V_{IH(S)} = 2.4V$	40	μA
					$V_{IH(S)} = V_{CC}$	1	mA
$I_{IL(S)}$	Low Level Input Current to Strobe Input				-1.6	mA	
V_{OH}	High Level Output Voltage	(Figure 1)	2.4			V	
V_{OL}	Low Level Output Voltage	(Figure 1)			0.45	V	
I_{OS}	Short-Circuit Output Current (Note 5)	(Figure 4)	-18		-70	mA	
I_{OFF}	Output Disable Leakage Current	(Figure 7)			40	μA	
I_{CCH}	High Logic Level Supply Current from V_{CC}	(Figure 2)		45	60	mA	
I_{EEH}	High Logic Level Supply Current from V_{EE}	(Figure 2)		-17	-30	mA	

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 3: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS3650. All typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 5V$ and $V_{EE} = -5V$.

Note 4: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 5: Only one output at a time should be shorted.

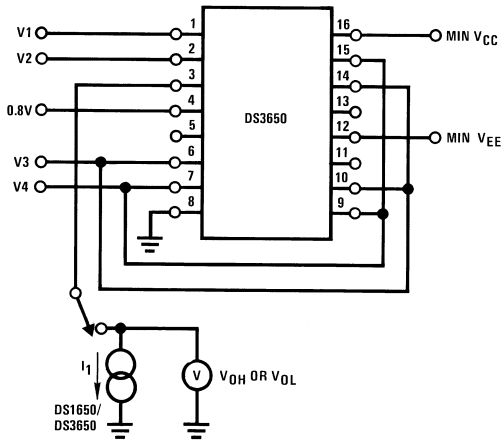
Note 6: A parameter which is of primary concern when designing with line receivers is, what is the minimum differential input voltage required as the receiver input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS3650 is specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200 Ω at each input.

Switching Characteristics

($V_{CC} = 5 V_{DC}$, $V_{EE} = -5 V_{DC}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	(Figure 8)		21	25	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)			20	25	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	(Figure 9)		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)			7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)			19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)			14	29	ns

Electrical Characteristic Test Circuits



	V1	V2	V3	V4	I ₁
V _{OH}	+2.975V -3.0V	+3.0V -2.975V	+3.0V GND	GND -3.0V	-0.4 mA -0.4 mA
V _{OL}	+3.0V -2.975V	+2.975V -3.0V	GND -3.0V	+3.0V GND	+16 mA +16 mA

Channel A shown under test. Other channels are tested similarly.

FIGURE 1. V_{OH} and V_{OL}

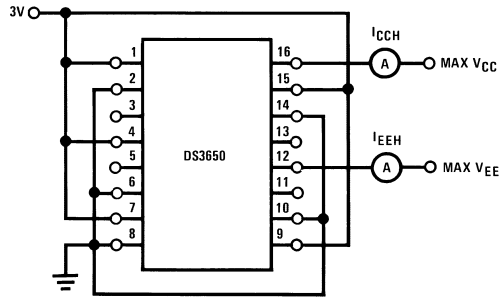


FIGURE 2. I_{CCH} and I_{EEH}

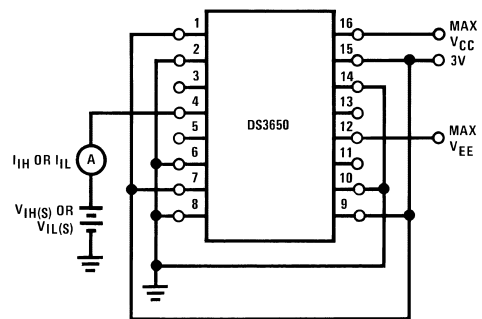
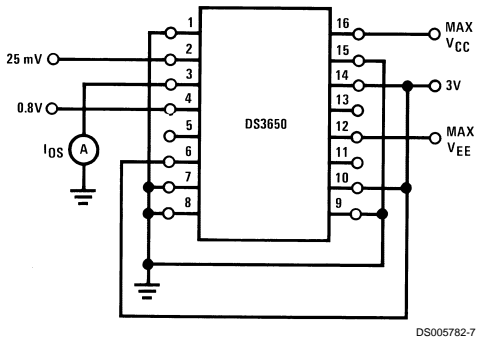


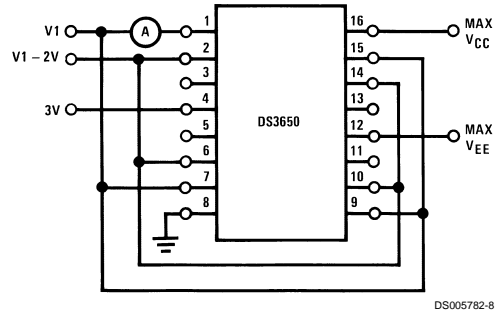
FIGURE 3. I_{IH(S)} and I_{IL(S)}

(Continued)



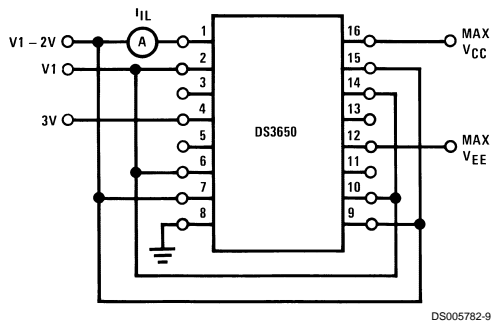
Note: Channel A shown under test, other channels are tested similarly. Only one output shorted at a time.

FIGURE 4. I_{OS}



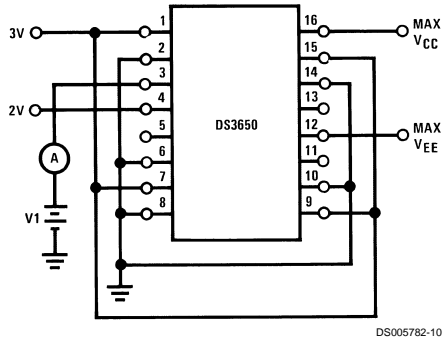
Note: Channel A(-) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to -3V.

FIGURE 5. I_{IH}



Note: Channel A(-) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to -3V.

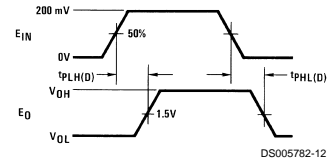
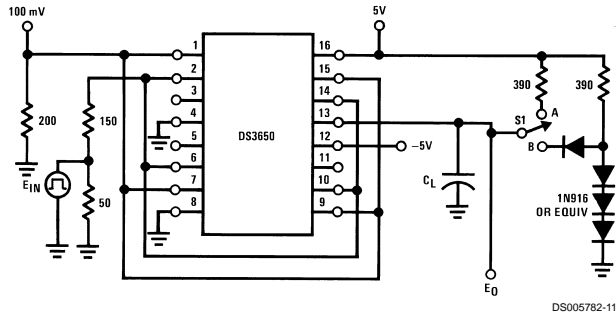
FIGURE 6. I_{IL}



Note: Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4V and 2.4V.

FIGURE 7. I_{OFF}

AC Test Circuits and Switching Time Waveforms

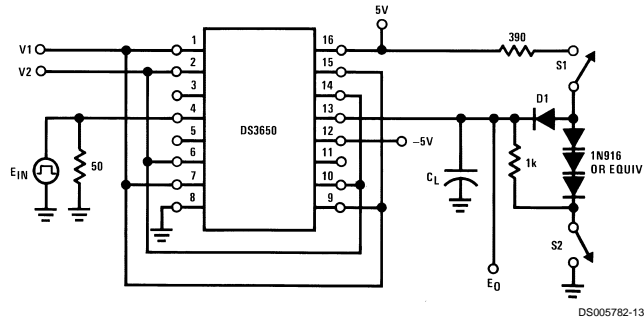


Note. E_{IN} waveform characteristics:
 t_{TLH} and $t_{THL} \leq 10$ ns measured
 10% to 90%
 PRR = 1 MHz
 Duty Cycle = 50%

Note. Output of Channel B shown under test, other channels are tested similarly.
 S1 at "B" for DS1650/DS3650
 $C_L = 50$ pF total for DS3650

FIGURE 8. Receiver Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$

(Continued)



DS005782-13

Note. Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C _L
t _{PLO(S)}	100 mV	GND	Closed	Closed	15 pF
t _{POL(S)}	100 mV	GND	Closed	Open	50 pF
t _{PHO(S)}	GND	100 mV	Closed	Closed	15 pF
t _{POH(S)}	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.

E_{IN} waveform characteristics: t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%

PRR = 1 MHz

Duty Cycle = 50%

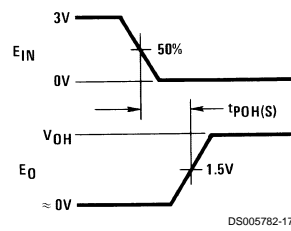
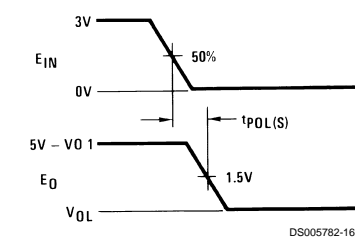
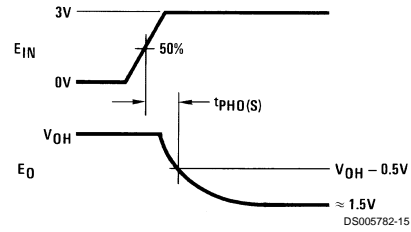
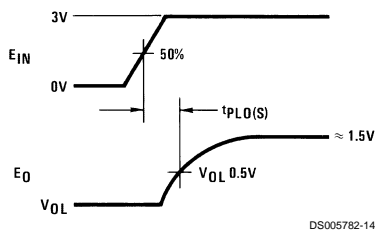
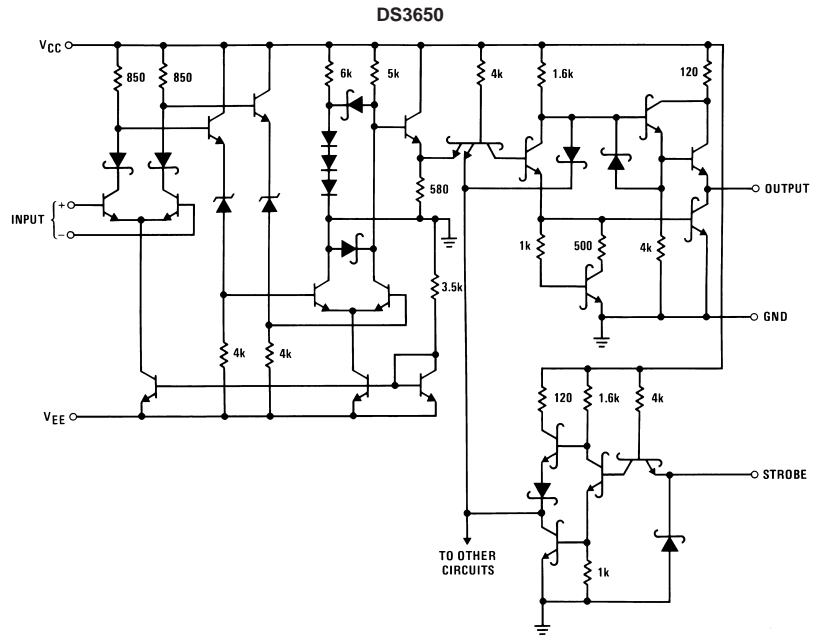


FIGURE 9. Strobe Propagation Delay t_{PLO(S)}, t_{POL(S)}, t_{PHO(S)} and t_{POH(S)}

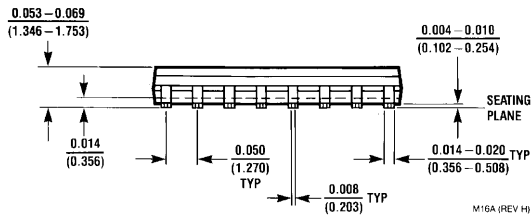
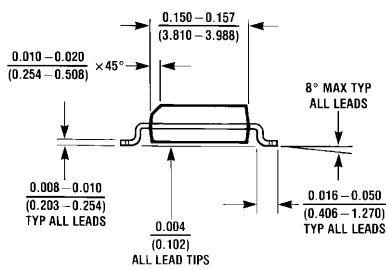
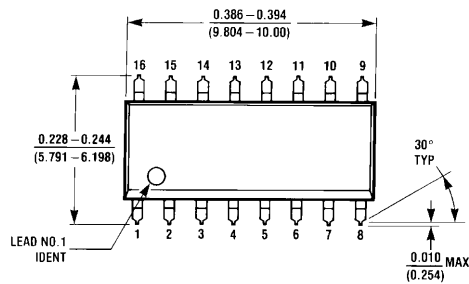
Schematic Diagrams



1/4 of circuit shown

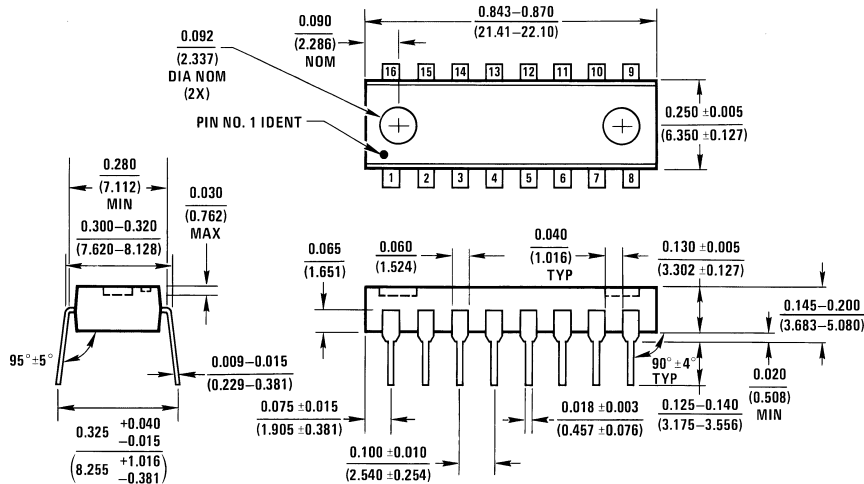
DS005782-20

Physical Dimensions inches (millimeters) unless otherwise noted



M16A (REV H)

SO Package (M)
Order Number DS3650M
NS Package Number M16A



N16A (REV E)

Molded Dual-In-Line Package (N)
Order Number DS3650N
NS Package Number N16A

Notes

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