DSL Line Driver with Power-Down

AD8019

FEATURES

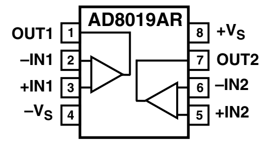
- Low Distortion, High Output Current Amplifiers
  - Operate from 12 V to ±12 V Power Supplies, Ideal for High-Performance ADSL CPE, and xDSL Modems
- Low Power Operation
  - 9 mA/Amp (Typ) Supply Current
  - Digital (1-Bit) Power-Down
- Voltage Feedback Amplifiers
- Low Distortion
  - Out-of-Band SFDR –80 dBc @ 100 kHz into 100 Ω Line
- High Speed
  - 175 MHz Bandwidth (–3 dB), G = +1
  - 400 V/μs Slew Rate
- High Dynamic Range
- V_{OUT} to within 1.2 V of Power Supply

APPLICATIONS

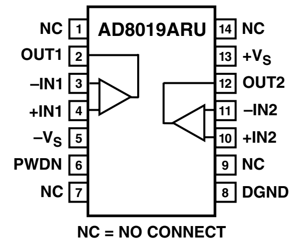
ADSL, VDSL, HDSL, and Proprietary xDSL USB, PCI, PCMCIA Modems, and Customer Premise Equipment (CPE)

PIN CONFIGURATIONS

8-Lead SOIC
(R-8)



14-Lead TSSOP
(RU-14)



PRODUCT DESCRIPTION

The AD8019 is a low cost xDSL line driver optimized to drive a minimum of 13 dBm into a 100 Ω load while delivering outstanding distortion performance. The AD8019 is designed on a 24 V high-speed bipolar process enabling the use of ±12 V power supplies or 12 V only. When operating from a single 12 V supply the highly efficient amplifier architecture can typically deliver 170 mA output current into low impedance loads through a 1:2 turns ratio transformer. Hybrid designs using ±12 V supplies enable the use of a 1:1 turns ratio transformer, minimizing attenuation of the receive signal. The AD8019 typically draws 9 mA/amplifier quiescent current. A 1-bit digital power down feature reduces the quiescent current to approximately 1.6 mA/amplifier.

Figure 1 shows typical Out of Band SFDR performance under ADSL CPE (upstream) conditions. SFDR is measured while driving a 13 dBm ADSL DMT signal into a 100 Ω line with 50 Ω back termination.

The AD8019 comes in thermally enhanced 8-lead SOIC and 14-lead TSSOP packages. The 8-lead SOIC is pin-compatible with the AD8017 12 V line driver.

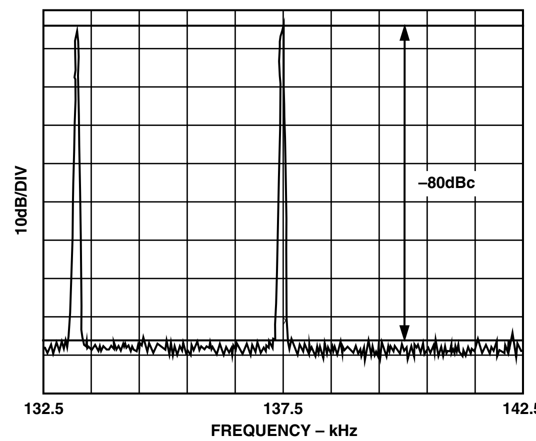


Figure 1. Out-of-Band SFDR; V_S = ±12 V; 13 dBm Output Power into 200 Ω, Upstream

REV. 0

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AD8019–SPECIFICATIONS (@ 25°C, V_S = 12 V, R_L = 25 Ω, R_F = 500 Ω, T_{MIN} = –40°C, T_{MAX} = +85°C, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +5		35		MHz
	G = +1, V_{OUT} < 0.4 V p-p, R_L = 100 Ω	175	180		MHz
	G = +2, V_{OUT} < 0.4 V p-p, R_L = 100 Ω	70	75		MHz
0.1 dB Bandwidth	V_{OUT} < 0.4 V p-p, R_L = 100 Ω		6		MHz
	G = +5, V_{OUT} < 0.4 V p-p, R_L = 100 Ω		35		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p		50		MHz
Slew Rate	Noninverting, V_{OUT} = 4 V p-p		450		V/µs
Rise and Fall Time	Noninverting, V_{OUT} = 2 V p-p		5.5		ns
Settling Time	0.1%, V_{OUT} = 2 V p-p		40		ns
NOISE/DISTORTION PERFORMANCE					
Distortion	V_{OUT} = 3 V p-p (Differential)				
Second Harmonic	100 kHz, $R_{L(DM)}$ = 50 Ω		–78		dBc
	500 kHz, $R_{L(DM)}$ = 50 Ω		–74		dBc
Third Harmonic	100 kHz, $R_{L(DM)}$ = 50 Ω		–85		dBc
	500 kHz, $R_{L(DM)}$ = 50 Ω		–80		dBc
Out-of-Band SFDR	144 kHz–1.1 MHz, Differential R_L = 70 Ω		–80		dBc
MTPR	25 kHz–138 kHz, Differential R_L = 70 Ω		–72		dBc
Input Voltage Noise	f = 100 kHz		8		nV/√Hz
Input Current Noise	f = 100 kHz		0.9		pA√Hz
Crosstalk	f = 1 MHz, G = +2		–80		dB
DC PERFORMANCE					
Input Offset Voltage			8	20	mV
	T_{MIN}–T_{MAX}		10	23	mV
Input Offset Voltage Match			1	12	mV
	T_{MIN}–T_{MAX}		2	17	mV
Open-Loop Gain	V_{OUT} = 6 V p-p, R_L = 25 Ω	72	80		dB
	T_{MIN}–T_{MAX}	72	80		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance			0.5		pF
+Input Bias Current		–3	+1	+3	µA
	T_{MIN}–T_{MAX}	–4		+4	µA
–Input Bias Current		–1.5	–0.5	+1.5	µA
	T_{MIN}–T_{MAX}	–1.8		+1.8	µA
+Input Bias Current Match		–1.0	–0.2	+1.0	µA
	T_{MIN}–T_{MAX}	–1.5		+1.5	µA
–Input Bias Current Match		–0.5	+0.1	+0.5	µA
	T_{MIN}–T_{MAX}	–0.8		+0.8	µA
CMRR	ΔV_{CM} = –4 V to +4 V	71	74		dB
Input CM Voltage Range		2		10	V
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
Output Voltage Swing	R_L = 25 Ω	–4.8		+4.8	V
Output Current	SFDR –80 dBc into 25 Ω at 100 kHz	175	200		mA
Short Circuit Current[1]			400		mA
POWER SUPPLY					
Supply Current/Amp	PWDN = 5 V		9	10.5	mA
	T_{MIN}–T_{MAX}			14.5	mA
	PWDN = 0 V		0.8	2.0	mA
Operating Range	Dual Supply	±4.0		±6.0	V
Power Supply Rejection Ratio	$\Delta\pm V_S$ = +1.0 V to –1.0 V	65	68		dB
LOGIC LEVELS	V_{PWDN} = 0 V to 3 V; V_{IN} = 10 MHz, G = +5				
t_{ON}			120		ns
t_{OFF}			80		ns
PWDN = "1" Voltage		1.8		$+V_S$	V
PWDN = "0" Voltage				0.5	V
PWDN = "1" Bias Current			220		µA
PWDN = "0" Bias Current			–100		µA

NOTES
[1]This device is protected from overheating during a short-circuit by a thermal shutdown circuit.
Specifications subject to change without notice.

(@ 25°C, V_S = ±12 V, R_L = 100 Ω, R_F = 500 Ω, T_{MIN} = –40°C, T_{MAX} = +85°C, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +5		35		MHz
	G = +1, V_{OUT} < 0.4 V p-p	175	180		MHz
	G = +2, V_{OUT} < 0.4 V p-p	70	75		MHz
0.1 dB Bandwidth	V_{OUT} < 0.4 V p-p		5.5		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p		50		MHz
Slew Rate	Noninverting, V_{OUT} = 4 V p-p		400		V/μs
Rise and Fall Time	Noninverting, V_{OUT} = 2 V p-p		5.5		ns
Settling Time	0.1%, V_{OUT} = 2 V p-p		40		ns
NOISE/DISTORTION PERFORMANCE					
Distortion	V_{OUT} = 16 V p-p (Differential)				
Second Harmonic	100 kHz, $R_{L(DM)}$ = 200 Ω		–80		dBc
	500 kHz, $R_{L(DM)}$ = 200 Ω		–72		dBc
Third Harmonic	100 kHz, $R_{L(DM)}$ = 200 Ω		–85		dBc
	500 kHz, $R_{L(DM)}$ = 200 Ω		–80		dBc
Out-of-Band SFDR	144 kHz–500 kHz, Differential R_L = 200 Ω		–80		dBc
MTPR	25 kHz–138 kHz, Differential R_L = 200 Ω		–73		dBc
Input Voltage Noise	f = 100 kHz		8		nV/$\sqrt{Hz}$
Input Current Noise	f = 100 kHz		0.9		pA$\sqrt{Hz}$
Crosstalk	f = 1 MHz, G = +2		–85		dB
DC PERFORMANCE					
Input Offset Voltage			5	20	mV
	T_{MIN}–T_{MAX}		10		mV
Input Offset Voltage Match			1	12	mV
	T_{MIN}–T_{MAX}		2	18	mV
Open-Loop Gain	V_{OUT} = 18 V p-p, R_L = 100 Ω	86	92		dB
	T_{MIN}–T_{MAX}		90		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance			0.5		pF
+Input Bias Current		–3	–0.5	+3	μA
	T_{MIN}–T_{MAX}	–3.8		+3.8	μA
–Input Bias Current		–1.5	–0.2	+1.5	μA
	T_{MIN}–T_{MAX}	–1.7		+1.7	μA
+Input Bias Current Match		–1.0	+0.2	+1.0	μA
	T_{MIN}–T_{MAX}	–2.4		+2.4	μA
–Input Bias Current Match		–1.0	+0.1	+1.0	μA
	T_{MIN}–T_{MAX}	–2.5		+2.5	μA
CMRR	ΔV_{CM} = –10 V to +10 V	71	76		dB
Input CM Voltage Range		–10		+10	V
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
Output Voltage Swing	R_L = 100 Ω	–10.8		+10.8	V
Output Current	SFDR –80 dBc into 100 Ω at 100 kHz	125	170		mA
Short Circuit Current[1]			800		mA
POWER SUPPLY					
Supply Current/Amp	PWDN = High		9	10	mA
	T_{MIN}–T_{MAX}			11.5	mA
	PWDN = Low		0.8	1.75	mA
Operating Range	Dual Supply	±4.0		±12	V
Power Supply Rejection Ratio	$\Delta \pm V_S$ = +1.0 V to –1.0 V	61	64		dB
LOGIC LEVELS	V_{PWDN} = 0 V to 3 V; V_{IN} = 10 MHz, G = +5				
t_{ON}			120		ns
t_{OFF}			80		ns
PWDN = "1" Voltage		1.8		$+V_S$	V
PWDN = "0" Voltage				0.5	V
PWDN = "1" Bias Current			220		μA
PWDN = "0" Bias Current			–100		μA

NOTES

[1]This device is protected from overheating during a short-circuit by a thermal shutdown circuit.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . 26.4 V
Internal Power Dissipation
  TSSOP-14 Package[2] . . . . 2.2 W
  SOIC-8 Package[3] . . . . 1.4 W
Input Voltage (Common-Mode) . . . . $\pm V_S$
Differential Input Voltage . . . . $\pm V_S$
Output Short Circuit Duration
  . . . . Observe Power Derating Curves
Storage Temperature Range . . . . –65°C to +125°C
Operating Temperature Range . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device on a four-layer board with 10 inches^2 of 1 oz. copper at 85°C 14-lead TSSOP package: θ_{JA} = 90°C/W.
[3]Specification is for device on a four-layer board with 10 inches^2 of 1 oz. copper at 85°C 8-lead SOIC package: θ_{JA} = 100°C/W.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8019 is limited by the associated rise in junction temperature. The maximum safe junction temperature for a plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package.

The output stage of the AD8019 is designed for maximum load current capability. As a result, shorting the output to common can cause the AD8019 to source or sink 500 mA. To ensure proper operation, it is necessary to observe the maximum power derating curves. Direct connection of the output to either power supply rail can destroy the device.

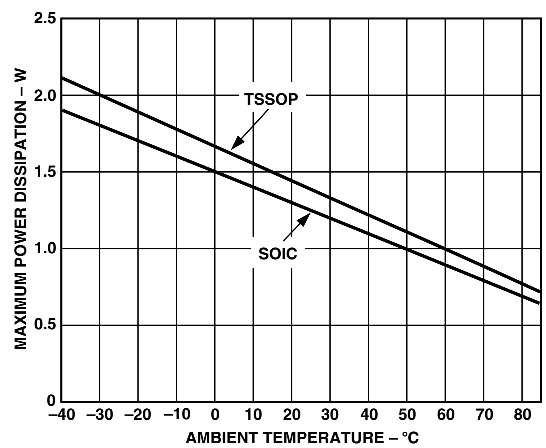


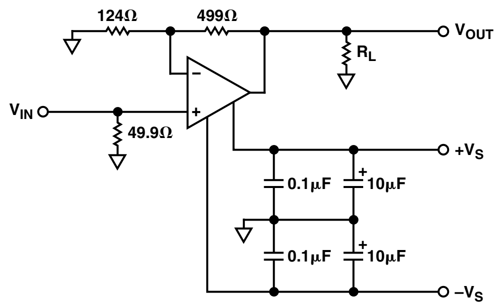
Figure 2. Plot of Maximum Power Dissipation vs. Temperature for AD8019 for T_J = 150°C

ORDERING GUIDE

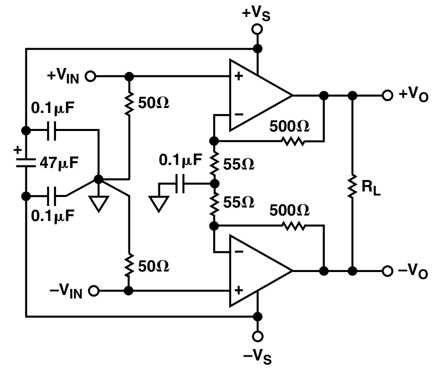
Model	Temperature Range	Package Description	Package Option
AD8019ARU	–40°C to +85°C	14-Lead TSSOP	RU-14
AD8019ARU-Reel	–40°C to +85°C	14-Lead TSSOP	RU-14 Reel
AD8019ARU-EVAL	–40°C to +85°C	Evaluation Board	ARU-EVAL
AD8019AR	–40°C to +85°C	8-Lead SOIC	R-8
AD8019AR-Reel	–40°C to +85°C	8-Lead SOIC	R-8 Reel
AD8019AR-EVAL	–40°C to +85°C	Evaluation Board	AR EVAL

CAUTION

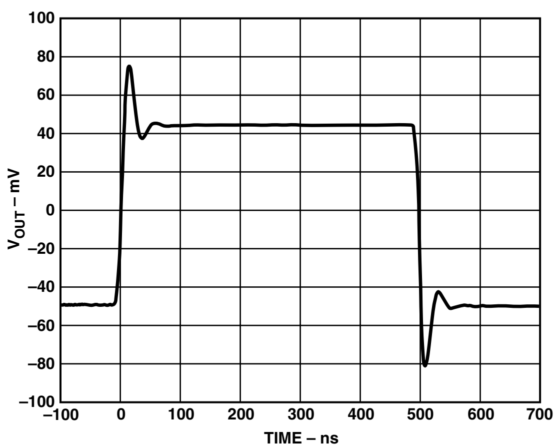
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8019 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



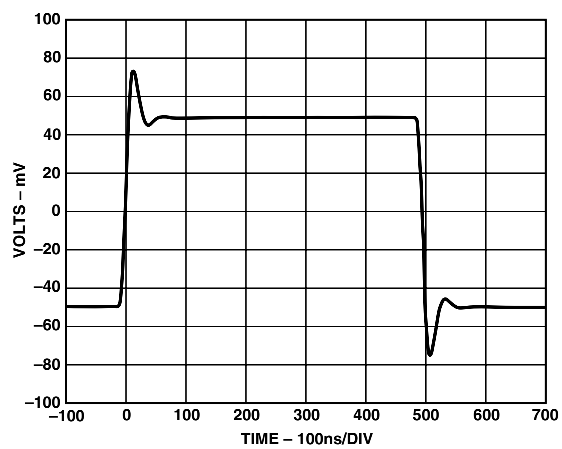
TPC 1. *Single-Ended Test Circuit; G = +5*



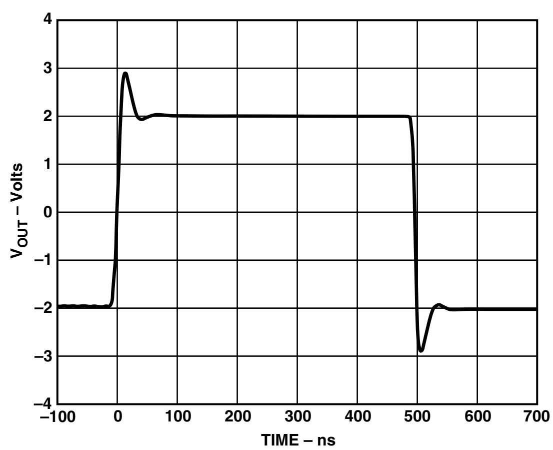
TPC 4. *Differential Test Circuit; G = +10*



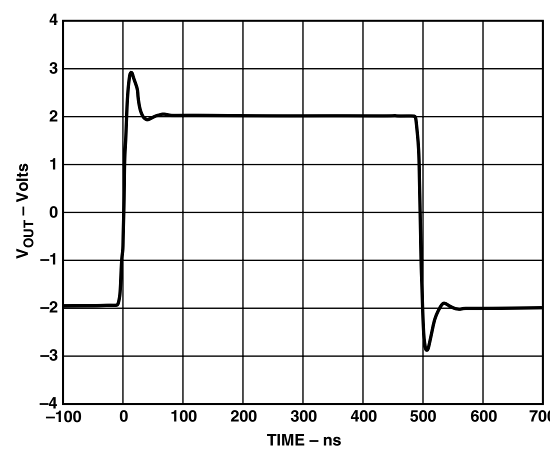
TPC 2. *100 mV Step Response; G = +5, V_S = ±6 V, R_L = 25 Ω, Single-Ended*



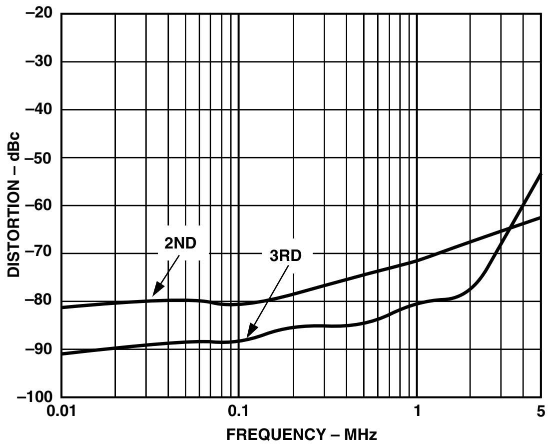
TPC 5. *100 mV Step Response; G = +5, V_S = ±12 V, R_L = 100 Ω, Single-Ended*



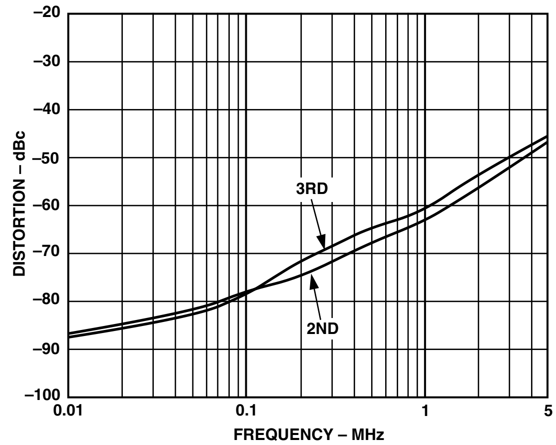
TPC 3. *4 V Step Response; G = +5, V_S = ±6 V, R_L = 25 Ω, Single-Ended*



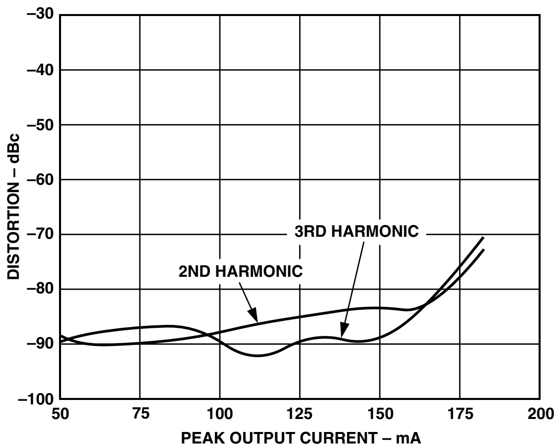
TPC 6. *4 V Step Response; G = +5, V_S = ±12 V, R_L = 100 Ω, Single-Ended*



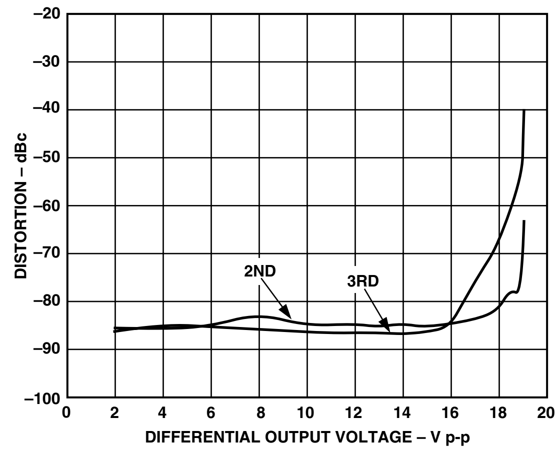
TPC 7. Distortion vs. Frequency; $V_S = \pm 12$ V, $R_L = 200\ \Omega$, Differential, $V_O = 16$ V p-p



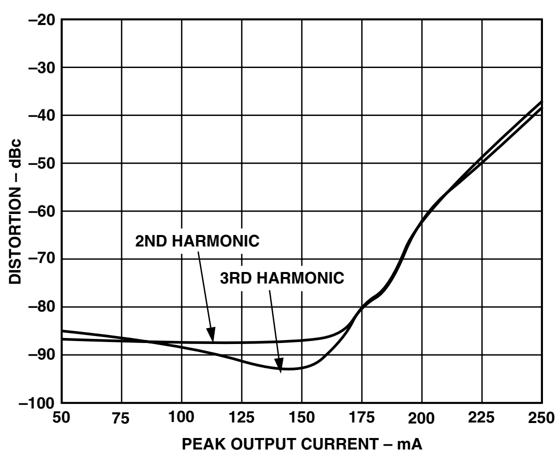
TPC 10. Distortion vs. Frequency; $V_S = \pm 6$ V, $R_L = 50\ \Omega$, Differential, $V_O = 3$ V p-p



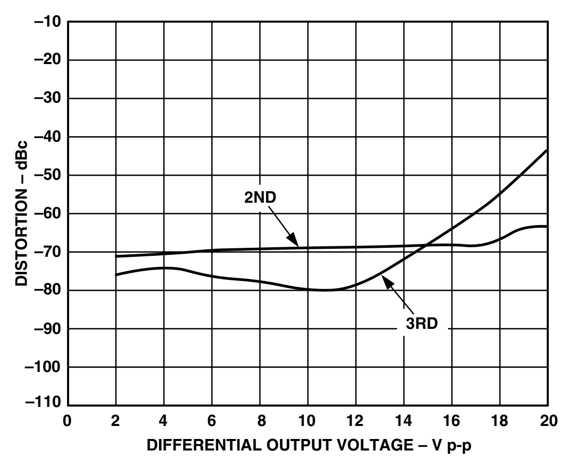
TPC 8. Distortion vs. Peak Output Current; $V_S = \pm 6$ V; $R_L = 10\ \Omega$; f = 100 kHz; Single-Ended; Second Harmonic



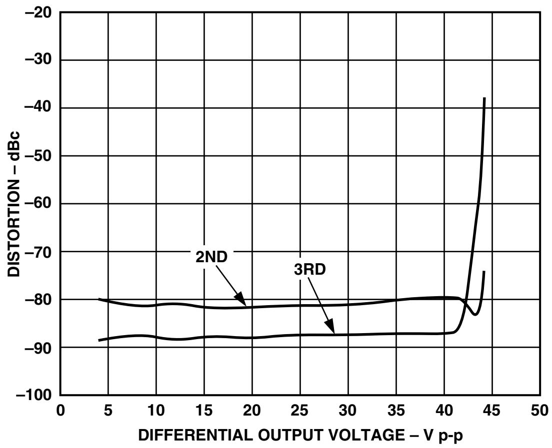
TPC 11. Distortion vs. Output Voltage; f = 100 kHz, $V_S = \pm 6$ V, G = +10, $R_L = 50\ \Omega$, Differential



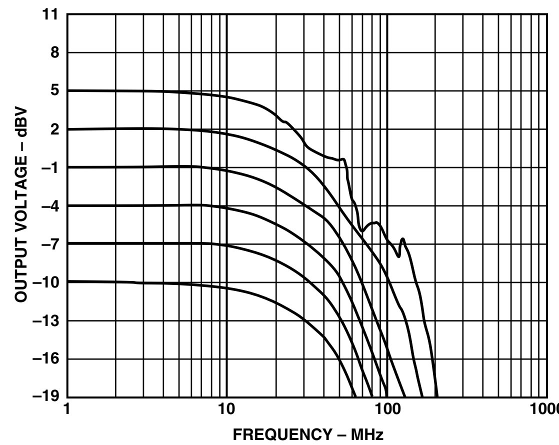
TPC 9. Distortion vs. Peak Output Current; $V_S = \pm 12$ V; $R_L = 25\ \Omega$; f = 100 kHz; Single-Ended; Second Harmonic



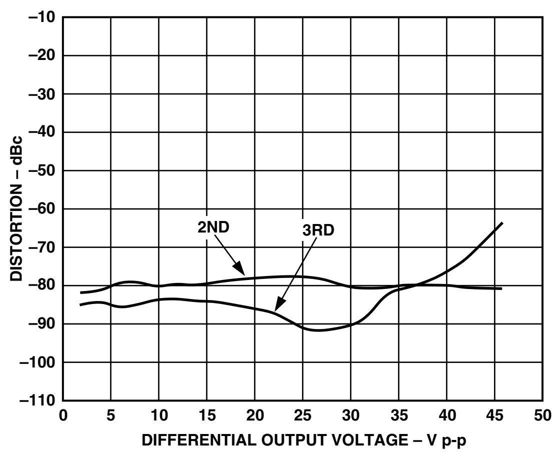
TPC 12. Distortion vs. Output Voltage; f = 500 kHz, $V_S = \pm 6$ V, G = +10, $R_L = 50\ \Omega$, Differential



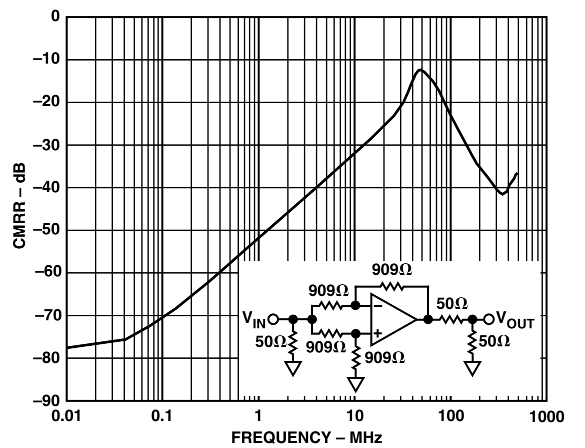
TPC 13. Distortion vs. Output Voltage; f = 100 kHz, $V_S = \pm 12$ V, G = +10, $R_L = 200\ \Omega$, Differential



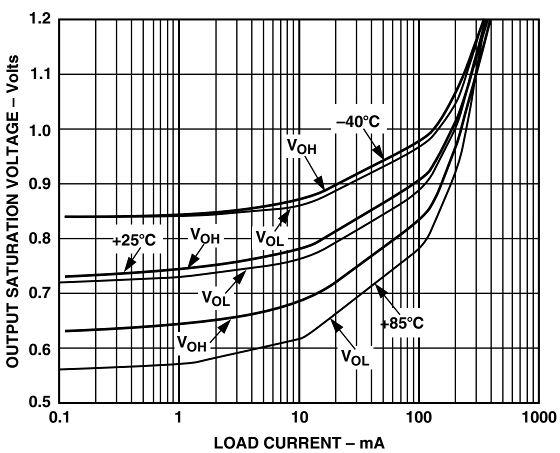
TPC 16. Output Voltage vs. Frequency; $V_S = \pm 12$ V, $R_L = 100\ \Omega$; G = +5



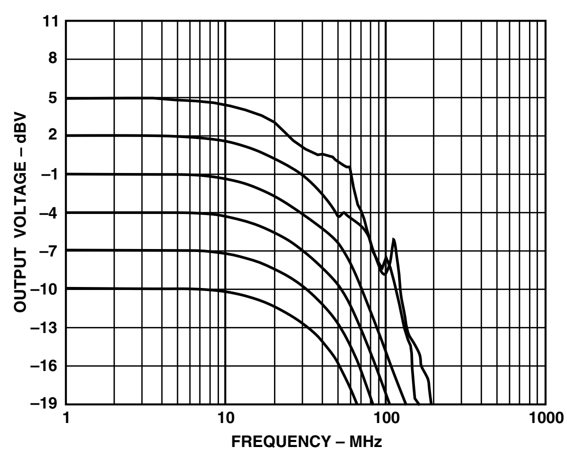
TPC 14. Distortion vs. Output Voltage; f = 500 kHz, $V_S = \pm 12$ V, G = +10, $R_L = 200\ \Omega$, Differential



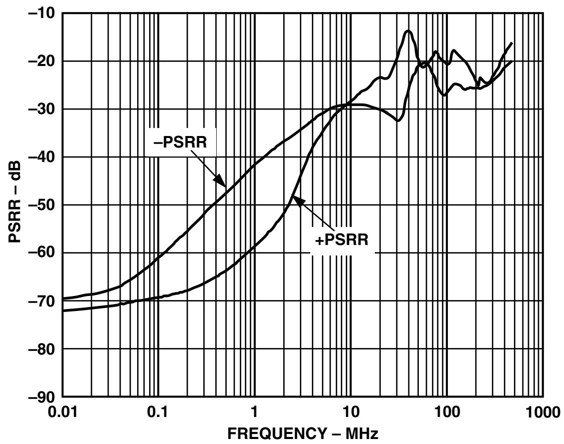
TPC 17. CMRR vs. Frequency; $V_S = \pm 12$ V, $R_L = 100\ \Omega$



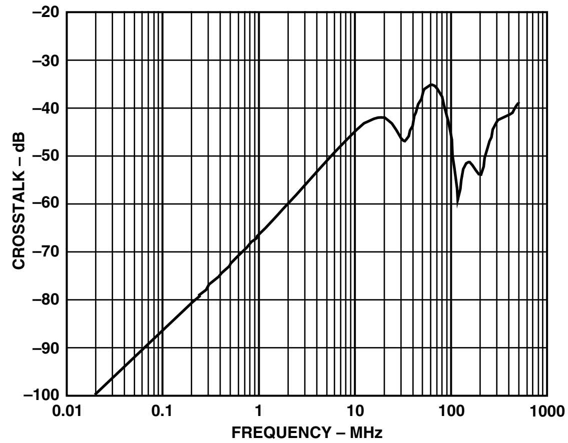
TPC 15. Output Saturation Voltage vs. Load; $V_S = \pm 12$ V, $V_S = \pm 6$ V



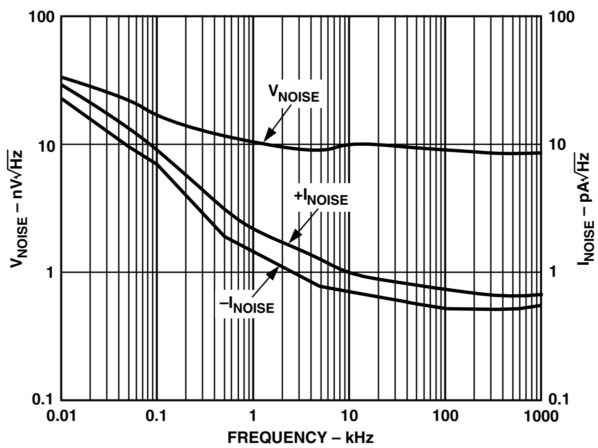
TPC 18. Output Voltage vs. Frequency; $V_S = \pm 6$ V, $R_L = 100\ \Omega$; G = +5



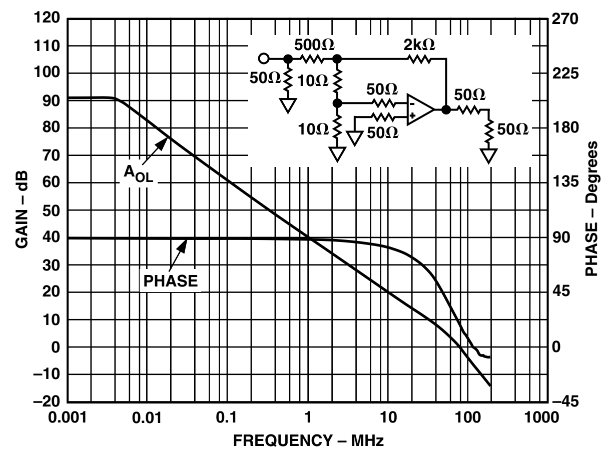
TPC 19. PSRR vs. Frequency; $R_L = 100\ \Omega$



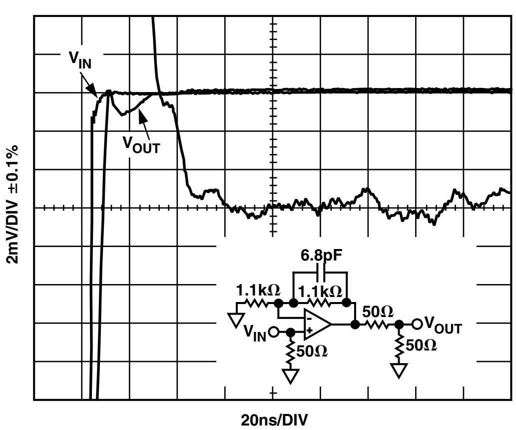
TPC 22. Crosstalk vs. Frequency, $V_S = \pm 12$ V, $V_S = \pm 6$ V; G = +2; V_{IN} = 10 dBm



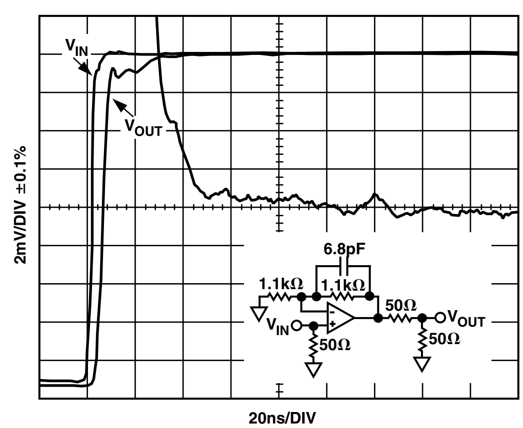
TPC 20. Noise vs. Frequency



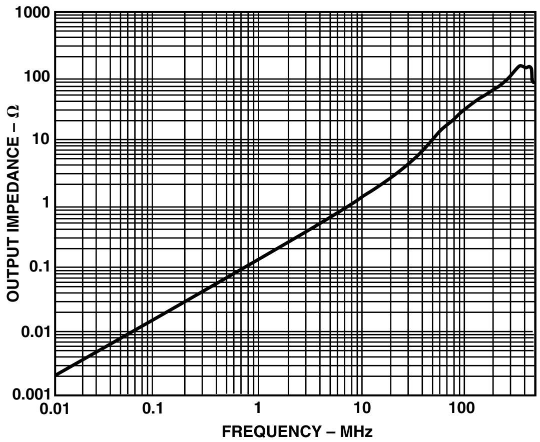
TPC 23. Open-Loop Gain and Phase vs. Frequency



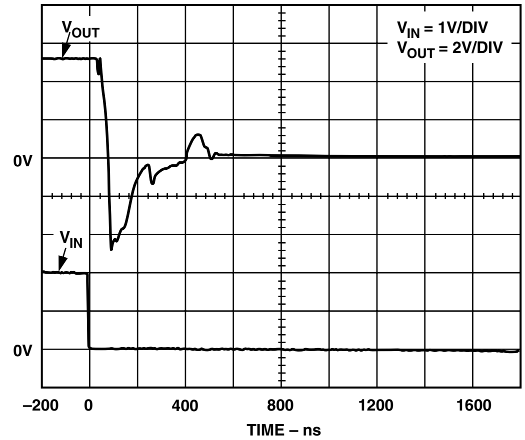
TPC 21. Settling Time 0.1%; $V_S = \pm 12$ V, $R_L = 100\ \Omega$, V_{OUT} = 2 V p-p



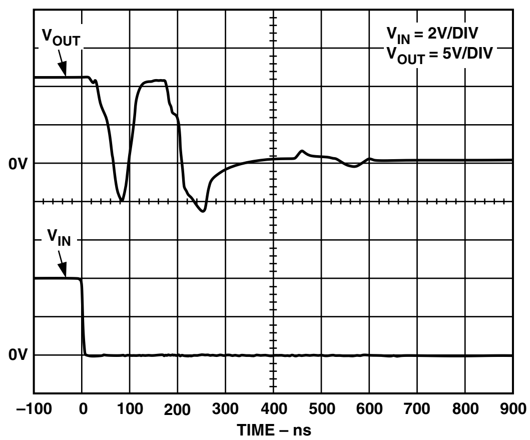
TPC 24. Settling Time 0.1%; $V_S = \pm 6$ V, $R_L = 100\ \Omega$, V_{OUT} = 2 V p-p



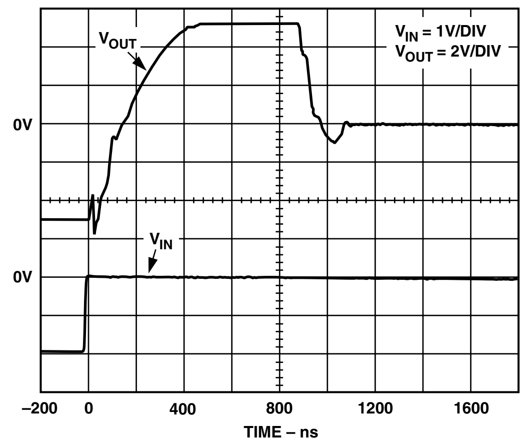
TPC 25. Output Impedance vs. Frequency; $V_S = \pm 12$ V; $V_S = \pm 6$ V



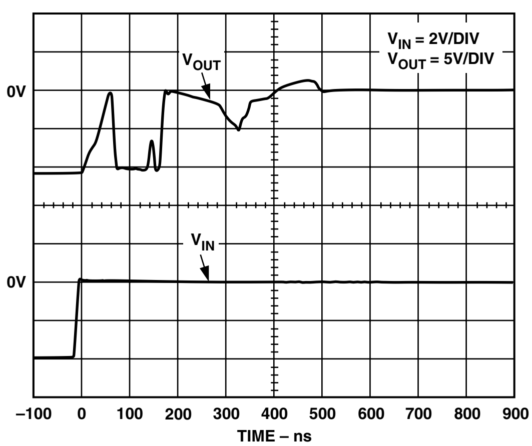
TPC 28. Overload Recovery; $V_S = \pm 6$ V, G = +5, R_L = 100 Ω



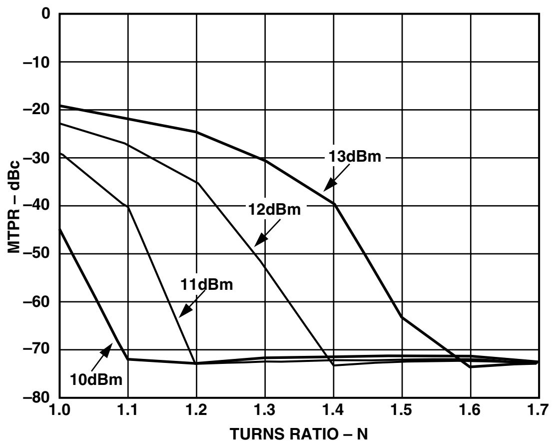
TPC 26. Overload Recovery; $V_S = \pm 12$ V, G = +5, R_L =100 Ω



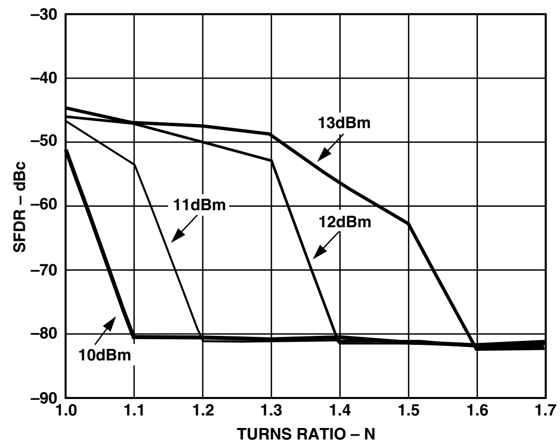
TPC 29. Overload Recovery; $V_S = \pm 6$ V, G = +5, R_L = 100 Ω



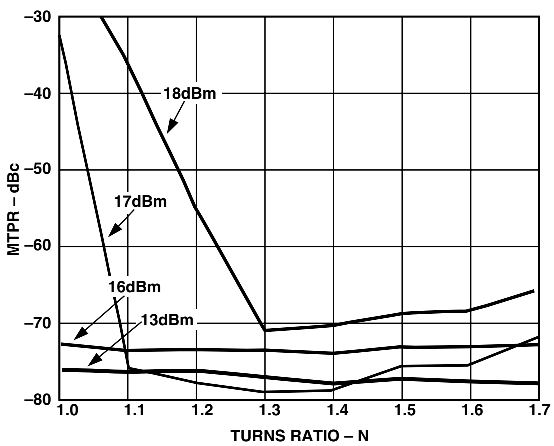
TPC 27. Overload Recovery; $V_S = \pm 12$ V, G = +5, R_L = 100 Ω



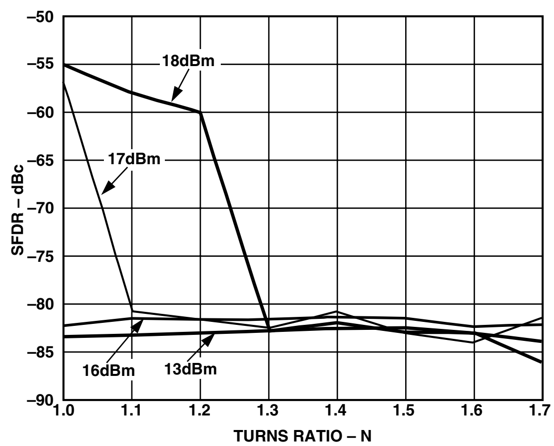
TPC 30. MTPR vs. Turns Ratio; $V_S = \pm 6$ V, $R_L = 100\ \Omega$ Line



TPC 32. SFDR vs. Turns Ratio; $V_S = \pm 6$ V, $R_L = 100\ \Omega$ Line



TPC 31. MTPR vs. Turns Ratio; $V_S = \pm 12$ V, $R_L = 100\ \Omega$ Line



TPC 33. SFDR vs. Turns Ratio; $V_S = \pm 12$ V, $R_L = 100\ \Omega$ Line

GENERAL INFORMATION

The AD8019 is a voltage feedback amplifier with high output current capability. As a voltage feedback amplifier, the AD8019 features lower current noise and more applications flexibility than current feedback designs. It is fabricated on Analog Devices' proprietary High Voltage eXtra Fast Complementary Bipolar Process (XFCB-HV), which enables the construction of PNP and NPN transistors with similar f_Ts in the 4 GHz region. The process is dielectrically isolated to eliminate the parasitic and latch-up problems caused by junction isolation. These features enable the construction of high-frequency, low-distortion amplifiers.

POWER-DOWN FEATURE

A digitally programmable logic pin (PWDN) is available on the TSSOP-14 package. It allows the user to select between two operating conditions, full on and shutdown. The DGND pin is the logic reference. The threshold for the PWDN pin is typically 1.8 V above DGND. If the power-down feature is not being used, it is better to tie the DGND pin to the lowest potential that the AD8019 is tied to and place the PWDN pin at a potential at least 3 V higher than that of the DGND pin, but lower than the positive supply voltage.

POWER SUPPLY AND DECOUPLING

The AD8019 can be powered with a good quality (i.e., low-noise) supply anywhere in the range from +12 V to ±12 V. In order to optimize the ADSL upstream drive capability of 13 dBm and maintain the best Spurious Free Dynamic Range (SFDR), the AD8019 circuit should be powered with a well-regulated supply.

Careful attention must be paid to decoupling the power supply. High quality capacitors with low equivalent series resistance (ESR) such as multilayer ceramic capacitors (MLCCs) should be used to minimize supply voltage ripple and power dissipation. In addition, 0.1 µF MLCC decoupling capacitors should be located no more than 1/8 inch away from each of the power supply pins. A large, usually tantalum, 10 µF to 47 µF capacitor is required to provide good decoupling for lower frequency signals and to supply current for fast, large signal changes at the AD8019 outputs.

POWER DISSIPATION

It is important to consider the total power dissipation of the AD8019 in order to properly size the heat sink area of an application. Figure 3 is a simple representation of a differential driver. With some simplifying assumptions we can estimate the total power dissipated in this circuit. If the output current is large compared to the quiescent current, computing the dissipation in the output devices and adding it to the quiescent power dissipation will give a close approximation of the total power dissipation in the package. A factor α (~0.6-1) corrects for the slight error due to the Class A/B operation of the output stage. It can be estimated by subtracting the quiescent current in the output stage from the total quiescent current and ratioing that to the total quiescent current. For the AD8019, $\alpha = 0.833$.

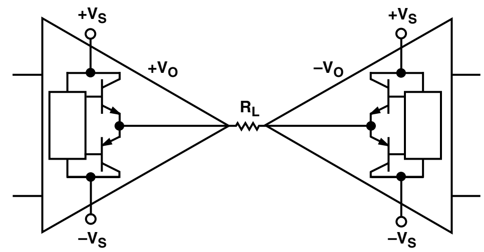


Figure 3. Simplified Differential Driver

Remembering that each output device only dissipates for half the time gives a simple integral that computes the power for each device:

$$\frac{1}{2}\int\left[(V_S - V_O)\times\frac{(2\,V_O)}{R_L}\right]$$

The total supply power can then be computed as:

$$P_{TOT} = 4\,(V_S\int|V_O| - \int V_O^{\,2})\times\frac{1}{2} + 2\,\alpha\,I_Q\,V_S + P_{OUT}$$

In this differential driver, V_O is the voltage at the output of one amplifier, so 2 V_O is the voltage across R_L. R_L is the total impedance seen by the differential driver, including back termination. Now, with two observations the integrals are easily evaluated. First, the integral of V_O^2 is simply the square of the rms value of V_O. Second, the integral of $|V_O|$ is equal to the average rectified value of V_O, sometimes called the mean average deviation, or MAD. It can be shown that for a DMT signal, the MAD value is equal to 0.8 times the rms value.

$$P_{TOT} = 4\,(0.8\,V_O\;rms\,V_S - V_O\;rms^2)\times\frac{1}{R_L} + 2\,\alpha\,I_Q\,V_S + P_{OUT}$$

For the AD8019 operating on a single 12 V supply and delivering a total of 16 dBm (13 dBm to the line and 3 dBm to the matching network) into 17.3 Ω (100 Ω reflected back through a 1:1.7 transformer plus back termination), the dissipated power is:

$$= 332\;mW + 40\;mW$$

$$= 372\;mW$$

Using these calculations and a θ_{JA} of 90°C/W for the TSSOP package and 100°C/W for the SOIC, Tables I–IV show junction temperature versus power delivered to the line for several supply voltages while operating with an ambient temperature of 85°C. The shaded areas indicate operation at a junction temperature over the absolute maximum rating of 150°C, and should be avoided.

Table I. Junction Temperature vs. Line Power and Operating Voltage for TSSOP

	V_{SUPPLY}		
P_{LINE}, dBm	±12	±12.5	±13
13	132	134	137
14	134	137	139
15	136	139	141
16	139	141	144
17	141	144	147
18	143	147	150

Table II. Junction Temperature vs. Line Power and Operating Voltage for SOIC

	V_{SUPPLY}		
P_{LINE}, dBm	±12	±12.5	±13
13	137	140	143
14	140	142	145
15	142	145	148
16	145	148	151
17	147	150	154
18	150	153	157

Table III. Junction Temperature vs. Line Power and Operating Voltage for TSSOP

	V_{SUPPLY}	
P_{LINE}, dBm	+12	+13
13	115	118
14	116	119
15	118	121
16	120	123

Table IV. Junction Temperature vs. Line Power and Operating Voltage for SOIC

	V_{SUPPLY}	
P_{LINE}, dBm	+12	+13
13	118	121
14	120	123
15	122	125
16	124	128

Thermal stitching, which connects the outer layers to the internal ground plane(s), can help to utilize the thermal mass of the PCB to draw heat away from the line driver and other active components.

LAYOUT CONSIDERATIONS

As is the case with all high-speed applications, careful attention to printed circuit board layout details will prevent associated board parasitics from becoming problematic. Proper RF design technique is mandatory. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low-impedance return path. Removing the ground plane on all layers from the areas near the input and output pins will reduce stray capacitance, particularly in the area of the inverting inputs. The signal routing should be short and direct in order to minimize parasitic inductance and capacitance associated with these traces. Termination resistors and loads should be located as close as possible to their respective inputs and outputs. Input and output traces should be kept as far apart as possible to minimize coupling (crosstalk) though the board.

Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize balanced performance. When running differential signals over a long distance, the traces on the PCB should be close together or any differential wiring should be twisted together to minimize the area of the loop that is formed. This will reduce the radiated energy and make the circuit less susceptible to RF interference. Adherence to stripline design techniques for long signal traces (greater than about 1 inch) is recommended.

Evaluation Board

The AD8019 is available installed on an evaluation board for both package styles. Figures 8 and 9 show the schematics for the TSSOP evaluation board.

The receiver circuit on these boards is typically unpopulated. Requesting samples of the AD8022AR, along with either of the AD8019 evaluation boards, will provide the capability to evaluate the AD8019 along with other Analog Devices products in a typical transceiver circuit. The evaluation circuits have been designed to replicate the CPE side analog transceiver hybrid circuits.

The circuit mentioned above is designed using a 1-transformer transceiver topology including a line receiver, line driver, line matching network, an RJ11 jack for interfacing to line simulators, and differential inputs.

AC-coupling capacitors of 0.1 µF, C8, and C10, in combination with 10 kΩ, resistors R24 and R25, will form a 1st order high-pass pole at 160 Hz.

Transformer Selection

Customer premise ADSL requires the transmission of a 13 dBm (20 mW) DMT signal. The DMT signal has a crest factor of 5.3, requiring the line driver to provide peak line power of 560 mW. 560 mW peak line power translates into a 7.5 V peak voltage on a 100 Ω telephone line. Assuming that the maximum low distortion output swing available from the AD8019 line driver on a ±12 V supply is 20 V and taking into account the power lost due to the termination resistance, a step-up transformer with turns ratio of 1:1 is adequate for most applications. If the modem designer desires to transmit more than 13 dBm down the twisted pair, a higher turns ratio can be used for the transformer. This trade-off comes at the expense of higher power dissipation by the line driver as well as increased attenuation of the downstream signal that is received by the transceiver.

In the simplified differential drive circuit shown in Figure 7, the AD8019 is coupled to the phone line through a step-up transformer with a 1:1 turns ratio. R1 and R2 are back termination or line matching resistors, each 50 Ω ($100\ \Omega/(2 \times 1^2)$) where 100 Ω is the approximate phone line impedance. A transformer reflects impedance from the line side to the IC side as a value inversely proportional to the square of the turns ratio. The total differential load for the AD8019, including the termination resistors, is 200 Ω. Even under these conditions the AD8019 provides low distortion signals to within 2 V of the power supply rails.

One must take care to minimize any capacitance present at the outputs of a line driver. The sources of such capacitance can include, but are not limited to EMI suppression capacitors, overvoltage protection devices and the transformers used in the hybrid. Transformers have two kinds of parasitic capacitances, distributed, or bulk capacitance, and interwinding capacitance. Distributed capacitance is a result of the capacitance created between each adjacent winding on a transformer. Interwinding capacitance is the capacitance that exists between the windings on the primary and secondary sides of the transformer. The existence of these capacitances is unavoidable, but in specifying a transformer, one should do so in a way to minimize them in order to avoid operating the line driver in a potentially unstable environment. Limiting both distributed and interwinding capacitance to less than 20 pF each should be sufficient for most applications.

Stability Enhancements

Voltage feedback amplifiers may exhibit sensitivity to capacitance present at the inverting input. Parasitic capacitance, as small as several picofarads, in combination with the high-impedance of the input can create a pole that can dramatically decrease the phase margin of the amplifier. In the case of the AD8019, a compensation capacitor of 10 pF–20 pF in parallel with the feedback resistor will form a zero that can serve to cancel out the effects of the parasitic capacitance. Placing 100 Ω in series with each of the noninverting inputs serves to isolate the inputs from each other and from any high frequency signals that may be coupled into the amplifier via the midsupply bias.

It may also be necessary to configure the line driver as two separate, noninverting amplifiers rather than a single differential driver. When doing this, the two gain resistors can share an ac coupling capacitor of 0.1 μF to minimize any dc errors.

Adhering to previously mentioned layout techniques will also be of assistance in keeping the amplifier stable.

Receive Channel Considerations

A transformer used at the output of the differential line driver to step up the differential output voltage to the line has the inverse effect on signals received from the line. A voltage reduction or attenuation equal to the inverse of the turns ratio is realized in the receive channel of a typical bridge hybrid. The turns ratio of the transformer may also be dictated by the ability of the receive circuitry to resolve low-level signals in the noisy twisted pair telephone plant. While higher turns ratio transformers boost transmit signals to the appropriate level, they also effectively reduce the received signal to noise ratio due to the reduction in the received signal strength.

Using a transformer with as low a turns ratio as possible will limit degradation of the received signal.

The AD8022, a dual amplifier with typical RTI voltage noise of only 2.5 nV/$\sqrt{\text{Hz}}$ and a low supply current of 4 mA/amplifier is recommended for the receive channel.

DMT Modulation, Multi-Tone Power Ratio (MTPR) and Out-of-Band SFDR

ADSL systems rely on Discrete Multi-Tone (or DMT) modulation to carry digital data over phone lines. DMT modulation appears in the frequency domain as power contained in several individual frequency subbands, sometimes referred to as tones or bins, each of which are uniformly separated in frequency. A uniquely encoded, Quadrature Amplitude Modulation (QAM)-like signal occurs at the center frequency of each subband or tone. See Figure 4 for an example of a DMT waveform in the frequency domain, and Figure 5 for a time domain waveform. Difficulties will exist when decoding these subbands if a QAM signal from one subband is corrupted by the QAM signal(s) from other subbands, regardless of whether the corruption comes from an adjacent subband or harmonics of other subbands.

Conventional methods of expressing the output signal integrity of line drivers such as single tone harmonic distortion or THD, two-tone Intermodulation Distortion (IMD) and third order intercept (IP3) become significantly less meaningful when amplifiers are required to process DMT and other heavily modulated waveforms. A typical ADSL upstream DMT signal can contain as many as 27 carriers (subbands or tones) of QAM signals. Multi-Tone Power Ratio (MTPR) is the relative difference between the measured power in a typical subband (at one tone or carrier) versus the power at another subband specifically selected to contain no QAM data. In other words, a selected subband (or tone) remains open or void of intentional power (without a QAM signal) yielding an empty frequency bin. MTPR, sometimes referred to as the 'empty bin test,' is typically expressed in dBc, similar to expressing the relative difference between single tone fundamentals and second or third harmonic distortion components. Measurements of MTPR are typically made on the line side or secondary side of the transformer.

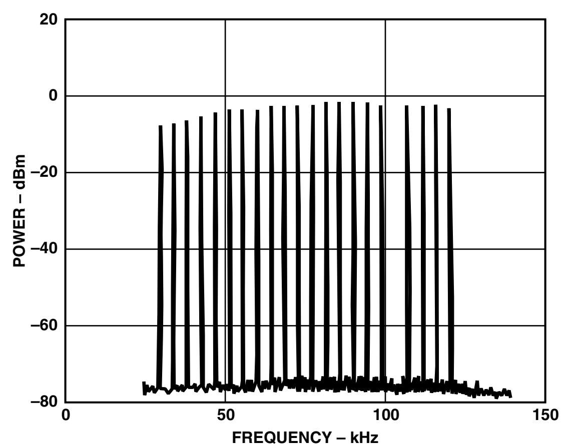


Figure 4. DMT Waveform in the Frequency Domain

MTPR versus transformer turns ratio is depicted in TPCs 30 and 31 and covers a variety of line power ranging from 10 dBm to 18 dBm. As the turns ratio increases, the driver hybrid can deliver more undistorted power to the load due to the high output current capability of the AD8019. Significant degradation of MTPR will occur if the output of the driver swings to the rails, causing clipping at the DMT voltage peaks. Driving DMT signals to such extremes not only compromises "in band" MTPR, but will also produce spurs that exist outside of the frequency spectrum containing the transmitted signal. "Out-of-band" spurious free dynamic range (SFDR) can be defined as the relative difference in amplitude between these spurs and a tone in one of the upstream bins. Compromising out-of-band SFDR is the equivalent of increasing near-end cross talk (NEXT). Regardless of terminology, maintaining out-of-band SFDR while reducing NEXT will improve the overall performance of the modems connected at either end of the twisted pair.

Generating DMT Signals

At this time, DMT-modulated waveforms are not typically menu-selectable items contained within arbitrary waveform generators. Even using (AWG) software to generate DMT signals, AWGs that are available today may not deliver DMT signals sufficient in performance with regard to MTPR due to limitations in the D/A converters and output drivers used by AWG manufacturers. Similar to evaluating single-tone distortion performance of an amplifier, MTPR evaluation requires a DMT signal generator capable of delivering MTPR performance better than that of the driver under evaluation. Generating DMT signals can be accomplished using a Tektronics AWG 2021 equipped with Option 4, (12-/24-bit, TTL Digital Data Out), digitally coupled to Analog Devices' AD9754, a 14-bit TxDAC®, buffered by an AD8002 amplifier configured as a differential driver. Note that the DMT waveforms, available on the Analog Devices website, www.analog.com, or similar. WFM files are needed to produce the necessary digital data required to drive the TxDAC from the optional TTL Digital Data output of the TEK AWG2021.

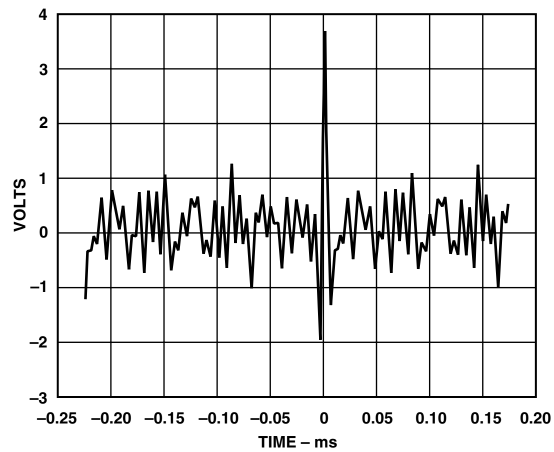


Figure 5. DMT Signal in the Time Domain

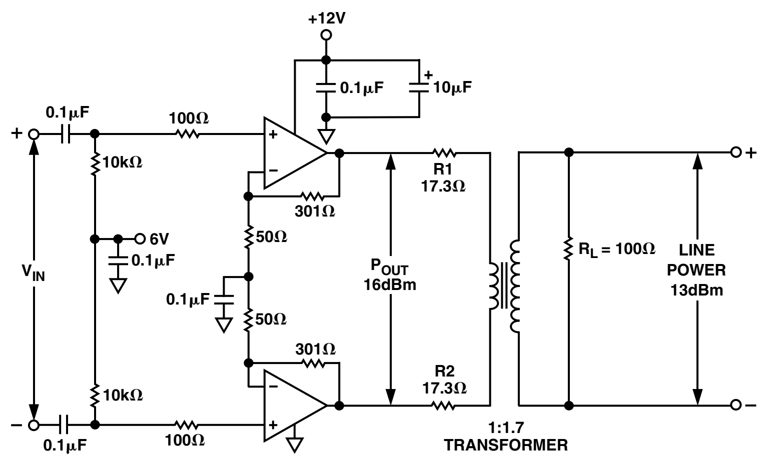


Figure 6. Recommended Application Circuit for Single +12 V Supply

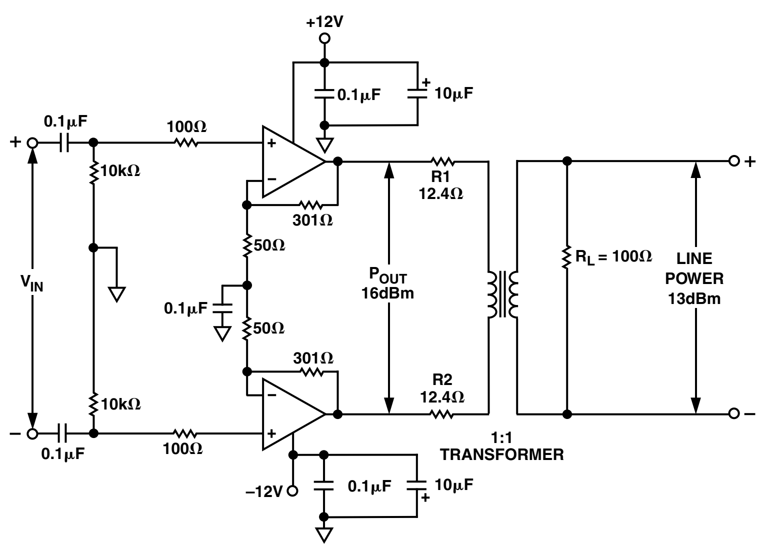


Figure 7. Recommended Application Circuit for ±12 V Supply

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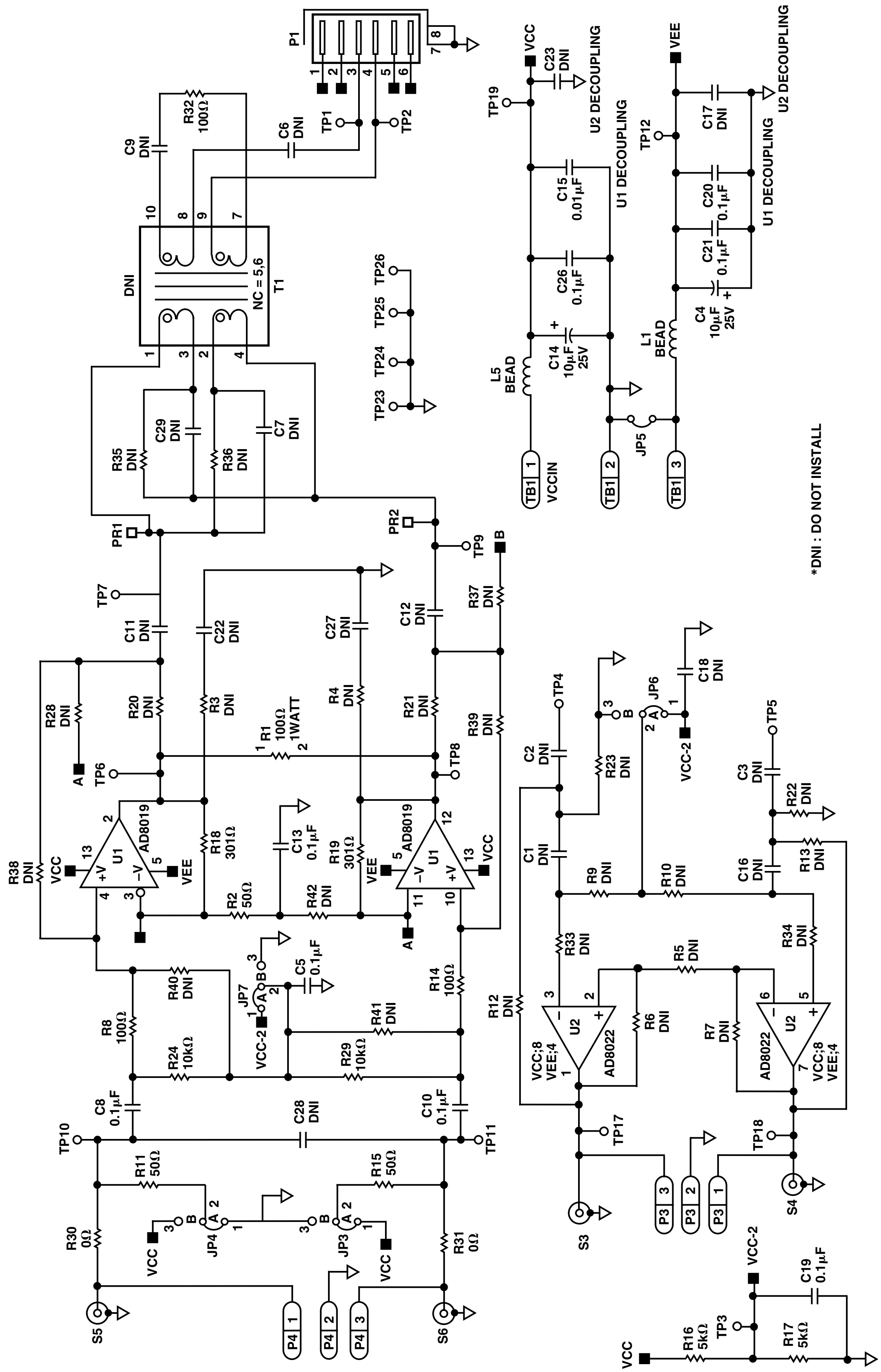


Figure 8. TSSOP Noninverting DSL Evaluation Board Schematic

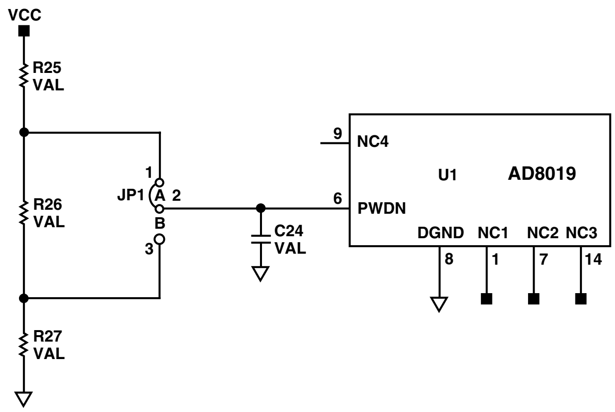


Figure 9. DSL Driver Input Control Circuit

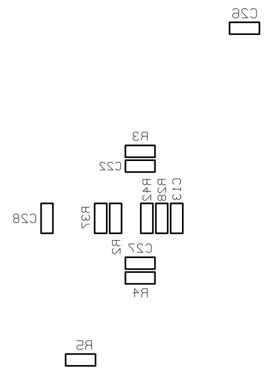


Figure 11. TSSOP Evaluation Board Silkscreen Bottom

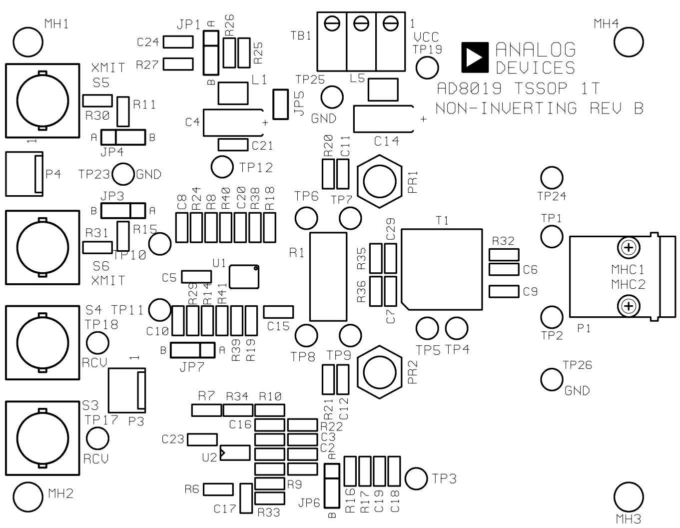


Figure 10. TSSOP Evaluation Board Silkscreen Top

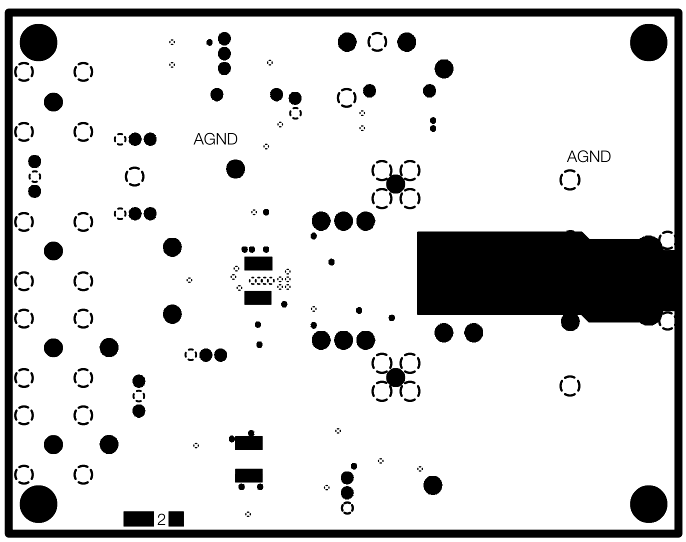


Figure 12. TSSOP Evaluation Board Power Plane

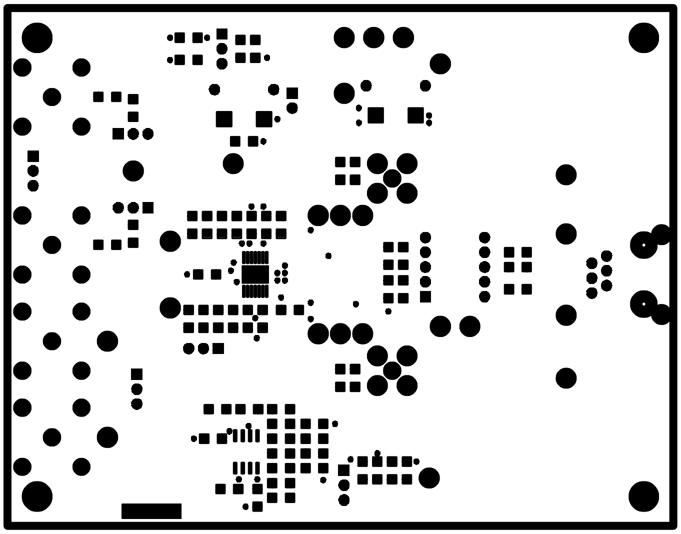


Figure 13. Solder Mask Top

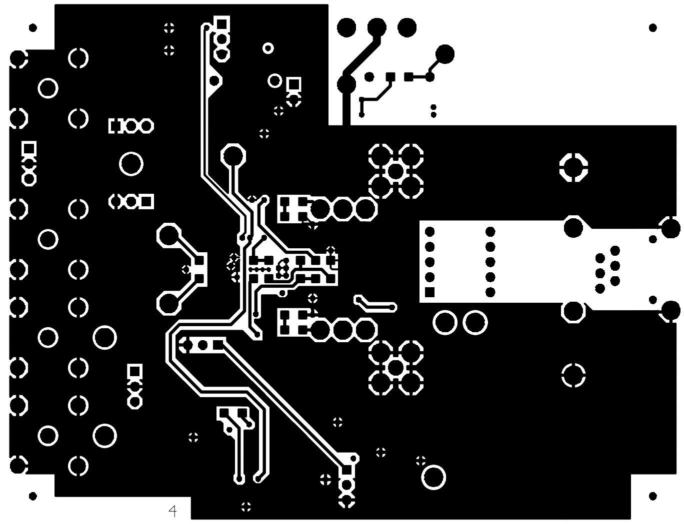


Figure 15. Ground Plane Bottom

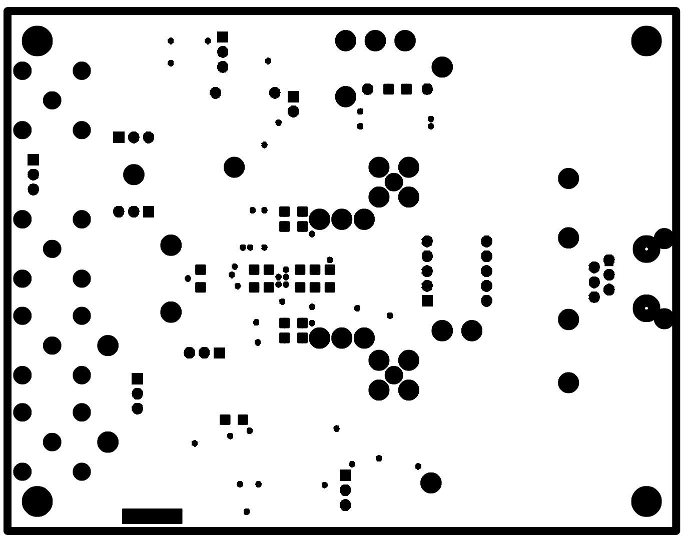


Figure 14. Solder Mask Bottom

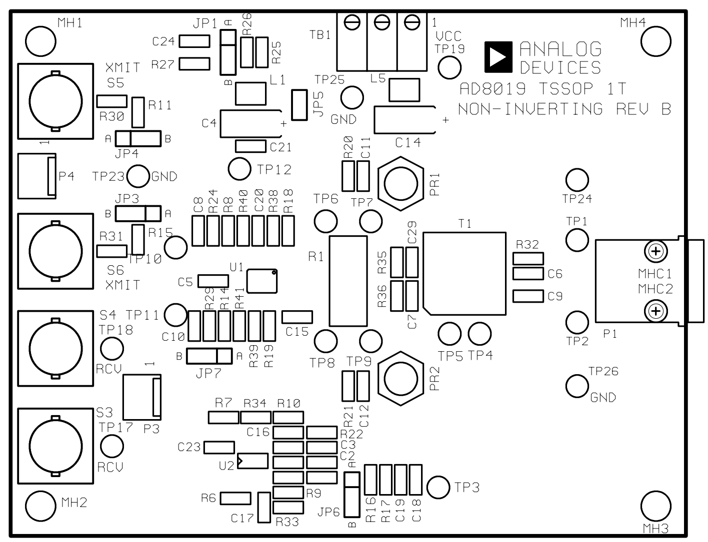


Figure 16. Assembly Top

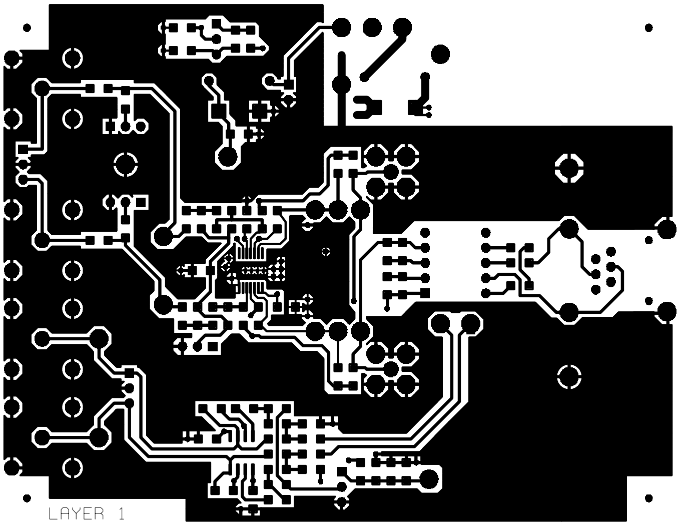


Figure 17. Ground Plane Top

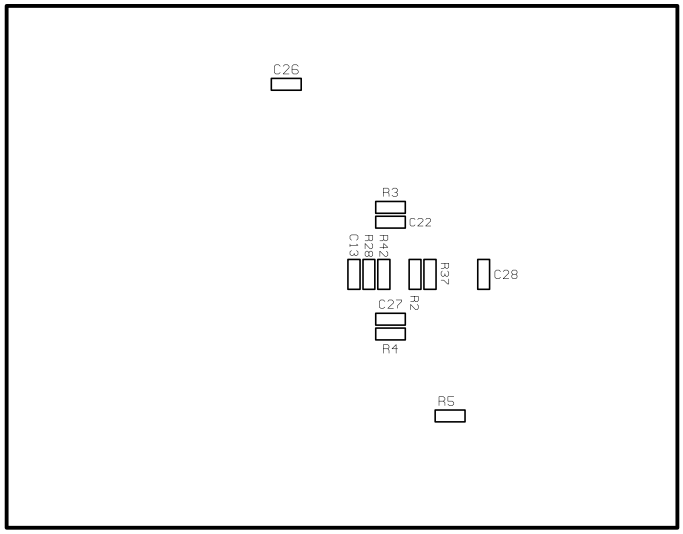


Figure 18. Assembly Bottom

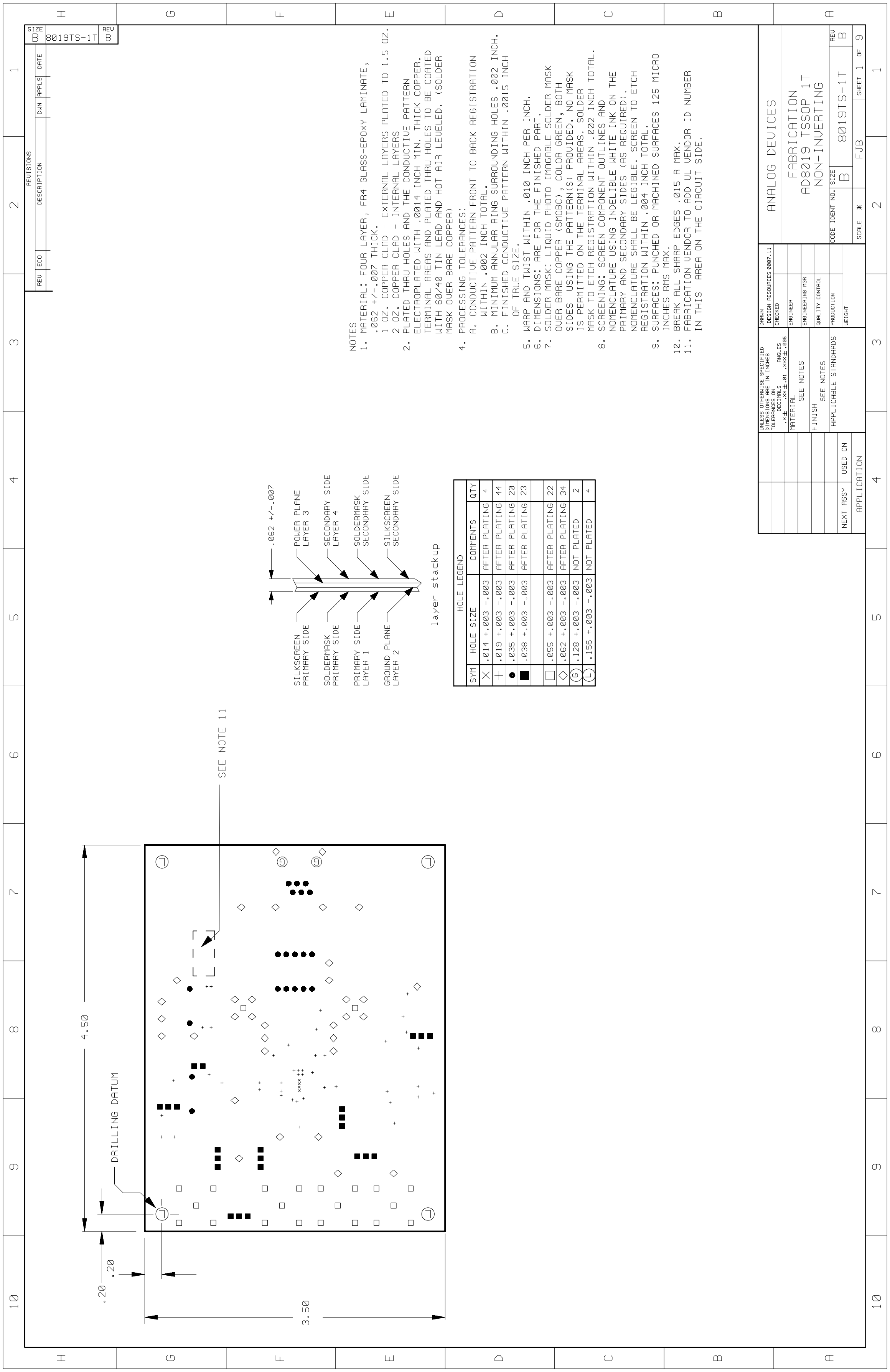
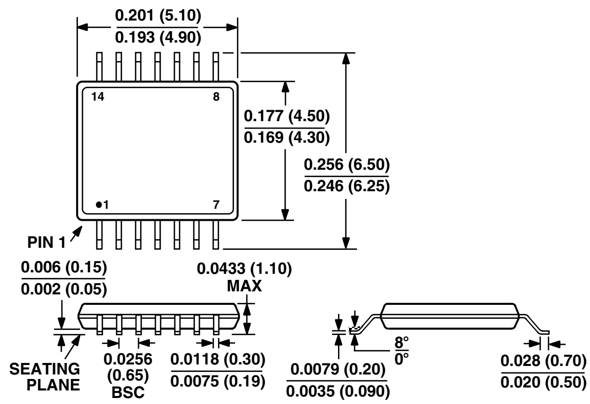


Figure 19. Board Fabrication

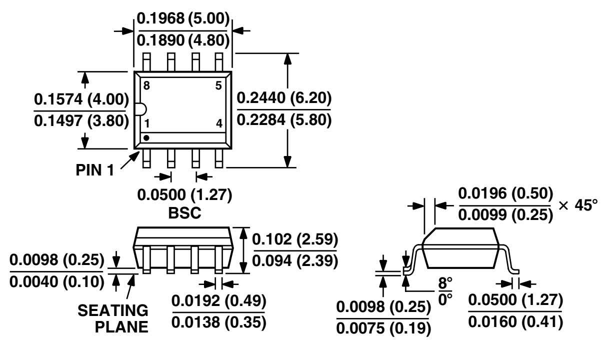
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead TSSOP
(RU-14)



8-Lead SOIC
(R-8)



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