

## FIN1026 3.3V LVDS 2-Bit High Speed Differential Receiver

### General Description

This dual receiver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100mV, to LVTTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1026 can be paired with its companion driver, the FIN1025, or any other LVDS driver.

### Features

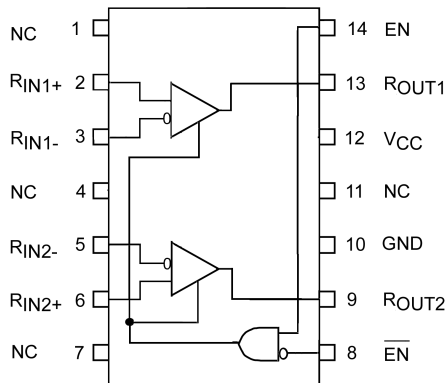
- Greater than 400Mbps data rate
- Flow-through pinout simplifies PCB layout
- 3.3V power supply operation
- 0.4ns maximum differential pulse skew
- 2.5ns maximum propagation delay
- Low power dissipation
- Power-Off protection
- Fail safe protection for open-circuit, shorted and terminated non-driven input conditions
- Meets or exceeds the TIA/EIA-644 LVDS standard
- 14-Lead TSSOP package saves space

### Ordering Code:

Order Number	Package Number	Package Description
FIN1026MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Pin Descriptions

Pin Name	Description
$R_{OUT1}, R_{OUT2}$	LVTTTL Data Outputs
$R_{IN1+}, R_{IN2+}$	Non-Inverting LVDS Inputs
$R_{IN1-}, R_{IN2-}$	Inverting LVDS Inputs
EN	Driver Enable Pin
$\overline{EN}$	Inverting Driver Enable Pin
$V_{CC}$	Power Supply
GND	Ground
NC	No Connect

### Truth Table

Inputs				Outputs
EN	$\overline{EN}$	$R_{IN+}$	$R_{IN-}$	$R_{OUT}$
H	L or Open	H	L	H
H	L or Open	L	H	L
H	L or Open	Fail Safe Condition		H
X	H	X	X	Z
L or Open	X	X	X	Z

H = HIGH Logic Level  
L = LOW Logic Level  
X = Don't Care  
Z = High Impedance  
Fail Safe = Open, Shorted, Terminated

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
LVDS DC Input Voltage ( $V_{IN}$ )	-0.5V to +4.6V
LVTTL DC Input Voltage ( $V_{IN}$ )	-0.5V to 6V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to 6V
DC Output Current ( $I_O$ )	16mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Max Junction Temperature ( $T_J$ )	150°C
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C
ESD (Human Body Model)	10,000V
ESD (Machine Model)	600V

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	3.0V to 3.6V
Magnitude of Differential Voltage ( $ V_{ID} $ )	100mV to $V_{CC}$
Common-Mode Input Voltage ( $V_{IC}$ )	0.05V to 2.35V
Input Voltage ( $V_{IN}$ )	0 to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

**DC Electrical Characteristics**

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
$V_{TH}$	Differential Input Threshold HIGH	See Figure 1, $V_{IC} = +0.05V, +1.2V, \text{ or } 2.35V$			100	mV
$V_{TL}$	Differential Input Threshold LOW	See Figure 1, $V_{IC} = +0.05V, +1.2V, \text{ or } 2.35V$	-100			mV
$I_{IN}$	Input Current	$V_{IN} = 0V \text{ or } V_{CC}$			$\pm 20$	$\mu A$
$I_{I(OFF)}$	Power-Off Input Current	$V_{CC} = 0V, V_{IN} = 0V \text{ or } 3.6V$			$\pm 20$	$\mu A$
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -100 \mu A$	$V_{CC} - 0.2$	3.29		V
		$I_{OH} = -8 \text{ mA}$	2.4	3.1		
$V_{OL}$	Output LOW Voltage	$I_{OH} = 100 \mu A$		0	0.2	V
		$I_{OL} = 8 \text{ mA}$		0.18	0.5	
$I_{OZ}$	Disabled Output Leakage Current	$EN = 0.8 \text{ and } EN^* = 2V, V_{OUT} = 3.6V \text{ or } 0V$			$\pm 20$	$\mu A$
$V_{IK}$	Input Clamp Voltage	$I_{IK} = -18 \text{ mA}$	-1.5	-0.8		V
$I_{OS}$	Output Short Circuit Current	Receiver Enabled, $V_{OUT} = 0V$ (one output shorted at a time)	-15		-100	mA
$I_{CCZ}$	Disabled Power Supply Current	Receiver Disabled		2.6	5	mA
$I_{CC}$	Power Supply Current	Receiver Enabled, ( $R_{IN+} = 1V \text{ and } R_{IN-} = 1.4V$ ) or ( $R_{IN+} = 1.4V \text{ and } R_{IN-} = 1V$ )		4.8	8.5	mA

**Note 2:** All typical values are at  $T_A = 25^\circ C$  and with  $V_{CC} = 3.3V$ .

## AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

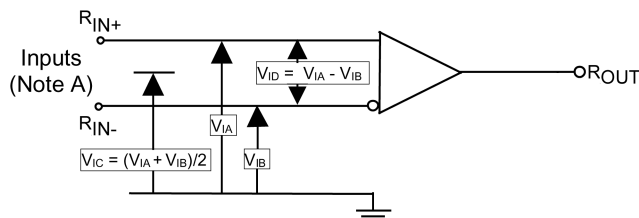
Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units	
$t_{PLH}$	Propagation Delay LOW-to-HIGH	$ V_{ID}  = 400 \text{ mV}$ , $C_L = 10 \text{ pF}$ See Figure 1 and Figure 2	1.0		2.5	ns	
$t_{PHL}$	Propagation Delay HIGH-to-LOW		1.0		2.5	ns	
$t_{TLH}$	Output Rise Time (20% to 80%)				0.7	1.2	ns
$t_{THL}$	Output Fall Time (80% to 20%)				0.7	1.2	ns
$t_{SK(P)}$	Pulse Skew $ t_{PLH} - t_{PHL} $					0.4	ns
$t_{SK(LH)}$	Channel-to-Channel Skew (Note 4)					0.3	ns
$t_{SK(HL)}$							
$t_{SK(PP)}$	Part-to-Part Skew (Note 5)				1.0	ns	
$f_{MAX}$	Maximum Operating Frequency (Note 6)		200	375		MHz	
$t_{PZH}$	LVTTTL Output Enable Time from Z to HIGH	$R_L = 1 \text{ k}\Omega$ , $C_L = 10 \text{ pF}$ , See Figure 3			6.0	ns	
$t_{PZL}$	LVTTTL Output Enable Time from Z to LOW				6.0	ns	
$t_{PHZ}$	LVTTTL Output Disable Time from HIGH to Z				6.0	ns	
$t_{PLZ}$	LVTTTL Output Disable Time from LOW to Z				6.0	ns	
$C_{IN}$	Input Capacitance	Enable Inputs		3.0		pF	
		$R_{IN}$ Inputs		4.2			
$C_{OUT}$	Output Capacitance			6		pF	

**Note 3:** All typical values are at  $T_A = 25^\circ\text{C}$  and with  $V_{CC} = 3.3\text{V}$ .

**Note 4:**  $t_{SK(LH)}$ ,  $t_{SK(HL)}$  is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

**Note 5:**  $t_{SK(PP)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

**Note 6:**  $f_{MAX}$  Criteria: Input  $t_R = t_F < 1 \text{ ns}$ ,  $V_{ID} = 300 \text{ mV}$ , (1.05V to 1.35V pp), 50% duty cycle; Output duty cycle 40% to 60%,  $V_{OL} < 0.5\text{V}$ ,  $V_{OH} > 2.4\text{V}$ . All channels switching in phase.



**Note A:** All differential input pulses have frequency = 10MHz,  $t_R$  or  $t_F = 1 \text{ ns}$

**FIGURE 1. Differential Receiver Voltage Definitions**

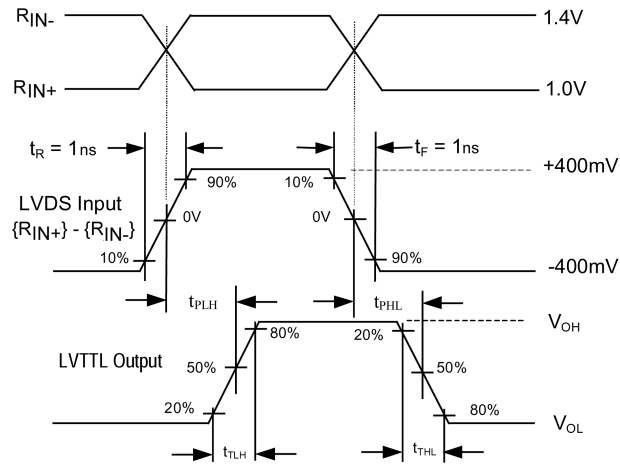
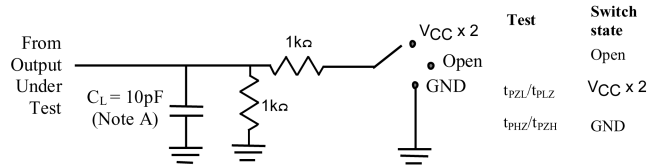


FIGURE 2. LVDS Input to LVTTTL Output AC Waveforms

Test Circuit for LVTTTL Outputs



Voltage Waveforms Enable and Disable Times

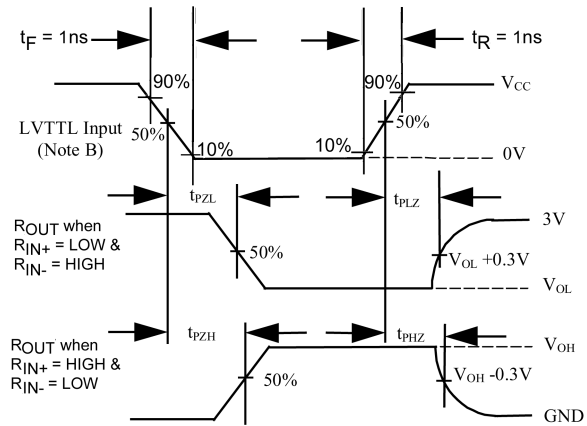
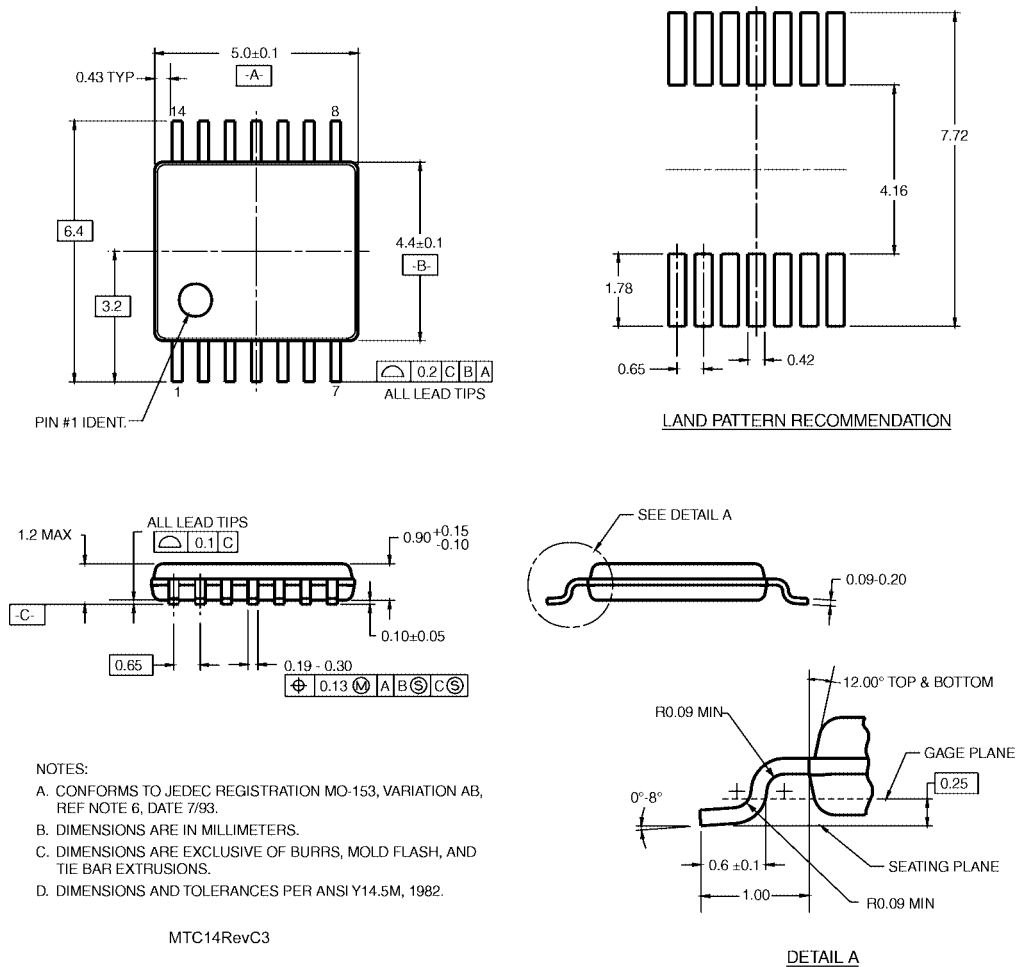


FIGURE 3. LVTTTL Outputs Test Circuit and AC Waveforms

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

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