



Single Channel Type-1 M-LVDS to LVTTTL Transceiver IDT5V5201

**Version -
May 18, 2006**

6024 Silver Creek Valley Road, San Jose, CA 95138
Telephone: (800) 345-7015 • TWX: 910-338-2070 • FAX: (408) 284-2775
Printed in U.S.A.
© 2006 Integrated Device Technology, Inc.

DISCLAIMER

Integrated Device Technology, Inc. reserves the right to make changes to its products or specifications at any time, without notice, in order to improve design or performance and to supply the best possible product. IDT does not assume any responsibility for use of any circuitry described other than the circuitry embodied in an IDT product. The Company makes no representations that circuitry described herein is free from patent infringement or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent, patent rights or other rights, of Integrated Device Technology, Inc.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any components of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



Table of Contents

TABLE OF CONTENTS	3
LIST OF TABLES	4
LIST OF FIGURES	5
FEATURES.....	6
APPLICATIONS.....	6
DESCRIPTION.....	6
FUNCTIONAL BLOCK DIAGRAM	7
1 PIN ASSIGNMENT	8
2 PIN DESCRIPTION	9
3 ELECTRICAL SPECIFICATION	10
3.1 ABSOLUTE MAXIMUM RATING AND RECOMMENDED OPERATION CONDITIONS	10
3.2 LVTTTL DRIVER/RECEIVER CHARACTERISTICS	11
3.2.1 M-LVDS to LVTTTL.....	11
3.3 M-LVDS DRIVER TYPE-1 RECEIVER CHARACTERISTICS	12
ORDERING INFORMATION.....	18



List of Tables

Table-1	Pin Description	9
Table-2	Absolute Maximum Rating	10
Table-3	Recommended Operation Conditions	10
Table-4	LVTTL DC Parameters	11
Table-5	LVTTL AC Parameters.....	11
Table-6	M-LVDS Type-1 Receiver Input Threshold Test Voltages	12
Table-7	M-LVDS DC Parameters.....	13
Table-8	M-LVDS Input Current Parameters	15
Table-9	M-LVDS AC Parameters.....	16
Table-10	M-LVDS Type-1 Receiver AC Parameters	17
Table-11	M-LVDS Driver AC Parameter	17



List of Figures

Figure-1	Functional Block Diagram	7
Figure-2	IDT5V5201 SOIC8 Package Pin Assignment	8
Figure-3	LVTTTL Output Test Circuit and Waveforms	11
Figure-4	M-LVDS Driver Output Voltage Test Circuit	13
Figure-5	M-LVDS Driver Short-Circuit Test Circuit	14
Figure-6	M-LVDS Type-1 Receiver Input Common-mode Range Test Circuit	14
Figure-7	Various Input Currents Test Circuit	15
Figure-8	Differential Skew	16
Figure-9	M-LVDS Output Voltage Test Circuit	16
Figure-10	Timing and Voltage Definitions for the Output Signal	17



FEATURES

◆ Main Features

-
- Up to 166 MHz LVTTTL input/output signal
- M-LVDS interface allows common-mode voltage: -1 V to 3.4 V
- Power up and power down glitch free
- M-LVDS interface pins in high impedance state when the device is powered down or $V_{DD} < 1.5$ V
- Capable of driving bus load from 30 Ω to 55 Ω

◆ Other Features

- Low power consumption < 120 mW
- Hot swappable
- 8-pin SOIC package

APPLICATIONS

- Backplane transmission
- Telecommunication system
- Data communications
- ATCA clock distribution

DESCRIPTION

The IDT5V5201 is a transceiver which can interchange data across multipoint data bus structures.

The device has a LVTTTL driver and receiver, a selectable Type-1 M-LVDS receiver and M-LVDS driver. It translates between LVTTTL signals

and M-LVDS signals. The drivers and the receivers can be enabled or disabled by external pins. The M-LVDS driver is capable of driving bus load from 30 Ω to 55 Ω . The M-LVDS interface allows common-mode voltage range of -1 V to 3.4 V.

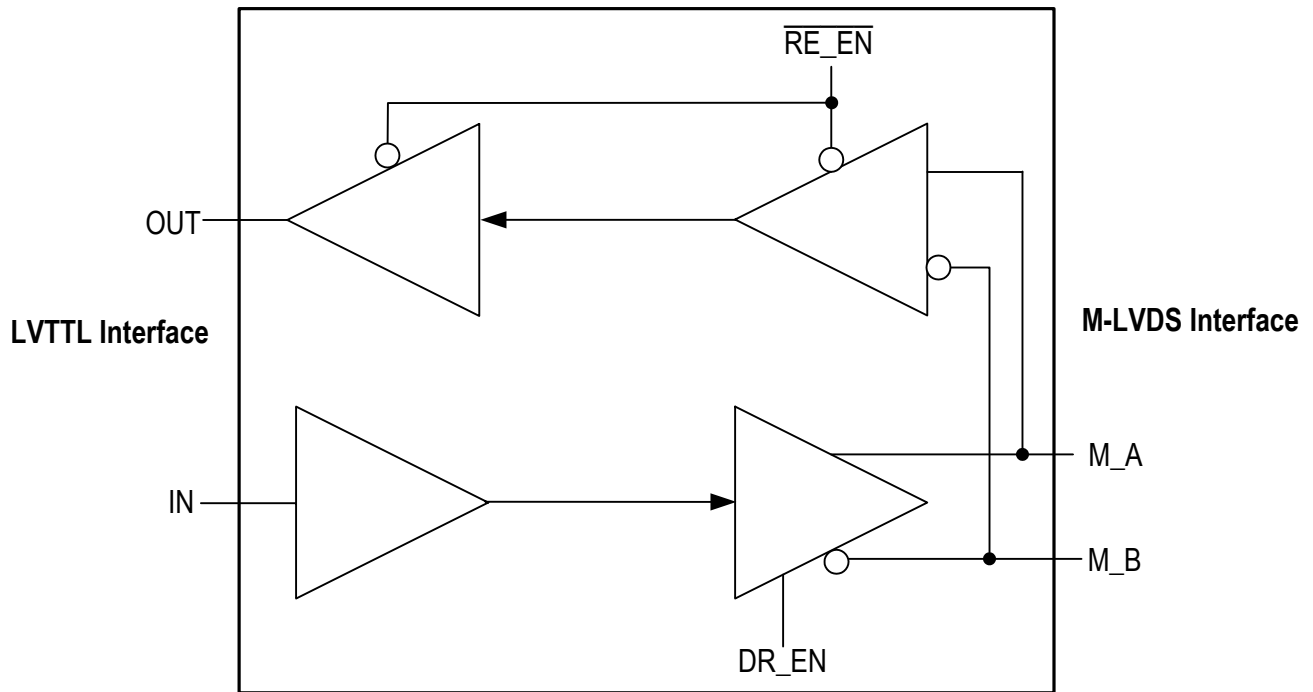
FUNCTIONAL BLOCK DIAGRAM

Figure-1 Functional Block Diagram

1 PIN ASSIGNMENT

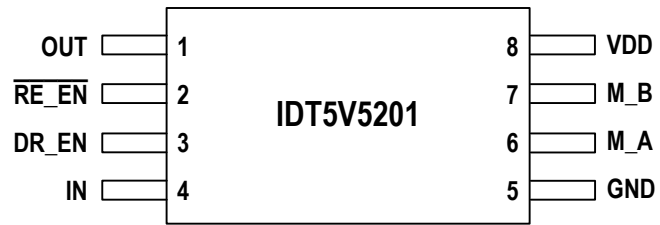


Figure-2 IDT5V5201 SOIC8 Package Pin Assignment

2 PIN DESCRIPTION

Table-1 Pin Description

Name	Pin No.	I/O	Type	Description
Global Signal				
DR_EN	3	I Pull-down	LVTTTL	DR_EN: M-LVDS Driver Enable This pin controls the M-LVDS driver: high for enable and low for disable.
$\overline{\text{RE_EN}}$	2	I Pull-up	LVTTTL	$\overline{\text{RE_EN}}$: Type-1 M-LVDS Receiver and LVTTTL Driver Enable This pin controls the Type-1 M-LVDS receiver and LVTTTL driver: high for disable and low for enable. Note that the LVTTTL driver is in high impedance state when disabled.
LVTTTL Interface				
IN	4	I	LVTTTL	IN: LVTTTL Input An up to 166 MHz LVTTTL signal is input on this pin.
OUT	1	O	LVTTTL	OUT: LVTTTL Output This pin outputs an up to 166 MHz signal.
M-LVDS Interface				
M_A M_B	6 7	I/O	M-LVDS	M_A/M_B: Positive/Negative M-LVDS Data Bus Interface This pair of pins are connected to the M-LVDS data bus.
Power Supply and Ground				
VDD	8	Power	-	3.3 V Power Supply
GND	5	Ground	-	Ground

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATING AND RECOMMENDED OPERATION CONDITIONS

Table-2 Absolute Maximum Rating

Symbol	Parameter		Range
V_{DD}	Supply Voltage		-0.5 V to 4.1 V
V_{IN}	Input Voltage	$\overline{RE_EN}$, DR_EN, IN_A, IN_B	-0.5 V to 4.1 V
		M_A, M_B	-1.8 V to 4 V
V_{OUT}	Output Voltage	OUT_A, OUT_B	-0.3 V to 4 V
		M_A, M_B	-1.8 V to 4 V
	Electrostatic Discharge	Human Body Model M_A, M_B	± 8 kV
		All pins	± 2 kV
T_J	Junction Temperature	150°C	
T_S	Storage Temperature	-65°C to 165°C	

Table-3 Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power Supply	3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage	2		3.0	V
V_{IL}	Low Level Input Voltage	0		0.8	V
	Voltage at any Bus Terminal	-1.4		3.8	V
	Magnitude of Differential Input Voltage	0.05		3.0	V
T_A	Ambient Operating Temperature	-40		85	°C

3.2 LVTTTL DRIVER/RECEIVER CHARACTERISTICS

3.2.1 M-LVDS TO LVTTTL

Table-4 LVTTTL DC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IHL}	Input High Level		2.0		$V_{DD} + 0.3$	V
V_{ILL}	Input Low Level		-0.3		0.8	V
I_{ILL}	Input Leakage Current		-1.0		1.0	μA
V_{OHL}	Output High Voltage	Output Current = 17 mA, $V_{DD} = 3\text{ V}$	2.4			V
V_{OLL}	Output Low Voltage	Output Current = 12 mA, $V_{DD} = 3\text{ V}$			0.4	V

Table-5 LVTTTL AC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_r	Rise Time	$C_{load} = 15\text{ pF}$, 10% - 90%			1.2	ns
t_f	Fall Time	$C_{load} = 15\text{ pF}$, 10% - 90%			1.2	ns
f_{ML}	Frequency				166	MHz

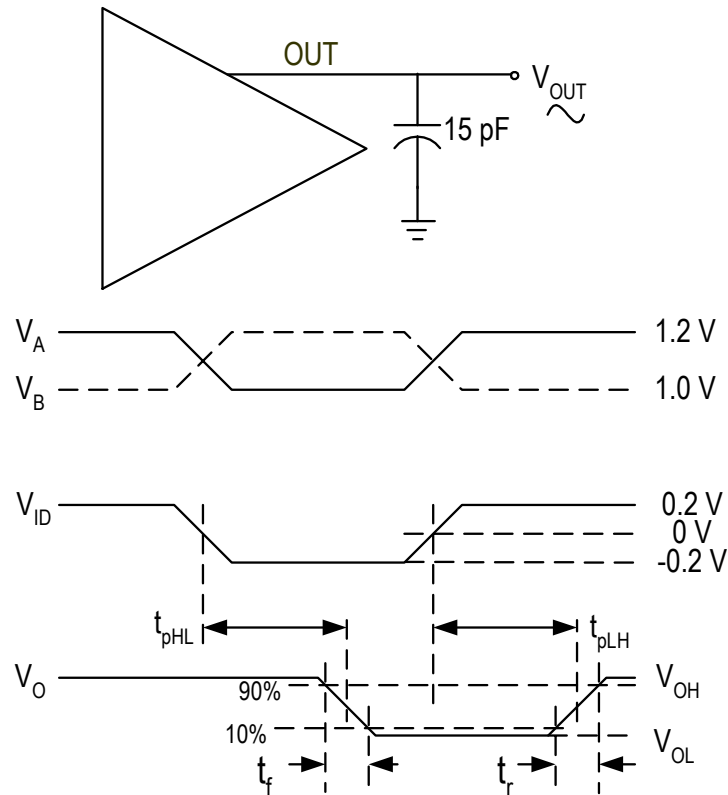


Figure-3 LVTTTL Output Test Circuit and Waveforms

3.3 M-LVDS DRIVER TYPE-1 RECEIVER CHARACTERISTICS

Table-6 M-LVDS Type-1 Receiver Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-mode Input Voltage	Receiver Output ⁽¹⁾
V _A	V _B			
2.400	0.000	2.400	1.200	High
0.000	2.400	-2.400	1.200	Low
3.425	3.375	0.050	3.4	High
3.375	3.425	-0.050	3.4	Low
-0.975	-1.025	0.050	-1	High
-1.025	-0.975	-0.050	-1	Low

¹: The receiver is enabled (The RE_EN pin is pulled low).

Table-7 M-LVDS DC Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{ODM}	Differential Output Voltage		480		650	mV
ΔV_{ODM}	Change in V_{ODM} for Complimentary Output States, $\Delta V_{ODM} = V_{ODM1} - V_{ODM0} $		-50		50	mV
V_{OSM}	Offset Voltage		0.8		1.2	V
ΔV_{OSM}	Change in V_{OSM} for Complimentary Output States		-50		50	mV
$V_{OSM(p-p)}$	Peak-to-peak Common-mode Output Voltage				150	mV
I_{OM}	Output Short Circuit Current				20	mA
I_{IZM}	High Impedance Input Current		-10		10	μ A
V_{THM}	Differential Input High Threshold	Type-1	50			mV
V_{TLM}	Differential Input Low Threshold	Type-1			-50	mV
V_{CMM}	Input Common-mode Range	$V_{INA} - V_{INB} = 200$ mV	-1		3.4	V
I_{INM}	Input Current	Input Voltage = 0 V to 2.4 V	-20		20	μ A

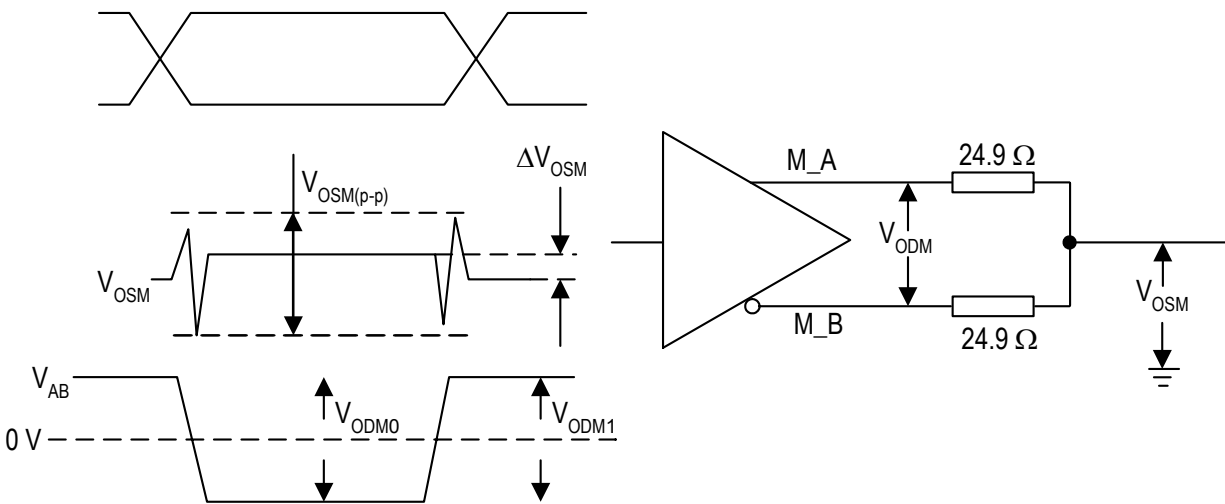


Figure-4 M-LVDS Driver Output Voltage Test Circuit

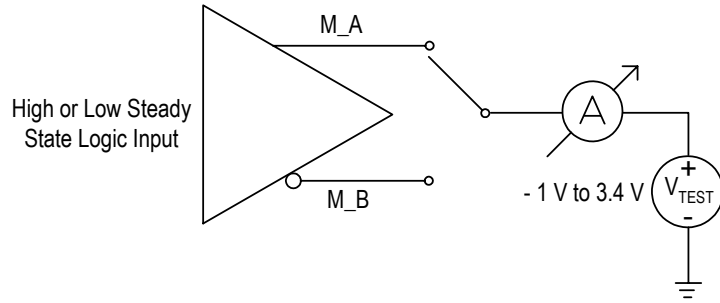


Figure-5 M-LVDS Driver Short-Circuit Test Circuit

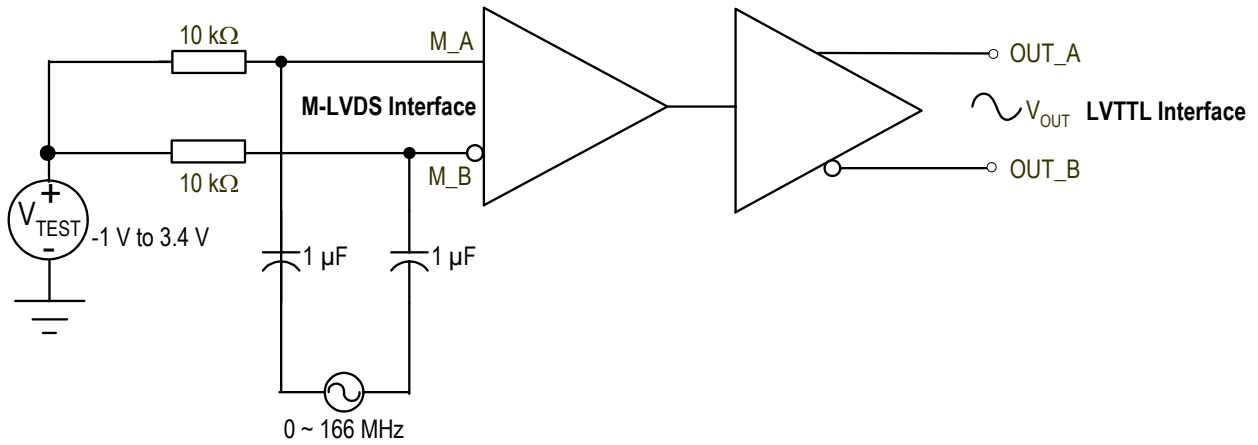


Figure-6 M-LVDS Type-1 Receiver Input Common-mode Range Test Circuit

Table-8 M-LVDS Input Current Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_A	Receiver or Transceiver with Driver Disabled Input Current	$V_A = 3.8 \text{ V}, V_B = 1.2 \text{ V}$	0		32	μA
		$V_A = 0 \text{ V or } 2.4 \text{ V}, V_B = 1.2 \text{ V}$	-20		20	
		$V_A = -1.4 \text{ V}, V_B = 1.2 \text{ V}$	-32		0	
I_B	Receiver or Transceiver with Driver Disabled Input Current	$V_B = 3.8 \text{ V}, V_A = 1.2 \text{ V}$	0		32	μA
		$V_B = 0 \text{ V or } 2.4 \text{ V}, V_A = 1.2 \text{ V}$	-20		20	
		$V_B = -1.4 \text{ V}, V_A = 1.2 \text{ V}$	-32		0	
I_{AB}	Receiver or Transceiver with Driver Differential Current ($I_A - I_B$)	$V_A = V_B, -1.4 \text{ V} < V_A < 3.8 \text{ V}$	-4		4	μA
$I_{A(\text{OFF})}$	Receiver or Transceiver Power-off Input Current	$V_A = 3.8 \text{ V}, V_B = 1.2 \text{ V}, 0 \text{ V} < V_{\text{DD}} < 1.5 \text{ V}$	0		32	μA
		$V_A = 0 \text{ or } 2.4 \text{ V}, V_B = 1.2 \text{ V}, 0 \text{ V} < V_{\text{DD}} < 1.5 \text{ V}$	-20		20	
		$V_A = -1.4 \text{ V}, V_B = 1.2 \text{ V}, 0 \text{ V} < V_{\text{DD}} < 1.5 \text{ V}$	-32		0	
$I_{B(\text{OFF})}$	Receiver or Transceiver Power-off Input Current	$V_B = 3.8 \text{ V}, V_A = 1.2 \text{ V}, 0 \text{ V} < V_{\text{DD}} < 1.5 \text{ V}$	0		32	μA
		$V_B = 0 \text{ or } 2.4 \text{ V}, V_A = 1.2 \text{ V}, 0 \text{ V} < V_{\text{DD}} < 1.5 \text{ V}$	-20		20	
		$V_B = -1.4 \text{ V}, V_A = 1.2 \text{ V}, 0 \text{ V} < V_{\text{DD}} < 1.5 \text{ V}$	-32		0	
$I_{AB(\text{OFF})}$	Receiver or Transceiver Power-off Differential Input Current ($I_A - I_B$)	$V_A = V_B, 0 \text{ V} < V_{\text{DD}} < 1.5 \text{ V}, -1.4 \text{ V} < V_A < 3.8 \text{ V}$	-4		4	μA
C_{AB}	Transceiver with driver disabled differential input capacitance	$V_{AB} = 0.4 \sin(30E6\pi t) \text{ V}$			4	pF

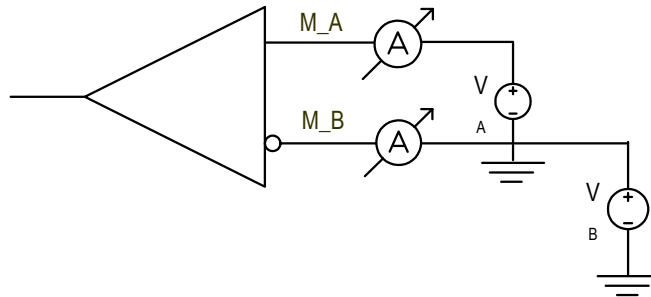


Figure-7 Various Input Currents Test Circuit

Table-9 M-LVDS AC Parameters

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
t_r	Rise Time	10% - 90%	0.8		1.5	ns
t_f	Fall Time	10% - 90%	0.8		1.5	ns
t_{TSL}	Differential Skew, $t_{TSL} = \{t_{TSL1}, t_{TSL2}\}$		-100		100	ps
f_{ML}	Frequency				166	MHz

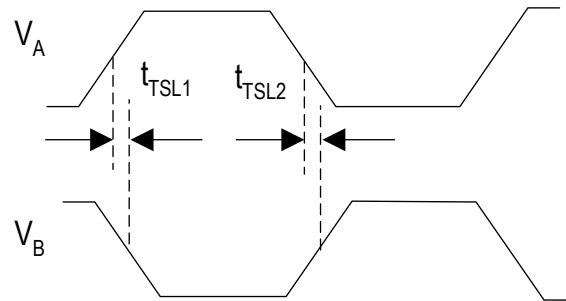


Figure-8 Differential Skew

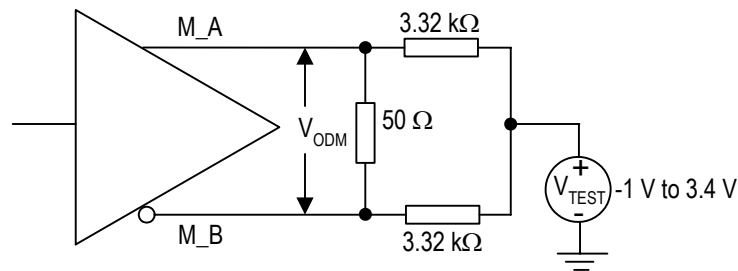


Figure-9 M-LVDS Output Voltage Test Circuit

Table-10 M-LVDS Type-1 Receiver AC Parameters

Output mode	Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
LVTTTL	t_{pLH}	Delay, Low to High Level	Input clock: freq = 50 MHz, Impedance = 150 Ω , Voltage = -200 mV - 200 mV. See Figure-3	2.5	5.5	6.5	ns
	t_{pHL}	Delay, High to Low Level		2.5	5.5	6.5	ns
	t_{sk} Type-1	Pulse Skew, $t_{sk} = t_{pLH} - t_{pHL} $			100	300	ps
	T_r (10% - 90%)	Rise Time		1		2.4	ns
	T_f (10% - 90%)	Fall Time		1		2.4	ns
	$T_{jit(per)}$	Period jitter, rms(1 standard deviation)			4	7	ps
		Output to Output Skew					200

Table-11 M-LVDS Driver AC Parameter

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
t_{pLH}	Delay, Low to High Level	Input clock: freq = 15 MHz, $T_r = T_f = 1.2$ ns, Impedance = 300 Ω , Voltage = 0 V - 3.3 V. See Figure-4	2.5	3.7	5.5	ns
t_{pHL}	Delay, High to Low Level		2.5	3.7	5.5	ns
T_{sk} LVTTTL input	Pulse Skew, $t_{sk} = t_{pLH} - t_{pHL} $			40	100	ps
T_r (10% - 90%)	Rise Time		0.7	1.1	1.5	ns
T_f (10% - 90%)	Fall Time		0.7	1.1	1.5	ns
$T_{jit(per)}$	Period jitter, rms(1 standard deviation)			2	3	ps
	Output to Output Skew					100

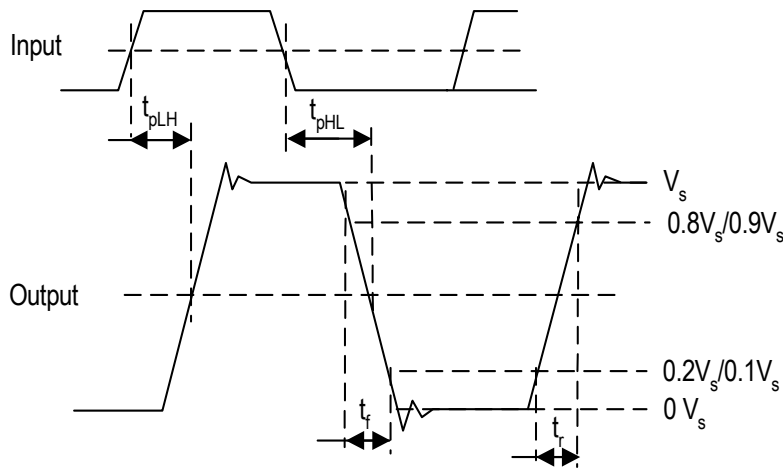
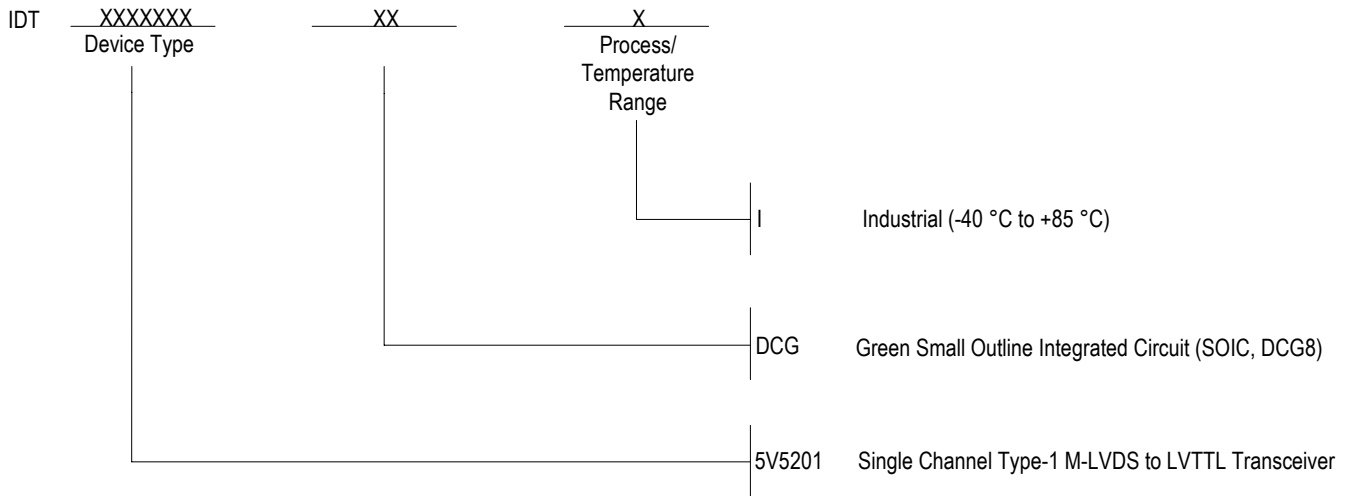


Figure-10 Timing and Voltage Definitions for the Output Signal

ORDERING INFORMATION

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
1-800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
408-360-1552
email:TELECOMhelp@idt.com

IDT and the IDT logo are trademarks of Integrated Device Technology, Inc.