

FEATURES

Voltage feedback

Wide output swing

18.4 V p-p differential, $R_{LOAD, DIFF} = 20 \Omega$ from 12 V supply

High output current

Linear output current of 450 mA peak

Low distortion

-65 dBc for Profile 8b @ 20.4 dBm

-55 dBc for Profile 17a @ 14.5 dBm

High speed

85 MHz bandwidth ($A_{V, DIFF} = 5$)

APPLICATIONS

ADSL2+/VDSL2 CO/CPE line drivers

PLC line drivers

Consumer xDSL modems

Twisted pair line drivers

FUNCTIONAL BLOCK DIAGRAM

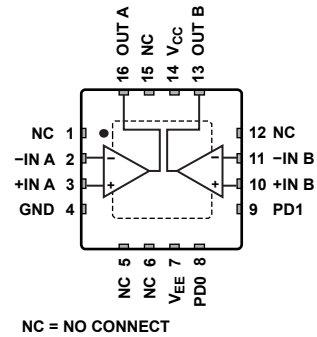


Figure 1. Thermally Enhanced, 4 mm × 4 mm, 16-Lead LFCSP_WQ

TYPICAL APPLICATION DIAGRAM

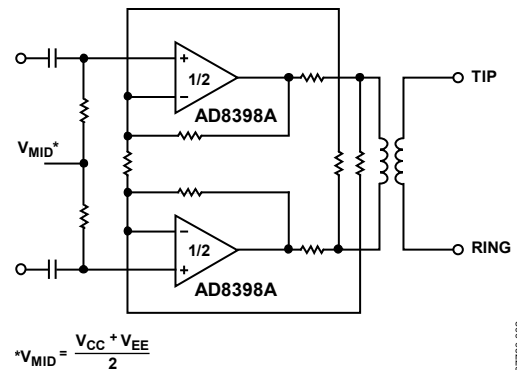


Figure 2. Typical VDSL2 Application

GENERAL DESCRIPTION

The AD8398A comprises two high speed, voltage feedback operational amplifiers. When configured as a differential line driver, the AD8398A is an ideal choice for ADSL2+, VDSL2, and power line communications (PLC) applications. It has high output current, high bandwidth, and fast slew rate, combined with exceptional multitone power ratio (MTPR) and common-mode stability. The AD8398A is available in a thermally enhanced 4 mm × 4 mm, 16-lead LFCSP.

The AD8398A incorporates power management functionality via two CMOS-compatible control pins, PD0 and PD1. These pins select one of four operating modes: full power, medium power, low power, or complete power-down. In the power-down mode, the quiescent current drops to 0.7 mA.

The AD8398A operates in the industrial temperature range of -40°C to +85°C.

Rev. D

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TABLE OF CONTENTS

| | | | |
|---|---|---|----|
| Features | 1 | Typical Performance Characteristics | 6 |
| Applications | 1 | Applications Information | 8 |
| Functional Block Diagram | 1 | Power Control Modes of Operation | 8 |
| Typical Application Diagram | 1 | Exposed Thermal Pad Connections | 8 |
| General Description | 1 | Power Supply Bypassing | 8 |
| Revision History | 2 | Board Layout | 8 |
| Specifications | 3 | Multitone Power Ratio | 9 |
| Absolute Maximum Ratings | 4 | Lightning and AC Power Fault | 9 |
| Thermal Resistance | 4 | Outline Dimensions | 10 |
| Maximum Power Dissipation | 4 | Ordering Guide | 10 |
| ESD Caution | 4 | | |
| Pin Configuration and Function Descriptions | 5 | | |

REVISION HISTORY**9/10—Rev. C to Rev. D**

| | |
|---|---|
| Change to General Description Section | 1 |
|---|---|

3/10—Rev. B to Rev. C

| | |
|----------------------------|---|
| Changes to Figure 14 | 9 |
|----------------------------|---|

12/09—Rev. A to Rev. B

| | |
|--|---|
| Changes to Figure 13, Figure 14, and Figure 15 | 9 |
|--|---|

10/09—Rev. Sp0 to Rev. A

| | |
|--|---|
| Changed R_{LOAD} to $R_{LOAD, Diff}$ Throughout | 1 |
| Changes to DC Performance, Differential Input Offset Voltage Parameter, Table 1 | 3 |
| Changes to Figure 4 | 5 |
| Changes to Figure 8 and Figure 9 | 6 |
| Changes to Exposed Thermal Pad Connections Section | 8 |

11/08—Revision Sp0: Initial Version

SPECIFICATIONS

$V_S = 12\text{ V}$, $\pm 6\text{ V}$ at $T_A = 25^\circ\text{C}$, $A_{V\text{DIFF}} = 5$, $R_{\text{LOAD,DIFF}} = 20\ \Omega$, $\text{PD1} = 0$, $\text{PD0} = 0$, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|--|------|-----------|------|------------------------------|
| DYNAMIC PERFORMANCE | | | | | |
| –3 dB Bandwidth | $A_{V\text{DIFF}} = 5$, $V_{\text{OUT}} = 2\text{ V}$ peak, measured differentially | | | | |
| | $\text{PD1} = 0$, $\text{PD0} = 0$ | | 85 | | MHz |
| | $\text{PD1} = 0$, $\text{PD0} = 1$ | | 85 | | MHz |
| Slew Rate | $\text{PD1} = 1$, $\text{PD0} = 0$ | | 75 | | MHz |
| | $V_{\text{OUT}} = 4\text{ V}$ peak, measured differentially | | 600 | | $\text{V}/\mu\text{s}$ |
| NOISE/DISTORTION PERFORMANCE | | | | | |
| MTPR | Profile 8b at 20.4 dBm in VDSL2 application | | –65 | | dBc |
| | Profile 17a at 14.5 dBm in VDSL2 application | | –55 | | dBc |
| Off Isolation | $\text{PD1} = 1$, $\text{PD0} = 1$ | | –80 | | dBc |
| Input Voltage Noise | $f = 100\text{ kHz}$ | | 4.8 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| Input Current Noise | $f = 100\text{ kHz}$ | | 0.9 | | $\text{pA}/\sqrt{\text{Hz}}$ |
| Differential Output Voltage Noise | $f = 100\text{ kHz}$ in VDSL2 application | | 120 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| DC PERFORMANCE | | | | | |
| Differential Input Offset Voltage | | –2 | ± 0.1 | +2 | mV |
| Input Offset Voltage | | | 16 | 55 | mV |
| Input Bias Current | | | 0.5 | 1 | μA |
| Open-Loop Gain | | | 63 | | dB |
| Common-Mode Rejection | Measured differentially | | –100 | –74 | dB |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | $f < 100\text{ kHz}$ | | 1.9 | | $\text{M}\Omega$ |
| OUTPUT CHARACTERISTICS | | | | | |
| Differential Swing | | 17.6 | 18.4 | | V p-p |
| Linear Peak Output Current | VDSL2 at 20.4 dBm, MTPR = –65 dBc | | 450 | | mA peak |
| POWER SUPPLY | | | | | |
| Operating Range | Dual supply | | ± 6 | | V |
| | Single supply | | 12 | | V |
| Supply Current | $\text{PD1} = 0$, $\text{PD0} = 0$ | 29 | 33.2 | 37 | mA |
| | $\text{PD1} = 0$, $\text{PD0} = 1$ | 20 | 22.9 | 25.5 | mA |
| | $\text{PD1} = 1$, $\text{PD0} = 0$ | 12 | 13.3 | 14.5 | mA |
| | $\text{PD1} = 1$, $\text{PD0} = 1$ | | 0.7 | 1.1 | mA |
| Power Supply Rejection | Measured differentially | | –94 | –74 | dB |
| POWER-DOWN PINS | | | | | |
| PD1 , PD0 V_{IL} | Referenced to GND | | 0.8 | | V |
| PD1 , PD0 V_{IH} | Referenced to GND | | 2 | | V |
| PD1 , PD0 Bias Current | PD1 , $\text{PD0} = 0\text{ V}$ | | 15 | 30 | μA |
| | PD1 , $\text{PD0} = 3\text{ V}$ | | 6 | 17 | μA |
| Enable Time | PD1 , $\text{PD0} = (1, 1) - (0, 0)$ | | 60 | | μs |
| Disable Time | PD1 , $\text{PD0} = (0, 0) - (1, 1)$ | | 600 | | μs |

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|--------------------------------------|--------------------------------|
| Power Supplies ($V_{CC} - V_{EE}$) | 13.2 V |
| Power Dissipation | $(T_{JMAX} - T_A)/\theta_{JA}$ |
| Storage Temperature Range | -65°C to +125°C |
| Operating Temperature Range | -40°C to +85°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified with the device soldered on a JEDEC circuit board and the thermal pad connected to the GND plane layer using six vias.

Table 3. Thermal Resistance

| Package Type | θ_{JA} | Unit |
|------------------|---------------|------|
| 16-Lead LFCSP_WQ | 35.6 | °C/W |

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8398A is limited by its junction temperature (T_J) on the die. The maximum safe T_J of plastic encapsulated devices, as determined by the glass transition temperature of the plastic, is 150°C. Temporarily exceeding this limit may cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding this limit for an extended period can result in device failure.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 16-lead LFCSP_WQ on a 4-layer board with six vias connecting the exposed pad to the GND plane layer.

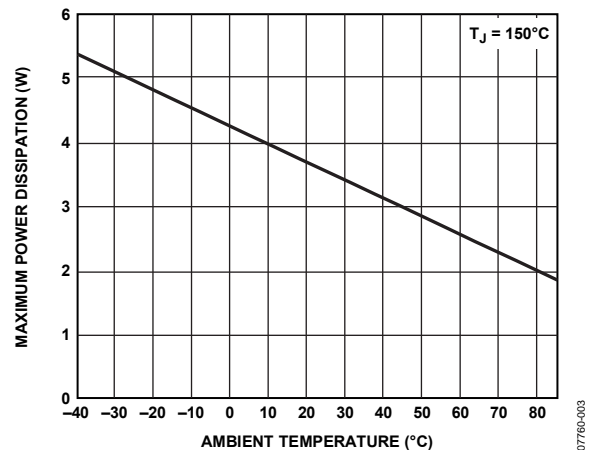


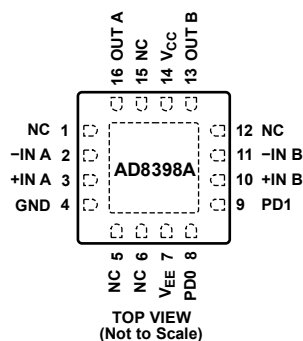
Figure 3. Maximum Safe Power Dissipation vs. Ambient Temperature, 4-Layer JEDEC Board with Six Thermal Vias

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NC = NO CONNECT
2. EXPOSED PADDLE (EPAD) IS FLOATING, NOT ELECTRICALLY CONNECTED INTERNALLY.

07766-004

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|-----------------|-----------------------|--|
| 1, 5, 6, 12, 15 | NC | No Connect. |
| 2 | -IN A | Amplifier A Inverting Input. |
| 3 | +IN A | Amplifier A Noninverting Input. |
| 4 | GND | Ground. |
| 7 | V_{EE} | Negative Power Supply Input. |
| 8 | PDO | Power Mode Control. |
| 9 | PD1 | Power Mode Control. |
| 10 | +IN B | Amplifier B Noninverting Input. |
| 11 | -IN B | Amplifier B Inverting Input. |
| 13 | OUT B | Amplifier B Output. |
| 14 | V_{CC} | Positive Power Supply Input. |
| 16 | OUT A | Amplifier A Output. |
| EPAD | Exposed Paddle (EPAD) | The exposed paddle is electrically isolated. |

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 6\text{ V}$, $V_{EE} = -6\text{ V}$, unless otherwise stated.

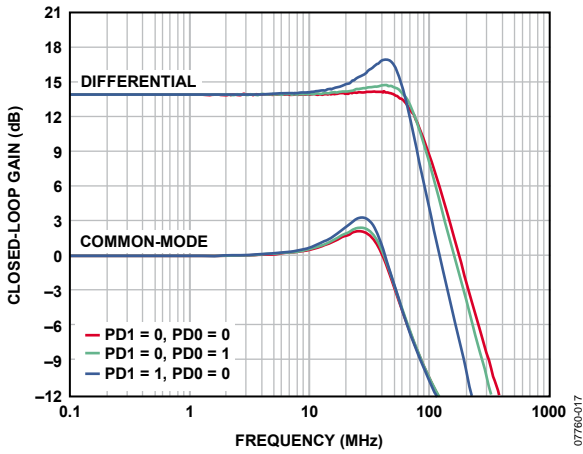
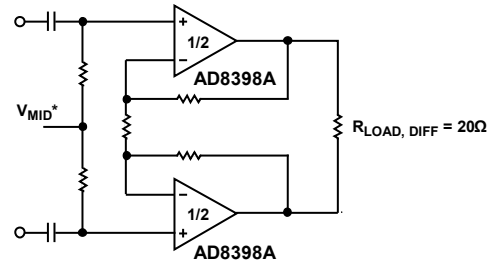


Figure 5. Small Signal Differential and Common-Mode Frequency Response; $A_{V,DIFF} = 5$ (See the Application Circuit in Figure 8)



$$V_{MID} = \frac{V_{CC} + V_{EE}}{2}$$

Figure 8. Typical Differential Application Circuit
 $R_{LOAD,DIFF} = 20\ \Omega$

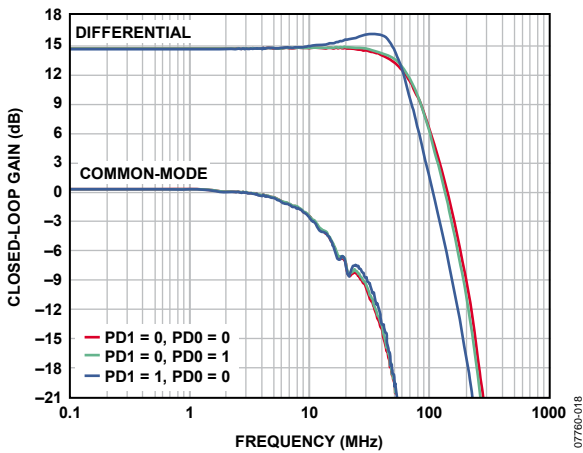
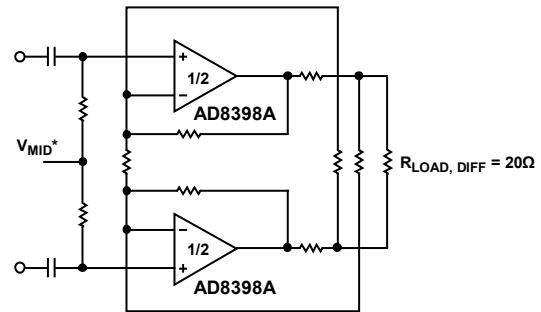


Figure 6. Small Signal Differential and Common-Mode Frequency Response (See the Application Circuit in Figure 9)



$$V_{MID} = \frac{V_{CC} + V_{EE}}{2}$$

Figure 9. Typical Differential Application Circuit with Positive Feedback
 $R_{LOAD,DIFF} = 20\ \Omega$

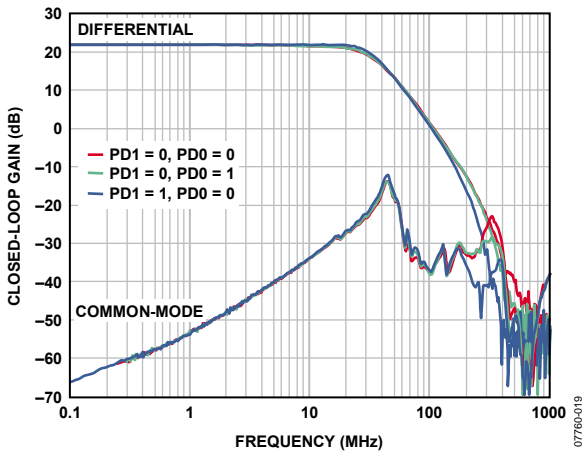
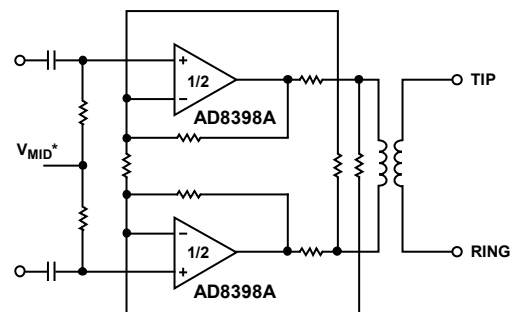


Figure 7. Small Signal Differential and Common-Mode Frequency Response (See the Application Circuit in Figure 10)



$$V_{MID} = \frac{V_{CC} + V_{EE}}{2}$$

Figure 10. Typical VDSL2 Application Circuit

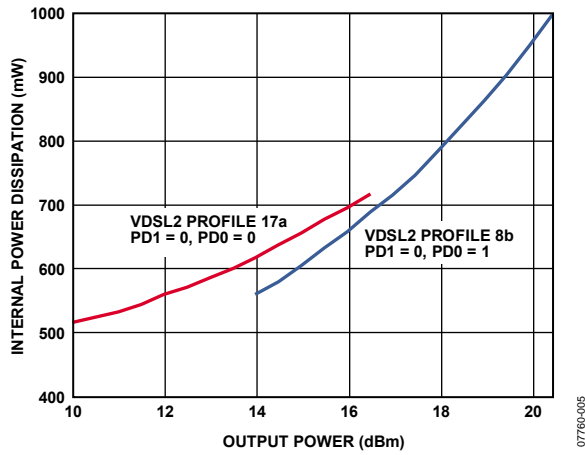


Figure 11. Internal Power Dissipation vs. Output Power

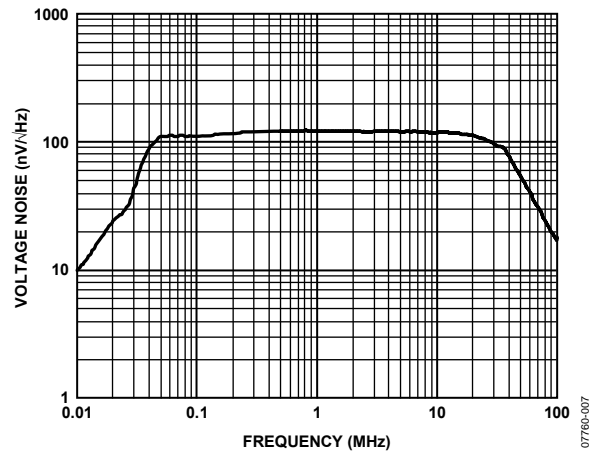


Figure 12. Differential Output Voltage Noise vs. Frequency in a Typical VDSL2 Application

APPLICATIONS INFORMATION

POWER CONTROL MODES OF OPERATION

The AD8398A features four power modes: full power, medium power, low power, and complete power-down. Two CMOS-compatible logic pins (PD0 and PD1) select the power mode. The power modes and associated logic states are listed in Table 5.

Table 5. Power Modes

| PD1 | PD0 | Power Mode | Total Supply Current (mA) |
|-----|-----|--------------|---------------------------|
| 0 | 0 | Full power | 33.2 |
| 0 | 1 | Medium power | 22.9 |
| 1 | 0 | Low power | 13.3 |
| 1 | 1 | Power-down | 0.7 |

EXPOSED THERMAL PAD CONNECTIONS

To ensure adequate heat transfer away from the die, connect the exposed thermal pad to a solid plane layer with low thermal resistance. To maximize the operating life of the AD8398A, the thermal design of the system should be kept below the junction temperature of 125°C.

Although it is electrically isolated, the thermal pad typically connects to the ground plane layer.

POWER SUPPLY BYPASSING

The AD8398A typically operates on ± 6 V or +12 V supplies. Power the AD8398A circuit with a well-regulated, properly decoupled power supply. To minimize supply voltage ripple and power dissipation, use high quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs). Place a decoupling 0.1 μ F MLCC no more than $\frac{1}{8}$ inch away from each of the power supply pins. In addition, a 10 μ F tantalum capacitor is recommended to provide good decoupling for lower frequency signals and to supply current for fast, large signal changes at the AD8398A outputs. Lay out bypass capacitors to keep return currents away from the inputs of the amplifiers. This layout minimizes any voltage drops that can develop due to ground currents flowing through the ground plane.

BOARD LAYOUT

As is the case with all high speed applications, careful attention to printed circuit board (PCB) layout details prevents associated board parasitics from becoming problematic. Proper RF design technique is mandatory.

The PCB has a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane on all layers from the area near the input and output pins of the AD8398A reduces stray capacitance.

Signal lines connecting the feedback and gain resistors should be as short as possible to minimize the inductance and stray capacitance associated with these traces. Place termination resistors and loads as close as possible to their respective inputs and outputs.

To minimize coupling (crosstalk) through the board, keep input and output traces as far apart as possible. Wherever there are complementary signals, provide a symmetrical layout to maximize balanced performance.

MULTITONE POWER RATIO

The discrete multitone (DMT) signal used in xDSL systems carries data in discrete tones or bins that appear in the frequency domain in evenly spaced 4.3125 kHz intervals. In applications using this type of waveform, multitone power ratio (MTPR) is a commonly used measure of linearity. Generally, designers are concerned with two types of MTPR: in band and out of band. In-band MTPR is defined as the measured difference from the peak of one tone that is loaded with data to the peak of an adjacent tone that is intentionally left empty. Out-of-band MTPR is defined as the spurious emissions that occur in the receive bands. Transmit band power and receive band MTPR are shown in Figure 13, Figure 14, and Figure 15 for Profile 17a, Profile 8b, and ADSL2+, respectively.

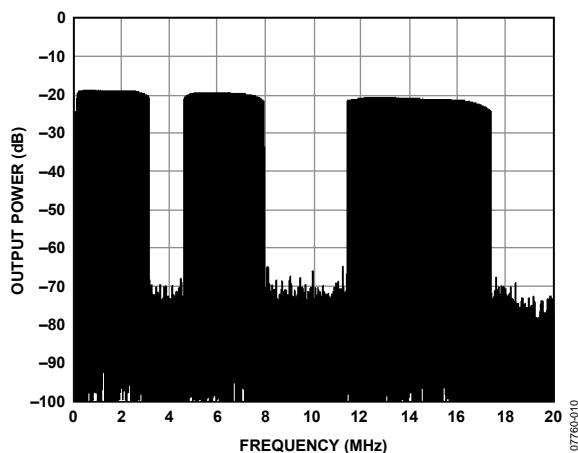


Figure 13. MTPR of a Typical VDSL2 Profile 17a DMT Test Signal, $V_S = \pm 6 V$, Output Power = 14.5 dBm

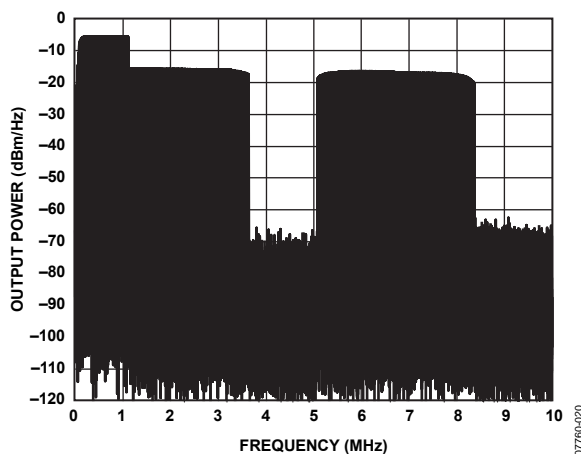


Figure 14. MTPR of a Typical VDSL2 Profile 8b DMT Test Signal, $V_S = \pm 6 V$, Output Power = 20.4 dBm

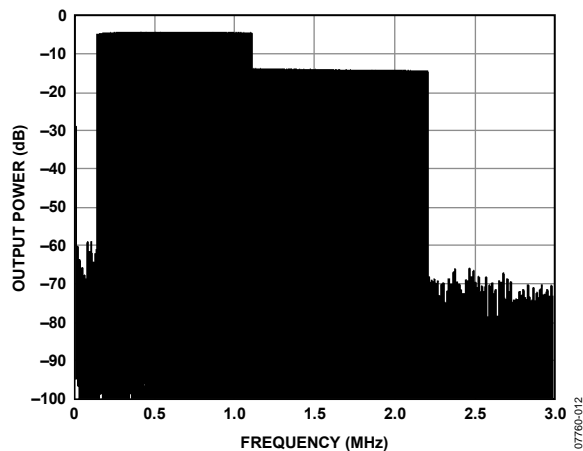
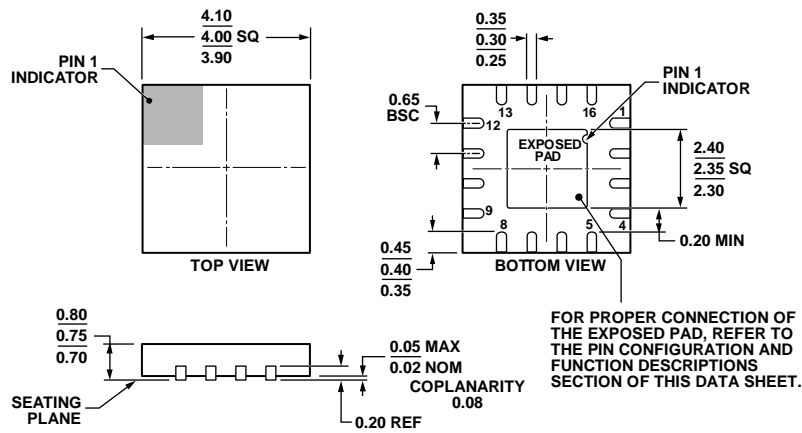


Figure 15. MTPR of a Typical ADSL2+ DMT Test Signal, $V_S = \pm 6 V$, Output Power = 20.4 dBm

LIGHTNING AND AC POWER FAULT

DSL line drivers are transformer-coupled to the twisted pair telephone line. In this environment, the AD8398A may be subject to large line transients resulting from events such as lightning strikes or downed power lines. Additional circuitry is required to protect the AD8398A from possible damage due to these events.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD

Figure 16. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
 4 mm × 4 mm Body, Very Very Thin Quad
 (CP-16-20)
 Dimensions shown in millimeters

101408-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|--|----------------|
| AD8398AAPZ-R2 | -40°C to +85°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-20 |
| AD8398AAPZ-R7 | -40°C to +85°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-20 |
| AD8398AAPZ-RL | -40°C to +85°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-20 |

¹ Z = RoHS Compliant Part.

NOTES

AD8398A

NOTES