

FIN1532 5V LVDS 4-Bit High Speed Differential Receiver

General Description

This quad receiver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100 mV, to LVTTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1532 can be paired with its companion driver, the FIN1531, or any other LVDS driver.

Features

- Greater than 400Mbps data rate
- 5V power supply operation
- 0.5 ns maximum differential pulse skew
- 3 ns maximum propagation delay
- Low power dissipation
- Power-Off protection for inputs and outputs
- Fail safe protection for open-circuit, shorted and terminated receiver inputs
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Pin compatible with equivalent RS-422 and PECL devices
- 16-Lead SOIC and TSSOP packages save space

Ordering Code:

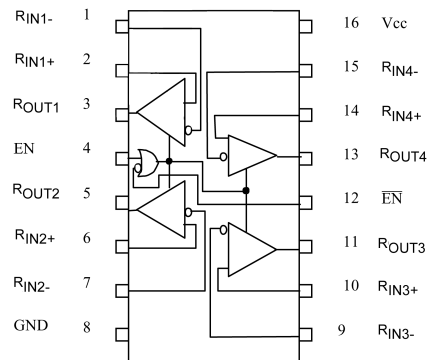
| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| FIN1532M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| FIN1532MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Pin Descriptions

| Pin Name | Description |
|---|-----------------------------|
| R _{OUT1} , R _{OUT2} , R _{OUT3} , R _{OUT4} | LVTTTL Data Outputs |
| R _{IN1+} , R _{IN2+} , R _{IN3+} , R _{IN4+} | Non-inverting LVDS Inputs |
| R _{IN1-} , R _{IN2-} , R _{IN3-} , R _{IN4-} | Inverting LVDS Inputs |
| EN | Driver Enable Pin |
| $\overline{\text{EN}}$ | Inverting Driver Enable Pin |
| V _{CC} | Power Supply |
| GND | Ground |

Connection Diagram



Top View

Function Table

| Input | | | Outputs | |
|-------|------------------------|---------------------|------------------|------------------|
| EN | $\overline{\text{EN}}$ | R _{IN+} | R _{IN-} | R _{OUT} |
| H | X | H | L | H |
| H | X | L | H | L |
| H | X | Fail Safe Condition | | H |
| X | L | H | L | H |
| X | L | L | H | L |
| X | L | Fail Safe Condition | | H |
| L | H | X | | Z |

H = HIGH Logic Level L = LOW Logic Level X = Don't Care
Z = High Impedance Fail Safe = Open, Shorted, Terminated

Absolute Maximum Ratings (Note 1)

| | |
|---|-----------------|
| Supply Voltage (V_{CC}) | -0.5 V to +6 V |
| DC Input Voltage (V_{IN}) | |
| Enable Inputs | -0.5 V to +6 V |
| Receiver Inputs | -0.5 V to +6 V |
| DC Output Voltage (V_{OUT}) | -0.5 V to +6 V |
| DC Output Current (I_O) | 16 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |
| Max Junction Temperature (T_J) | 150°C |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |
| ESD (Human Body Model) | ≥ 8000 V |
| ESD (Machine Model) | ≥ 300 V |

Recommended Operating Conditions

| | |
|--|--------------------------------------|
| Supply Voltage (V_{CC}) | 4.5 V to 5.5 V |
| Input Voltage (V_{IN}) | |
| Enable Inputs | 0 to V_{CC} |
| Receiver Inputs | 0 to 2.4 V |
| Magnitude of Differential Voltage ($ V_{ID} $) | 100 mV to 600 mV |
| Common-mode Input Voltage (V_{IC}) | $ V_{ID} /2$ to $(2.4 - V_{ID})/2$ |
| Operating Temperature (T_A) | -40°C to +85°C |

Note 1: The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ (Note 2) | Max | Units |
|--------------|--|--|----------------|--------------|----------|-------|
| V_{TH} | Differential Input Threshold HIGH | $V_{IC} = +1.2V$, See Figure 1 | | | 100 | mV |
| V_{TL} | Differential Input Threshold LOW | $V_{IC} = +1.2V$, See Figure 1 | -100 | | | mV |
| I_{IN} | Input Current EN or \overline{EN} | $V_{IN} = 0V$ or V_{CC} , $V_{CC} = 5.5$ or $0V$ | | | ±20 | μA |
| | Input Current Receiver Inputs | $V_{IN} = 0V$ or 2.4 V, $V_{CC} = 5.5$ or $0V$ | | | ±20 | μA |
| V_{IH} | Input High Voltage (EN or \overline{EN}) | | 2.0 | | V_{CC} | V |
| V_{IL} | Input Low Voltage (EN or \overline{EN}) | | GND | | 0.8 | V |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -100 \mu A$ | $V_{CC} - 0.2$ | 4.98 | | V |
| | | $I_{OH} = -8 \text{ mA}$ | 3.8 | 4.68 | | |
| V_{OL} | Output LOW Voltage | $I_{OH} = 100 \mu A$ | | 0.01 | 0.2 | V |
| | | $I_{OL} = 8 \text{ mA}$ | | 0.22 | 0.5 | |
| V_{IK} | Input Clamp Voltage | $I_{IK} = -18 \text{ mA}$ | -1.5 | -0.8 | | V |
| I_{OZ} | Disabled Output Leakage Current | EN = 0.8 and $\overline{EN} = 2V$, $V_{OUT} = 5.5V$ or $0V$ | | | ±20 | μA |
| $I_{O(OFF)}$ | Power-OFF Output Current | $V_{OUT} = 0V$ or 5.5V, $V_{CC} = 0V$ | | | 50 | μA |
| I_{OS} | Output Short Circuit Test | Receiver Enabled, $V_{OUT} = 0V$ (one output shorted at a time) | -15 | | -100 | mA |
| I_{CCZ} | Disabled Power Supply Current | Receiver Disabled | | 1.2 | 5 | mA |
| I_{CC} | Power Supply Current | Receiver Enabled, $R_{IN+} = 1V$ and $R_{IN-} = 1.4V$ | | 11 | 17 | mA |
| | | Receiver Enabled, $R_{IN+} = 1.4V$ and $R_{IN-} = 1V$ | | 15 | 23 | |
| $I_{PU/PD}$ | Output Power Up/Power Down High Z Leakage Current | $V_{CC} = 0V$ to 2.0V | | | ±20 | μA |
| C_{IN} | Input Capacitance | | | 5.5 | | pF |
| C_{OUT} | Output Capacitance | | | 4.5 | | pF |

Note 2: All typical values are at $T_A = 25^\circ\text{C}$ and with $V_{CC} = 5V$.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

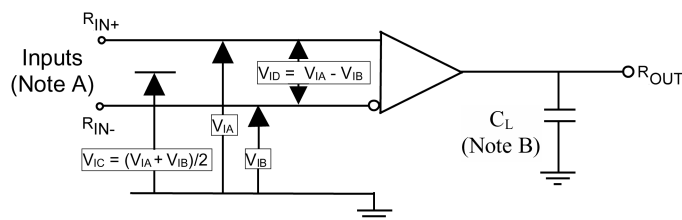
| Symbol | Parameter | Test Conditions | Min | Typ (Note 3) | Max | Units | |
|--------------|--|--|-----|--------------|------|-------|----|
| t_{PLH} | Propagation Delay LOW-to-HIGH | $ V_{ID} = 400 \text{ mV}$, $C_L = 10 \text{ pF}$, $R_L = 1 \text{ k}\Omega$ See Figure 1 and Figure 2 | 1.0 | 2.0 | 3.0 | ns | |
| t_{PHL} | Propagation Delay HIGH-to-LOW | | 1.0 | 2.0 | 3.0 | ns | |
| t_{TLH} | Output Rise Time (20% to 80%) | | | 1.3 | | ns | |
| t_{THL} | Output Fall Time (80% to 20%) | | | 1.1 | | ns | |
| $t_{SK(P)}$ | Pulse Skew $ t_{PLH} - t_{PHL} $ | | | | 0.2 | 0.5 | ns |
| $t_{SK(LH)}$ | Channel-to-Channel Skew (Note 4) | | | | 0.1 | 0.3 | ns |
| $t_{SK(HL)}$ | Channel-to-Channel Skew (Note 4) | | | | | | ns |
| $t_{SK(PP)}$ | Part-to-Part Skew (Note 5) | | | | 1.0 | ns | |
| f_{MAX} | Maximum Operating Frequency (Note 6) | $R_L = 1 \text{ k}\Omega$, $C_L = 10 \text{ pF}$, See Figure 1 and Figure 2 | 200 | 260 | | MHz | |
| t_{ZH} | LVTTL Output Enable Time from Z to HIGH | $R_L = 1 \text{ k}\Omega$, $C_L = 10 \text{ pF}$, See Figure 3 and Figure 4 | | 8 | 12.0 | ns | |
| t_{ZL} | LVTTL Output Enable Time from Z to LOW | | | 8 | 12.0 | ns | |
| t_{HZ} | LVTTL Output Disable Time from HIGH to Z | | | 4 | 8.0 | ns | |
| t_{LZ} | LVTTL Output Disable Time from LOW to Z | | | 4 | 8.0 | ns | |

Note 3: All typical values are at $T_A = 25^\circ\text{C}$ and with $V_{CC} = 5\text{V}$.

Note 4: $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

Note 5: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

Note 6: f_{MAX} Criteria: Input $t_R = t_F < 1 \text{ ns}$, $V_{ID} = 300 \text{ mV}$, (1.05V to 1.35V pp), 50% duty cycle; Output duty cycle 40% to 60%, $V_{OL} < 0.5\text{V}$, $V_{OH} > 2.4\text{V}$. All channels switching in phase.



Note A: All input pulses have frequency = 10 MHz, t_R or $t_F = 1 \text{ ns}$

Note B: C_L includes all probe and jig capacitances

FIGURE 1. Differential Receiver Voltage Definitions and Propagation Delay

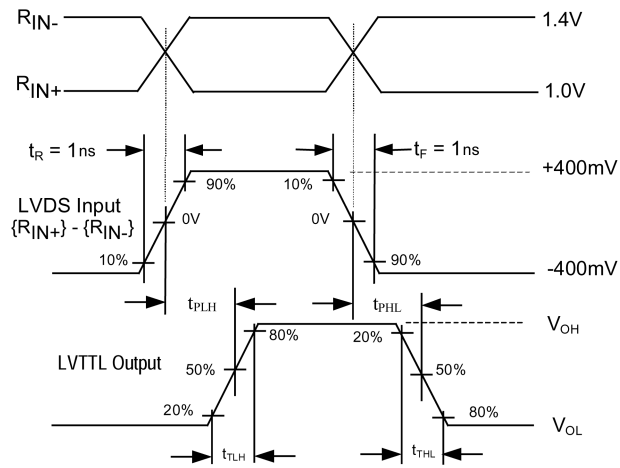


FIGURE 2. LVDS Input to LVTTTL Output AC Waveforms

Test Circuit for LVTTTL Outputs

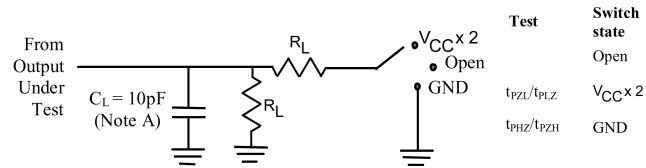
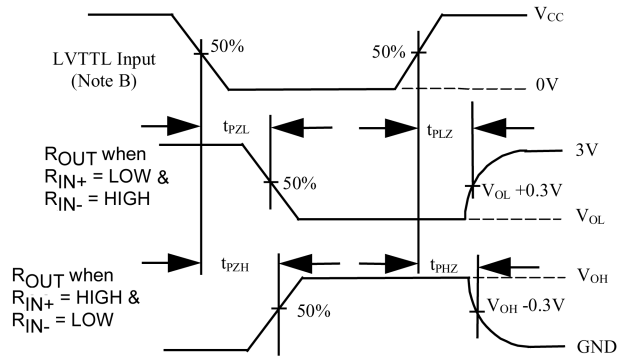


FIGURE 3. AC Loading Circuit for LVTTTL Outputs

Voltage Waveforms Enable and Disable Times

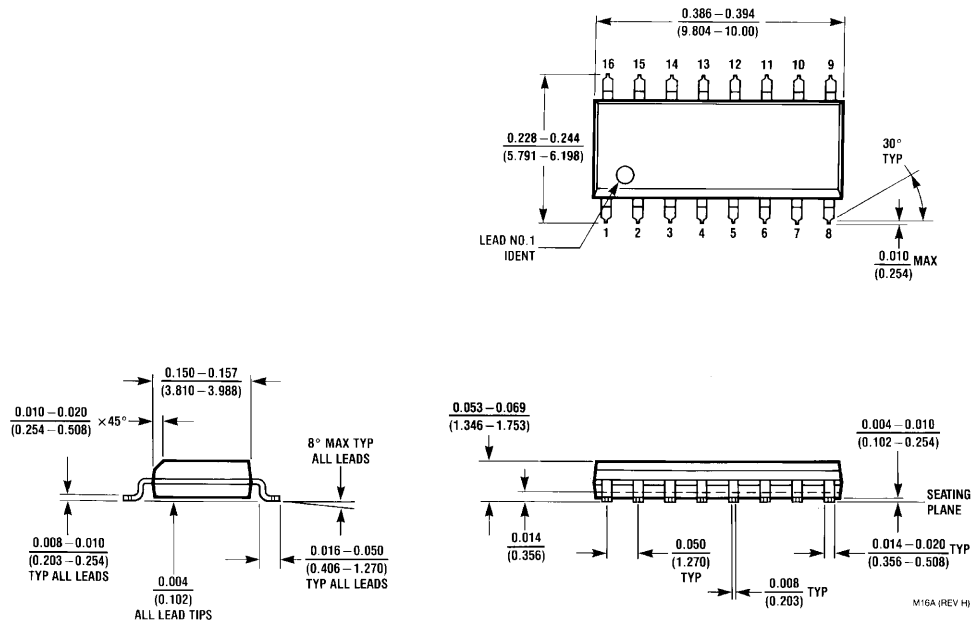


Note A: C_L includes probes and jig capacitance

Note B: All LVTTTL input pulses have the following characteristics: Frequency = 10 MHz, t_R or t_F = 2 ns

FIGURE 4. LVTTTL Outputs Test Circuit and AC Waveforms

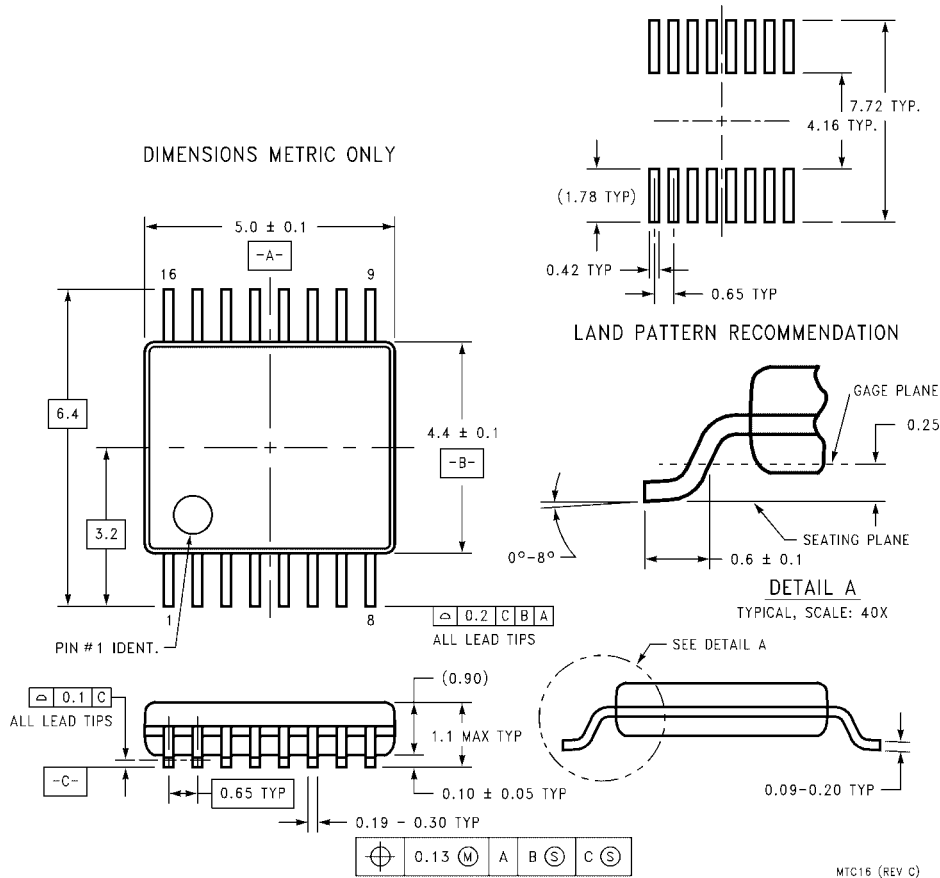
Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

M16A (REV H)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

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