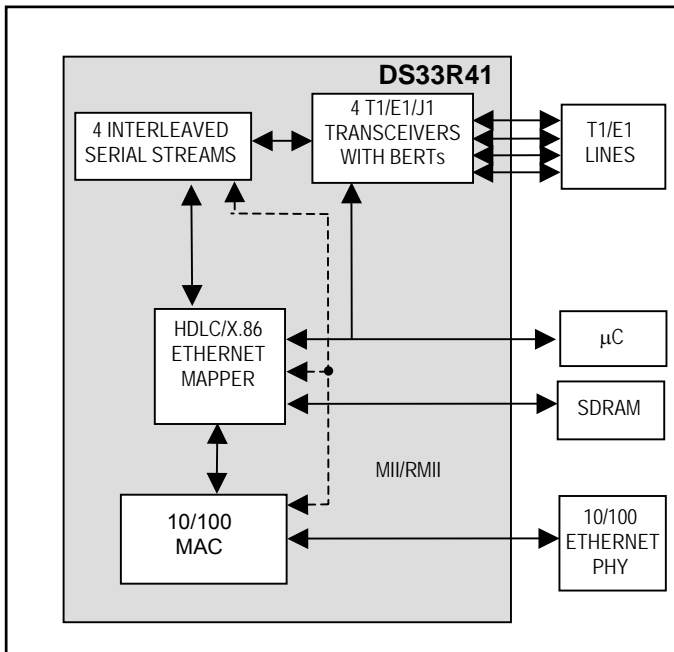


GENERAL DESCRIPTION

The DS33R41 extends a 10/100 Ethernet LAN segment by encapsulating MAC frames in HDLC or X.86 (LAPS) for transmission over four interleaved T1/E1/J1 lines using a robust, balanced, and programmable inverse multiplexing. Four integrated T1/E1/J1 transceivers provide framing and line interfacing functionality.

The device performs store-and-forward of packets with full wire-speed transport capability. The built-in committed information rate (CIR) controller provides fractional bandwidth allocation up to the line rate in increments of 512kbps.

FUNCTIONAL DIAGRAM



FEATURES

- 10/100 IEEE 802.3 Ethernet MAC (MII and RMII) Half/Full Duplex with Automatic Flow Control
- Layer 1 Inverse Multiplexing Over Four T1/E1/J1 Lines Through the Integrated Framers and LIUs
- Supports Up to 7.75ms Differential Delay
- Aggregate Bandwidth from Up to Four T1/E1/J1 Links
- T1/E1 Signaling Capability for OAM
- HDLC/LAPS Encapsulation with Programmable FCS, Interframe Fill
- CIR Controller Provides Fractional Allocations in 512kbps Increments
- Programmable BERTs
- External 16MB, 100MHz SDRAM Buffering
- Parallel Microprocessor Interface
- 1.8V, 3.3V Power Supplies
- IEEE 1149.1 JTAG Support

Features continued on page 11.

APPLICATIONS

Bonded Transparent LAN Service
 LAN Extension
 Ethernet Delivery Over T1/E1/J1

ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|---------|----------------|-------------|
| DS33R41 | -40°C to +85°C | 400 BGA |

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.

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1 DESCRIPTION

The DS33R41 provides interconnection and mapping functionality between Ethernet packet systems and T1/E1/J1 WAN time-division multiplexed (TDM) systems. The device is composed of a 10/100 Ethernet MAC, packet arbiter, committed information rate controller (CIR), HDLC/X.86 (LAPS) mapper, SDRAM interface, control ports, four bit error-rate testers (BERTs), and four integrated T1/E1/J1 transceivers. The packet interface consists of an MII/RMII Ethernet PHY interface. The Ethernet interface can be configured for 10Mbps or 100Mbps service. The DS33R41 encapsulates Ethernet traffic with HDLC or X.86 (LAPS) encoding to be transmitted over up to four T1, E1, or J1 lines. The T1/E1/J1 interfaces also receive encapsulated Ethernet packets and transmit the extracted packets over the Ethernet ports. Access is provided between the serial port and the integrated T1/E1/J1 transceivers to the intermediate signal bus that is based on the Dallas Semiconductor integrated bus operation (IBO), running at 8.192Mbps.

The device includes four software-selectable T1, E1, or J1 transceivers for short-haul and long-haul applications. Each transceiver is composed of a line interface unit (LIU), framer, and two additional HDLC controllers. The transceivers are software compatible with the popular DS2155 and DS21455.

The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0dB to 43dB or 0dB to 12dB for E1 applications and 0dB to 15dB or 0dB to 36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications) and can be placed in either transmit or receive data paths. An additional feature of the LIU is a CMI coder/decoder for interfacing to optical networks.

On the transmit side, clock/data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns and alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock/data and frame-sync signals to the backplane interface section.

The transmit and receive paths of the integrated transceivers also have two HDLC controllers. The HDLC controllers transmit and receive data via the framer block. The HDLC controllers can be assigned to any time slot, group of time slots, portion of a time slot, or to FDL (T1) or Sa bits (E1). Each controller has 128-bit FIFOs, thus reducing the amount of processor overhead required to manage the flow of data. In addition, built-in support for reducing the processor time required handles SS7 applications.

The backplane interface of the integrated transceivers provides a method of sending and receiving data from the integrated Ethernet Mapper over an interleaved 8.192MHz TDM (IBO) bus. The elastic stores are required for IBO operation and they manage slip conditions.

An 8-bit parallel microcontroller port provides access for control and configuration of all the features of the device. The internal 100MHz SDRAM controller interfaces to a 32-bit wide 128Mbit SDRAM. The SDRAM is used to buffer the data from the Ethernet and WAN ports for transport. The external SDRAM can accommodate up to 8192 frames with a maximum frame size of 2016 bytes. Diagnostic capabilities include SDRAM BIST, loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection. The DS33R41 operates with a 1.8V core supply and 3.3V I/O supply.

The integrated Ethernet mapper is software compatible with the DS33Z41 quad inverse-multiplexing Ethernet mapper. There are a few things to note when porting a DS33Z41 application to this device:

- RSER has been renamed to RSERI.
- RCLK has been renamed to RCLKI.
- TSER has been renamed to TSERO.
- TCLK has been renamed to TCLKE.

The integrated T1/E1/J1 transceivers are software compatible with the DS21458 quad T1/E1/J1 transceiver. There are a few things to note when porting a DS21458 application to this device:

- The facilities data link (FDL) support is available through software only. The TLINK, RLINK, TLCLK, RLCLK pins are not available on the DS33R41.
- Multiplexed microprocessor bus mode is not supported on the DS33R41.
- The extended system information bus (ESIB) is not supported on the DS33R41.
- The RSIGF signaling freeze indication hardware pin is not available.
- The user output pins UOP1, UOP2, UOP3, and UOP4 are not available.

2 FEATURE HIGHLIGHTS

2.1 General

- 400-pin, 27mm BGA package
- 1.8V and 3.3V supplies
- IEEE 1149.1 JTAG boundary scan
- Software access to device ID and silicon revision
- Development support includes evaluation kit, driver source code, and reference designs
- Programmable output clocks for fractional T1, E1, H0, and H12 applications

2.2 Microprocessor Interface

- Parallel control port with 8-bit data bus
- Nonmultiplexed Intel and Motorola timing modes
- Internal software reset and external hardware reset input pin
- Supports polled or interrupt-driven environments
- Software access to device ID and silicon revision
- Global interrupt output pin

2.3 Link Aggregation (Inverse Multiplexing)

- Link aggregation for up to four T1/E1 links
- 8.192Mbps IBO interface to Dallas Semiconductor Framers/Transceivers
- Differential delay compensation up to 7.75ms for the 4 T1/E1 links
- Handshaking protocol between local and distant end for establishment of aggregation

2.4 HDLC Ethernet Mapping

- Dedicated HDLC controller engine for protocol encapsulation
- Compatible with polled or interrupt driven environments
- Programmable FCS insertion and extraction
- Programmable FCS type
- Supports FCS error insertion
- Programmable packet size limits (minimum 64 bytes and maximum 2016 bytes)
- Supports bit stuffing/destuffing
- Selectable packet scrambling/descrambling ($X^{43}+1$)
- Separate FCS errored packet and aborted packet counts
- Programmable inter-frame fill for transmit HDLC

2.5 X.86 (Link Access Protocol for SONET/SDH) Ethernet Mapping

- Programmable X.86 address/control fields for transmit and receive
- Programmable 2-byte protocol (SAPI) field for transmit and receive
- 32-bit FCS
- Transmit transparency processing—7E is replaced by 7D, 5E
- Transmit transparency processing—7D replaced by 7D, 5D
- Receive rate adaptation (7D, DD) is deleted.
- Receive transparency processing—7D, 5E is replaced by 7E
- Receive transparency processing—7D, 5D is replaced by 7D
- Receive abort sequence the LAPS packet is dropped if 7D7E is detected
- Self-synchronizing $X^{43} + 1$ payload scrambling.

2.6 Additional HDLC Controllers in the Integrated T1/E1/J1 Transceiver

- Two additional independent HDLC controllers
- Fast load and unload features for FIFOs
- SS7 support for FISU transmit and receive
- Independent 128-byte Rx and Tx buffers with interrupt support
- Access FDL, Sa, or single/multiple DS0 channels
- DS0 access includes Nx64 or Nx56
- Compatible with polled or interrupt driven environments
- Bit-oriented code (BOC) support

2.7 Committed Information Rate (CIR) Controllers

- CIR controller limits transmission of data from the Ethernet Interface to the serial interface
- CIR granularity at 512kbps
- CIR Averaging for smoothing traffic peaks

2.8 SDRAM Interface

- Interface for 128Mbit, 32-bit wide SDRAM
- SDRAM Interface speed up to 100MHz
- Auto refresh timing
- Automatic precharge
- Master clock provided to the SDRAM
- No external components required for SDRAM connectivity

2.9 T1/E1/J1 Framer

- Fully independent transmit and receive functionality
- Full receive- and transmit-path transparency
- T1 framing formats include D4, ESF, J1-D4, J1-ESF and SLC-96
- Japanese J1 support for CRC6 and yellow alarm
- E1 framing formats include FAS, CAS, and CRC-4
- Detailed alarm- and status-reporting with optional interrupt support
- Large path- and line-error counters for:
 - T1—BPV, CV, CRC6, and framing bit errors
 - E1—BPV, CV, CRC-4, E-bit, and frame alignment errors
- Timed or manual update modes
- User-defined Idle Code Generation on a per-channel basis in both transmit and receive paths
- Digital milliwatt code generation on the receive path
- ANSI T1.403-1998 support
- G.965 V5.2 link detect
- RAI-CI, AIS-CI detection and generation
- Ability to monitor one DS0 channel in both the transmit and receive paths
- Three independent, In-band repeating-pattern generators and detectors
- Patterns from 1 bit to 8 bits or 16 bits in length
- RCL, RLOS, RRA, and RAIS alarms interrupt on change of state
- Flexible signaling support
 - Software- or hardware-based
 - Interrupt generated on change of signaling data
 - Receive-signaling freeze on loss of sync, carrier loss, or frame slip
 - Hardware pins to indicate carrier loss and signaling freeze
 - Automatic RAI generation to ETS 300 011 specifications
 - Expanded access to Sa and Si bits
- Option to extend carrier-loss criteria to a 1ms period as per ETS 300 233

2.10 Line Interface

- Requires a single master clock (MCLK) for both E1 and T1 operation. Master clock can be 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz. Option to use 1.544MHz, 3.088MHz, 6.276MHz, or 12.552MHz for T1-only operation
- Fully software configurable
- Short- and long-haul applications
- Automatic receive sensitivity adjustments
- Ranges include 0dB to -43dB or 0dB to -12dB for E1 applications; 0dB to -36dB or 0dB to -15dB for T1 applications
- Receive level indication in 2.5dB steps from -42.5dB to -2.5dB
- Internal receive termination option for 75Ω, 100Ω, and 120Ω lines
- Monitor application gain settings of 20dB, 26dB, and 32dB
- G.703 receive-synchronization signal-mode
- Flexible transmit-waveform generation
- T1 DSX-1 line build-outs
- T1 CSU line build-outs of -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted cables
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Square-wave output
- Open-drain output option
- NRZ format option
- Transmitter power-down
- Transmitter 50mA short-circuit limiter with exceeded indication of current limit
- Transmit open-circuit-detected indication
- Line interface function can be completely decoupled from the framer/formatter

2.11 MAC Interface

- MAC port with standard MII (less TX_ER) or RMII
- 10Mbps and 100Mbps data rates
- Configurable DTE or DCE modes
- Facilitates auto-negotiation by host microprocessor
- Programmable half- and full-duplex modes
- Flow control for both half-duplex (back-pressure) and full-duplex (PAUSE) modes
- Programmable Maximum MAC frame size up to 2016 bytes
- Minimum MAC frame size: 64 bytes
- Discards frames greater than programmed maximum MAC frame size and runt, nonoctet bounded, or bad-FCS frames upon reception
- Programmable threshold for SDRAM queues to initiate flow control and status indication
- MAC loopback support for transmit data looped to receive data at the MII/RMII interface

2.12 Clock Synthesizer

- Output frequencies include 2.048MHz, 4.096MHz, 8.192MHz, and 16.384MHz
- Derived from recovered line clock or master clock

2.13 Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 2.048MHz master clock for both E1 and T1 operation with the option to use 1.544MHz for T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

2.14 System Interface

- Dual two-frame, independent receive and transmit elastic stores
 - Independent control and clocking
 - Controlled-slip capability with status
 - Minimum-delay mode supported
- Supports T1 to E1 conversion
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation with rates of 4.096MHz, 8.192MHz, and 16.384MHz
- Hardware-signaling capability
 - Receive-signaling reinsertion to a backplane, multiframe sync
 - Availability of signaling in a separate PCM data stream
 - Signaling freezing
- Access to the data streams in between the framer/formatter and the elastic stores
- User-selectable synthesized clock output

2.15 Test and Diagnostics

- IEEE 1149.1 Support
- Programmable on-chip BERT
- Patterns include Pseudorandom QRSS, Daly, and user-defined repetitive patterns
- Error insertion for a single bit or continuous
- Insertion options include continuous and absolute number with selectable insertion rates
- Total-bit and errored-bit counters
- Payload Error Insertion
- Errors can be inserted over the entire frame or selected channels
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel payload loopback)

2.16 Specifications Compliance

The DS33R41 meets relevant telecommunications specifications. The following table provides the specifications and relevant sections that are applicable to the DS33R41.

Table 2-1. T1-Related Telecommunications Specifications

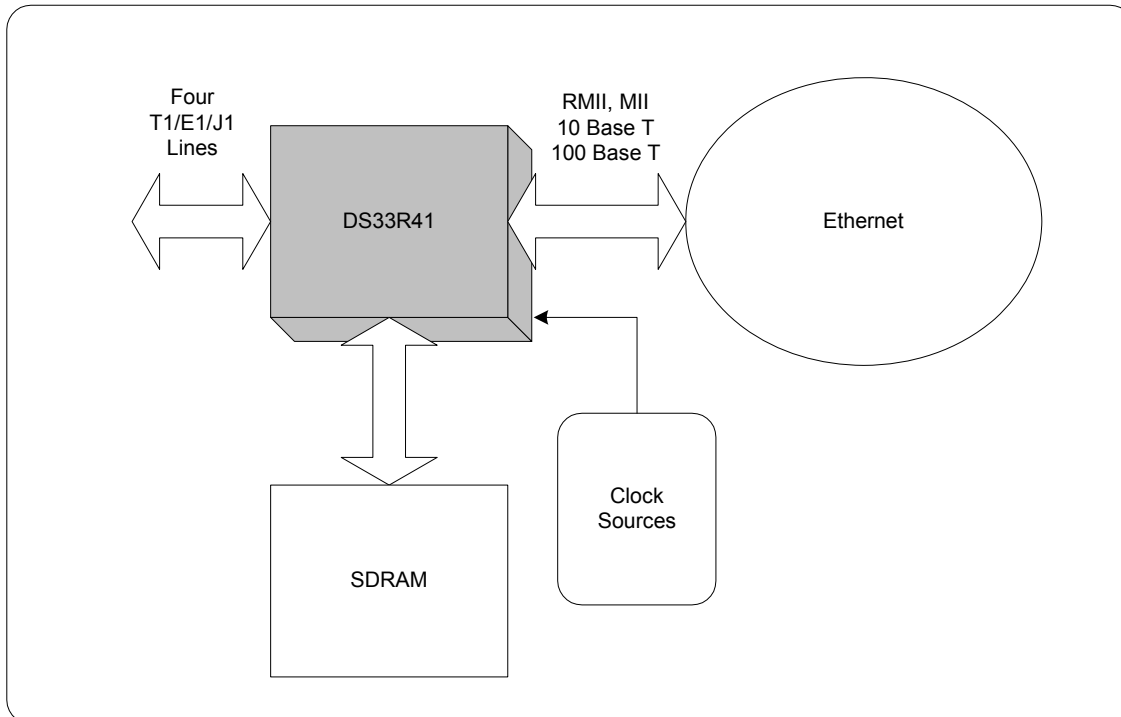
| |
|---|
| IEEE 802.3-2002 - CSMA/CD access method and physical layer specifications. |
| RFC1662 - PPP in HDLC-like Framing |
| RFC2615 - PPP over SONET/SDH |
| X.86 - Ethernet over LAPS |
| RMII - Industry Implementation Agreement for "Reduced MII Interface," Sept 1997 |
| ANSI - T1.403-1995, T1.231-1993, T1.408 |
| AT&T: TR54016, TR62411 |
| ITU: G.703, G.704, G.706, G.736, G.775, G.823, G.932, I.431, O.151, O.161 |
| ETS: ETS 300 011, ETS 300 166, ETS 300 233, CTR4, CTR12 |
| Japanese: JTG.703, JTI.431, JJ-20.11 (CMI coding only) |

3 APPLICATIONS

- Bonded Transparent LAN Service
- LAN Extension
- Ethernet Delivery over T1/E1/J1

Also see *Application Note 3411: DS33Z11—Ethernet LAN to Unframed T1/E1 WAN Bridge* for an example of a complete LAN to WAN design.

Figure 3-1. Quad T1E1 SCT to DS33R41



4 ACRONYMS AND GLOSSARY

- BERT - Bit Error Rate Tester
- DCE - Data Communication Interface
- DTE- Data Terminating Interface
- FCS - Frame Check Sequence
- HDLC - High Level Data Link Control
- MAC - Media Access Control
- MII - Media Independent Interface
- RMII - Reduced Media Independent Interface
- WAN - Wide Area Network

Note 1: Previous versions of this document used the term “Subscriber” to refer to the Ethernet Interface function. The register names have been allowed to remain with a “SU.” prefix to avoid register renaming.

Note 2: Previous versions of this document used the term “Line” to refer to the Serial Interface. The register names have been allowed to remain with a “LI.” prefix to avoid register renaming.

Note 3: The terms “Transmit Queue” and “Receive Queue” are with respect to the Ethernet Interface. The Receive Queue is the queue for the data that arrives on the MII/RMII interface, is processed by the MAC and stored in the SDRAM. Transmit queue is for data that arrives from the Serial port, is processed by the HDLC and stored in the SDRAM to be sent to the MAC transmitter.

Note 4: This data sheet assumes a particular nomenclature of the T1 and E1 operating environment. In each 125 μ s T1 frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. For T1 and E1 each channel is made up of 8 bits, which are numbered 1 to 8. Bit 1, the MSB, is transmitted first. Bit 8, the LSB, is transmitted last. The term “locked” is used to refer to two clock signals that are phase- or frequency-locked or derived from a common clock (i.e., a 1.544MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component).

TIME SLOT NUMBERING SCHEMES

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Time Slot | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| Channel | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| Phone Channel | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |

5 MAJOR OPERATING MODES

Microprocessor control is possible through the 8-bit parallel control port and provides configuration for all the features of the device. The Ethernet Link Transport Engine in the device can be configured for HDLC or X.86 encapsulation.

The integrated transceivers can be software configured for T1, E1, or J1 operation. Each is composed of a line interface unit (LIU), framer, two additional HDLC controllers, and a TDM backplane interface, and is controlled via an 8-bit parallel port configured for Intel or Motorola bus operations.

The LIUs are composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75 Ω coax and 120 Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0dB to 43dB or 0dB to 12dB for E1 applications and 0dB to 15dB or 0dB to 36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications) and can be placed in either transmit or receive data paths.

More information on microprocessor control is available in Section [8.1](#).

6 BLOCK DIAGRAMS

Figure 6-1. Detailed Block Diagram

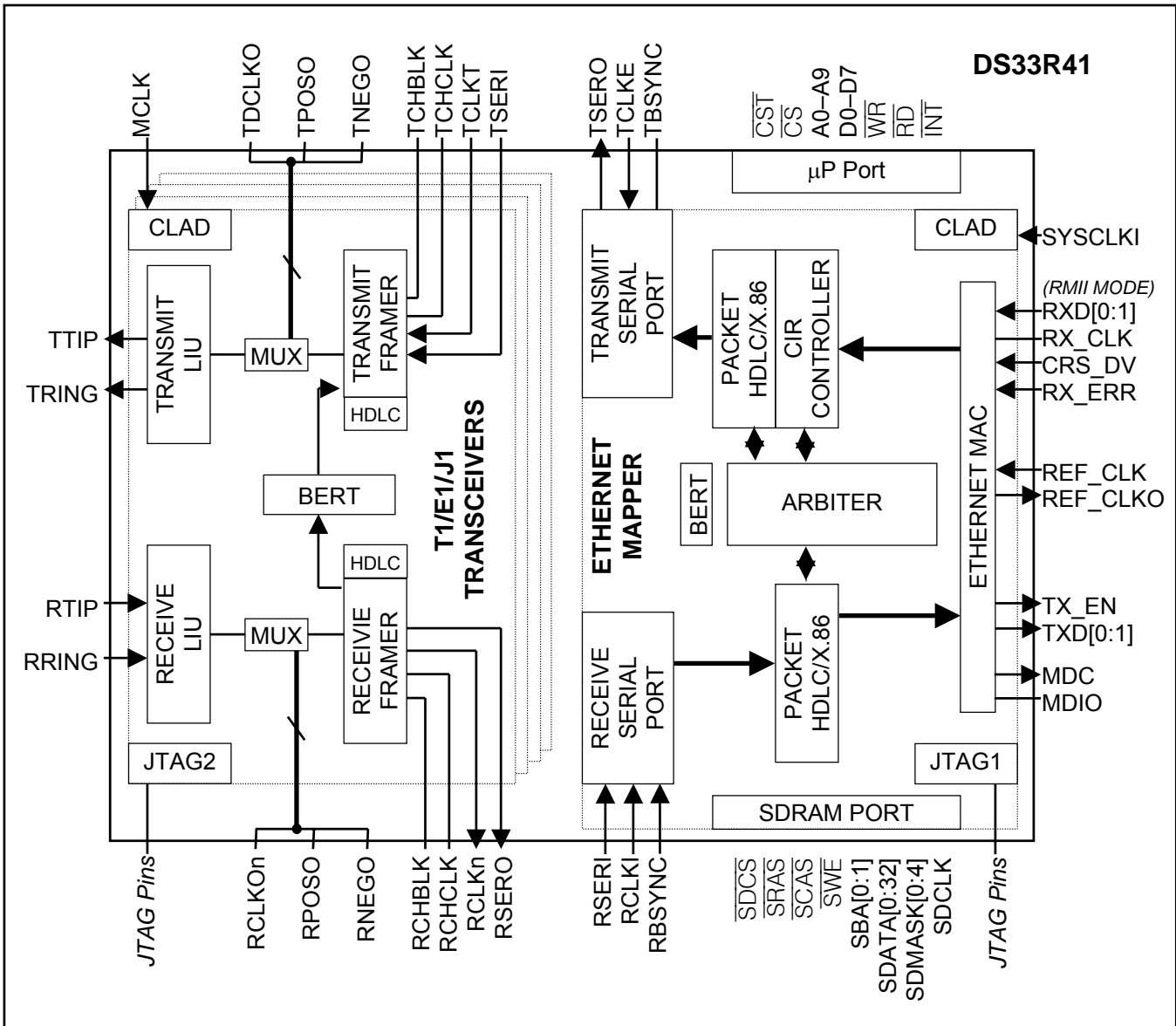
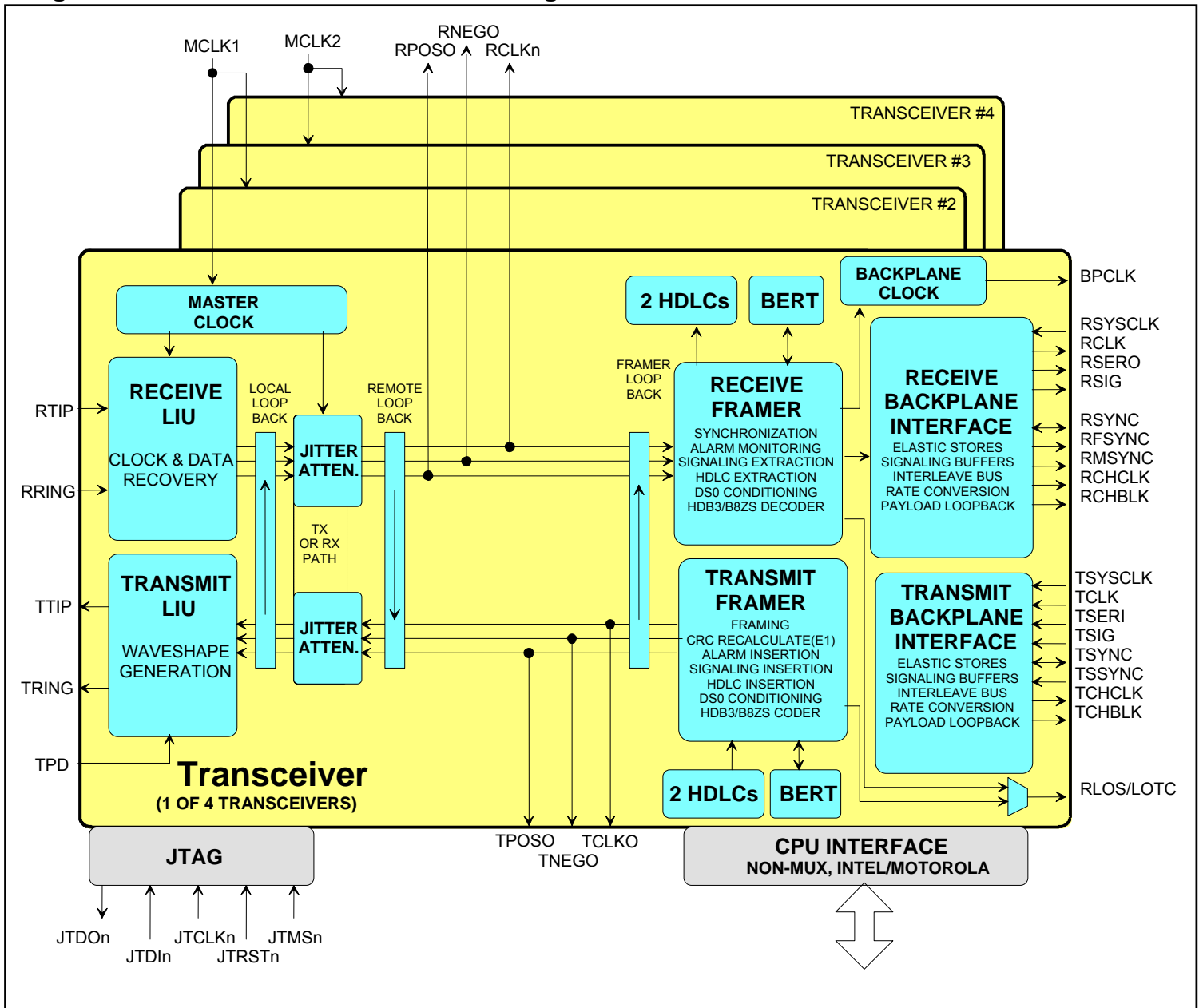


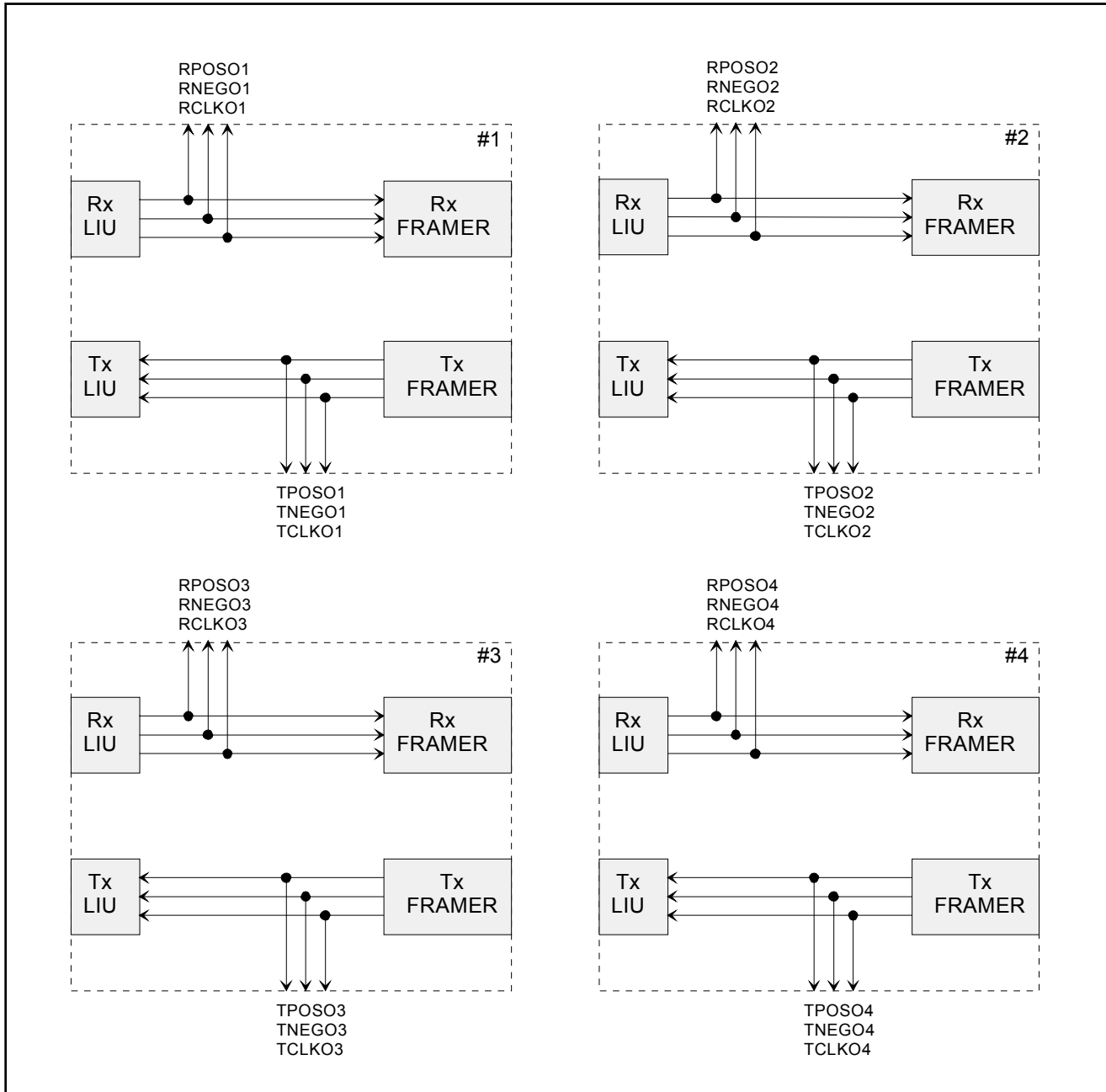
Figure 6-2. T1/E1/J1 Transceiver Block Diagram



6.1 Framer/LIU Interim Signals

The user has limited access to clock and data signals between the framer and LIU on all transceivers as shown in [Figure 6-3](#). Access to the clock and bipolar data signals between the framer and LIU function can be used for specialized applications.

Figure 6-3. Framer/LIU Interim Signals



7 PIN DESCRIPTIONS

7.1 Pin Functional Description

Note that all digital pins are inout pins in JTAG mode. This feature increases the effectiveness of board level ATPG patterns.

I = input, O = output, Ipu = input with pullup, Oz = output with tri-state, IO = bidirectional pin, IOz = bidirectional pin with tri-state

Table 7-1. Detailed Pin Descriptions

| NAME | PIN | TYPE | FUNCTION |
|-------------------------------|-----|------|---|
| MICROPROCESSOR PORT | | | |
| A0 | A19 | I | Address Bit 0. Address bit 0 of the microprocessor interface. Least Significant Bit. |
| A1 | A20 | I | Address Bit 1. Address bit 1 of the microprocessor interface. |
| A2 | C18 | I | Address Bit 2. Address bit 2 of the microprocessor interface. |
| A3 | B18 | I | Address Bit 3. Address bit 3 of the microprocessor interface. |
| A4 | E18 | I | Address Bit 4. Address bit 4 of the microprocessor interface. |
| A5 | A18 | I | Address Bit 5. Address bit 5 of the microprocessor interface. |
| A6 | E17 | I | Address Bit 6. Address bit 6 of the microprocessor interface. |
| A7 | C17 | I | Address Bit 7. Address bit 7 of the microprocessor interface. |
| A8 | D17 | I | Address Bit 8. Address bit 8 of the microprocessor interface. |
| A9 | C16 | I | Address Bit 9. Address bit 9 of the microprocessor interface. |
| D0 | G17 | IOZ | Data Bit 0. Bidirectional data bit 0 of the microprocessor interface. Least Significant Bit. Not driven when $\overline{CS} = 1$ or $\overline{RST} = 0$. |
| D1 | A17 | IOZ | Data Bit 1. Bidirectional data bit 1 of the microprocessor interface. Not driven when $CS = 1$ or $RST = 0$. |
| D2 | F17 | IOZ | Data Bit 2. Bidirectional data bit 2 of the microprocessor interface. Not driven when $CS = 1$ or $RST = 0$. |
| D3 | F16 | IOZ | Data Bit 3. Bidirectional data bit 3 of the microprocessor interface. Not driven when $CS = 1$ or $RST = 0$. |
| D4 | E16 | IOZ | Data Bit 4. Bidirectional data bit 4 of the microprocessor interface. Not driven when $CS = 1$ or $RST = 0$. |
| D5 | D16 | IOZ | Data Bit 5. Bidirectional data bit 5 of the microprocessor interface. Not driven when $CS = 1$ or $RST = 0$. |
| D6 | B15 | IOZ | Data Bit 6. Bidirectional data bit 6 of the microprocessor interface. Not driven when $CS = 1$ or $RST = 0$. |
| D7 | C15 | IOZ | Data Bit 7. Bidirectional data bit 7 of the microprocessor interface. Most Significant Bit. Not driven when $\overline{CS} = 1$ or $\overline{RST} = 0$. |
| $\overline{WR}/\overline{RW}$ | A16 | I | <p>Write (Intel Mode). The DS33R41 captures the contents of the data bus (D0–D7) on the rising edge of \overline{WR} and writes them to the addressed register location. \overline{CS} must be held low during write operations.</p> <p>Read Write (Motorola Mode). Used to indicate read or write operation. \overline{RW} must be set high for a register read cycle and low for a register write cycle.</p> |
| $\overline{RD}/\overline{DS}$ | F15 | I | <p>Read Data Strobe (Intel Mode). The DS33R41 drives the data bus (D0–D7) with the contents of the addressed register while \overline{RD} and \overline{CS} are both low.</p> <p>Data Strobe (Motorola Mode). Used to latch data through the microprocessor interface. \overline{DS} must be low during read and write operations.</p> |

| NAME | PIN | TYPE | FUNCTION |
|--------------------------------------|--------------------------|------|---|
| \overline{CS} | H16 | I | Chip Select for Protocol Conversion Device. This pin must be taken low for read/write operations. When \overline{CS} is high, the $\overline{RD/DS}$ and \overline{WR} signals are ignored. |
| \overline{CST} | W6 | I | Chip Select for the T1/E1/J1 Transceivers. Must be low to read or write the T1/E1/J1 Transceivers |
| \overline{INT} | E15 | OZ | Interrupt Output. Outputs a logic zero when an unmasked interrupt event is detected. \overline{INT} is deasserted when all interrupts have been acknowledged and serviced. Active low. Inactive state is programmable in register GL.CR1 . This pin is deasserted when all interrupts have been acknowledged and serviced. Active low. Inactive state is programmable in register GL.CR1. |
| MII/RMII PHY PORT | | | |
| COL_DET | N20 | I | Collision Detect (MII). Asserted by the MAC PHY to indicate that a collision is occurring. In DCE Mode this signal should be connected to ground. This signal is only valid in half duplex mode, and is ignored in full duplex mode |
| RX_CRS/ CRS_DV | N19 | I | Receive Carrier Sense (MII). Should be asserted (high) when data from the PHY (RXD[3:0]) is valid. For each clock pulse 4 bits arrive from the PHY. Bit 0 is the least significant bit. In DCE mode, connect to V_{DD} . Carrier Sense/Receive Data Valid (RMII). This signal is asserted (high) when data is valid from the PHY. For each clock pulse 2 bits arrive from the PHY. In DCE mode, this signal must be grounded. |
| RX_CLK | K19 | IO | Receive Clock (MII). Timing reference for RX_DV, RX_ERR and RXD[3:0], which are clocked on the rising edge. RX_CLK frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. In DCE mode, this is an output derived from REF_CLK providing 2.5MHz (10Mbps operation) or 25MHz (100Mbps operation). |
| RXD[0] RXD[1] RXD[2] RXD[3] | J19 H18 J18 H19 | O | Receive Data 0 through 3 (MII). Four bits of received data, sampled synchronously with the rising edge of RX_CLK. For every clock cycle, the PHY transfers 4 bits to the DS33R41. RXD[0] is the least significant bit of the data. Data is not considered valid when RX_DV is low. Receive Data 0 through 1 (RMII). Two bits of received data, sampled synchronously with REF_CLK with 100Mbps Mode. Accepted when CRS_DV is asserted. When configured for 10Mbps Mode, the data is sampled once every 10 clock periods. |
| RX_DV | K18 | I | Receive Data Valid (MII). This active high signal indicates valid data from the PHY. The data RXD is ignored if RX_DV is not asserted high. |
| RX_ERR | K20 | I | Receive Error (MII). Asserted by the MAC PHY for one or more RX_CLK periods indicating that an error has occurred. Active High indicates Receive code group is invalid. If CRS_DV is low, RX_ERR has no effect. This is synchronous with RX_CLK. In DCE mode, this signal must be grounded. Receive Error (RMII). Signal is synchronous to REF_CLK; |
| TX_CLK | L18 | IO | Transmit Clock (MII). Timing reference for TX_EN and TXD[3:0]. The TX_CLK frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. In DCE mode, this is an output derived from REF_CLK providing 2.5MHz (10Mbps operation) or 25MHz (100Mbps operation). |

| NAME | PIN | TYPE | FUNCTION |
|--------------------------------------|--------------------------|------|--|
| TXD[0] TXD[1] TXD[2] TXD[3] | L20 M19 M18 M20 | O | Transmit Data 0 through 3(MII). TXD [3:0] is presented synchronously with the rising edge of TX_CLK. TXD [0] is the least significant bit of the data. When TX_EN is low the data on TXD should be ignored. Transmit Data 0 through 1(RMII). Two bits of data TXD [1:0] presented synchronously with the rising edge of REF_CLK. |
| TX_EN | L19 | O | Transmit Enable (MII). This pin is asserted high when data TXD [3:0] is being provided by the DS33R41. The signal is deasserted prior to the first nibble of the next frame. This signal is synchronous with the rising edge TX_CLK. It is asserted with the first bit of the preamble. Transmit Enable (RMII). When this signal is asserted, the data on TXD [1:0] is valid. This signal is synchronous to the REF_CLK. |
| REF_CLK | C20 | I | Reference Clock (RMII and MII). When in RMII mode, all signals from the PHY are synchronous to this clock input for both transmit and receive. This required clock can be up to 50MHz and should have ± 100 ppm accuracy. When in MII mode in DCE operation, the DS33R41 uses this input to generate the RX_CLK and TX_CLK outputs as required for the Ethernet PHY interface. When the MII interface is used with DTE operation, this clock is not required and should be tied low. In DCE and RMII modes, this input must have a stable clock input before setting the RST pin high for normal operation. |
| REF_CLKO | G19 | O | Reference Clock Output (RMII and MII). A derived clock output up to 50MHz, generated by internal division of the SYSCLKI signal. Frequency accuracy of the REF_CLKO signal will be proportional to the accuracy of the user-supplied SYSCLKI signal. See Section 9.1.2 for more information. |
| DCEDTES | L17 | I | DCE or DTE Selection. The user must set this pin high for DCE Mode selection or low for DTE Mode. In DCE Mode, the DS33R41 MAC port can be directly connected to another MAC. In DCE Mode, the Transmit clock (TX_CLK) and Receive clock (RX_CLK) are output by the DS33R41. Note that there is no software bit selection of DCEDTES. Note that DCE Mode is only relevant when the MAC interface is in MII mode. |
| RMIIMIIS | K13 | I | RMII or MII Selection. Set high to configure the MAC for RMII interfacing. Set low for MII interfacing. |
| PHY MANAGEMENT BUS | | | |
| MDC | E20 | O | Management Data Clock (MII). Clocks management data between the PHY and DS33R41. The clock is derived from the SYSCLKI, with a maximum frequency is 1.67MHz. The user must leave this pin unconnected in the DCE Mode. |
| MDIO | F20 | IO | MII Management data IO (MII). Data path for control information between the PHY and DS33R41. When not used, pull to logic high externally through a 10k Ω resistor. The MDC and MDIO pins are used to write or read up to 32 Control and Status Registers in 32 PHY Controllers. This port can also be used to initiate Auto-Negotiation for the PHY. The user must leave this pin unconnected in the DCE Mode. |
| SDRAM CONTROLLER | | | |
| $\overline{\text{SCAS}}$ | R14 | O | SDRAM Column Address Strobe. Active low output, used to latch the column address on the rising edge of SDCLKO. It is used with commands for Bank Activate, Precharge, and Mode Register Write. |
| $\overline{\text{SRAS}}$ | P15 | O | SDRAM Row Address Strobe. Active low output, used to latch the row address on rising edge of SDCLKO. It is used with commands for Bank Activate, Precharge, and Mode Register Write. |
| $\overline{\text{SDCS}}$ | R15 | O | SDRAM Chip Select. Active low output enables SDRAM access. |

| NAME | PIN | TYPE | FUNCTION |
|--|--|----------|--|
| $\overline{\text{SWE}}$ | T15 | O | SDRAM Write Enable. This active low output enables write operation and auto precharge. |
| SBA[0] SBA[1] | R16 W15 | O | SDRAM Bank Select. These 2 bits select 1 of 4 banks for the read/write/precharge operations. Note: All SDRAM operations are controlled entirely by the DS33R41. No user programming for SDRAM buffering is required. |
| SDATA[0] SDATA[1] SDATA[2] SDATA[3] SDATA[4] SDATA[5] SDATA[6] SDATA[7] SDATA[8] SDATA[9] SDATA[10] SDATA[11] SDATA[12] SDATA[13] SDATA[14] SDATA[15] SDATA[16] SDATA[17] SDATA[18] SDATA[19] SDATA[20] SDATA[21] SDATA[22] SDATA[23] SDATA[24] SDATA[25] SDATA[26] SDATA[27] SDATA[28] SDATA[29] SDATA[30] SDATA[31] | W11 M15 Y11 M14 U12 T13 R13 W13 V13 W12 V12 V11 R12 T11 T12 U11 T18 W18 P19 P20 W19 Y20 V19 W20 U20 U19 T20 T19 Y19 U18 V18 R18 | IO | SDRAM Data Bus Bits 0 through 31. The 32 pins of the SDRAM data bus are inputs for read operations and outputs for write operations. At all other times, these pins are high-impedance. Note: All SDRAM operations are controlled entirely by the DS33R41. No user programming for SDRAM buffering is required. |
| SDA[0] SDA[1] SDA[2] SDA[3] SDA[4] SDA[5] SDA[6] SDA[7] SDA[8] SDA[9] SDA[10] SDA[11] | T17 U16 Y17 W17 U17 W16 Y16 V16 T16 V15 R17 P16 | O | SDRAM Address Bus 0 through 11. The 12 pins of the SDRAM address bus output the row address first, followed by the column address. The row address is determined by SDA0 to SDA11 at the rising edge of clock. Column address is determined by SDA0–SDA9 and SDA11 at the rising edge of the clock. SDA10 is used as an auto-precharge signal. Note: All SDRAM operations are controlled entirely by the DS33R41. No user programming for SDRAM buffering is required. |
| SDMASK[0] SDMASK[1] SDMASK[2] SDMASK[3] | Y13 P14 P18 V17 | O | SDRAM Mask 0 through 3. When high, a write is done for that byte. The least significant byte is SDATA7 to SDATA0. The most significant byte is SDATA31 to SDATA24. |
| SDCLKO | U14 | O 4mA | SDRAM CLK Out. System clock output to the SDRAM. This clock is a buffered version of SYSCLKI. |

| NAME | PIN | TYPE | FUNCTION |
|--|----------|------|--|
| T1/E1/J1 ANALOG LINE INTERFACES | | | |
| RTIP1 | N1 | I | Receive Analog Tip Input for Transceiver 1. Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details. |
| RRING1 | M1 | I | Receive Analog Ring Input for Transceiver 1. Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details. |
| RTIP2 | J13 | I | Receive Analog Tip Input for Transceiver 2. Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details. |
| RRING2 | J12 | I | Receive Analog Ring Input For Transceiver 2. Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details. |
| RTIP3 | E6 | I | Receive Analog Tip Input for Transceiver 3. Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details. |
| RRING3 | F6 | I | Receive Analog Ring Input for Transceiver 3. Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details. |
| RTIP4 | T9 | I | Receive Analog Tip Input for Transceiver 4. Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details. |
| RRING4 | R9 | I | Receive Analog Ring Input for Transceiver 4. Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the network. See Section 10 for details. |
| TTIP1 | T1, U1 | O | Transmit Analog Tip Output for Transceiver 1. Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details. |
| TRING1 | V1, W1 | O | Transmit Analog Ring Output for Transceiver 1. Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details. |
| TTIP2 | A12, B12 | O | Transmit Analog Tip Output for Transceiver 2. Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details. |
| TRING2 | A11, B11 | O | Transmit Analog Ring Output for Transceiver 2. Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details. |
| TTIP3 | E1, E2 | O | Transmit Analog Tip Output for Transceiver 3. Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details. |
| TRING3 | F1, F2 | O | Transmit Analog Ring Output for Transceiver 3. Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details. |
| TTIP4 | W8, Y8 | O | Transmit Analog Tip Output for Transceiver 4. Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details. |

| NAME | PIN | TYPE | FUNCTION |
|---|------------------------|------|---|
| TRING4 | W9, Y9 | O | Transmit Analog Ring Output for Transceiver 4. Analog line-driver outputs. Two connections are provided to improve signal quality. These pins connect via a 1:2 step-up transformer to the network. See Section 10 for details. |
| T1/E1/J1 TRANSMIT FRAMER INTERFACE | | | |
| TSERI1 TSERI2 TSERI3 TSERI4 | Y4 B9 J2 R7 | I | Transmit Serial Data for Transceivers 1–4. Transmit NRZ serial data. Sampled on the falling edge of TCLKT when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYCLK when the transmit-side elastic store is enabled. |
| TSYCLK1 TSYCLK2 TSYCLK3 TSYCLK4 | H4 J5 A6 Y5 | I | Transmit System Clock for Transceivers 1–4. 8.192MHz clock used for Interleaved Bus Operation. Used when the transmit-side elastic-store function is enabled. See the <i>Interleaved PCM Bus Operation</i> section for details on 8.192MHz operation using the IBO. |
| TSSYNC1 TSSYNC2 TSSYNC3 TSSYNC4 | W4 E13 A2 N13 | I | Transmit System Sync for Transceivers 1–4. Only used when the transmit-side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit-side elastic store. |
| TCLKT1 TCLKT2 TCLKT3 TCLKT4 | U4 A9 J3 N9 | I | Transmit Clock for Transceivers 1–4. 1.544MHz or a 2.048MHz primary clock. Used to clock data through the transmit-side formatter. Not used for most DS33R41 applications. |
| TCHBLK1 TCHBLK2 TCHBLK3 TCHBLK4 | M4 A14 D3 P11 | O | Transmit Channel Block for Transceivers 1–4. A user-programmable output that can be forced high or low during any of the channels. Synchronous with TSYCLK when the transmit-side elastic store is enabled. Useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. |
| TCHCLK1 TCHCLK2 TCHCLK3 TCHCLK4 | Y3 C13 E3 L9 | O | Transmit Channel Clock for Transceivers 1–4. A 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. Can also be programmed to output a gated transmit-bit clock for fractional T1/E1 applications. Synchronous with TSYCLK when the transmit-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data. |
| TSYNC1 TSYNC2 TSYNC3 TSYNC4 | W3 D13 C2 P6 | I/O | Transmit Sync for Transceivers 1–4. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Can be programmed to output either a frame or multiframe pulse. If this pin is set to output pulses at frame boundaries, it can also be set via IOCR1.3 to output double-wide pulses at signaling frames in T1 mode. |
| TSIG1 TSIG2 TSIG3 TSIG4 | V5 B8 H2 P7 | I | Transmit Signaling Input for Transceivers 1–4. When enabled, this input will sample signaling bits for insertion into outgoing PCM data stream. Sampled on the falling edge of TCLKT when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYCLK when the transmit-side elastic store is enabled. |

| NAME | PIN | TYPE | FUNCTION |
|--|------------------------|------|--|
| ETHERNET MAPPER TRANSMIT SERIAL INTERFACE | | | |
| TSERO | K15 | O | Transmit Serial Data Output. Output on the rising edge of TCLKE. Formatted to be IBO compatible. |
| TCLKE | K14 | I | Serial Interface Transmit Clock Input. The 8.192MHz clock reference for TSERO, which is output on the rising edge of the clock. |
| TBSYNC | K16 | IO | Transmit Data Enable Port n (Input). An 8kHz synchronization pulse, used to denote the first Channel 1 of the 8.192Mbps byte-interleaved IBO data stream. Note that this input is also used to generate the transmit byte synchronization if X.86 mode is enabled. |
| T1/E1/J1 RECEIVE FRAMER INTERFACE | | | |
| RSERO1 RSERO2 RSERO3 RSERO4 | K4 K9 B5 T7 | O | Receive Serial Data Output for T1/E1/J1 Transceivers 1–4. Received NRZ serial data. Updated on the rising edges of RSYCLK when the receive-side elastic store is enabled. In most DS33R41 applications, all 4 RSERO outputs should be tied together and connected to RSERI. |
| RSYSCLK1 RSYSCLK2 RSYSCLK3 RSYSCLK4 | K1 K10 C6 Y6 | I | Receive System Clock for T1/E1/J1 Transceivers 1–4. 8.192MHz system clock. Used when the receive-side elastic-store function is enabled. In most DS33R41 applications, all 4 RSYCLK inputs should be tied together and connected to RCLKI. See the <i>Interleaved PCM Bus Operation</i> section for details on 8.192MHz operation using the IBO. |
| RCLK1 RCLK2 RCLK3 RCLK4 | W5 C8 H1 N7 | O | Receive Clock Output from the Framer on Transceiver 1. Buffered recovered clock from Transceiver 1. Previously named RCLKO1-4. Not used for most DS33R41 applications. |
| RCHBLK1 RCHBLK2 RCHBLK3 RCHBLK4 | P3 B14 A4 M8 | O | Receive Channel Block for Transceivers 1–4. A user-programmable output that can be forced high or low during any of the 24 T1 or 32 E1 channels. Synchronous with RSYCLK when the receive-side elastic store is enabled. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See the <i>Channel Blocking Registers</i> section. |
| RCHCLK1 RCHCLK2 RCHCLK3 RCHCLK4 | P2 D14 B4 V7 | O | Receive Channel Clock for Transceivers 1–4. A 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel can also be programmed to output a gated receive-bit clock for fractional T1/E1 applications. Synchronous with RSYCLK when the receive-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data. |
| RSYNC1 RSYNC2 RSYNC3 RSYNC4 | Y2 A15 B3 M9 | I/O | Receive Sync for Transceivers 1–4. An extracted pulse, one RSYCLK wide, is output at this pin, which identifies either frame (TR.IOCR1.5 = 0) or multiframe (TR.IOCR1.5 = 1) boundaries. If set to output-frame boundaries then via TR.IOCR1.6, RSYNC can also be set to output double-wide pulses on signaling frames in T1 mode. If the receive-side elastic store is enabled, then this pin can be enabled to be an input via TR.IOCR1.4 at which a frame or multiframe boundary pulse is applied. |
| RFSYNC1 RFSYNC2 RFSYNC3 RFSYNC4 | R1 E14 C4 M10 | O | Receive Frame Sync (Pre Receive Elastic Store) for Transceivers 1–4. An extracted 8kHz pulse, one RSYCLK wide, is output at this pin, which identifies frame boundaries. |
| RMSYNC1 RMSYNC2 RMSYNC3 RMSYNC4 | Y1 F13 A3 V9 | O | Receive Multiframe Sync for Transceivers 1–4. An extracted pulse, one RSYCLK wide, is output at this pin, which identifies multiframe boundaries. |
| RSIG1 RSIG2 RSIG3 RSIG4 | M3 H11 D5 U8 | O | Receive Signaling Output for Transceivers 1–4. Outputs signaling bits in a PCM format. Updated on the rising edges of RSYCLK when the receive-side elastic store is enabled. |

| NAME | PIN | TYPE | FUNCTION |
|---|------------------------|------|---|
| ETHERNET MAPPER RECEIVE SERIAL INTERFACE | | | |
| RSERI | L16 | I | Receive Serial Data Input. Receive Serial data arrives on the rising edge of the clock. Note: Unused timeslots on this pin must be filled with all 1s. |
| RCLKI | L14 | I | Serial Interface Receive Clock Input. Reference clock for receive serial data on RSERI. Gapped clocking is supported, up to the maximum RCLKI frequency of 52MHz. |
| RBSYNC | L15 | I | Receive Data Enable Port n. An 8kHz synchronization pulse, used to denote the first Channel 1 of the 8.192Mbps byte-interleaved IBO data stream. Note that this input is also used to generate the receive byte synchronization if X.86 mode is enabled. |
| T1/E1/J1 FRAMER/LIU INTERIM SIGNALS | | | |
| RCLKO1 RCLKO2 RCLKO3 RCLKO4 | V4 D12 C1 P10 | O | Receive Clock Output from the LIU on Transceivers 1–4. Buffered recovered clock from the network. Previously named RDCLKO1-4. Not used for most DS33R41 applications. |
| RNEGO1 RNEGO2 RNEGO3 RNEGO4 | N4 G9 D7 V6 | O | Receive Negative Data from the LIU on Transceivers 1–4. Updated on the rising edge of RCLKOn with the bipolar data out of the line interface. Not used for most DS33R41 applications. |
| RPOSO1 RPOSO2 RPOSO3 RPOSO4 | N3 J10 A5 U7 | O | Receive Positive Data from the LIU on Transceivers 1–4. Updated on the rising edge of RCLKOn with bipolar data out of the line interface. Not used for most DS33R41 applications. |
| TCLKO1 TCLKO2 TCLKO3 TCLKO4 | R4 E11 G3 M11 | O | Transmit Clock Output from the Framer on Transceivers 1–4. Buffered clock that is used to clock data through the transmit-side formatter (either TCLKT or RCLKI). Not used for most DS33R41 applications. |
| TNEGO1 TNEGO2 TNEGO3 TNEGO4 | P4 C12 F3 N10 | O | Transmit Negative-Data Output from Framer on Transceivers 1–4. Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. Not used for most DS33R41 applications. |
| TPOSO1 TPOSO2 TPOSO3 TPOSO4 | R3 E12 F4 N11 | O | Transmit Positive-Data Output from Framer on Transceivers 1–4. Updated on the rising edge of TCLKO with the bipolar data out of the transmit-side formatter. Can be programmed to source NRZ data via the output-data format (TR.IOCR1.0)-control bit. Not used for most DS33R41 applications. |

| NAME | PIN | TYPE | FUNCTION |
|--|-----------------------|------|---|
| HARDWARE AND STATUS PINS | | | |
| TSTRST | L2 | I | Test/Reset. A dual-function pin. A zero-to-one transition issues a hardware reset to the transceiver register set. A reset clears all configuration registers. Configuration register contents are set to zero. Leaving TSTRST high will tri-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing. |
| $\overline{\text{RST}}$ | H15 | I | Reset. An active low signal on this pin resets the internal registers and logic. This pin should remain low until power, SYSCLKI, RX_CLK, and TX_CLK are stable, then set high for normal operation. This input requires a clean edge with a rise time of 25ns or less to properly reset the device. |
| TPD | D6 | I | Transceiver Transmit Power-Down. The TPD pin along with the TPD bit in the LIC1 register (LIC1.0) controls the state of the Transmit Power-Down function. See the TPD bit description in Section 12 and Table 12-9 . |
| MODEC[0], MODEC[1] | E7, G15 | I | Mode Control 00 = Read/Write Strobe Used (Intel Mode) 01 = Data Strobe Used (Motorola Mode) 10 = Reserved. Do not use. 11 = Reserved. Do not use. |
| RLOS/LOT1C1 RLOS/LOT1C2 RLOS/LOT1C3 RLOS/LOT1C4 | R2 C14 D4 V8 | O | Receive Loss of Sync/Loss of Transmit Clock for Transceiver 1. A dual-function output that is controlled by the TR.CCR1.0 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLKT pin has not been toggled for 5 μ s. |
| QOVF | G18 | O | Queue Overflow. This pin goes high when the transmit or receive queue has overflowed. This pin will go low when the high watermark is reached again. |

| NAME | PIN | TYPE | FUNCTION |
|----------------------------|-----|------|--|
| SYSTEM CLOCKS | | | |
| SYCLKI | Y14 | I | System Clock In. 100MHz System Clock input to the DS33R41, used for internal operation. This clock is buffered and provided at SDCLKO for the SDRAM interface. The DS33R41 also provides a divided version output at the REF_CLKO pin. A clock supply with ± 100 ppm frequency accuracy is suggested. |
| BPCLK1 | L3 | O | Backplane Clock, Transceiver 1. A user-selectable synthesized clock output that is referenced to the clock that is output at the RCLK1 pin. |
| BPCLK2 | G8 | O | Backplane Clock, Transceiver 2. A user-selectable synthesized clock output that is referenced to the clock that is output at the RCLK2 pin. |
| MCLK1 | K2 | I | Master Clock for Transceiver 1 and Transceiver 2. A (50ppm) clock source. This clock is used internally for both clock/data recovery and for the jitter attenuator for both T1 and E1 modes. The clock rate can be 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz. When using the transceiver in T1-only operation a 1.544MHz (50ppm) clock source can be used. MCLK1 and MCLK2 can be driven from a common clock. |
| MCLK2 | L12 | I | Master Clock for Transceiver 3 and Transceiver 4. A (50ppm) clock source. This clock is used internally for both clock/data recovery and for the jitter attenuator for both T1 and E1 modes. The clock rate can be 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz. When using the transceiver in T1-only operation a 1.544MHz (50ppm) clock source can be used. MCLK1 and MCLK2 can be driven from a common clock. |
| JTAG INTERFACES | | | |
| JTCLK1 | J17 | Ipu | JTAG Clock for the Ethernet Mapper. This signal is used to shift data into JTDI1 on the rising edge and out of JTDO1 on the falling edge. |
| JTDI1 | K17 | Ipu | JTAG Data In for the Ethernet Mapper. Test instructions and data are clocked into this pin on the rising edge of JTCLK1. This pin has a 10k Ω pullup resistor. |
| $\overline{\text{JTRST1}}$ | G14 | Ipu | JTAG Reset for the Ethernet Mapper. $\overline{\text{JTRST1}}$ is used to asynchronously reset the test access port controller. After power up, a rising edge on $\overline{\text{JTRST1}}$ will reset the test port and cause the device I/O to enter the JTAG DEVICE ID mode. Pulling $\overline{\text{JTRST1}}$ low restores normal device operation. $\overline{\text{JTRST1}}$ is pulled HIGH internally via a 10k Ω resistor operation. If boundary scan is not used, this pin should be held low. |
| JTDO1 | H14 | Oz | JTAG Data Out for the Ethernet Mapper. Test instructions and data are clocked out of this pin on the falling edge of JTCLK1. If not used, this pin should be left unconnected. |
| JTMS1 | G13 | Ipu | JTAG Mode Select for the Ethernet Mapper. This pin is sampled on the rising edge of JTCLK1 and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10k Ω pullup resistor. |
| JTCLK2 | P9 | Ipu | JTAG Clock 2 for the T1/E1/J1 Transceivers. This signal is used to shift data into JTDI2 on the rising edge and out of JTDO2 on the falling edge |
| JTDI2 | C7 | Ipu | JTAG Data In 2 for the T1/E1/J1 Transceivers. Test instructions and data are clocked into this pin on the rising edge of JTCLK2. This pin has a 10k Ω pullup resistor. |
| $\overline{\text{JTRST2}}$ | L13 | Ipu | JTAG Reset 2 for the T1/E1/J1 Transceivers. $\overline{\text{JTRST2}}$ is used to asynchronously reset the test access port controller. After power-up, $\overline{\text{JTRST2}}$ must be toggled from low to high. This action will set the device into the JTAG DEVICE ID mode. Normal device operation is restored by pulling $\overline{\text{JTRST2}}$ low. $\overline{\text{JTRST2}}$ is pulled HIGH internally via a 10k Ω resistor operation. |
| JTDO2 | L10 | Oz | JTAG Data Out 2 for the T1/E1/J1 Transceivers. Test instructions and data are clocked out of this pin on the falling edge of JTCLK2. If not used, this pin should be left unconnected. |

| NAME | PIN | TYPE | FUNCTION |
|--------------------------|--|------|---|
| JTMS2 | L11 | Ipu | JTAG Mode Select 2 for the T1/E1/J1 Transceivers. This pin is sampled on the rising edge of JTCLK2 and is used to place the test-access port into the various defined IEEE 1149.1 states. This pin has a 10kΩ pullup resistor. |
| POWER SUPPLY PINS | | | |
| V _{DD1.8} | J16, M13, M17, N14, N15, N16, N17, P17, R20, T14, V20, W14, Y15, Y18 | I | V_{DD1.8}. Connect to 1.8V power supply. |
| V _{DD3.3} | B16, B17, B19, B20, C19, D18, D19, D20, E19, F18, F19, G16 | I | V_{DD3.3}. Connect to 3.3V power supply. |
| V _{SS} | A1, D15, F11, F14, G4, G5, G7, G12, G20, H5–H10, H20, J6, J7, J8, J9, J15, J20, K3, K5–K8, L4–L8, M5, M6, M7, M12, M16, N12, N18, P12, P13, R11, R19, U13, U15, V14, Y12 | I | V_{SS}. Connect to the common supply ground. |
| RVDD | F7, J14, P1, R8 | — | Receive Analog Positive Supply. Connect to 3.3V power supply. |
| RVSS | E5, F5, G6, H12, H13, J11, L1, M2, N2, R10, T8, T10 | — | Receive Analog Signal Ground |
| TVDD | A10, B10, G1, G2, V2, W2, W10, Y10 | — | Transmit Analog Positive Supply. Connect to 3.3V power supply. |
| TVSS | A13, B13, D1, D2, T2, U2, W7, Y7 | — | Transmit Analog Signal Ground |
| DVDD | B6, C9, C10, C11, D8–D11, E8, E9, E10, F8, F9, F10, J4 | — | Digital Positive Supply. Connect to 3.3V power supply. |
| DVSS | B1, B2, C3, F12, G10, G11, H3, J1, N5, N6, N8, P5, P8, R5, R6, T3, T4, T5, T6, U5, U6, U9, U10, V10 | — | Digital Signal Ground |
| N.C. | A7, A8, B7, C5, E4, H17, K11, K12, U3, V3 | — | No Connection. Do not connect these pins. Leave these pins open. |

Figure 7-1. DS33R41 400-Ball BGA Pinout

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|----------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|---------------------|---------------------|-------------------------------|-------------------------------|--------------------|--------------------|--------------------|--------------------|
| A | V _{SS} | TSSYNC3 | RMSYNC3 | RCHBLK3 | RPOSO3 | TSYSCLK3 | N.C. | N.C. | TCLKT2 | TV _{DD} | TRING2 | TTIP2 | TV _{SS} | TCHBLK2 | RSYNC2 | $\overline{WR}/\overline{RW}$ | D1 | A5 | A0 | A1 |
| B | DV _{SS} | DV _{SS} | RSYNC3 | RCHCLK3 | RSERO3 | DV _{DD} | N.C. | TSIG2 | TSERI2 | TV _{DD} | TRING2 | TTIP2 | TV _{SS} | RCHBLK2 | D6 | V _{DD0.3} | V _{DD0.3} | A3 | V _{DD0.3} | V _{DD0.3} |
| C | RCLK03 | TSYNC3 | DV _{SS} | RFSYNC3 | N.C. | RSYSCLK3 | JTDI2 | RCLK2 | DV _{DD} | DV _{DD} | DV _{DD} | TNEG02 | TCHCLK2 | RLOS/LOT2 | D7 | A9 | A7 | A2 | V _{DD0.3} | REF_CLK |
| D | TV _{SS} | TV _{SS} | TCHBLK3 | RLOS/LOT3 | RSIG3 | TPD | RNEGO3 | DV _{DD} | DV _{DD} | DV _{DD} | DV _{DD} | RCLK02 | TSYNC2 | RCHCLK2 | V _{SS} | D5 | A8 | V _{DD0.3} | V _{DD0.3} | V _{DD0.3} |
| E | TTIP3 | TTIP3 | TCHCLK3 | N.C. | RV _{SS} | RTIP3 | MODEC[0] | DV _{DD} | DV _{DD} | DV _{DD} | TCLK02 | TPOSO2 | TSSYNC2 | RFSYNC2 | \overline{INT} | D4 | A6 | A4 | V _{DD0.3} | MDC |
| F | TRING3 | TRING3 | TNEG03 | TPOSO3 | RV _{SS} | RRING3 | RV _{DD} | DV _{DD} | DV _{DD} | DV _{DD} | V _{SS} | DV _{SS} | RMSYNC2 | V _{SS} | $\overline{RD}/\overline{DS}$ | D3 | D2 | V _{DD0.3} | V _{DD0.3} | MDIO |
| G | TV _{DD} | TVDD | TCLK03 | V _{SS} | V _{SS} | RV _{SS} | V _{SS} | BPCLK2 | RNEGO2 | DV _{SS} | DV _{SS} | V _{SS} | JTMS1 | $\overline{JTRST1}$ | MODEC[1] | V _{DD0.3} | D0 | QOVF | REF_CLKO | V _{SS} |
| H | RCLK3 | TSIG3 | DV _{SS} | TSYSCLK1 | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | RSIG2 | RV _{SS} | RV _{SS} | JTD01 | \overline{RST} | \overline{CS} | N.C. | RXD[1] | RXD[3] | V _{SS} |
| J | DV _{SS} | TSERI3 | TCLKT3 | DV _{DD} | TSYSCLK2 | V _{SS} | V _{SS} | V _{SS} | V _{SS} | RPOSO2 | RV _{SS} | RRING2 | RTIP2 | RV _{DD} | V _{SS} | V _{DD0.8} | JTCLK1 | RXD[2] | RXD[0] | V _{SS} |
| K | RSYSCLK1 | MCLK1 | V _{SS} | RSERO1 | V _{SS} | V _{SS} | V _{SS} | V _{SS} | RSERO2 | RSYSCLK2 | N.C. | N.C. | RMIMIS | TCLKE | TSERO | TBSYNC | JTDI1 | RX_DV | RX_CLK | RX_ERR |
| L | RV _{SS} | TSTRST | BPCLK1 | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | TCHCLK4 | JTD02 | JTMS2 | MCLK2 | $\overline{JTRST2}$ | RCLK1 | RBSYNC | RSERI | DCEDTES | TX_CLK | TX_EN | TXD[0] |
| M | RRING1 | RV _{SS} | RSIG1 | TCHBLK1 | V _{SS} | V _{SS} | V _{SS} | RCHBLK4 | RSYNC4 | RFSYNC4 | TCLK04 | V _{SS} | V _{DD0.8} | SDATA[3] | SDATA[1] | V _{SS} | V _{DD0.8} | TXD[2] | TXD[1] | TXD[3] |
| N | RTIP1 | RV _{SS} | RPOSO1 | RNEGO1 | DV _{SS} | DV _{SS} | RCLK4 | DV _{SS} | TCLKT4 | TNEG04 | TPOSO4 | V _{SS} | TSSYNC4 | V _{DD0.8} | V _{DD0.8} | V _{DD0.8} | V _{DD0.8} | V _{SS} | RX_CRS/CRS_DV | COL_DET |
| P | RV _{DD} | RCHCLK1 | RCHBLK1 | TNEG01 | DV _{SS} | TSYNC4 | TSIG4 | DV _{SS} | JTCLK2 | RCLK04 | TCHBLK4 | V _{SS} | V _{SS} | SDMASK[1] | \overline{SPRAS} | SDA[11] | V _{DD0.8} | SDMASK[2] | SDATA[18] | SDATA[19] |
| R | RFSYNC1 | RLOS/LOT1 | TPOSO1 | TCLK01 | DV _{SS} | DV _{SS} | TSERI4 | RV _{DD} | RRING4 | RV _{SS} | V _{SS} | SDATA[12] | SDATA[6] | SCAS | \overline{SDCS} | SBA[0] | SDA[10] | SDATA[31] | V _{SS} | V _{DD0.8} |
| T | TTIP1 | TV _{SS} | DV _{SS} | DV _{SS} | DV _{SS} | DV _{SS} | RSERO4 | RV _{SS} | RTIP4 | RV _{SS} | SDATA[13] | SDATA[14] | SDATA[5] | V _{DD0.8} | \overline{SWE} | SDA[8] | SDA[0] | SDATA[16] | SDATA[27] | SDATA[26] |
| U | TTIP1 | TV _{SS} | N.C. | TCLKT1 | DV _{SS} | DV _{SS} | RPOSO4 | RSIG4 | DV _{SS} | DV _{SS} | SDATA[15] | SDATA[4] | V _{SS} | SDCLKO | V _{SS} | SDA[1] | SDA[4] | SDATA[29] | SDATA[25] | SDATA[24] |
| V | TRING1 | TV _{DD} | N.C. | RCLK01 | TSIG1 | RNEGO4 | RCHCLK4 | RLOS/LOT4 | RMSYNC4 | DV _{SS} | SDATA[11] | SDATA[10] | SDATA[8] | V _{SS} | SDA[9] | SDA[7] | SDMASK[3] | SDATA[30] | SDATA[22] | V _{DD0.8} |
| W | TRING1 | TV _{DD} | TSYNC1 | TSSYNC1 | RCLK1 | \overline{CST} | TV _{SS} | TTIP4 | TRING4 | TV _{DD} | SDATA[0] | SDATA[9] | SDATA[7] | V _{DD0.8} | SBA[1] | SDA[5] | SDA[3] | SDATA[17] | SDATA[20] | SDATA[23] |
| Y | RMSYNC1 | RSYNC1 | TCHCLK1 | TSERI1 | TSYSCLK4 | RSYSCLK4 | TV _{SS} | TTIP4 | TRING4 | TV _{DD} | SDATA[2] | V _{SS} | SDMASK[0] | SYCLKI | V _{DD0.8} | SDA[6] | SDA[2] | V _{DD0.8} | SDATA[28] | SDATA[21] |

8 FUNCTIONAL DESCRIPTION

The DS33R41 provides interconnection and mapping functionality between Ethernet Packet Systems and T1/E1/J1 WAN Time-Division Multiplexed (TDM) systems. The device is composed of a 10/100 Ethernet MAC, Packet Arbiter, Committed Information Rate Controller (CIR), HDLC/X.86 (LAPS) Mapper, SDRAM interface, control ports, four Bit Error Rate Testers (BERTs), and four integrated T1/E1/J1 Transceivers. The packet interface consists of a MII/RMII Ethernet PHY interface. The Ethernet interface can be configured for 10Mbps or 100Mbps service. The DS33R41 encapsulates Ethernet traffic with HDLC or X.86 (LAPS) encoding to be transmitted over up to four T1, E1, or J1 lines. The T1/E1/J1 interfaces also receive encapsulated Ethernet packets and transmit the extracted packets over the Ethernet ports. Access is provided between the Serial port and the integrated T1/E1/J1 Transceivers to the intermediate signal bus that is based on the Dallas Semiconductor Integrated Bus Operation (IBO), running at 8.192Mbps.

The Ethernet Packet interface supports both MII and RMII mode, allowing the DS33R41 to connect to commercially available Ethernet PHY and MAC devices. The Ethernet interface can be individually configured for 10Mbps or 100Mbps service, in DTE and DCE configurations. The DS33R41 MAC interface can be configured to reject frames with bad FCS and short frames (less than 64 bytes).

Ethernet frames are queued and stored in external 32-bit SDRAM. The DS33R41 SDRAM controller enables connection to a 128Mbit SDRAM without external glue logic, at clock frequencies up to 100MHz. The SDRAM is used for both the Transmit and Receive Data Queues. The Receive Queue stores data to be sent from the Packet interface to the WAN interface. The Transmit Queue stores data to be sent from the WAN interface to the Packet interface. The external SDRAM can accommodate up to 8192 frames with a maximum frame size of 2016 bytes. The sizing of the queues can be adjusted by software. The user can also program high and low watermarks for each queue that can be used for automatic or manual flow control. The packet data stored in the SDRAM is encapsulated in HDLC or X.86 (LAPS) to be transmitted over the WAN interfaces. The device also provides the capability for bit and packet scrambling.

The WAN interface also receives encapsulated Ethernet packets and transmits the extracted packets over the Ethernet port. The WAN physical interface supports up to 4 serial data streams on a 8.192Mbps IBO bus. The WAN serial port can operate with a gapped clock, and can be connected to a framer or T/E-Carrier transceiver for transmission to the WAN. The WAN interface can be seamlessly connected to the Dallas Semiconductor/Maxim T1/E1/J1 Framers and Single-Chip Transceivers (SCTs).

The DS33R41 can be configured through an 8-bit microprocessor interface port. The DS33R41 also provides 2 on-board clock dividers for the System Clock input and Reference Clock Input for the 802.3 interfaces, further reducing the need for ancillary devices.

The four integrated T1/E1/J1 transceivers can be software configured for T1, E1, or J1 operation. Each transceiver is composed of a line interface unit (LIU), framer, dual HDLC controllers, and a TDM backplane interface. The transceivers are software compatible with the DS21455, DS21458, and the older DS21Q55.

The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0dB to 43dB or 0dB to 12dB for E1 applications and 0dB to 15dB or 0dB to 36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications) and can be placed in either transmit or receive data paths.

On the transmit side, clock/data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns and alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock/data and frame-sync signals to the backplane interface section.

Both the transmit and receive path have two HDLC controllers. The HDLC controllers transmit and receive data via the framer block. The HDLC controllers can be assigned to any time slot, group of time slots, portion of a time slot, or to FDL (T1) or Sa bits (E1). Each controller has 128-bit FIFOs, thus reducing the amount of processor overhead required to manage the flow of data. In addition, built-in support for reducing the processor time required handles SS7 applications.

The backplane interface of the integrated transceivers provides a method of sending and receiving data from the integrated Ethernet Mapper over an interleaved 8.192MHz TDM (IBO) bus. The Elastic Stores are required for IBO operation, and manage slip conditions.

The parallel port provides access for control and configuration of all the transceiver's features. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection.

8.1 Processor Interface

Microprocessor control of the DS33R41 is accomplished through the interface pins of the microprocessor port. The 8-bit parallel data bus can be configured for Intel or Motorola modes of operation with the two MODEC[0:1] pins. When MODEC = 00, bus timing is in Intel mode, as shown in [Figure 14-9](#) and [Figure 14-10](#). When MODEC = 01, bus timing is in Motorola mode, as shown in [Figure 14-11](#) and [Figure 14-12](#). The address space is mapped through the use of 10 address lines, A0 – A9. Multiplexed Mode is not supported on the processor interface.

The Chip Select (\overline{CS}) pin must be brought to a logic low level to gain read and write access to the microprocessor port of the Ethernet Mapper. The \overline{CS} pin must be brought to a logic low level to gain read and write access to the microprocessor port of the integrated T1/E1 transceivers. With Intel timing selected, the Read (\overline{RD}) and Write (\overline{WR}) pins are used to indicate read and write operations and latch data through the interface. With Motorola timing selected, the Read-Write (\overline{RW}) pin is used to indicate read and write operations while the Data Strobe (\overline{DS}) pin is used to latch data through the interface.

The interrupt output pin (\overline{INT}) is an open-drain output that will assert a logic-low level upon a number of software maskable interrupt conditions. This pin is normally connected to the microprocessor interrupt input. The register map is shown in [Table 12-1](#).

8.1.1 Read-Write/Data Strobe Modes

The processor interface can operate in either read-write strobe mode or data strobe mode. When $MODEC = 00$ the read-write strobe mode is enabled and a negative pulse on \overline{RD} performs a read cycle, and a negative pulse on \overline{WR} performs a write cycle. When $MODEC = 01$ the data strobe mode is enabled and a negative pulse on \overline{DS} when \overline{RW} is high performs a read cycle, and a negative pulse on \overline{DS} when \overline{RW} is low performs a write cycle. The read-write strobe mode is commonly called the “Intel” mode, and the data strobe mode is commonly called the “Motorola” mode. See the timing diagrams in the *AC Electrical Characteristics* for more details.

8.1.2 Clear on Read

The latched status registers will clear on a read access. It is important to note that in a multi-task software environment, the user should handle all status conditions of each register at the same time to avoid inadvertently clearing status conditions. The latched status register bits are carefully designed so that an event occurrence cannot collide with a user read access.

8.1.3 Interrupt and Pin Modes

The interrupt (\overline{INT}) pin is configurable to drive high or float when not active. The $INTM$ bit controls the pin configuration, when it is set the \overline{INT} pin will drive high when not active. After reset, the \overline{INT} pin is in high impedance mode until an interrupt source is active and enabled to drive the interrupt pin.

9 ETHERNET MAPPER

9.1 Ethernet Mapper Clocks

The DS33R41 clocks sources and functions are as follows:

- Serial Transmit Data (TCLKE) and Serial Receive Data (RCLKI) clock inputs are used to transfer data from the serial interface. These clocks can be continuous or gapped.
- System Clock (SYSCLKI) input. Used for internal operation. This clock input cannot be a gapped clock. A clock supply with ± 100 ppm frequency accuracy is suggested. A buffered version of this clock is provided on the SDCLKO pin for the operation of the SDRAM. A divided and buffered version of this clock is provided on REF_CLKO for the RMII/MII interface.
- Packet Interface Reference clock (REF_CLK) input that can be 25MHz or 50MHz. This clock is used as the timing reference for the RMII/MII interface.
- The Transmit and Receive clocks for the MII Interface (TX_CLK and RX_CLK). In DTE mode, these are input pins and accept clocks provided by an Ethernet PHY. In the DCE mode, these are output pins and will output an internally generated clock to the Ethernet PHY. The output clocks are generated by internal division of REF_CLK. In RMII mode, only the REF_CLK input is used.
- REF_CLKO is an output clock that is generated by dividing the 100MHz System clock (SYSCLKI) by 2 or 4.
- A Management Data Clock (MDC) output is derived from SYSCLKI and is used for information transfer between the internal Ethernet MAC and external PHY. The MDC clock frequency is 1.67MHz.

The following table provides the different clocking options for the Ethernet interface.

Table 9-1. Clocking Options for the Ethernet Interface

| RMII/MII Pin | Speed | DCE/DTE | REF_CLKO Output | REF_CLK Input | RX_CLK | TX_CLK | MDC Output |
|--------------|---------|---------|-----------------|---------------------|-----------------|-----------------|------------|
| 0 (MII) | 10Mbps | DTE | 25MHz | 25MHz ± 100 ppm | Input from PHY | Input from PHY | 1.67MHz |
| 0 (MII) | 10Mbps | DCE | 25MHz | 25MHz ± 100 ppm | 2.5MHz (Output) | 2.5MHz (Output) | 1.67MHz |
| 0 (MII) | 100Mbps | DCE | 25MHz | 25MHz ± 100 ppm | 25MHz (Output) | 25MHz (Output) | 1.67MHz |
| 1 (RMII) | 10Mbps | — | 50MHz | 50MHz ± 100 ppm | Not Applicable | Not Applicable | 1.67MHz |
| 1 (RMII) | 100Mbps | — | 50MHz | 50MHz ± 100 ppm | Not Applicable | Not Applicable | 1.67MHz |

9.1.1 Serial Interface Clock Modes

The Serial Interface timing is determined by the line clocks. 8.192MHz is the required clock rate for interfacing the IBO bus to Dallas Semiconductor Framers and Single-Chip Transceivers. Both the transmit and receive clocks (TCLKE and RCLKI) are inputs.

9.1.2 Ethernet Interface Clock Modes

The Ethernet PHY interface has several different clocking requirements, depending on the mode of operation. [Table 9-1](#) outlines the possible clocking modes for the Ethernet Interface. The buffered REF_CLKO output is generated by division of the 100MHz system clock input by the user on SYSCLKI. The frequency of the REF_CLKO pin is automatically determined by the DS33R41 based on the state of the RMIIMIIS pin. The REF_CLKO output can be used as a REF_CLK for the Ethernet Interface by connecting REF_CLKO to REF_CLK. The REF_CLKO function can be turned off with the [GL.CR1](#).RFOO bit. Note that in DCE and RMI operating modes, the REF_CLKO signal should not be used to provide an input to REF_CLK, due to the reset requirements in these operating modes.

In RMII mode, receive and transmit timing is always synchronous to a 50MHz clock input on the REF_CLK pin. The source of REF_CLK is expected to be the external PHY. The user has the option of using the 50MHz REF_CLKO output as the timing source for the PHY. More information on RMII mode can be found in [Section 9.13.2](#).

While using MII mode with DTE operation, the MII clocks (RX_CLK and TX_CLK) are inputs that are expected to be provided by the external PHY. While using MII mode with DCE operation, the MII clocks (TX_CLK and RX_CLK) are output by the DS33R41, and are derived from the 25MHz REF_CLK input. More information on MII mode can be found in [Section 9.13.1](#).

9.2 Resets and Low-Power Modes

The external $\overline{\text{RST}}$ pin and the global reset bit in [GL.CR1](#) create an internal global reset signal. The global reset signal resets the status and control registers on the chip (except the GL.CR1.RST bit) to their default values and resets all the other flops to their reset values. The processor bus output signals are also placed in high-impedance mode when the $\overline{\text{RST}}$ pin is active (low). The global reset bit (GL.CR1.RST) stays set after a one is written to it, but is reset to zero when the external $\overline{\text{RST}}$ pin is active or when a zero is written to it. Allow 5ms after initiating a reset condition for the reset operation to complete.

The Serial Interface reset bit in [LI.RSTPD](#) resets all the status and control registers on the Serial Interface to their default values, except for the LI.RSTPD.RST bit. The Serial Interface includes the HDLC encoder/decoder, X86 encoder and decoder and the corresponding serial port. The Serial Interface reset bit (LI.RSTPD.RST) stays set after a one is written to it, but is reset to zero when the global reset signal is active or when a zero is written to it.

Table 9-2. Reset Functions

| RESET FUNCTION | LOCATION | COMMENTS |
|------------------------|--------------------------------|--|
| Hardware Device Reset | $\overline{\text{RST}}$ Pin | Transition to a logic 0 level resets the device. |
| Hardware JTAG Reset | $\overline{\text{JTRST1}}$ Pin | Resets the JTAG test port. |
| Global Software Reset | GL.CR1 | Writing to this bit resets the device. |
| Serial interface Reset | LI.RSTPD | Writing to this bit resets a Serial Interface. |
| Queue Pointer Reset | GL.C1QPR | Writing to this bit resets the Queue Pointers |

There are several features in the device to reduce power consumption. The reset bit in the [LI.RSTPD](#) register minimizes power usage in the Serial Interface. Additionally, the $\overline{\text{RST}}$ pin or [GL.CR1](#).RST bit may be held in reset indefinitely to keep the device in a low-power mode. Note that exiting a reset condition requires re-initialization and configuration. For the lowest possible standby current, clocks may be externally gated.

9.3 Initialization and Configuration

EXAMPLE DEVICE INITIALIZATION SEQUENCE:

STEP 1: Apply 3.3V supplies, then apply 1.8V supplies.

STEP 2: Reset the device by pulling the $\overline{\text{RST}}$ pin low or by using the software reset bits outlined in Section [9.2](#). Clear all reset bits. Allow 5ms for the reset recovery.

STEP 3: Reset the integrated T1/E1/J1 Transceivers through hardware using the TSTRST pin or through software using the SFTRST function in the master mode register.

STEP 4: The LIRST (TR.LIC2.6) should be toggled from 0 to 1 to reset the line interface circuitry. Allow 40ms for the reset recovery.

STEP 5: Check the Ethernet Mapper Device ID in the [GL.IDRL](#) and [GL.IDRH](#) registers.

STEP 6: Check the T1/E1/J1 Transceiver Device ID in the TR.IDR register.

STEP 7: Configure the system clocks. Allow the clock system to properly adjust.

STEP 8: Initialize the entire remainder of the register space with 00h (or otherwise if specifically noted in the register's definition), including the reserved bits and reserved register locations.

STEP 9: Write FFFFFFFFh to the MAC indirect addresses 010Ch through 010Fh.

STEP 10: Setup connection in the GL.CON1 register.

STEP 11: Configure the Serial Port register space as needed.

STEP 12: Configure the Ethernet Port register space as needed.

STEP 13: Configure the Ethernet MAC indirect registers as needed.

STEP 14: Configure the T1/E1/J1 Framer as needed.

STEP 15: Configure the T1/E1/J1 LIU as needed.

STEP 16: Configure the external Ethernet PHY through the MDIO interface.

STEP 17: Enable the elastic store on each of the integrated T1/E1 transceivers.

STEP 18: Configure each T1/E1 transceiver's position on the IBO bus through TR.IBOC.

STEP 19: Choose a T1/E1 transceiver to as the 8kHz frame sync source, and configure its RSYNC as an output.

STEP 20: Clear all counters and latched status bits.

STEP 21: Set Queue sizes in the Arbiter and reset the queue pointers for the Ethernet and serial interfaces.

STEP 22: After the TSYCLK and RSYCLK inputs to the T1/E1/J1 transceivers are stable, the receive and transmit elastic stores should be reset.

STEP 23: Enable Interrupts as needed.

STEP 24: Initiate link aggregation as discussed in Section [9.8](#).

STEP 25: Begin handling interrupts and latched status events.

9.4 Global Resources

In order to maintain software compatibility with the multiport devices in the product family, a set of Global registers are located at 0F0h-0FFh. The global registers include Global resets, global interrupt status, interrupt masking, clock configuration, and the Device ID registers. See the Global Register Definitions in [Table 12-2](#).

9.5 Per-Port Resources

Multi-port devices in this product family share a common set of global registers and Arbiters. All other resources are per-port.

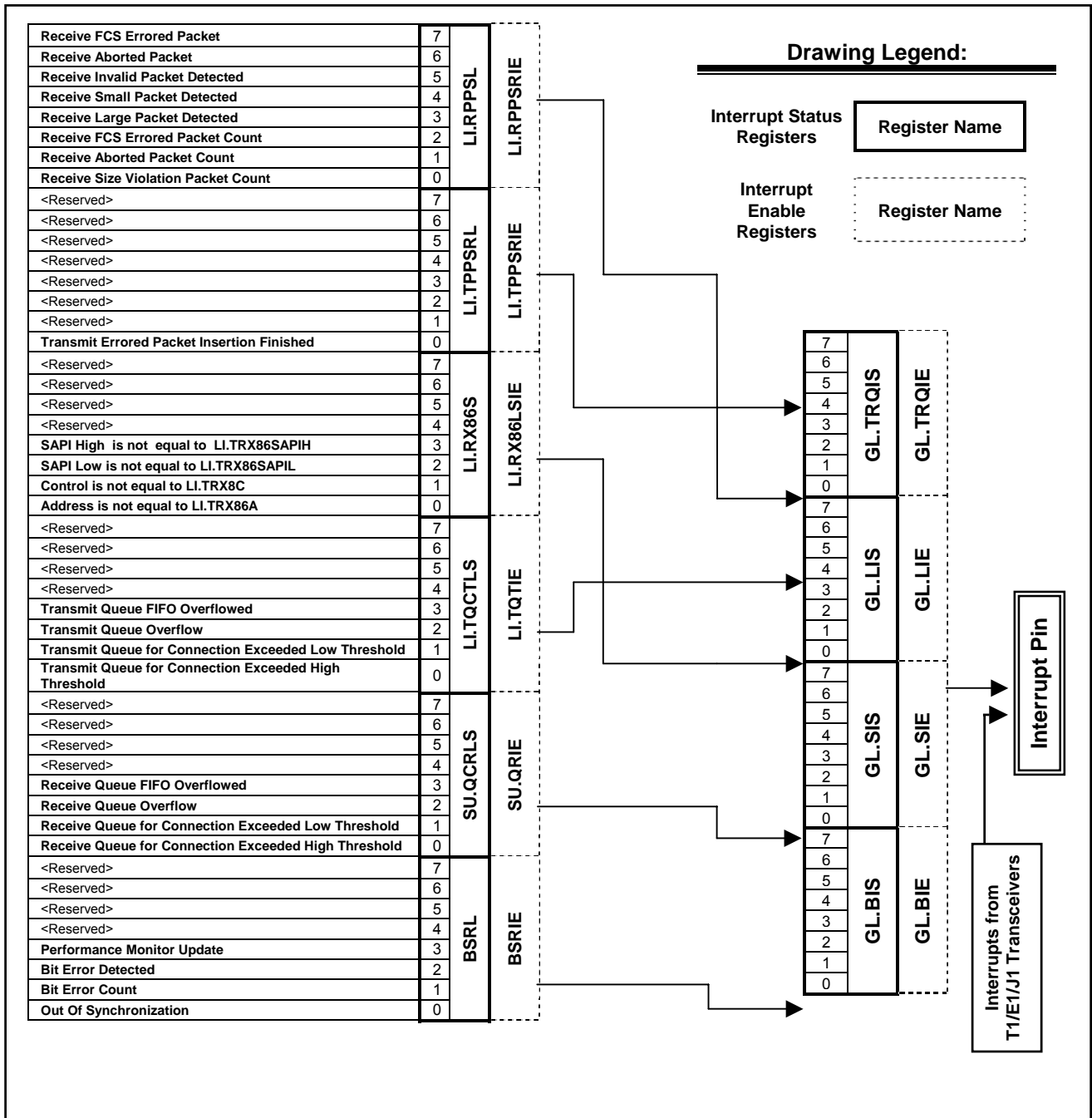
9.6 Device Interrupts

[Figure 9-2](#) diagrams the flow of interrupt conditions from their source status bits through the multiple levels of information registers and mask bits to the interrupt pin. When an interrupt occurs, the host can read the Global Latched Status registers [GL.LIS](#), [GL.SIS](#), [GL.IBIS](#), [GL.TRQIS](#), [GL.IMXSLS](#), [GL.IMXDFDELS](#), and [GL.IMXOOFLS](#) to initially determine the source of the interrupt. The host can then read the [LI.TQCTLS](#), [LI.TPPSRL](#), [LI.RPPSRL](#), [LI.RX86S](#), [SU.QCRLS](#), and BSRL registers to further identify the source of the interrupt(s). In order to maintain software compatibility with the multiport devices in the product family, the global interrupt status and interrupt enable registers have been preserved, but do not need to be used. If [GL.TRQIS](#) is determined to be the interrupt source, the host will then read the [LI.TPPSRL](#) and [LI.RPPSRL](#) registers for the cause of the interrupt. If [GL.LIS](#) is determined to be the interrupt source, the host will then read the [LI.TQCTLS](#), [LI.TPPSRL](#), [LI.RPPSRL](#), and [LI.RX86S](#) registers for the source of the interrupt. If [GL.SIS](#) is the source, the host will then read the [SU.QCRLS](#) register for the source of the interrupt. If [GL.IBIS](#) is the source, the host will then read the BSRL register for the source of the interrupt. All Global Interrupt Status Register bits are real-time bits that will clear once the appropriate interrupt has been serviced and cleared, as long as no additional, enabled interrupt conditions are present in the associated status register. All Latched Status bits must be cleared by the host writing a "1" to the bit location of the interrupt condition that has been serviced. In order for individual status conditions to transmit their status to the next level of interrupt logic, they must be enabled by placing a "1" in the associated bit location of the correct Interrupt Enable Register. The Interrupt enable registers are [LI.TPPSRIE](#), [LI.RPPSRIE](#), [LI.RX86LSIE](#), BSRIE, SU.QRIE, GL.LIE, GL.SIE, GL.IBIE, GL.TRQIE, GL.IMXSIE, GL.IMXDFEIE, and GL.IMXOOFIE. Latched Status bits that have been enabled via Interrupt Enable registers are allowed to pass their interrupt conditions to the Global Interrupt Status Registers. The Interrupt enable registers allow individual Latched Status conditions to generate an interrupt, but when set to zero, they do not prevent the Latched Status bits from being set. Therefore, when servicing interrupts, the user should AND the Latched Status with the associated Interrupt Enable Register in order to exclude bits for which the user wished to prevent interrupt service. This architecture allows the application host to periodically poll the latched status bits for non-interrupt conditions, while using only one set of registers. Note the bit-orders of SU.QRIE and SU.QCRLS are different.

Note that the inactive state of the interrupt output pin is configurable. The INTM bit in [GL.CR1](#) controls the inactive state of the interrupt pin, allowing selection of a pull-up resistor or active driver.

The interrupt structure is designed to efficiently guide the user to the source of an enabled interrupt source. The latched status bits for the interrupting entity must be read to clear the interrupt. Also reading the latched status bit will reset all bits in that register. During a reset condition, interrupts cannot be generated. The interrupts from any source can be blocked at a global level by the placing a zero in the global interrupt enable registers ([GL.LIE](#), [GL.SIE](#), [GL.IBIE](#), [GL.TRQIE](#), [GL.IMXSIE](#), [GL.IMXDFEIE](#), and [GL.IMXOOFIE](#)). Reading the Latched Status bit for all interrupt generating events will clear the interrupt status bit and Interrupt signal will be deasserted.

Figure 9-2. Device Interrupt Information Flow Diagram



9.7 Serial Interface

The Serial Interface consists of physical serial port, IMUX/IBO Formatter, and HDLC/X.86 engine. The Serial Interface supports time-division multiplexed serial data, in a format compatible with Dallas Semiconductor's 8.192Mbps Channel Interleaved Bus Operation (IBO). The Serial Interface receives and transmits the encapsulated Ethernet packets. The physical interface consists of Transmit Data, Transmit Clock, Transmit Synchronization, Receive Data, Receive Clock, and Receive Synchronization. The Serial Interface can be seamlessly connected to the IBO bus of the four integrated Single-Chip Transceivers (SCTs).

- Byte-aligned data is always input through the RSERI pin at a rate of 8.192Mbps. RSYNC is an 8kHz reference input used to determine the position of channel 1 for the first T1/E1 link. Note that if the device is configured to use less than four T1/E1 links, the time slots on the RSERI input to the Ethernet Mapper associated with the unused links must be all 1s.
- Data on the IBO bus is byte-interleaved (by channel) for up to 4 T1/E1 interfaces, and is "byte-striped" across the available links. The Channel 1 byte arrives (MSB first) for all four T1/E1 links, followed by the Channel 2 byte for all four T1/E1 links, etc.
- Channel 1 is never used for data. In T1 mode, channels 5, 9, 13, 17, 21, 25, 29 are also not used for data. Bytes for all unused timeslots will be replaced with FFh. All four TDM links must be configured for T1 operation, or all 4 links must be configured for E1 operation.
- Channel 2 is reserved for link management and coordination. This timeslot is used for inter-node communication to initiate, control, and monitor the IMUX function. The IMUX operation is initiated with a handshaking procedure and if successful, followed by a data phase. There is no data transfer during the handshaking phase. During data transfer, channel 2 is used to provide frame sequence numbers. The receiver uses the sequence numbers (0-63) to reassemble the frames to compensate for a differential delay of up to 7.75ms. If the differential delay exceeds 7.75ms, packet errors will occur.
- Byte-aligned data is output on the TSERO pin at a rate of 8.192Mbps. TSYNC is used as an 8kHz synchronization for the TSERO data and is used to determine the position of channel 1 for the first T1/E1 link. If the device is configured to use less than four T1/E1 links, data bytes on TSERO associated with the unused links are set to FFh.

9.8 Link Aggregation (IMUX)

The DS33R41 has a link aggregation feature that allows data from the Ethernet interface to be inverse-multiplexed over up to four aggregated T1/E1 links. The T1/E1 data streams are input and output from the device on an 8.192Mbps Interleaved Bus (IBO). The IMUX function is shown graphically in [Figure 9-3](#) and [Figure 9-4](#).

Figure 9-3. IMUX Interface to T1/E1 Transceivers

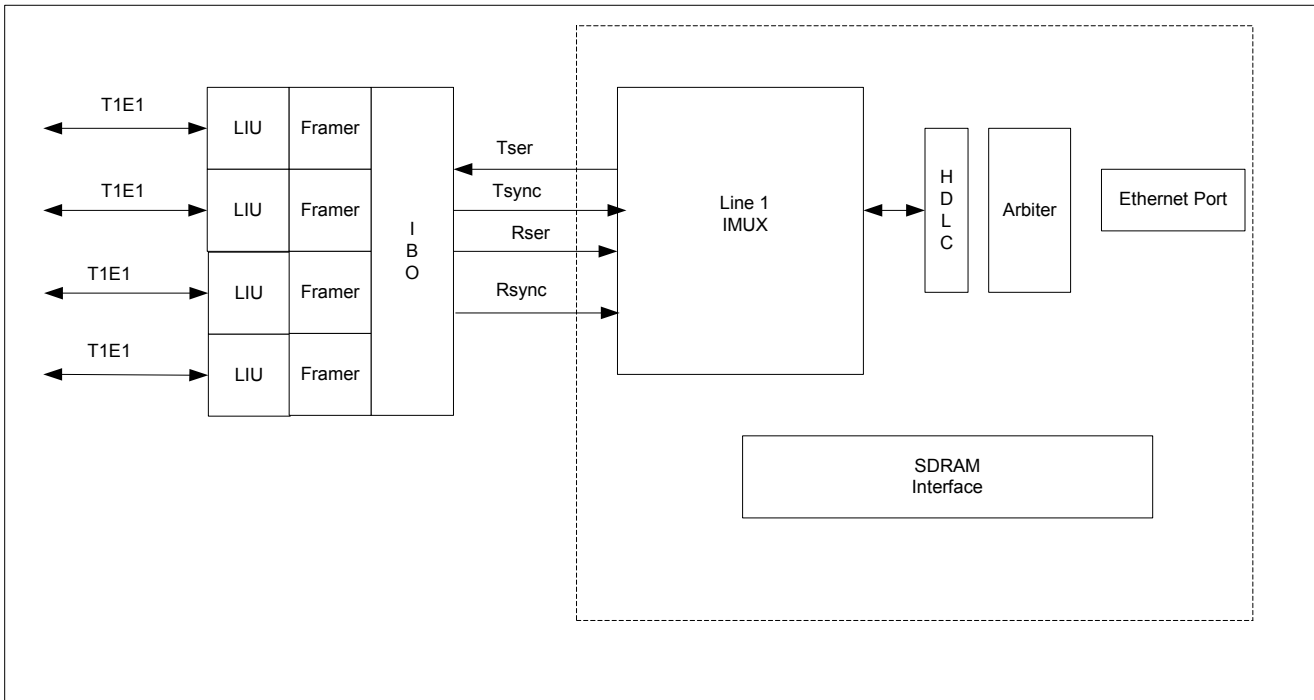
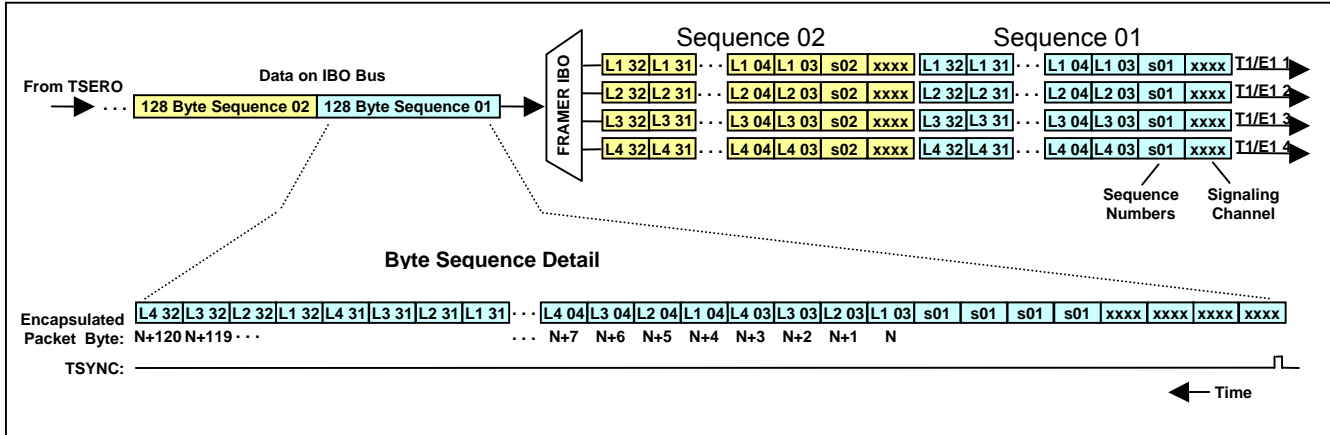


Figure 9-4. Diagram of Data Transmission with IMUX Operation



9.8.1 Microprocessor Requirements

Link aggregation requires an external host microprocessor to issue instructions and to monitor the IMUX function of the device. The host microprocessor is responsible for the following tasks to open a transmit channel:

- Configuring [GL.IMXCN](#) to control the links participating in the aggregation.
- Issuing a link start command through [GL.IMXC](#).
- Monitoring the ITSYNC1-4 status from [GL.IMXSS](#) or [GL.IMXSLS](#).
- Monitoring [GL.IMXDFDELS](#).IDDELS0 to ensure that differential delay is not larger than 7.75ms.
- Setting [GL.IMXCN](#).SENDE to begin transmitting data after all links are synchronized.
- Resetting the queue pointers in [GL.C1QPR](#).
- Monitoring the TOOFLS1-4 status from [GL.IMXOOFLS](#) to restart handshaking procedure if needed.

The host microprocessor is also responsible for the following tasks to open a receive channel:

- Monitoring the status of IRSYNC1-4 and setting [GL.IMXCN](#).RXE to receive data.

When in the data phase, if any of the links are detected to be out of frame (OOF), data will be corrupted. The link initialization procedure must be initiated again. Note that the serial HDLC or X.86 encoded data is sent on 4 T1/E1 links, each link will not have separate HDLC/X.86 encoded data. The HDLC/X.86 encoding and decoding is data is only available when the device has performed IMUX function. Hence on the line the FCS for a given HDLC packet could transport on a separate link than the HDLC data.

9.8.2 IMUX Command Protocol

The format for all commands sent and received in Channel 2 of the IBO Serial Interface is shown in [Figure 9-5](#). The MSB for all commands is a "1." The next 6 bits contain the actual opcode for the command. The LSB is the even parity calculation for the byte. These commands will be sent and received on Channel 2 of each of the T1/E1 interleaved IBO data. The commands that are possible are outlined in [Table 9-3](#). Note that the 4 portions of the IMUX link are separate and the Channel 2 for each link will send and receive commands specific to that link. The microprocessor can disable links that are not to be aggregated.

Figure 9-5. Command Structure for IMUX Function

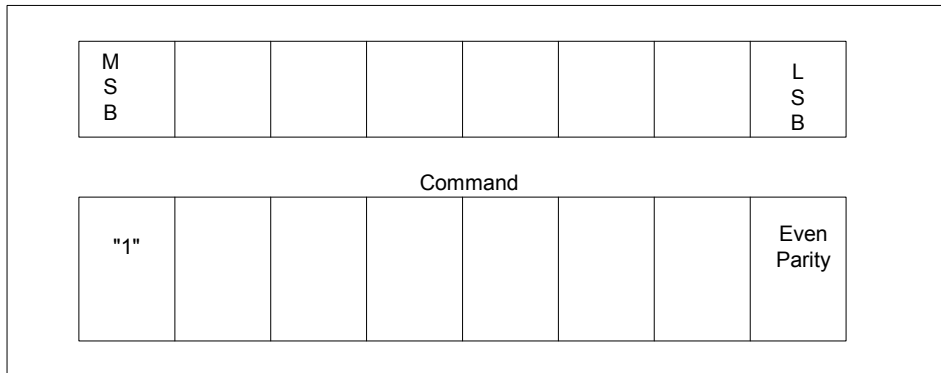


Table 9-3. Commands Sent and Received on the IMUX Links

| COMMAND NAME | COMMAND BYTE (P IS EVEN PARITY) | TRANSMIT / RECEIVE | COMMENTS |
|--------------|---------------------------------|--------------------|---|
| Link Start | 1000 001P | Tx or Rx | Initiate the link. The receiver will then search for 3 consecutive sequence numbers. |
| Sequence | 1sss 010P | Tx or Rx | "sss" contains the frame sequence number for packet segmentation and reassembly. |
| Rsync | 1000 011P | Tx or Rx | This command is sent to indicate to the distant node that link synchronization has been achieved. |
| OOF | 1000 100P | Tx or Rx | The transmitting device has detected an out of frame condition. |
| Nop | 1111 111P | Tx or Rx | No operation. |

The command and status registers for the IMUX function are detailed below:

Table 9-4. Command and Status for the IMUX for Processor Communication

| REGISTER | NAME | COMMENTS |
|--|-----------------------------|---|
| IMUX Configuration Register | GL.IMXCN | Used to configure the number of links participating and select T1 or E1. |
| IMUX Command Register | GL.IMXC | Used to issue commands for link management |
| IMUX Sync Status Register | GL.IMXSS | Provides the real time sync status of the 4 transmit and receive links |
| IMUX Sync Latched Status Register | GL.IMXSLS | Latched status register for the IMXSS register. |
| IMUX Interrupt Mask Register | GL.IMXSIE | Interrupt enable bits for Sync Latched Status bits |
| Differential Delay Register | GL.IMXDFD | Provides the largest differential delay value for the receive path. Measured only at link initialization. |
| Differential Delay Error Interrupt Enable Register | GL.IMXDIE | Interrupt enable for the differential delay register. |
| Differential Delay Latched Status Register | GL.IMXDLELS | Latched Status for GL.IMXDFD. Note that differential delay is measured only at link initiation. |
| OOF Interrupt Enable | GL.IMXOOFIE | Interrupt enable for the IMXOOFLS register. |
| OOF Latched Status Register | GL.IMXOOFLS | Indicates out of frame conditions for both ends of the communication. If detected, the user must re-initiate all links. |

9.8.3 Out of Frame (OOF) Monitoring

Once the links are in synchronization, frame synchronization monitoring is started. The device will declare an out of frame (OOF) if 2 consecutive sequence errors are received. The device automatically adjusts for single-frame slips by increasing or decreasing the expected frame sequence number. If a frame sequence number is neither repeated nor skipped by one (indicating a single-frame slip), it is considered a sequence error. Two consecutive frames with sequence errors result in an OOF state being declared. The OOF state is used to set OOF Latched bits in [GL.IMXOOFLS](#) and an OOF command is sent to the distant end. If an OOF command is received from the distant end, the latched status register will be updated.

9.8.4 Data Transfer

Once synchronization is established, data transfer is enabled by the microprocessor setting the [GL.IMXCN.RXE](#) and [GL.IMXCN.SENDE](#) bits. The user must then reset the queue pointers ([GL.C1QPR](#)) for proper data transfer. Data is byte-stripped across the available links.

9.9 Connections and Queues

The multi-port devices in this product family provide bi-directional cross-connections between the multiple Ethernet ports and Serial ports when operating in software mode. A single connection is preserved in this single-port device to provide software compatibility with multi-port devices. The connection will have an associated transmit and receive queue. Note that the terms “Transmit Queue” and “Receive Queue” are with respect to the Ethernet Interface. The Receive queue is for data arriving from Ethernet interface to be transmitted to the WAN interface. The Transmit queue is for data arriving from the WAN to be transmitted to the Ethernet interface. Hence the transmit and receive direction terminology is the same as is used for the Ethernet MAC port.

The user can define the connection and the size of the transmit and receive queues. The size is adjustable in units of 32 (by 2048 byte) packets. The external SDRAM can hold up to 8192 packets of data. The user must ensure that all the connection queues do not exceed this limit. The user also must ensure that the transmit and receive queues do not overlap each other. Unidirectional connections are not supported.

When the user changes the queue sizes, the connection must be torn down and re-established. When a connection is disconnected all transmit and receive queues associated with the connection are flushed and a “1” is sourced towards the Serial transmit and the HDLC receiver. The clocks to the HDLC are sourced a “0.”

The user can also program High and Low watermarks. If the queue size grows past the High watermark, an interrupt is generated if enabled. The registers of relevance are described in [Table 9-5](#). The [AR.TQSC1](#) size provides the size of the transmit queue for the connection. The High Watermark will set a latched status bit. The latched status bit will clear when the register is read. The status bit is indicated by [LI.TQCTLS](#).TQHTS. Interrupts can be enabled on the latched bit events by [LI.TQTIE](#). A latched status bit ([LI.TQCTLS](#).TQLTS) is also set when the queue crosses a low watermark.

The Receive Queue functions in a similar manner. Note that the user must ensure that sizes and watermarks are set in accordance with the configuration speed of the Ethernet and Serial interfaces. The device does not provide error indication if the user creates a connection and queue that overwrites data for another connection queue. The user must take care in setting the queue sizes and watermarks. The registers of relevance are [AR.RQSC1](#) and [SU.QCRLS](#). Queue size should never be set to 0.

It is recommended that the user reset the queue pointers for the connection after disconnection. The pointers must be reset before a connection is made. If this disconnect/connect procedure is not followed, incorrect data may be transmitted. The proper procedure for setting up a connection follows:

- Set up the queue sizes for both transmit and receive queue ([AR.TQSC1](#) and [AR.RQSC1](#)).
- Set up the high/low thresholds and interrupt enables if desired ([GL.TRQIE](#), [LI.TQTIE](#), [SU.QRIE](#))
- Reset all the pointers for the connection desired ([GL.C1QPR](#))
- Set up the connections ([GL.CON1](#))
- If a connection is disconnected, reset the queue pointers after the disconnection.

Table 9-5. Registers Related to Connections and Queues

| REGISTER | NAME | FUNCTION |
|--|---------------------------|---|
| Connection Register for Ethernet Interface 1 | GL.CON1 | Enables connection between the Ethernet Interface and the Serial Interface. Note that once connection is set up, then the queues and thresholds can be setup for that connection. |
| Arbiter Transmit Queue Size Connection 1 | AR.TQSC1 | Size for the Transmit Queue in Number of 32—2K packets. |
| Arbiter Receive Queue Size Connection 1 | AR.RQSC1 | Size for the Receive Queue in Number of 32—2K packets. |
| Global Transmit Receive Queue Interrupt Enable | GL.TRQIE | Interrupt enable for items related to the connections at the global level. |
| Global Transmit Receive Queue Interrupt Status | GL.TRQIS | Interrupt enable status for items related to the connections at the global level. |
| Serial Interface Transmit Queue Cross Threshold Interrupt Enable | LI.TQTIE | Enables for the Transmit queue crossing high and low thresholds. |
| Serial Interface Transmit Queue Cross Threshold Latched Status | LI.TQCTLS | Latched status bits for connection high and low thresholds for the transmit queue. |
| Receive Queue Cross Threshold Enable | SU.QRIE | Enables for the receive queue crossing high and low thresholds. |
| Queue Cross Threshold Latched Status | SU.QCRLS | Latched status bits for receive queue high and low thresholds. |
| Connection 1 Queue Pointer Reset | GL.C1QPR | Resets the connection pointer. |

9.10 Arbiter

The Arbiter manages the transport between the Ethernet port and the Serial port. It is responsible for queuing and dequeuing packets to a single external SDRAM. The arbiter handles requests from the HDLC and MAC to transfer data to and from the SDRAM.

9.11 Flow Control

Flow control may be required to ensure that data queues do not overflow and packets are not lost. The device allows for optional flow control based on the queue high watermark or through host processor intervention. There are 2 basic mechanisms that are used for flow control:

- In half duplex mode, a jam sequence is sent that causes collisions at the far end. The collisions cause the transmitting node to reduce the rate of transmission.
- In full duplex mode, flow control is initiated by the receiving node sending a pause frame. The pause frame has a timer parameter that determines the pause timeout to be used by the transmitting node.

Note that the terms “transmit queue” and “receive queue” are with respect to the Ethernet Interface. The Receive Queue is the queue for the data that arrives on the MII/RMII interface, is processed by the MAC and stored in the SDRAM. Transmit queue is for data that arrives from the Serial port, is processed by the HDLC and stored in the SDRAM to be sent to the MAC transmitter.

The following flow control options are possible:

- Automatic flow control can be enabled in software mode with the [SU.GCR.ATFLOW](#) bit. Note that the user does not have control over [SU.MACFCR.FCE](#) and [FCB](#) bits if [ATFLOW](#) is set. The mechanism of sending pause or jam is dependent only on the receive queue high threshold.
- Manual flow control can be performed through software when [SU.GCR.ATFLOW](#)=0. The host processor must monitor the receive queues and generate pause frames (full duplex) and/or jam bytes through the [SU.MACFCR.FCB](#), [SU.GCR.JAME](#), and [SU.MACFCR.FCE](#) bits.

Note that in order to use flow control, the receive queue size (in [AR.RQSC1](#)) must be 02h or greater. The receive queue high threshold (in [SU.RQHT](#)) must be set to 01h or greater, but must be less than the queue size. If the high threshold is set to the same value as the queue size, automatic flow control will not be effective. The high threshold must always be set to less than the corresponding queue size.

The following table provides all of the flow control options for the device.

Table 9-6. Options for Flow Control

| OPTION | MODE | | | |
|----------------------------|--|---|-------------------------------------|---|
| | Half Duplex; Manual Flow Control | Half Duplex; Automatic Flow Control | Full Duplex; Manual Flow Control | Full Duplex; Automatic Flow Control |
| ATFLOW Bit | 0 | 1 | 0 | 1 |
| JAME Bit | Controlled By User | Controlled Automatically | N/A | N/A |
| FCB Bit (Pause) | NA | NA | Controlled by User | Controlled Automatically |
| FCE Bit | Controlled by User | Controlled Automatically | Controlled by User | Controlled Automatically |
| Pause Timer | N/A | N/A | Programmed by User | Programmed by User |

9.11.1 Full Duplex Flow Control

Automatic flow control is enabled by default. The host processor can disable this functionality with [SU.GCR.ATFLOW](#). The flow control mechanism is governed by the high watermarks ([SU.RQHT](#)). The [SU.RQLT](#) low threshold can be used as indication that the network congestion is clearing up. The value of [SU.RQLT](#) does not affect the flow control. When the connection queue high threshold is exceeded the device will send a pause frame with the timer value programmed by the user. See [Table 9-8](#) for more information. It is recommended that 80 slots (80 by 64 bytes or 5120 bytes) be used as the standard timer value.

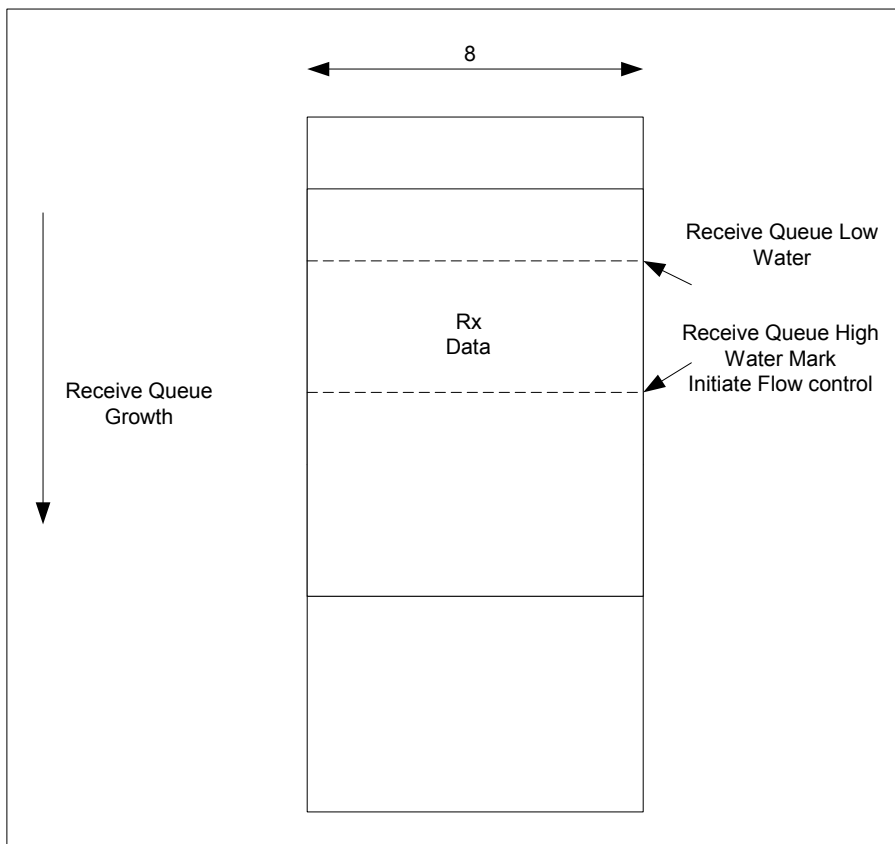
The pause frame causes the distant transmitter to “pause for a time” before starting transmission again. The pause command has a multicast address 01-80-62-00-00-01. The high and low thresholds for the receive queue are

configurable by the user but it is recommended that the high threshold be set approximately 96 packets from the maximum size of the queue and the low threshold 96 packets lower than the high threshold. The device will send a pause frame as the queue has crossed the high threshold and a frame is received. Pause is sent every time a frame is received in the “high threshold state.” Pause control will only take care of temporary congestion. Pause control does not take care of systems where the traffic throughput is too high for the queue sizes selected. If the flow control is not effective the receive queue will eventually overflow. This is indicated by [SU.QCRLS.RQOVFL](#) latched bit. If the receive queue is overflowed any new frames will not be received.

The user has the option of not enabling automatic flow control. In this case the thresholds and corresponding interrupt mechanism to send pause frame by writing to flow control busy bit in the MAC flow control registers [SU.MACFCR.FCB](#), [SU.GCR.JAME](#), and [SU.MACFCR](#). This allows the user to set not only the watermarks but also to decide when to send a pause frame or not based on watermark crossings.

On the receive side the user has control over whether to respond to the pause frame sent by the distant end (PCF bit). Note that if automatic flow control is enabled the user cannot modify the FCE bit in the MAC flow control register. On the Transmit queue the user has the option of setting high and low thresholds and corresponding interrupts. **There is no automatic flow control mechanism for data received from the Serial side waiting for transmission over the Ethernet interface during times of heavy Ethernet congestion.**

Figure 9-6. Flow Control Using Pause Control Frame



9.11.2 Half Duplex Flow Control

Half duplex flow control uses a jamming sequence to exert backpressure on the transmitting node. The receiving node jams the first 4 bytes of a packet that are received from the MAC in order to cause collisions at the distant end. In both 100Mbps and 10Mbps MII/RMII modes, 4 bytes are jammed upon reception of a new frame. Note that the jamming mechanism does not jam the current frame that is being received during the watermark crossing, but will wait to jam the next frame after the [SU.RQHT](#) bit is set. If the queue remains above the high threshold, received frames will continue to be jammed. This jam sequence is stopped when the queue falls below the high threshold.

9.11.3 Host-Managed Flow Control

Although automatic flow control is recommended, flow control by the host processor is also possible. By utilizing the high watermark interrupts, the host processor can manually issue pause frames or jam incoming packets to exert backpressure on the transmitting node. Pause frames can be initiated with SU.MACFCR.FCB bit. Jam sequences can be initiated by setting SU.GCR.JAME. The host can detect pause frames by monitoring SU.RFSB3.UF and SU.RFSB3.CF. Jammed frames will be indistinguishable from packet collisions.

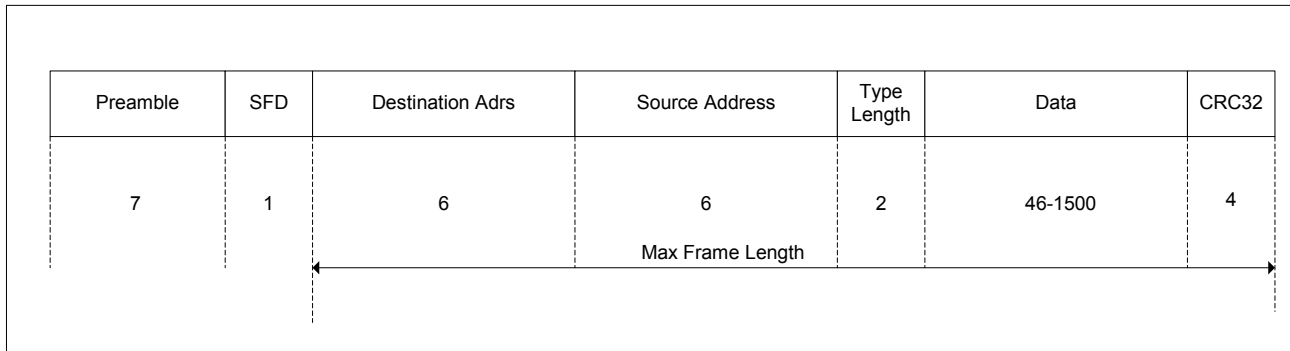
9.12 Ethernet Interface Port

The Ethernet port interface allows for direct connection to an Ethernet PHY. The interface consists of a 10/100Mbps MII/RMII interface and an Ethernet MAC. In RMII operation, the interface contains seven signals with a reference clock of 50MHz. In MII operation, the interface contains 17 signals and a clock reference of 25MHz. The device can be configured to RMII or MII interface by the Hardware pin RMIIMIS. If the port is configured for MII in DCE mode, REF_CLK must be 25MHz. The device will internally generate the TX_CLK and RX_CLK outputs (at 25MHz for 100Mbps, 2.5MHz for 10Mbps) required for DCE mode from the REF_CLK input. In MII mode with DTE operation, the TX_CLK and RX_CLK signals are generated by the PHY and are inputs to the device. For more information on clocking the Ethernet Interface, see Section [9.1.2](#).

The data received from the MII or RMII interface is processed by the internal IEEE 802.3-compliant Ethernet MAC. The user can select the maximum frame size (up to 2016 bytes) that is received with the [SU.RMFSRH](#) and [SU.RMFSRL](#) registers. The maximum frame length (in bits) is the number specified in SU.RMFSRH and SU.RMFSRL multiplied by 8. **Any programmed value greater than 2016 bytes will result in unpredictable behavior and should be avoided.** The maximum frame size is shown in [Figure 9-7](#). The length includes only destination address, source address, VLAN tag (2 bytes), type length field, data and CRC32. The frame size is different than the 802.3 “type length field.”

Frames coming from the Ethernet PHY or received from the packet processor are rejected if greater than the maximum frame size specified. Each Ethernet frame sent or received generates status bits ([SU.TFSH](#) and [SU.TFSL](#) and [SU.RFSB0](#) to [SU.RFSB3](#)). These are real time status registers and will change as each frame is sent or received. Hence they are useful to the user only when one frame is sent or received and the status is associated with the frame sent or received.

Figure 9-7. IEEE 802.3 Ethernet Frame



The distant end will normally reject the sent frames if jabber timeout, loss of carrier, excessive deferral, late collisions, excessive collisions, under run, deferred or collision errors occur. Transmission of a frame under any of these errors will generate a status bit in SU.TFSL, SU.TFSH. The device provides user the option to automatically retransmit the frame if any of the errors have occurred through the bit settings in [SU.TFRC](#). Deferred frames and heartbeat fail have separate resend control bits ([SU.TFRC.TFBFCB](#) and [SU.TFRC.TPRHBC](#)). If there is no carrier (indicated by the MAC Transmit Packet Status), the transmit queue (data from the Serial Interface to the SDRAM to Ethernet Interface) can be selectively flushed. This is controlled by [SU.TFRC.NCFQ](#).

The MAC circuitry generates a frame status for every frame that is received. This real time status can be read by [SU.RFSB0](#) to [SU.RFSB3](#). Note the frame status is the “real time” status and hence the value will change as new frames are received. Hence the real time status reflects the status in time and may not correspond to the current received frame being processed. This is also true for the transmitted frames.

Frames with errors are usually rejected by the device. The user has the option of accepting frames by settings in Receive Frame Rejection Control register ([SU.RFRC](#)). The user can program whether to reject or accept frames with the following errors:

- MII error asserted during the reception of the frame
- Dribbling bits occurred in the frame
- CRC error occurred
- Length error occurred—the length indicated by the frame length is inconsistent with the number of bytes received
- Control frame was received. The mode must be full duplex
- Unsupported control frame was received

Note that frames received that are runt frames or frames with collision will automatically be rejected.

Table 9-7. Registers Related to the Ethernet Port

| REGISTER | NAME | FUNCTION |
|--|---|---|
| Transmit Frame Resend Control | SU.TFRC | This register determines if the current frame is retransmitted due to various transmit errors. |
| Transmit Frame Status Low and Transmit Frame Status High | SU.TFSL and SU.TFSH | These 2 registers provide the real time status of the transmit frame. Only apply to the last frame transmitted. |
| Receive Frame Status Byte 0 to 3 | SU.RFSB0 to SU.RFSB3 | These registers provide the real time status for the received frame. Only apply to the last frame received. |
| Receive Frame Rejection Control | SU.RFRC | This register provides settings for reception or rejection of frame based on errors detected by the MAC. |
| Receiver Maximum Frame High Register and Receiver Maximum Frame Low Register | SU.RMFSRH and SU.RMFSRL | The settings for this register provide the maximum size of frames to be accepted from the MII/RMII receive interface. |
| MAC Control Register | SU.MACCR | This register provides configuration control for the MAC. |

9.12.1 DTE and DCE Mode

The Ethernet MII/RMII port can be configured for DCE or DTE Mode. When the port is configured for the DTE Mode it can be connected to an Ethernet PHY. In DCE mode, the port can be connected to MII/RMII MAC devices other than an Ethernet PHY. The DTE/DCE connections for the device in MII mode are shown in the following two figures.

In DCE Mode, the transmitter is connected to an external receiver and the receiver is connected to an external MAC transmitter. The selection of DTE or DCE mode is done by the hardware pin DCEDTES.

Figure 9-8. Configured as DTE Connected to an Ethernet PHY in MII Mode

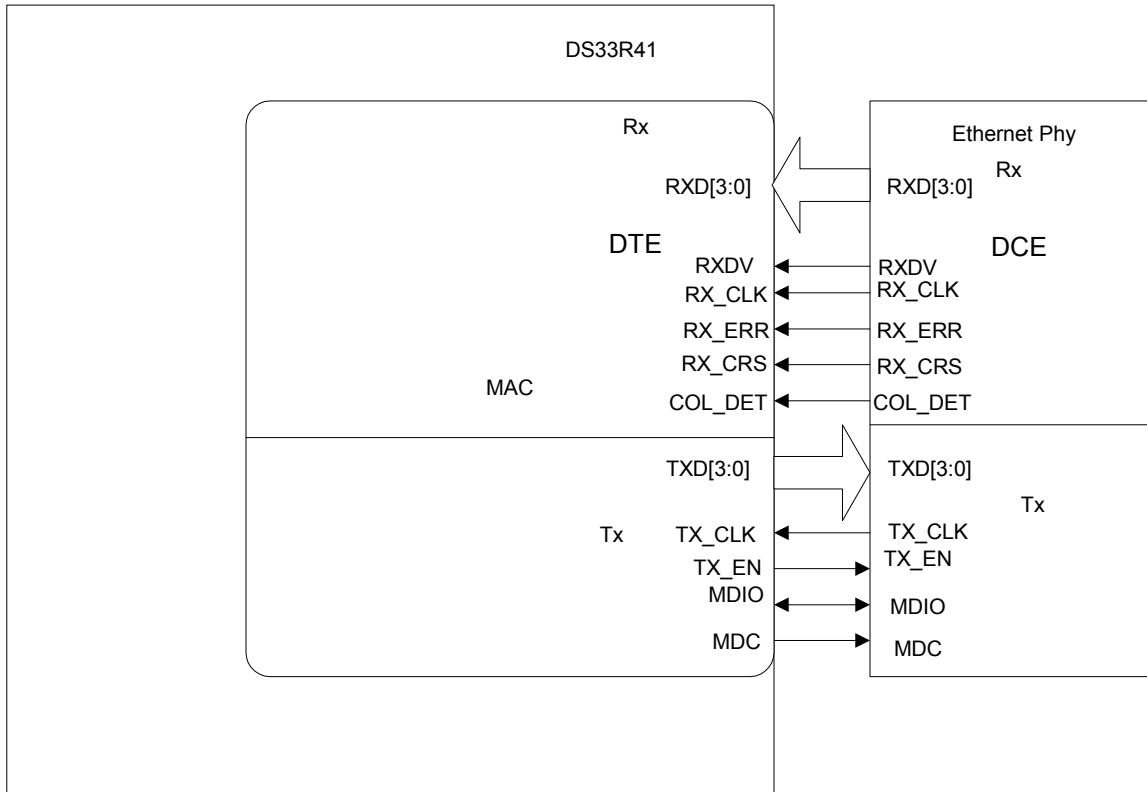
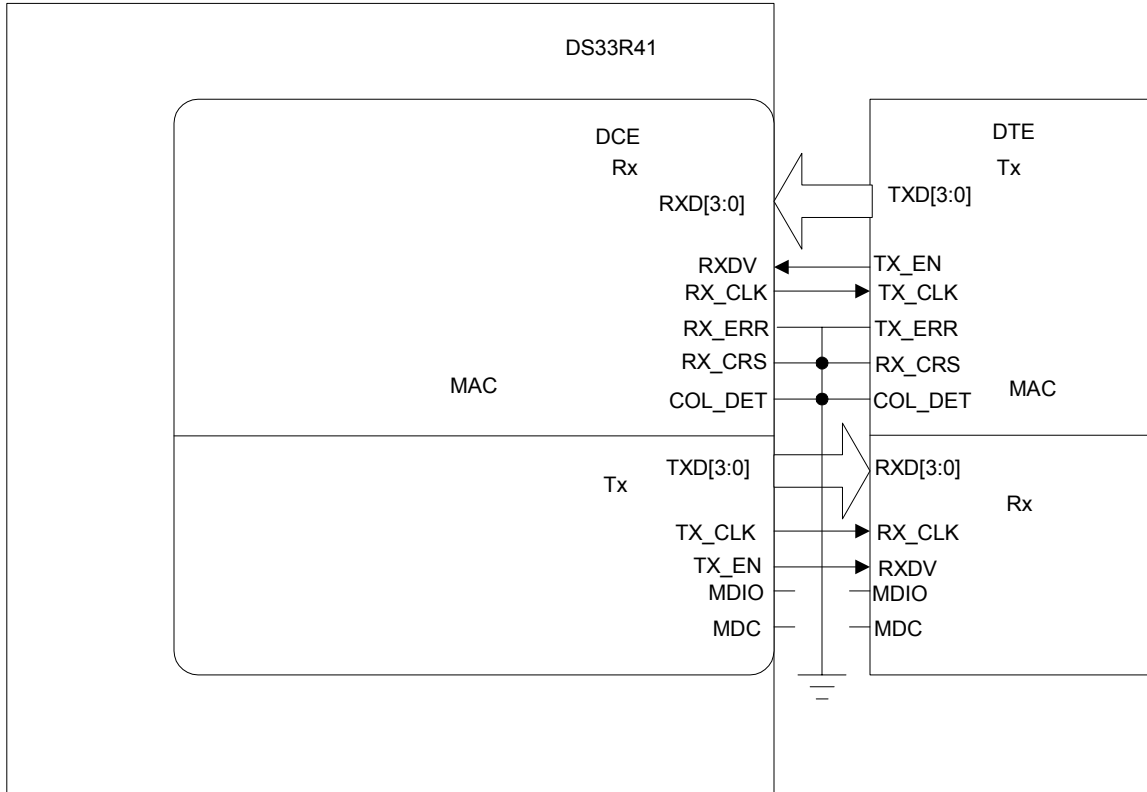


Figure 9-9. DS33R41 Configured as a DCE in MII Mode

9.13 Ethernet MAC

Indirect addressing is required to access the MAC register settings. Writing to the MAC registers requires the [SU.MACWD0-SU.MACRD3](#) registers to be written with 4 bytes of data. The address must be written to [SU.MACAWL](#) and [SU.MACAWH](#). A write command is issued by writing a zero to [SU.MACRWC.MCRW](#) and a one to [SU.MACRWC.MCS](#) (MAC command status). MCS is cleared by the device when the operation is complete.

Reading from the MAC registers requires the [SU.MACRADH](#) and [SU.MACRADL](#) registers to be written with the address for the read operation. A read command is issued by writing a one to [SU.MACRWC.MCRW](#) and a zero to [SU.MACRWC.MCS](#). [SU.MACRWC.MCS](#) is cleared by the device when the operation is complete. After MCS is clear, valid data is available in [SU.MACRD0-SU.MACRD3](#). Note that only one operation can be initiated (read or write) at one time. Data cannot be written or read from the MAC registers until the MCS bit has been cleared by the device. The MAC Registers are detailed in the following table.

Table 9-8. MAC Control Registers

| ADDRESS | REGISTER | REGISTER DESCRIPTION |
|-------------|------------|--|
| 0000h-0003h | SU.MACCR | MAC Control Register. This register is used for programming full duplex, half duplex, promiscuous mode, and back-off limit for half duplex. The transmit and receive enable bits must be set for the MAC to operate. |
| 0004h-0007h | SU.MACAH | MAC Address High Register. This provides the physical address for this MAC. |
| 0008h-000Bh | SU.MACAL | MAC Address Low Register. This provides the physical address for this MAC. |
| 0014h-0017h | SU.MACMIIA | MII Address Register. The address for PHY access through the MDIO interface. |
| 0018h-001Bh | SU.MACMIID | MII Data Register. Data to be written to (or read from) the PHY through MDIO interface. |
| 001Ch-001Fh | SU.MACFCR | Flow Control Register |
| 0100h-0103h | SU.MMCCTRL | MMC Control Register bit 0 for resetting the status counters |

Table 9-9. MAC Status Registers

| ADDRESS | REGISTER | REGISTER DESCRIPTION |
|-------------|-----------------|--|
| 0200h-0203h | SU.RxFrmCntr | All Frames Received counter |
| 0204h-0207h | SU.RxFrmOKCtr | Number of Received Frames that are Good |
| 0300h-0303h | SU.TxFrmCntr | Number of Frames Transmitted |
| 0308h-030Bh | SU.TxBytesCtr | Number of Bytes Transmitted |
| 030Ch-030Fh | SU.TxBytesOkCtr | Number of Bytes Transmitted with good frames |
| 0334h-0337h | SU.TxFrmUndr | Transmit FIFO underflow counter |
| 0338h-033Bh | SU.TxBdFrmsCtr | Transmit Number of Frames Aborted |

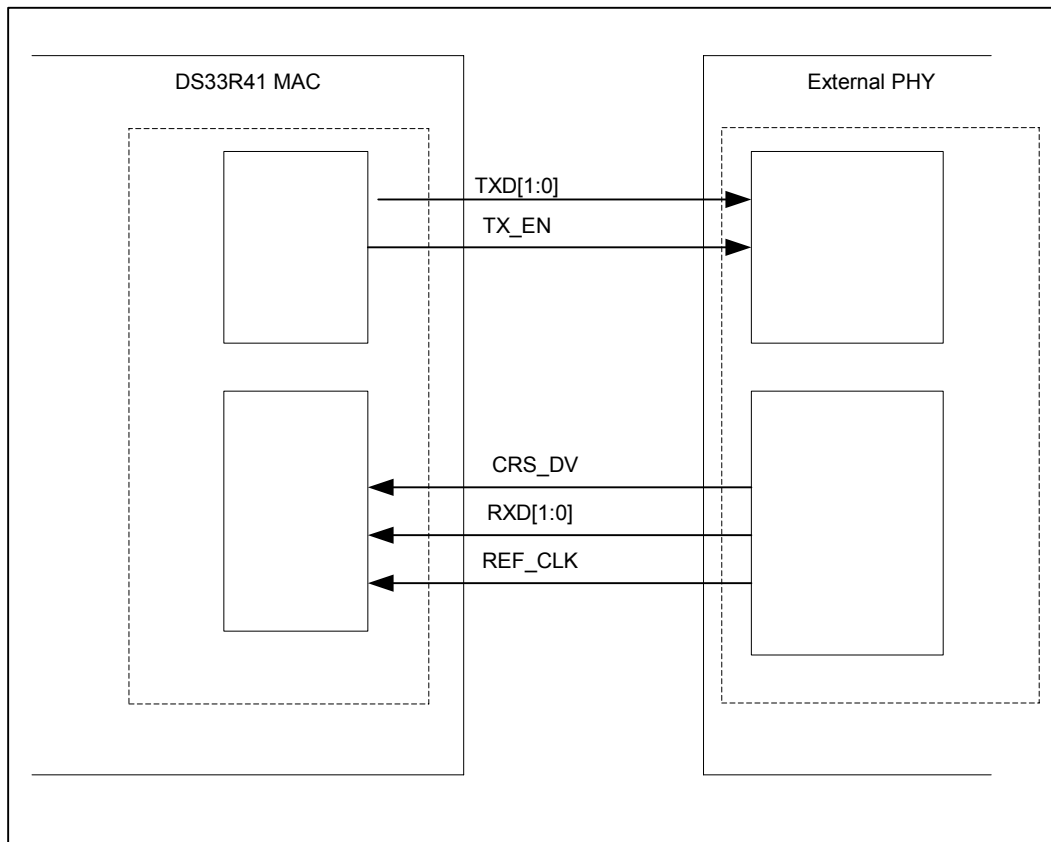
9.13.1 MII Mode

The Ethernet interface can be configured for MII operation by setting the hardware pin RMIIMIIS low. The MII interface consists of 17 pins. For instructions on clocking the Ethernet Interface while in MII mode, see Section 9.1.2. Diagrams of system connections for MII operation are shown in [Figure 9-8](#) and [Figure 9-9](#).

9.13.2 RMII Mode

The Ethernet interface can be configured for RMII operation by setting the hardware pin RMIIMIIS high. RMII interface operates synchronously from the external 50MHz reference (REF_CLK). Only seven signals are required. The following figure shows the RMII architecture. Note that DCE mode is not supported for RMII mode and RMII is valid only for full duplex operation.

Figure 9-10. RMII Interface



9.13.3 PHY MII Management Block and MDIO Interface

The MII Management Block allows for the host to control up to 32 PHYs, each with 32 registers. The MII block communicates with the external PHY using 2-wire serial interface composed of MDC (serial clock) and MDIO for data. The MDIO data is valid on the rising edge of the MDC clock. The Frame format for the MII Management Interface is shown [Figure 9-11](#). The read/write control of the MII Management is accomplished through the indirect SU.MACMIIA MII Management Address Register and data is passed through the indirect SU.MACMIID Data Register. These indirect registers are accessed through the MAC Control Registers defined in [Table 9-8](#). The MDC clock is internally generated and runs at 1.67MHz. Note that the device provides a single MII Management port, and all control registers for this function are located in MAC 1.

Figure 9-11. MII Management Frame

| | Preamble 32 bits | Start 2 bits | Opcode 2 bits | Phy Adrs 5 bits | Phy Reg 5 bits | Turn Around 2 bits | Data 16 bits | Idle 1 Bit |
|-------|---------------------|-----------------|------------------|--------------------|-------------------|--------------------------|--------------------|------------------|
| READ | 111...111 | 01 | 10 | PHYA[4:0] | PHYR[4:0] | ZZ | ZZZZZZZZ | Z |
| WRITE | 111...111 | 01 | 01 | PHYA[4:0] | PHYR[4:0] | 10 | PHYD[15:0] | Z |

9.14 Transmit Packet Processor

The Transmit Packet Processor accepts data from the Transmit FIFO performs bit reordering, FCS processing, packet error insertion, stuffing, packet abort sequence insertion, inter-frame padding, and packet scrambling. The data output from the Transmit Packet Processor to the Transmit Serial Interface is a serial data stream (bit synchronous mode). HDLC processing can be disabled (clear channel enable). Disabling HDLC processing disables FCS processing, packet error insertion, stuffing, packet abort sequence insertion, and inter-frame padding. Only bit reordering and packet scrambling are not disabled.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the outgoing 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is output from the Transmit FIFO with the MSB in TFD[7] (or 15, 23, or 31) and the LSB in TFD[0] (or 8, 16, or 24) of the transmit FIFO data TFD[7:0] 15:8, 23:16, or 31:24). If bit reordering is enabled, the outgoing 8-bit data stream DT[1:8] is output from the Transmit FIFO with the MSB in TFD[0] and the LSB in TFD[7] of the transmit FIFO data TFD[7:0]. In bit synchronous mode, DT [1] is the first bit transmitted.

FCS processing calculates an FCS and appends it to the packet. FCS calculation is a CRC-16 or CRC-32 calculation over the entire packet. The polynomial used for FCS-16 is $x^{16} + x^{12} + x^5 + 1$. The polynomial used for FCS-32 is $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$. The FCS is inverted after calculation. The FCS type is programmable. If FCS append is enabled, the calculated FCS is appended to the packet. If FCS append is disabled, the packet is transmitted without an FCS. The FCS append mode is programmable. If packet processing is disabled, FCS processing is not performed.

Packet error insertion inserts errors into the FCS bytes. A single FCS bit is corrupted in each errored packet. The FCS bit corrupted is changed from errored packet to errored packet. Error insertion can be controlled by a register or by the manual error insertion input ([LI.TMEI.TMEI](#)). The error insertion initiation type (register or input) is programmable. If a register controls error insertion, the number and frequency of the errors are programmable. If FCS append is disabled, packet error insertion will not be performed. If packet processing is disabled, packet error insertion is not performed.

Stuffing inserts control data into the packet to prevent packet data from mimicking flags. A packet start indication is received, and stuffing is performed until, a packet end indication is received. Bit stuffing consists of inserting a '0' directly following any five contiguous '1's. If packet processing is disabled, stuffing is not performed.

There is at least one flag plus a programmable number of additional flags between packets. The inter-frame fill can be flags or all '1's followed by a start flag. If the inter-frame fill is all '1's, the number of '1's between the end and start flags does not need to be an integer number of bytes, however, there must be at least 15 consecutive '1's between the end and start flags. The inter-frame padding type is programmable. If packet processing is disabled, inter-frame padding is not performed.

Packet abort insertion inserts a packet abort sequences as necessary. If a packet abort indication is detected, a packet abort sequence is inserted and inter-frame padding is done until a packet start flag is detected. The abort sequence is FFh. If packet processing is disabled, packet abort insertion is not performed.

The packet scrambler is a $x^{43} + 1$ scrambler that scrambles the entire packet data stream. The packet scrambler runs continuously, and is never reset. In bit synchronous mode, scrambling is performed one bit at a time. In byte synchronous mode, scrambling is performed 8 bits at a time. Packet scrambling is programmable.

Once all packet processing has been completed serial data stream is passed on to the Transmit Serial Interface.

9.15 Receive Packet Processor

The Receive Packet Processor accepts data from the Receive Serial Interface performs packet descrambling, packet delineation, inter-frame fill filtering, packet abort detection, destuffing, packet size checking, FCS error monitoring, FCS byte extraction, and bit reordering. The data coming from the Receive Serial Interface is a serial data stream. Packet processing can be disabled (clear channel enable). Disabling packet processing disables packet delineation, inter-frame fill filtering, packet abort detection, destuffing, packet size checking, FCS error monitoring, and FCS byte extraction. Only packet descrambling and bit reordering are not disabled.

The packet descrambler is a self-synchronous $x^{43} + 1$ descrambler that descrambles the entire packet data stream. Packet descrambling is programmable. The descrambler runs continuously, and is never reset. The descrambling is performed one bit at a time. Packet descrambling is programmable. If packet processing is disabled, the serial data stream is demultiplexed in to an 8-bit data stream before being passed on.

If packet processing is disabled, a packet boundary is arbitrarily chosen and the data is divided into "packets" of programmable size (dependent on maximum packet size setting). These packets are then passed on to bit reordering with packet start and packet end indications. Data then bypasses packet delineation, inter-frame fill filtering, packet abort detection, destuffing, packet size checking, FCS error monitoring, and FCS byte extraction.

Packet delineation determines the packet boundary by identifying a packet start or end flag. Each time slot is checked for a flag sequence (7Eh). Once a flag is found, it is identified as a start/end flag and the packet boundary is set. The flag check is performed one bit at a time. If packet processing is disabled, packet delineation is not performed.

Inter-frame fill filtering removes the inter-frame fill between packets. When a packet end flag is detected, all data is discarded until a packet start flag is detected. The inter-frame fill can be flags or all '1's. The number of '1's between flags does not need to be an integer number of bytes, and if at least 7 '1's are detected in the first 16 bits after a flag, all data after the flag is discarded until a start flag is detected. There may be only one flag between packets. When the inter-frame fill is flags, the flags may have a shared zero (011111101111110). If there is less than 16 bits between two flags, the data is discarded. If packet processing is disabled, inter-frame fill filtering is not performed.

Packet abort detection searches for a packet abort sequence. Between a packet start flag and a packet end flag, if an abort sequence is detected, the packet is marked with an abort indication, the aborted packet count is incremented, and all subsequent data is discarded until a packet start flag is detected. The abort sequence is seven consecutive ones. If packet processing is disabled, packet abort detection is not performed.

Destuffing removes the extra data inserted to prevent data from mimicking a flag or an abort sequence. A start flag is detected, a packet start is set, the flag is discarded, destuffing is performed until an end flag is detected, a packet end is set, and the flag is discarded. In bit synchronous mode, bit destuffing is performed. Bit destuffing consists of discarding any '0' that directly follows five contiguous '1's. After destuffing is completed, the serial bit stream is demultiplexed into an 8-bit parallel data stream and passed on with packet start, packet end, and packet abort indications. If there is less than eight bits in the last byte, an invalid packet flag is raised, the packet is tagged with an abort indication, and the packet size violation count is incremented. If packet processing is disabled, destuffing is not performed.

Packet size checking checks each packet for a programmable maximum and programmable minimum size. As the packet data comes in, the total number of bytes is counted. If the packet length is below the minimum size limit, the packet is marked with an aborted indication, and the packet size violation count is incremented. If the packet length is above the maximum size limit, the packet is marked with an aborted indication, the packet size violation count is incremented, and all packet data is discarded until a packet start is received. The minimum and maximum lengths include the FCS bytes, and are determined after destuffing has occurred. If packet processing is disabled, packet size checking is not performed.

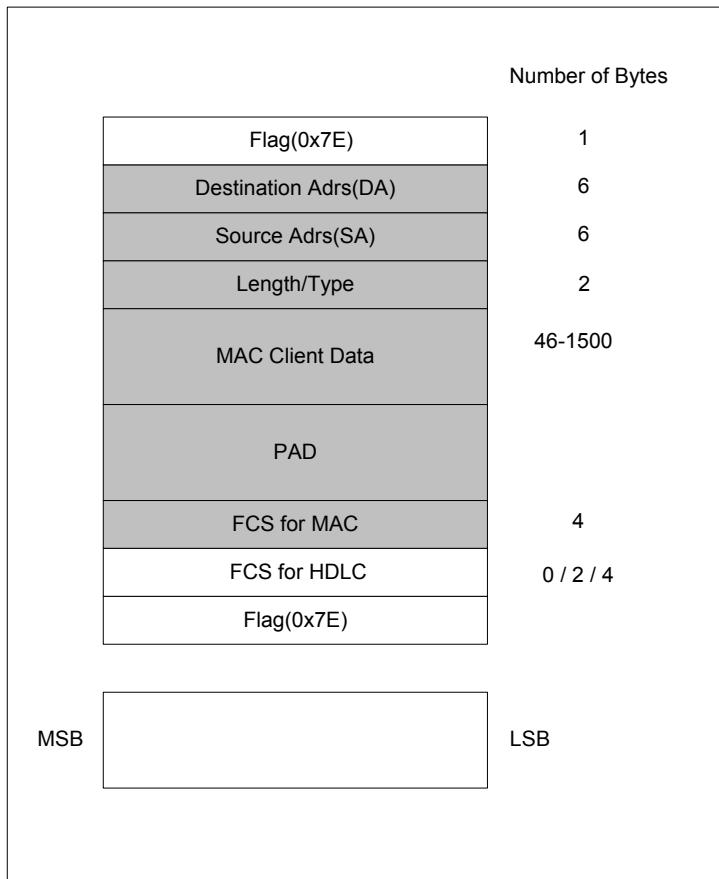
FCS error monitoring checks the FCS and aborts errored packets. If an FCS error is detected, the FCS errored packet count is incremented and the packet is marked with an aborted indication. If an FCS error is not detected, the receive packet count is incremented. The FCS type (16-bit or 32-bit) is programmable. If FCS processing or packet processing is disabled, FCS error monitoring is not performed.

FCS byte extraction discards the FCS bytes. If FCS extraction is enabled, the FCS bytes are extracted from the packet and discarded. If FCS extraction is disabled, the FCS bytes are stored in the receive FIFO with the packet. If FCS processing or packet processing is disabled, FCS byte extraction is not performed.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the incoming 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is output to the Receive FIFO with the MSB in RFD[7] (or 15, 23, or 31) and the LSB in RFD[0] (or 8, 16, or 24) of the receive FIFO data RFD[7:0] (or 15:8, 23:16, or 31:24). If bit reordering is enabled, the incoming 8-bit data stream DT[1:8] is output to the Receive FIFO with the MSB in RFD[0] and the LSB in RFD[7] of the receive FIFO data RFD[7:0]. DT[1] is the first bit received from the incoming data stream.

Once all the packet processing has been completed, the 8-bit parallel data stream is demultiplexed into a 32-bit parallel data stream. The Receive FIFO data is passed on to the Receive FIFO with packet start, packet end, packet abort, and modulus indications. At a packet end, the 32-bit word may contain 1, 2, 3, or 4 bytes of data depending on the number of bytes in the packet. The modulus indications indicate the number of bytes in the last data word of the packet.

Figure 9-12. HDLC Encapsulation of MAC Frame



9.16 X.86 Encoding and Decoding

X.86 protocol provides a method for encapsulating Ethernet Frame onto LAPS. LAPS provides an HDLC-type framing structure for encapsulation of Ethernet frames, but does not inflict dynamic bandwidth expansion as HDLC does. LAPS encapsulated frames can be used to send data onto a SONET/SDH network. The device expects a byte synchronization signal to provide the byte boundary for the X.86 receiver. This is provided by the RSYNC pin. The functional timing is shown in [Figure 14-7](#). The X.86 transmitter provides a byte boundary indicator with the signal TSYNC. The functional timing is shown in [Figure 14-6](#). Note that in some cases, additional logic may be required to meet RSYNC/TSYNC synchronization timing requirements when operating in X.86 mode.

Figure 9-13. LAPS Encoding of MAC Frames Concept

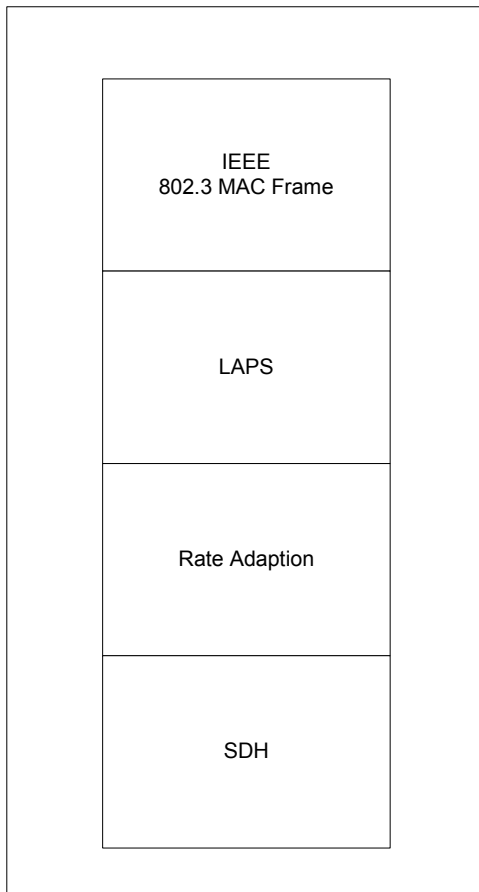
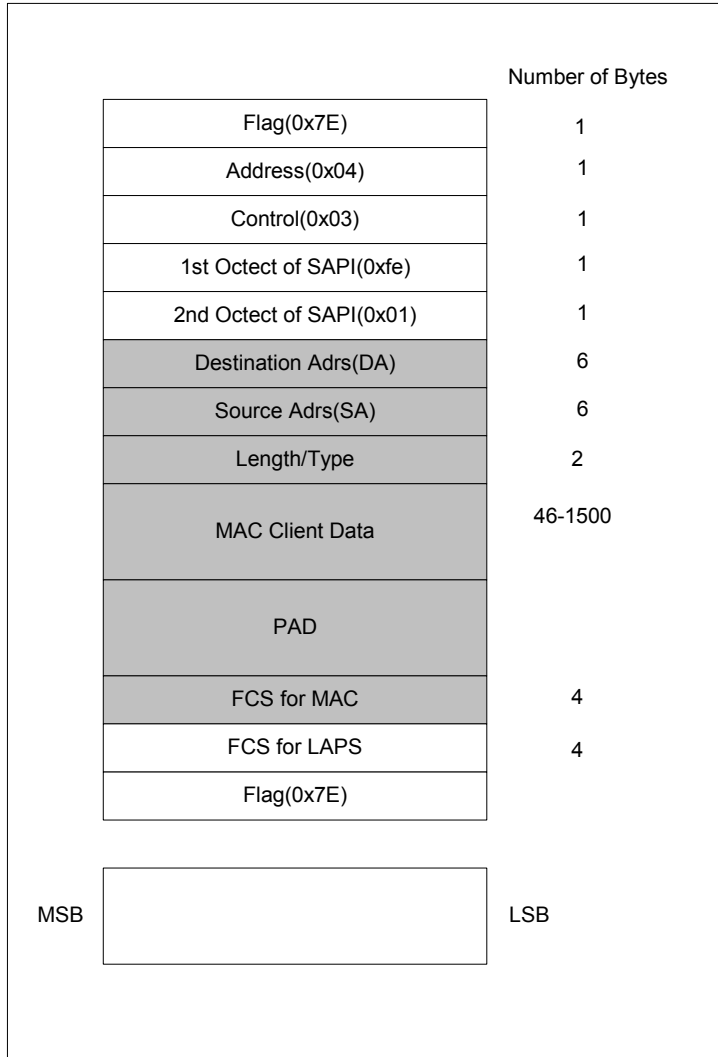


Figure 9-14. X.86 Encapsulation of the MAC field

The device will encode the MAC Frame with the LAPS encapsulation on a complete serial stream if configured for X.86 mode in the register [LI.TX86E](#). The device provides the following functions:

- Control Registers for Address, SAPI, Destination Address, Source Address
- 32 bit FCS enabled
- Programmable $X^{43}+1$ scrambling

The sequence of processing performed by the receiver is as follows:

- Programmable octets $X^{43}+1$ descrambling
- Detect the Start Flag (7E)
- Remove Rate adaptation octets 7d, dd.
- Perform transparency-processing 7d, 5e is converted to 7e and 7d, 5d is converted to 7d.
- Check for a valid Address, Control and SAPI fields ([LI.TRX86A](#) to [LI.TRX86SAPIL](#))
- Perform FCS checking
- Detect the closing flag.

The X86 received frame is aborted if:

- If 7d,7E is detected. This is an abort packet sequence in X.86
- Invalid FCS is detected
- The received frame has less than 6 octets
- Control, SAPI and address field are mismatched to the programmed value
- Octet 7d and octet other than 5d, 5e, 7e, or dd is detected

For the transmitter if X.86 is enabled the sequence of processing is as follows:

- Construct frame including start flag SAPI, Control and MAC frame
- Calculate FCS
- Perform transparency processing - 7E is translated to 7D5E, 7D is translated to 7D5D
- Append the end flag(7E)
- Scramble the sequence $X^{43}+1$

Note that the Serial transmit and receive registers apply to the X.86 implementations with specific exceptions. The exceptions are outlined in the Serial Interface transmit and receive register sections.

9.17 Committed Information Rate Controller

The device provides a CIR provisioning facility. The CIR can be used to restrict the transport of received MAC data to the serial port at a programmable rate. This is shown in the Main Block Diagram in [Figure 6-1](#). The CIR will restrict the data flow from the Receive MAC to Transmit HDLC. This can be used for provisioning and billing functions towards the WAN. The user must set the CIR register to control the amount of data throughput from the MAC to the HDLC/X.86 transmitter. The CIR register is in granularity of 500kbps with a range of 0 to 52Mbps. The operation of the CIR is as follows:

- The CIR block counts the credits that are accumulated at the end of every 125ms.
- If data is received and stored in the SDRAM to be sent to the Serial Interface, the interface will request the data if there is a positive credit balance. If the credit balance is negative, transmit interface does not request data.
- New credit balance is calculated: $\text{credit balance} = \text{old credit balance} - \text{frame size in bytes after the frame is sent}$.
- The credit balance is incremented every 125ms by $\text{CIR}/8$.
- Credit balances not used in 250ms are reset to 0.
- The maximum value of CIR can not exceed the transmit line rate.
- If the data rate received from the Ethernet interface is higher than the CIR, the receive queue buffers will fill and the high threshold water mark will invoke flow control to reduce the incoming traffic rate.
- CIR function is only available in data received at the Ethernet Interface to be sent to WAN. There is not CIR functionality for data arriving from the WAN to be sent to the Ethernet Interface.
- Negative credits are not allowed, if there is not a credit balance, no frames are sent until there is a credit balance again.

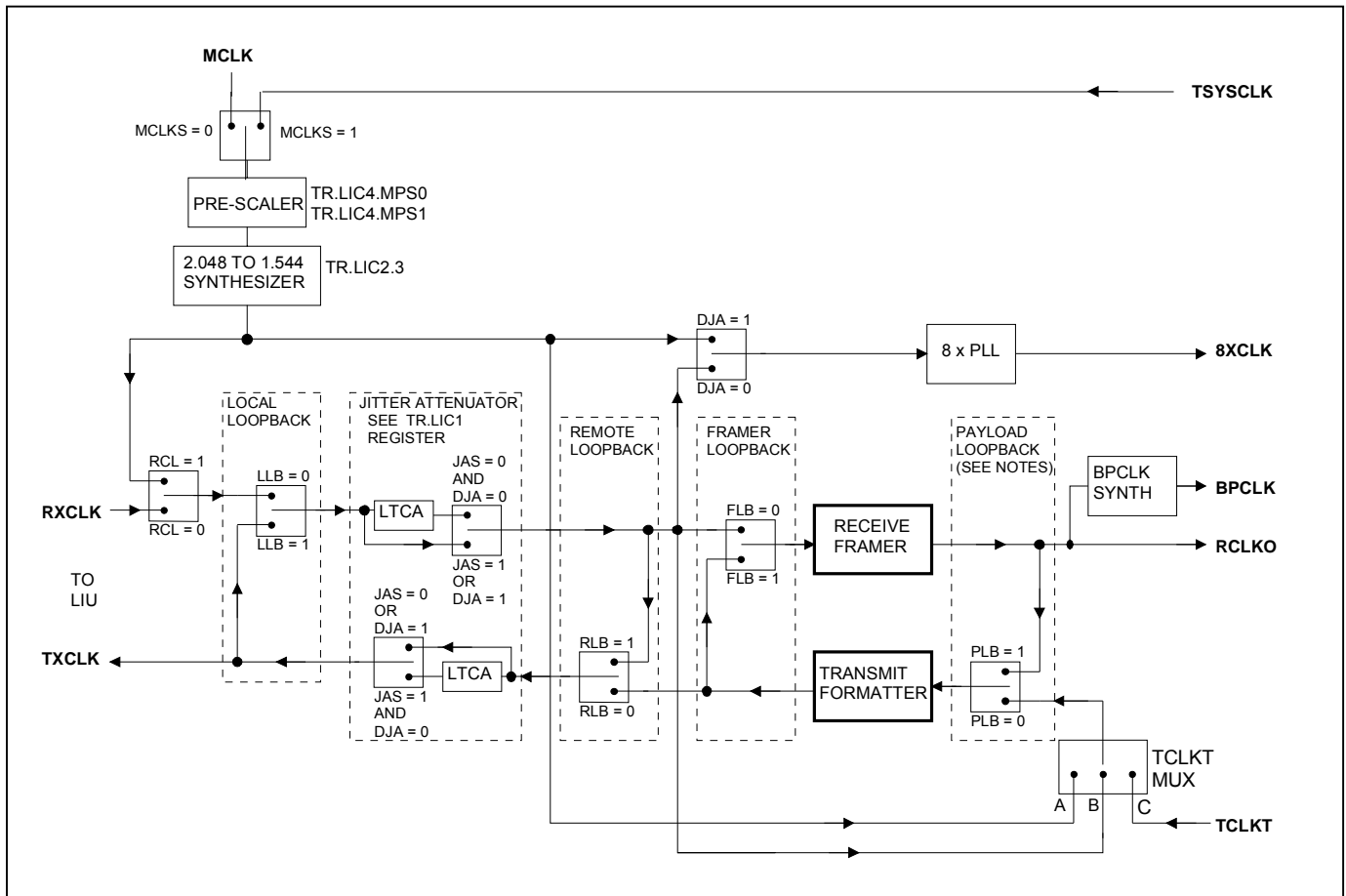
10 INTEGRATED T1/E1/J1 TRANSCEIVERS

10.1 T1/E1/J1 Transceiver Clocks

The device contains an on-chip clock synthesizer that generates a user-selectable clock referenced to the recovered receive clock (RCLK). The synthesizer uses a phase-locked loop to generate low-jitter clocks. Common applications include generation of port and backplane system clocks.

Figure 10-1 shows the clock map of the transceivers. The routing for the transmit and receive clocks are shown for the various loopback modes and jitter attenuator positions. Although there is only one jitter attenuator, which can be placed in the receive or transmit path, two are shown for simplification and clarity.

Figure 10-1. Transceiver Clock Structure



The TCLKT MUX is dependent on the state of the TCSS0 and TCSS1 bits in the TR.CCR1 register and the state of the TCLKT pin.

Table 10-1. T1/E1/J1 Transmit Clock Source

| TCSS1 | TCSS0 | Transmit Clock Source |
|-------|-------|--|
| 0 | 0 | The TCLKT pin (C) is always the source of transmit clock. |
| 0 | 1 | Switch to the recovered clock (B) when the signal at the TCLKT pin fails to transition after one channel time. |
| 1 | 0 | Use the scaled signal (A) derived from MCLK as the transmit clock. The TCLKT pin is ignored. |
| 1 | 1 | Use the recovered clock (B) as the transmit clock. The TCLKT pin is ignored. |

10.2 Per-Channel Operation

Some of the features described in the data sheet that operate on a per-channel basis use a special method for channel selection. There are five registers involved: per-channel pointer register (TR.PCPR) and per-channel data registers 1–4 (TR.PCDR1–4). The user selects which function or functions are to be applied on a per-channel basis by setting the appropriate bit(s) in the TR.PCPR register. The user then writes to the TR.PCDR registers to select the channels for that function. The following is an example of mapping the transmit and receive BERT function to channels 9–12, 20, and 21.

```
Write 11h to TR.PCPR
Write 00h to TR.PCDR1
Write 0fh to TR.PCDR2
Write 18h to TR.PCDR3
Write 00h to TR.PCDR4
```

The user may write to the TR.PCDR1-4 with multiple functions in the [TR.PCPR](#) register selected, but can only read the values from the TR.PCDR1-4 registers for a single function at a time. More information about how to use these per-channel features can be found in the [TR.PCPR](#) register.

10.3 T1/E1/J1 Transceiver Interrupts

Various alarms, conditions, and events in the T1/E1/J1 transceiver can cause interrupts. For simplicity, these are all referred to as events in this explanation. All status registers can be programmed to produce interrupts. Each status register has an associated interrupt mask register. For example, TR.SR1 (status register 1) has an interrupt control register called TR.IMR1 (interrupt mask register 1). Status registers are the only sources of interrupts in the device. On power-up, all writeable registers of the T1/E1/J1 transceiver are automatically cleared. Since bits in the TR.IMRx registers have to be set = 1 to allow a particular event to cause an interrupt, no interrupts can occur until the host selects which events are to produce interrupts. Since there are potentially many sources of interrupts on the device, several features are available to help sort out and identify which event is causing an interrupt. When an interrupt occurs, the host should first read the TR.IIR1 and TR.IIR2 registers (interrupt information registers) to identify which status register (or registers) is producing the interrupt. Once that is determined, the individual status register or registers can be examined to determine the exact source.

Once an interrupt has occurred, the interrupt handler routine should set the INTDIS bit (TR.CCR3.6) to stop further activity on the interrupt pin. After all interrupts have been determined and processed, the interrupt handler routine should re-enable interrupts by setting the INTDIS bit = 0.

Note that the integrated Ethernet Mapper also generates interrupts, as discussed in Section [9.6](#).

10.4 T1 Framer/Formatter Control and Status

The T1 framer portion of the transceiver is configured through a set of nine control registers. Typically, the control registers are only accessed when the system is first powered up. Once the transceiver has been initialized, the control registers only need to be accessed when there is a change in the system configuration. There are two receive control registers (TR.T1RCR1 and TR.T1RCR2), two transmit control registers (TR.T1TCR1 and TR.T1TCR2), and a common control register (TR.T1CCR1). Each of these registers is described in this section.

10.4.1 T1 Transmit Transparency

The software signaling insertion-enable registers, TR.SSIE1–TR.SSIE4, can be used to select signaling insertion from the transmit signaling registers, TS1–TS12, on a per-channel basis. Setting a bit in the TR.SSIE_x register allows signaling data to be sourced from the signaling registers for that channel.

In transparent mode, bit 7 stuffing and/or robbed-bit signaling is prevented from overwriting the data in the channels. If a DS0 is programmed to be clear, no robbed-bit signaling is inserted nor does the channel have bit 7 stuffing performed. However, in the D4 framing mode, bit 2 is overwritten by a 0 when a Yellow Alarm is transmitted. Also, the user has the option to globally override the TR.SSIE_x registers from determining which channels are to have bit 7 stuffing performed. If the TR.T1TCR1.3 and TR.T1TCR2.0 bits are set to 1, then all 24 T1 channels have bit 7 stuffing performed on them, regardless of how the TR.SSIE_x registers are programmed. In this manner, the TR.SSIE_x registers are only affecting the channels that are to have robbed-bit signaling inserted into them.

10.4.2 AIS-CI and RAI-CI Generation and Detection

The device can transmit and detect the RAI-CI and AIS-CI codes in T1 mode. These codes are compatible with and do not interfere with the standard RAI (Yellow) and AIS (Blue) alarms. These codes are defined in ANSI T1.403.

The AIS-CI code (alarm indication signal-customer installation) is the same for both ESF and D4 operation. Setting the TAIS-CI bit in the TR.T1CCR1 register and the TBL bit in the TR.T1TCR1 register causes the device to transmit the AIS-CI code. The RAIS-CI status bit in the TR.SR4 register indicates the reception of an AIS-CI signal.

The RAI-CI (remote alarm indication-customer installation) code for T1 ESF operation is a special form of the ESF Yellow Alarm (an unscheduled message). Setting the RAIS-CI bit in the TR.T1CCR1 register causes the device to transmit the RAI-CI code. The RAI-CI code causes a standard Yellow Alarm to be detected by the receiver. When the host processor detects a Yellow Alarm, it can then test the alarm for the RAI-CI state by checking the BOC detector for the RAI-CI flag. That flag is a 011111 code in the 6-bit BOC message.

The RAI-CI code for T1 D4 operation is a 10001011 flag in all 24 time slots. To transmit the RAI-CI code the host sets all 24 channels to idle with a 10001011 idle code. Since this code meets the requirements for a standard T1 D4 Yellow Alarm, the host can use the receive channel monitor function to detect the 100001011 code whenever a standard Yellow Alarm is detected.

10.4.3 T1 Receive-Side Digital-Milliwatt Code Generation

Receive-side digital-milliwatt code generation involves using the receive digital-milliwatt registers (TR.T1RDMR1/2/3) to determine which of the 24 T1 channels of the T1 line going to the backplane should be overwritten with a digital-milliwatt pattern. The digital-milliwatt code is an 8-byte repeating pattern that represents a 1kHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). Each bit in the TR.T1RDMRx registers represents a particular channel. If a bit is set to a 1, then the receive data in that channel is replaced with the digital-milliwatt code. If a bit is set to 0, no replacement occurs.

Table 10-2. T1 Alarm Criteria

| ALARM | | SET CRITERIA | CLEAR CRITERIA |
|---|---|---|---|
| Blue Alarm (AIS) (Note 1) | | When over a 3ms window, five or fewer 0s are received | When over a 3ms window, six or more 0s are received |
| Yellow Alarm (RAI) | D4 Bit 2 Mode (TR.T1RCR2.0 = 0) | When bit 2 of 256 consecutive channels is set to 0 for at least 254 occurrences | When bit 2 of 256 consecutive channels is set to 0 for fewer than 254 occurrences |
| | D4 12th F-Bit Mode (TR.T1RCR2.0 = 1; this mode is also referred to as the “Japanese Yellow Alarm”) | When the 12th framing bit is set to 1 for two consecutive occurrences | When the 12th framing bit is set to 0 for two consecutive occurrences |
| | ESF Mode | When 16 consecutive patterns of 00FF appear in the FDL | When 14 or fewer patterns of 00FF hex out of 16 possible appear in the FDL |
| Red Alarm (LRCL) (Also referred to as loss of signal) | | When 192 consecutive 0s are received | When 14 or more 1s out of 112 possible bit positions are received |

Note 1: The definition of Blue Alarm (or AIS) is an unframed all-ones signal. Blue Alarm detectors should be able to operate properly in the presence of a 10E-3 error rate and they should not falsely trigger on a framed all-1s signal. Blue Alarm criteria in the device has been set to achieve this performance. It is recommended that the RBL bit be qualified with the RLOS bit.

Note 2: ANSI specifications use a different nomenclature than this document. The following terms are equivalent:

RBL = AIS
RCL = LOS
RLOS = LOF
RYEL = RAI

10.5 E1 Framer/Formatter Control and Status

The E1 framer portion of the transceiver is configured by a set of four control registers. Typically, the control registers are only accessed when the system is first powered up. Once the device has been initialized, the control registers need only to be accessed when there is a change in the system configuration. There are two receive control registers (TR.E1RCR1 and TR.E1RCR2) and two transmit control registers (TR.E1TCR1 and TR.E1TCR2). There are also four status and information registers. Each of these eight registers is described in this section.

Table 10-3. E1 Sync/Resync Criteria

| FRAME OR MULTIFRAME LEVEL | SYNC CRITERIA | RESYNC CRITERIA | ITU SPEC. |
|---------------------------|---|--|-------------------------|
| FAS | FAS present in frame N and N + 2; FAS not present in frame N + 1 | Three consecutive incorrect FAS received Alternate: (TR.E1RCR1.2 = 1) The above criteria is met or three consecutive incorrect bit 2 of non-FAS received | G.706 4.1.1 4.1.2 |
| CRC4 | Two valid MF alignment words found within 8ms | 915 or more CRC4 code words out of 1000 received in error | G.706 4.2 and 4.3.2 |
| CAS | Valid MF alignment word found and previous time slot 16 contains code other than all 0s | Two consecutive MF alignment words received in error | G.732 5.2 |

10.5.1 Automatic Alarm Generation

The device can be programmed to automatically transmit AIS or remote alarm. When automatic AIS generation is enabled (TR.E1TCR2.1 = 1), the device monitors the receive-side framer to determine if any of the following conditions are present: loss-of-receive frame synchronization, AIS alarm (all ones) reception, or loss-of-receive carrier (or signal). The framer forces either an AIS or remote alarm if any one or more of these conditions is present.

When automatic RAI generation is enabled (TR.E1TCR2.0 = 1), the framer monitors the receive side to determine if any of the following conditions are present: loss-of-receive-frame synchronization, AIS alarm (all ones) reception, loss-of-receive carrier (or signal), or if CRC4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC4 is enabled). If any one or more of these conditions is present, then the framer transmits an RAI alarm. RAI generation conforms to ETS 300 011 specifications and a constant remote alarm is transmitted if the device cannot find CRC4 multiframe synchronization within 400ms as per G.706.

Note: It is an invalid state to have both automatic AIS generation and automatic remote alarm generation enabled at the same time.

Table 10-4. E1 Alarm Criteria

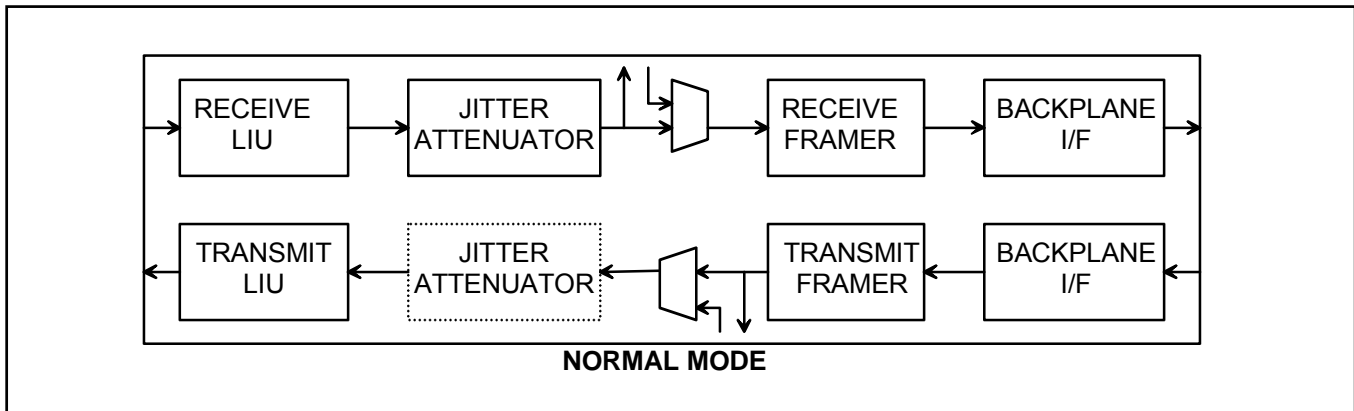
| ALARM | SET CRITERIA | CLEAR CRITERIA | ITU SPECIFICATION |
|--------|---|--|-------------------|
| RLOS | An RLOS condition exists on power-up prior to initial synchronization, when a resync criteria has been met, or when a manual resync has been initiated by TR.E1RCR1.0 | | |
| RCL | 255 or 2048 consecutive 0s received as determined by TR.E1RCR2.0 | At least 32 1s in 255-bit times are received | G.775/G.962 |
| RRA | Bit 3 of nonalign frame set to 1 for three consecutive occasions | Bit 3 of nonalign frame set to 0 for three consecutive occasions | O.162 2.1.4 |
| RUA1 | Fewer than three 0s in two frames (512 bits) | More than two 0s in two frames (512 bits) | O.162 1.6.1.2 |
| RDMA | Bit 6 of time slot 16 in frame 0 has been set for two consecutive multiframes | | |
| V52LNK | Two out of three Sa7 bits are 0 | | G.965 |

10.6 Loopback Configurations

The transceivers have four loopback configurations including Framer, Payload, Local, and Remote loopback. [Figure 10-2](#) depicts a normal signal flow without any loopbacks enabled.

Payload loopback may be done on a per-channel basis if both the transmit and receive paths are synchronous (RCLK = TCLKT and RSYNC = TSYNC). See Section [10.6.1](#).

Figure 10-2. Normal Signal Flow Diagram



10.6.1 Per-Channel Payload Loopback

The per-channel loopback registers (PCLRs) determine which channels (if any) from the backplane should be replaced with the data from the receive side or, i.e., off of the T1 or E1 line. If this loopback is enabled, then transmit and receive clocks and frame syncs must be synchronized. One method to accomplish this is to connect RCLK_n to TCLKT and RFSYNC to TSYNC. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

Each of the bit positions in the per-channel loopback registers (TR.PCLR1/TR.PCLR2/TR.PCLR3/TR.PCLR4) represents a DS0 channel in the outgoing frame. When these bits are set to a 1, data from the corresponding receive channel replaces the data on TSER1 for that channel.

10.7 Error Counters

The transceiver contains four counters that are used to accumulate line-coding errors, path errors, and synchronization errors. Counter update options include one-second boundaries, 42ms (T1 mode only), 62ms (E1 mode only), or manual. See *Error-Counter Configuration Register (TR.ERCNT)*. When updated automatically, the user can use the interrupt from the timer to determine when to read these registers. All four counters saturate at their respective maximum counts, and they do not roll over. Note: Only the line-code violation count register has the potential to overflow, but the bit error would have to exceed $10E-2$ before this would occur.

10.7.1 Line-Code Violation Counter (TR.LCVCR)

In T1 mode, code violations are defined as bipolar violations (BPVs) or excessive 0s. If the B8ZS mode is set for the receive side, then B8ZS code words are not counted. This counter is always enabled; it is not disabled during receive loss-of-synchronization (RLOS = 1) conditions. [Table 10-5](#) shows what the LCVCRs count.

Table 10-5. T1 Line Code Violation Counting Options

| COUNT EXCESSIVE ZEROS? (TR.ERCNT.0) | B8ZS ENABLED? (TR.T1RCR2.5) | COUNTED IN THE LCVCRs |
|--|--------------------------------|------------------------------------|
| No | No | BPVs |
| Yes | No | BPVs + 16 consecutive 0s |
| No | Yes | BPVs (B8ZS code words not counted) |
| Yes | Yes | BPVs + 8 consecutive 0s |

In E1 mode, either bipolar violations or code violations can be counted. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receive side, then HDB3 code words are not counted as BPVs. If TR.ERCNT.3 is set, then the LVC counts code violations as defined in ITU O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the framer should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss-of-sync conditions. The counter saturates at 65,535 and does not roll over. The bit-error rate on an E1 line would have to be greater than 10^{-2} before the VCR would saturate ([Table 10-6](#)).

Table 10-6. E1 Line-Code Violation Counting Options

| E1 CODE VIOLATION SELECT (TR.ERCNT.3) | COUNTED IN THE LCVCRs |
|--|-----------------------|
| 0 | BPVs |
| 1 | CVs |

10.7.2 Path Code Violation Count Register (TR.PCVCR)

In T1 mode, the path code violation count register records Ft, Fs, or CRC6 errors in T1 frames. When the receive side of a framer is set to operate in the T1 ESF framing mode, TR.PCVCR records errors in the CRC6 code words. When set to operate in the T1 D4 framing mode, TR.PCVCR counts errors in the Ft framing bit position. Through the TR.ERCNT.2 bit, a framer can be programmed to also report errors in the Fs framing bit position. The TR.PCVCR is disabled during receive loss-of-synchronization (RLOS = 1) conditions. [Table 10-7](#) shows what errors the TR.PCVCR counts.

Table 10-7. T1 Path Code Violation Counting Arrangements

| FRAMING MODE | COUNT Fs ERRORS? | COUNTED IN THE PCVCRs |
|--------------|------------------|---------------------------------------|
| D4 | No | Errors in the Ft pattern |
| D4 | Yes | Errors in both the Ft and Fs patterns |
| ESF | Don't Care | Errors in the CRC6 code words |

In E1 mode, the path code violation-count register records CRC4 errors. Since the maximum CRC4 count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss-of-sync at either the FAS or CRC4 level; it continues to count if loss-of-multiframe sync occurs at the CAS level.

Path code violation-count register 1 (TR.PCVCR1) is the most significant word and TR.PCVCR2 is the least significant word of a 16-bit counter that records path violations (PVs).

10.7.3 Frames Out-of-Sync Count Register (TR.FOSCR)

In T1 mode, TR.FOSCR is used to count the number of multiframes that the receive synchronizer is out of sync. This number is useful in ESF applications needing to measure the parameters loss-of-frame count (LOFC) and ESF error events as described in AT&T publication TR54016. When TR.FOSCR is operated in this mode, it is not disabled during receive loss-of-synchronization (RLOS = 1) conditions. TR.FOSCR has an alternate operating mode whereby it counts either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When TR.FOSCR is operated in this mode, it is disabled during receive loss-of-synchronization (RLOS = 1) conditions. [Table 10-8](#) shows what the FOSCR is capable of counting.

Table 10-8. T1 Frames Out-of-Sync Counting Arrangements

| FRAMING MODE (TR.T1RCR1.3) | COUNT MOS OR F-BIT ERRORS (TR.ERCNT.1) | COUNTED IN THE FOSCRs |
|-------------------------------|--|-----------------------------------|
| D4 | MOS | Number of multiframes out-of-sync |
| D4 | F-Bit | Errors in the Ft pattern |
| ESF | MOS | Number of multiframes out-of-sync |
| ESF | F-Bit | Errors in the FPS pattern |

In E1 mode, TR.FOSCR counts word errors in the FAS in time slot 0. This counter is disabled when RLOS is high. FAS errors are not counted when the framer is searching for FAS alignment and/or synchronization at either the CAS or CRC4 multiframe level. Since the maximum FAS word error count in a one-second period is 4000, this counter cannot saturate.

The frames out-of-sync count register 1 (TR.FOSCR1) is the most significant word and TR.FOSCR2 is the least significant word of a 16-bit counter that records frames out-of-sync.

10.7.4 E-Bit Counter (TR.EBCR)

This counter is only available in E1 mode. E-bit count register 1 (TR.EBCR1) is the most significant word and TR.EBCR2 is the least significant word of a 16-bit counter that records far-end block errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers increment once each time the received E-bit is set to 0. Since the maximum E-bit count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss-of-sync at either the FAS or CRC4 level; it continues to count if loss-of-multiframe sync occurs at the CAS level.

10.8 DS0 Monitoring Function

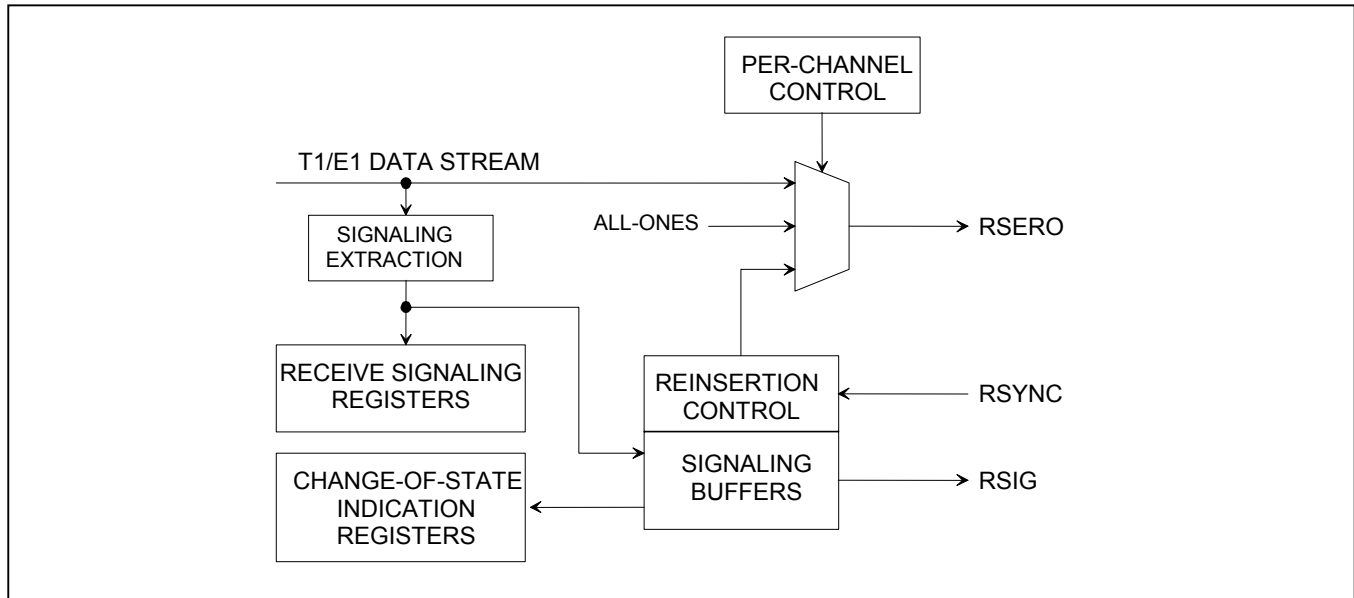
The transceiver has the ability to monitor one DS0 64kbps channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction, the user determines which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the TR.TDS0SEL register. In the receive direction, the RCM0 to RCM4 bits in the TR.RDS0SEL register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits appear in the transmit DS0 monitor (TR.TDS0M) register. The DS0 channel pointed to by the RCM0 to RCM4 bits appear in the receive DS0 (TR.RDS0M) register. The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate T1 or E1 channel. T1 channels 1 through 24 map to register values 0 through 23. E1 channels 1 through 32 map to register values 0 through 31. For example, if DS0 channel 6 in the transmit direction and DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into TR.TDS0SEL and TR.RDS0SEL:

| | |
|----------|----------|
| TCM4 = 0 | RCM4 = 0 |
| TCM3 = 0 | RCM3 = 1 |
| TCM2 = 1 | RCM2 = 1 |
| TCM1 = 0 | RCM1 = 1 |
| TCM0 = 1 | RCM0 = 0 |

10.9 Signaling Operation

There are two methods to access receive signaling data and provide transmit signaling data, processor-based (software-based) or hardware-based. Processor-based refers to access through the transmit and receive signaling registers RS1–RS16 and TS1–TS16. Hardware-based refers to the TSIG and RSIG pins. Both methods can be used simultaneously.

Figure 10-3. Simplified Diagram of Receive Signaling Path



10.9.1 Processor-Based Receive Signaling

The robbed-bit signaling (T1) or TS16 CAS signaling (E1) is sampled in the receive data stream and copied into the receive signaling registers, RS1–RS16. In T1 mode, only RS1–RS12 are used. The signaling information in these registers is always updated on multiframe boundaries. This function is always enabled.

10.9.1.1 Change-of-State

To avoid constant monitoring of the receive signaling registers, the transceiver can be programmed to alert the host when any specific channel or channels undergo a change of their signaling state. TR.RSCSE1–TR.RSCSE4 for E1 and TR.RSCSE1–TR.RSCSE3 for T1 are used to select which channels can cause a change-of-state indication. The change-of-state is indicated in status register 5 (TR.SR1.5). If signaling integration (TR.CCR1.5) is enabled, then the new signaling state must be constant for three multiframes before a change-of-state is indicated. The user can enable the INT pin to toggle low upon detection of a change in signaling by setting the TR.IMR1.5 bit. The signaling integration mode is global and cannot be enabled on a channel-by-channel basis.

The user can identify which channels have undergone a signaling change-of-state by reading the TR.RSINFO1–TR.RSINFO4 registers. The information from these registers inform the user which TR.RSx register to read for the new signaling data. All changes are indicated in the TR.RSINFO1–TR.RSINFO4 registers regardless of the TR.RSCSE1–TR.RSCSE4 registers.

10.9.2 Hardware-Based Receive Signaling

In hardware-based signaling the signaling data can be obtained from the RSERO pin or the RSIG pin. RSIG is a signaling PCM stream output on a channel-by-channel basis from the signaling buffer. The signaling data, T1 robbed bit or E1 TS16, is still present in the original data stream at RSERO. The signaling buffer provides signaling data to the RSIG pin and also allows signaling data to be reinserted into the original data stream in a different alignment that is determined by a multiframe signal from the RSYNC pin. In this mode, the receive elastic store can be enabled or disabled. If the receive elastic store is enabled, then the backplane clock (RSYSCLK) can be either 1.544MHz or 2.048MHz. In the ESF framing mode, the ABCD signaling bits are output on RSIG in the lower nibble of each channel. The RSIG data is updated once a multiframe (3ms) unless a freeze is in effect. In the D4 framing mode, the AB signaling bits are output twice on RSIG in the lower nibble of each channel. Hence, bits 5 and 6 contain the same data as bits 7 and 8, respectively, in each channel. The RSIG data is updated once a multiframe (1.5ms) unless a freeze is in effect. See the timing diagrams in Section [12](#) for some examples.

10.9.2.1 Receive Signaling Reinsertion at RSERO

In this mode, the user provides a multiframe sync at the RSYNC pin and the signaling data is reinserted based on this alignment. In T1 mode, this results in two copies of the signaling data in the RSERO data stream, the original signaling data and the realigned data. This is of little consequence in voice channels. Reinsertion can be avoided in data channels since this feature is activated on a per-channel basis. In this mode, the elastic store must be enabled; however, the backplane clock can be either 1.544MHz or 2.048MHz.

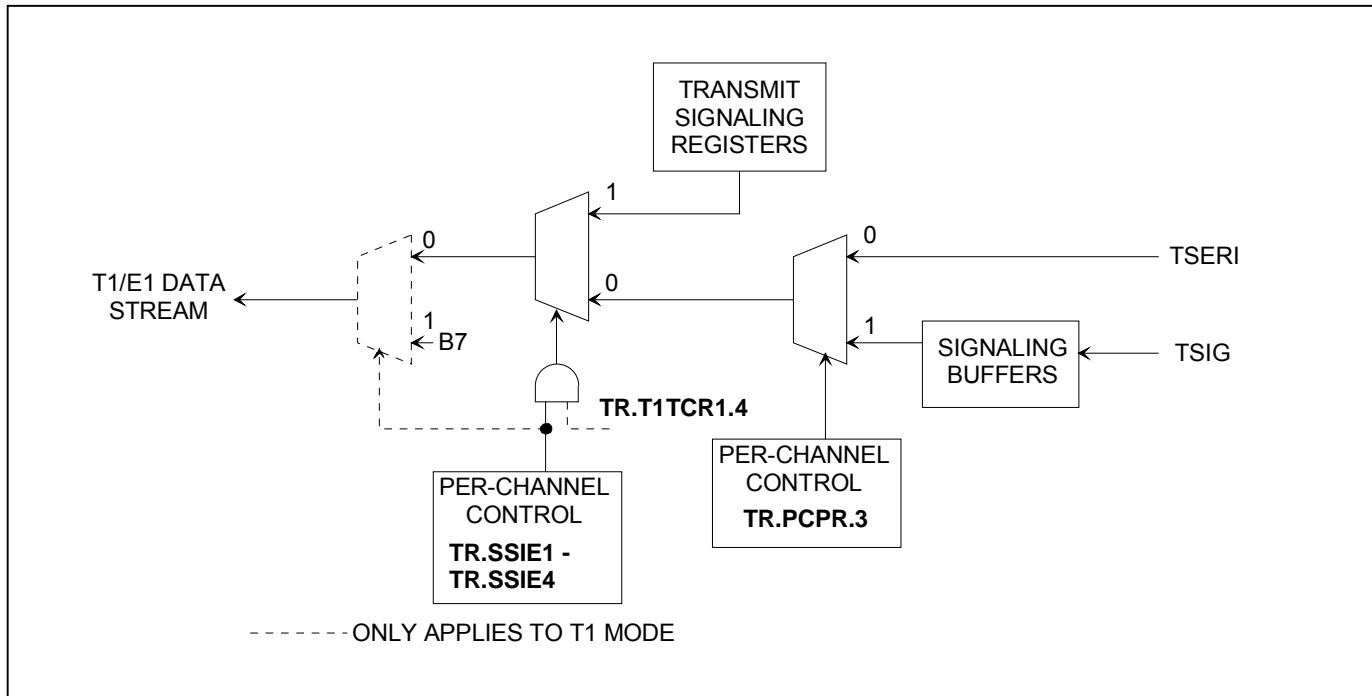
Signaling reinsertion can be enabled on a per-channel basis by setting the RSRCS bit high in the TR.PCPR register. The channels that will have signaling reinserted are selected by writing to the TR.PCDR1–TR.PCDR3 registers for T1 mode and TR.PCDR1–TR.PCDR4 registers for E1 mode. In E1 mode, the user generally selects all channels or none for reinsertion. In E1 mode, signaling reinsertion on all channels can be enabled with a single bit, TR.SIGCR.7 (GRSRE). This bit allows the user to reinsert all signaling channels without having to program all channels through the per-channel function.

10.9.2.2 Force Receive Signaling All Ones

In T1 mode, the user can, on a per-channel basis, force the robbed-bit signaling bit positions to a 1 by using the per-channel register (Section [10.2](#)). The user sets the BTCS bit in the TR.PCPR register. The channels that will be forced to 1 are selected by writing to the TR.PCDR1–TR.PCDR3 registers.

10.9.2.3 Receive Signaling Freeze

The signaling data in the four multiframe signaling buffers is frozen in a known good state upon either a loss of synchronization (OOF event), carrier loss, or frame slip. This action meets the requirements of BellCore TR-TSY-000170 for signaling freezing. To allow this freeze action to occur, the RFE control bit (TR.SIGCR.4) should be set high. The user can force a freeze by setting the RFF control bit (TR.SIGCR.3) high. The RSIGF output pin provides a hardware indication that a freeze is in effect. The four-multiframe buffer provides a three-multiframe delay in the signaling bits provided at the RSIG pin (and at the RSERO pin if receive signaling reinsertion is enabled). When freezing is enabled (RFE = 1), the signaling data is held in the last-known good state until the corrupting error condition subsides. When the error condition subsides, the signaling data is held in the old state for at least an additional 9ms (or 4.5ms in D4 framing mode) before updating with new signaling data.

Figure 10-4. Simplified Diagram of Transmit Signaling Path

10.9.3 Processor-Based Transmit Signaling

In processor-based mode, signaling data is loaded into the transmit signaling registers (TS1–TS16) by the host interface. On multiframe boundaries, the contents of these registers are loaded into a shift register for placement in the appropriate bit position in the outgoing data stream. The user can employ the transmit multiframe interrupt in status register 4 (TR.SR4.4) to know when to update the signaling bits. The user need not update any transmit signaling register for which there is no change-of-state for that register.

Each transmit signaling register contains the robbed-bit signaling (T1) or TS16 CAS signaling (E1) for two time slots that are inserted into the outgoing stream, if enabled to do so through TR.T1TCR1.4 (T1 mode) or TR.E1TCR1.6 (E1 mode). In T1 mode, only TS1–TS12 are used.

Signaling data can be sourced from the TR.TS registers on a per-channel basis by using the software signaling insertion enable registers, TR.SSIE1–TR.SSIE4.

10.9.3.1 T1 Mode

In T1 ESF framing mode, there are four signaling bits per channel (A, B, C, and D). TS1–TS12 contain a full multiframe of signaling data. In T1 D4 framing mode, there are only two signaling bits per channel (A and B). In T1 D4 framing mode, the framer uses the C and D bit positions as the A and B bit positions for the next multiframe. In D4 mode, two multiframes of signaling data can be loaded into TS1–TS12. The framer loads the contents of TS1–TS12 into the outgoing shift register every other D4 multiframe. In D4 mode, the host should load new contents into TS1–TS12 on every other multiframe boundary and no later than 120µs after the boundary. In T1 mode, only registers TR.SSIE1–TR.SSIE3 are used since there are only 24 channels in a T1 frame.

10.9.3.2 E1 Mode

In E1 mode, TS16 carries the signaling information. This information can be in either CCS (common channel signaling) or CAS (channel associated signaling) format. The 32 time slots are referenced by two different channel number schemes in E1. In “Channel” numbering, TS0–TS31 are labeled channels 1 through 32. In “Phone Channel” numbering, TS1–TS15 are labeled channel 1 through channel 15 and TS17–TS31 are labeled channel 15 through channel 30. In E1 CAS mode, the CAS signaling alignment/alarm byte can be sourced from the transmit signaling registers along with the signaling data.

Table 10-9. Time Slot Numbering Schemes

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TS | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| Channel | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| Phone Channel | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |

10.9.4 Hardware-Based Transmit Signaling

In hardware-based mode, signaling data is input through the TSIG pin. This signaling PCM stream is buffered and inserted to the data stream being input at the TSERI pin.

Signaling data can be inserted on a per-channel basis by the transmit hardware-signaling channel-select (THSCS) function. The user can control which channels are to have signaling data from the TSIG pin inserted into them on a per-channel basis. See Section [10.2](#) for details on using this per-channel (THSCS) feature. The signaling insertion capabilities of the framer are available whether the transmit-side elastic store is enabled or disabled. If the elastic store is enabled, the backplane clock (TSYSCLK) can be either 1.544MHz or 2.048MHz. Also, if the elastic is enabled in conjunction with transmit hardware signaling, CCR3.7 must be set = 0.

10.10 Per-Channel Idle Code Generation

Channel data can be replaced by an idle code on a per-channel basis in the transmit and receive directions. When operated in the T1 mode, only the first 24 channels are used by the device, the remaining channels, CH25–CH32, are not used.

The device contains a 64-byte idle code array accessed by the idle array address register (TR.IAAR) and the per-channel idle code register (TR.PCICR). The contents of the array contain the idle codes to be substituted into the appropriate transmit or receive channels. This substitution can be enabled and disabled on a per-channel basis by the transmit-channel idle code-enable registers (TR.TCICE1–4) and receive-channel idle code-enable registers (TR.RCICE1–4).

To program idle codes, first select a channel by writing to the TR.IAAR register. Then write the idle code to the TR.PCICR register. For successive writes there is no need to load the TR.IAAR with the next consecutive address. The TR.IAAR register automatically increments after a write to the TR.PCICR register. The auto increment feature can be used for read operations as well. Bits 6 and 7 of the TR.IAAR register can be used to block write a common idle code to all transmit or receive positions in the array with a single write to the TR.PCICR register. Bits 6 and 7 of the TR.IAAR register should not be used for read operations. TR.TCICE1–4 and TR.RCICE1–4 are used to enable idle code replacement on a per-channel basis.

Table 10-10. Idle-Code Array Address Mapping

| BITS 0 to 5 OF IAAR REGISTER | MAPS TO CHANNEL |
|-------------------------------------|------------------------|
| 0 | Transmit Channel 1 |
| 1 | Transmit Channel 2 |
| 2 | Transmit Channel 3 |
| — | — |
| — | — |
| 30 | Transmit Channel 31 |
| 31 | Transmit Channel 32 |
| 32 | Receive Channel 1 |
| 33 | Receive Channel 2 |
| 34 | Receive Channel 3 |
| — | — |
| — | — |
| 62 | Receive Channel 31 |
| 63 | Receive Channel 32 |

10.10.1 Idle-Code Programming Examples

Example 1

Sets transmit channel 3 idle code to 7Eh.

```
Write TR.IAAR = 02h ;select channel 3 in the array
Write TR.PCICR = 7Eh ;set idle code to 7Eh
```

Example 2

Sets transmit channels 3, 4, 5, and 6 idle code to 7Eh and enables transmission of idle codes for those channels.

```
Write TR.IAAR = 02h ;select channel 3 in the array
Write TR.PCICR = 7Eh ;set channel 3 idle code to 7Eh
Write TR.PCICR = 7Eh ;set channel 4 idle code to 7Eh
Write TR.PCICR = 7Eh ;set channel 5 idle code to 7Eh
Write TR.PCICR = 7Eh ;set channel 6 idle code to 7Eh
Write TR.TCICE1 = 3Ch ;enable transmission of idle codes for channels 3,4,5, and 6
```

Example 3

Sets transmit channels 3, 4, 5, and 6 idle code to 7Eh, EEh, FFh, and 7Eh, respectively.

```
Write TR.IAAR = 02h
Write TR.PCICR = 7Eh
Write TR.PCICR = EEh
Write TR.PCICR = FFh
Write TR.PCICR = 7Eh
```

Example 4

Sets all transmit idle codes to 7Eh.

```
Write TR.IAAR = 4xh
Write TR.PCICR = 7Eh
```

Example 5

Sets all receive and transmit idle codes to 7Eh and enables idle code substitution in all E1 transmit and receive channels.

```
Write TR.IAAR = Cxh ;enable block write to all transmit and receive positions in the array
Write TR.PCICR = 7Eh ;7Eh is idle code
Write TR.TCICE1 = FEh ;enable idle code substitution for transmit channels 2 through 8
;Although an idle code was programmed for channel 1 by the block write
;function above, enabling it for channel 1 would step on the frame
;alignment, alarms, and Sa bits
Write TR.TCICE2 = FFh ;enable idle code substitution for transmit channels 9 through 16
Write TR.TCICE3 = FEh ;enable idle code substitution for transmit channels 18 through 24
;Although an idle code was programmed for channel 17 by the block write
;function above, enabling it for channel 17 would step on the CAS frame
;alignment, and signaling information
Write TR.TCICE4 = FFh ;enable idle code substitution for transmit channels 25 through 32
Write TR.RCICE1 = FEh ;enable idle code substitution for receive channels 2 through 8
Write TR.RCICE2 = FFh ;enable idle code substitution for receive channels 9 through 16
Write TR.RCICE3 = FEh ;enable idle code substitution for receive channels 18 through 24
Write TR.RCICE4 = FFh ;enable idle code substitution for receive channels 25 through 32
```

The transmit-channel idle-code enable registers (TR.TCICE1/2/3/4) are used to determine which of the 24 T1 or 32 E1 channels from the backplane to the T1 or E1 line should be overwritten with the code placed in the per-channel code array.

The receive-channel idle-code enable registers (TR.RCICE1/2/3/4) are used to determine which of the 24 T1 or 32 E1 channels from the backplane to the T1 or E1 line should be overwritten with the code placed in the per-channel code array.

10.11 Channel Blocking Registers

The receive channel blocking registers (TR.RCBR1/TR.RCBR2/TR.RCBR3/TR.RCBR4) and the transmit channel blocking registers (TR.TCBR1/TR.TCBR2/TR.TCBR3/TR.TCBR4) control RCHBLK and TCHBLK pins, respectively. The RCHBLK and TCHBLK pins are user-programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN-PRI applications. When the appropriate bits are set to a 1, the RCHBLK and TCHBLK pins are held high during the entire corresponding channel time. Channels 25 through 32 are ignored when the device is operated in the T1 mode.

10.12 Elastic Stores Operation

The device contains dual two-frame elastic stores, one for the receive direction and one for the transmit direction. Both elastic stores are fully independent. The transmit and receive-side elastic stores can be enabled/disabled independently of each other. Also, each elastic store can interface to either a 1.544MHz or 2.048MHz/4.096MHz/8.192MHz/16.384MHz backplane without regard to the backplane rate the other elastic store is interfacing to. **In most DS33R41 applications, all elastic stores will be enabled.**

The elastic stores have two main purposes. Firstly, they can be used for rate conversion. When the device is in the T1 mode, the elastic stores can rate-convert the T1 data stream to a 2.048MHz backplane. In E1 mode, the elastic store can rate-convert the E1 data stream to a 1.544MHz backplane. Secondly, they can be used to absorb the differences in frequency and phase between the T1 or E1 data stream and an asynchronous (i.e., not locked) backplane clock, which can be 1.544MHz or 2.048MHz. In this mode, the elastic stores manage the rate difference and perform controlled slips, deleting or repeating frames of data in order to manage the difference between the network and the backplane. The elastic stores can also be used to multiplex T1 or E1 data streams into higher backplane rates.

The elastic stores are used to multiplex the four T1/E1 data streams into an 8.192MHz backplane rate for connection with the integrated Ethernet Mapper. See the *Interleaved PCM Bus Operation* section.

10.12.1 Receive Side

See the TR.IOCR1 and TR.IOCR2 registers for information on clock and I/O configurations. If the receive-side elastic store is enabled, then the user must provide either a 1.544MHz or 2.048MHz clock at the RSYCLK pin. For higher rate system-clock applications, see the *Interleaved PCM Bus Operation* section. The user has the option of either providing a frame/multiframe sync at the RSYNC pin or having the RSYNC pin provide a pulse on frame/multiframe boundaries. If signaling reinsertion is enabled, signaling data in TS16 is realigned to the multiframe-sync input on RSYNC. Otherwise, a multiframe-sync input on RSYNC is treated as a simple frame boundary by the elastic store. The framer will always indicate frame boundaries on the network side of the elastic store via the RFSYNC output whether the elastic store is enabled or not. Multiframe boundaries will always be indicated via the RMSYNC output. If the elastic store is enabled, then RMSYNC will output the multiframe boundary on the backplane side of the elastic store.

10.12.1.1 T1 Mode

If the user selects to apply a 2.048MHz clock to the RSYCLK pin, then the data output at RSERO will be forced to all ones every fourth channel and the F-bit will be passed into the MSB of TS0. Hence, channels 1 (bits 1–7), 5, 9, 13, 17, 21, 25, and 29 (time slots 0 (bits 1–7), 4, 8, 12, 16, 20, 24, and 28) will be forced to a one. Also, in 2.048MHz applications, the RCHBLK output will be forced high during the same channels as the RSERO pin. This is useful in T1 to E1 conversion applications. If the two-frame elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data will be repeated at RSERO and the TR.SR5.0 and TR.SR5.1 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the TR.SR5.0 and TR.SR5.2 bits will be set to a one.

10.12.1.2 E1 Mode

If the elastic store is enabled, then either CAS or CRC-4 multiframe boundaries will be indicated via the RMSYNC output. If the user selects to apply a 1.544MHz clock to the RSYCLK pin, then every fourth channel of the received E1 data will be deleted and a F-bit position (which will be forced to one) will be inserted. Hence, channels 1, 5, 9, 13, 17, 21, 25, and 29 (time slots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted from the received E1 data stream. Also, in 1.544MHz applications, the RCHBLK output will not be active in channels 25 through 32 (or in other words, RCBR4 is not active). If the two-frame elastic buffer either fills or empties, a controlled slip will occur.

If the buffer empties, then a full frame of data will be repeated at RSERO and the TR.SR5.0 and TR.SR5.1 bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the TR.SR5.0 and TR.SR5.2 bits will be set to a one.

10.12.2 Transmit Side

See the TR.IOCR1 and TR.IOCR2 registers for information on clock and I/O configurations. The operation of the transmit elastic store is very similar to the receive side. If the transmit-side elastic store is enabled a 1.544MHz or 2.048MHz clock can be applied to the TSYSClk input. For higher-rate system clock applications, see the *Interleaved PCM Bus Operation* section. Controlled slips in the transmit elastic store are reported in the TR.SR5.3 bit and the direction of the slip is reported in the TR.SR5.4 and TR.SR5.5 bits.

10.12.2.1 T1 Mode

If the user selects to apply a 2.048MHz clock to the TSYSClk pin, then the data input at TSER1 will be ignored every fourth channel. Hence, channels 1, 5, 9, 13, 17, 21, 25, and 29 (time slots 0, 4, 8, 12, 16, 20, 24, and 28) will be ignored. The user can supply frame or multiframe sync pulse to the TSSync input. Also, in 2.048MHz applications, the TCHBLK output will be forced high during the channels ignored by the framer.

10.12.2.2 E1 Mode

A 1.544MHz or 2.048MHz clock can be applied to the TSYSClk input. The user must supply a frame-sync pulse or a multiframe-sync pulse to the TSSync input.

10.12.3 Elastic Stores Initialization

There are two elastic-store initializations that can be used to improve performance in certain applications: elastic store reset and elastic store align. Both of these involve the manipulation of the elastic store's read and write pointers and are useful primarily in synchronous applications (RSYSClk/TSYSClk are locked to RCLK/TCLKT, respectively). See [Table 10-11](#) for details.

Table 10-11. Elastic Store Delay After Initialization

| INITIALIZATION | REGISTER BIT | DELAY |
|------------------------------|--------------|------------------------------|
| Receive Elastic Store Reset | TR.ESCR.2 | 8 Clocks < Delay < 1 Frame |
| Transmit Elastic Store Reset | TR.ESCR.6 | 1 Frame < Delay < 2 Frames |
| Receive Elastic Store Align | TR.ESCR.3 | ½ Frame < Delay < 1 ½ Frames |
| Transmit Elastic Store Align | TR.ESCR.7 | ½ Frame < Delay < 1 ½ Frames |

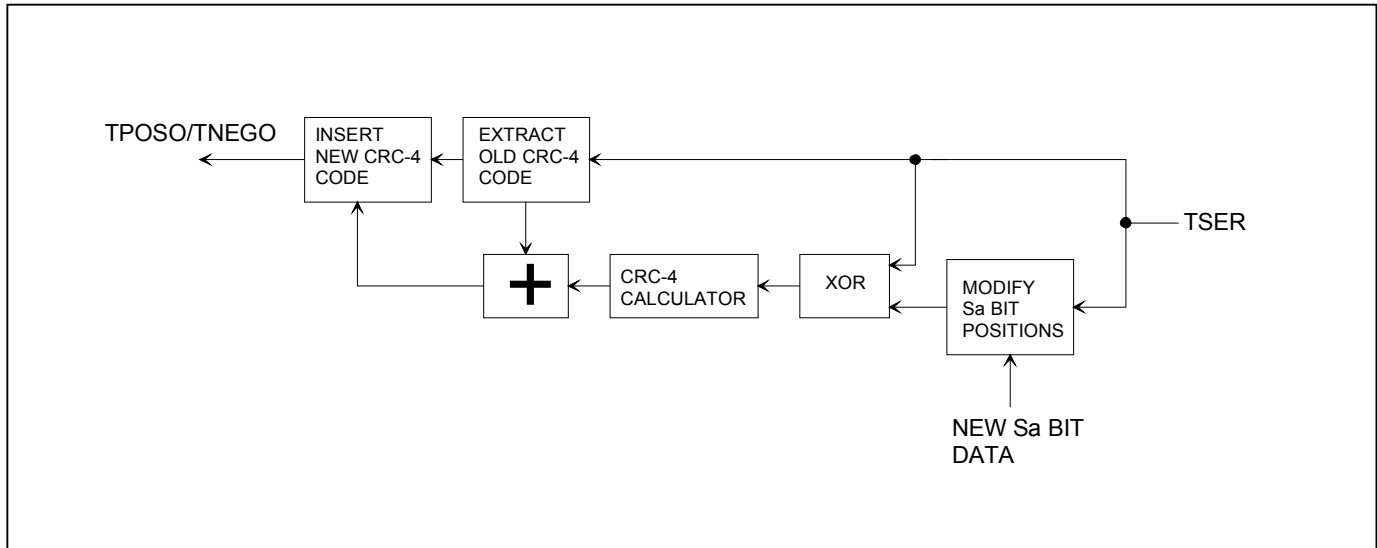
10.12.3.1 Minimum-Delay Mode

When minimum delay mode is enabled the elastic stores will be forced to a maximum depth of 32 bits instead of the normal two-frame depth. TR.ESCR.5 and TR.ESCR.1 enable the transmit and receive elastic store minimum-delay modes. This feature is useful primarily in applications that interface T1 to a 2.048MHz bus without adding the latency that would be associated with using the elastic store in full buffer mode. **Certain restrictions apply when minimum delay mode is used.** Minimum-delay mode can only be used when the elastic store's system clock is locked to its network clock (e.g., RCLK locked to RSYSClk for the receive side and TCLKT locked to TSYSClk for the transmit side). RSYNC must be configured as an output. In E1 operation TSYNC must be configured as an input when transmit minimum delay mode is enabled. In T1 operation TSYNC can be configured as an input or output when transmit minimum delay mode is enabled. In a typical application RSYSClk and TSYSClk are locked to RCLK, and RSYNC (frame output mode) is connected to TSSync (frame input mode). All of the slip contention logic in the framer is disabled (since slips cannot occur). On power-up, after the RSYSClk and TSYSClk signals have locked to their respective network clock signals, the elastic store reset bits (TR.ESCR.2 and TR.ESCR.6) should be toggled from a zero to a one to ensure proper operation.

10.13 G.706 Intermediate CRC-4 Updating (E1 Mode Only)

The device can implement the G.706 CRC-4 recalculation at intermediate path points. When this mode is enabled, the data stream presented at TSER1 already has the FAS/NFAS, CRC multiframe alignment word, and CRC-4 checksum in time slot 0. The user can modify the Sa bit positions. This change in data content is used to modify the CRC-4 checksum. This modification, however, does not corrupt any error information the original CRC-4 checksum may contain. In this mode of operation, TSYNC must be configured to multiframe mode. The data at TSER1 must be aligned to the TSYNC signal. If TSYNC is an input, then the user must assert TSYNC aligned at the beginning of the multiframe relative to TSER1. If TSYNC is an output, the user must multiframe-align the data presented to TSER1.

Figure 10-5. CRC-4 Recalculate Method



10.14 T1 Bit-Oriented Code (BOC) Controller

The transceiver contains a BOC generator on the transmit side and a BOC detector on the receive side. The BOC function is available only in T1 mode.

10.14.1 Transmit BOC

Bits 0 to 5 in the TR.TFDL register contain the BOC message to be transmitted. Setting TR.BOCC.0 = 1 causes the transmit BOC controller to immediately begin inserting the BOC sequence into the FDL bit position. The transmit BOC controller automatically provides the abort sequence. BOC messages are transmitted as long as TR.BOCC.0 is set.

Transmit a BOC

- 1) Write 6-bit code into the TR.TFDL register.
- 2) Set the SBOC bit in TR.BOCC = 1.

10.15 Receive BOC

The receive BOC function is enabled by setting TR.BOCC.4 = 1. The TR.RFDL register now operates as the receive BOC message and information register. The lower six bits of the TR.RFDL register (BOC message bits) are preset to all 1s. When the BOC bits change state, the BOC change-of-state indicator, TR.SR8.0, alerts the host. The host then reads the TR.RFDL register to get the BOC status and message. A change-of-state occurs when either a new BOC code has been present for a time determined by the receive BOC filter bits RBF0 and RBF1 in the TR.BOCC register, or a invalid code is being received.

Receive a BOC

- 1) Set integration time through TR.BOCC.1 and TR.BOCC.2.
- 2) Enable the receive BOC function (TR.BOCC.4 = 1).
- 3) Enable interrupt (TR.IMR8.0 = 1).
- 4) Wait for interrupt to occur.
- 5) Read the TR.RFDL register.
- 6) If TR.SR2.7 = 1, then a valid BOC message was received. The lower six bits of the TR.RFDL register comprise the message.

10.16 Additional (Sa) and International (Si) Bit Operation (E1 Only)

When operated in the E1 mode, the transceiver provides two methods for accessing the Sa and the Si bits. The first method involves using the internal TR.RAF/TR.RNAF and TR.TAF/TR.TNAF registers (Section [10.16.1](#)). The second method, which is covered in Section [10.16.2](#), involves an expanded version of the first method.

10.16.1 Method 1: Internal Register Scheme Based on Double-Frame

On the receive side, the TR.RAF and TR.RNAF registers always report the data as it received in the Sa and Si bit locations. The TR.RAF and TR.RNAF registers are updated on align-frame boundaries. The setting of the receive align frame bit in Status Register 4 (TR.SR4.0) indicates that the contents of the TR.RAF and TR.RNAF have been updated. The host can use the TR.SR4.0 bit to know when to read the TR.RAF and TR.RNAF registers. The host has 250µs to retrieve the data before it is lost.

On the transmit side, data is sampled from the TR.TAF and TR.TNAF registers with the setting of the transmit align frame bit in Status Register 4 (TR.SR4.3). The host can use the TR.SR4.3 bit to know when to update the TR.TAF and TR.TNAF registers. It has 250µs to update the data or else the old data is retransmitted. **If the TR.TAF and TR.TNAF registers are only being used to source the align frame and nonalign frame-sync patterns, then the host need only write once to these registers.** Data in the Si bit position is overwritten if either the framer is (1) programmed to source the Si bits from the TSER1 pin, (2) in the CRC4 mode, or (3) has automatic E-bit insertion enabled. Data in the Sa bit position is overwritten if any of the TR.E1TCR2.3 to TR.E1TCR2.7 bits are set to 1.

10.16.2 Method 2: Internal Register Scheme Based on CRC4 Multiframe

The receive side contains a set of eight registers (TR.RSiAF, TR.RSiNAF, TR.RRA, and TR.RSa4–TR.RSa8) that report the Si and Sa bits as they are received. These registers are updated with the setting of the receive CRC4 multiframe bit in Status Register 2 (TR.SR4.1). The host can use the TR.SR4.1 bit to know when to read these registers. The user has 2ms to retrieve the data before it is lost. The MSB of each register is the first received. See the following register descriptions for more details.

The transmit side also contains a set of eight registers (TR.TSiAF, TR.TSiNAF, TR.TRA, and TR.TSa4–TR.TSa8) that, through the transmit Sa bit control register (TR.TSACR), can be programmed to insert Si and Sa data. Data is sampled from these registers with the setting of the transmit multiframe bit in Status Register 2 (TR.SR4.4). The host can use the TR.SR4.4 bit to know when to update these registers. It has 2ms to update the data or else the old data is retransmitted. The MSB of each register is the first bit transmitted. See the register descriptions for more details.

10.17 Additional HDLC Controllers in T1/E1/J1 Transceiver

This device has two enhanced HDLC controllers, HDLC #1 and HDLC #2. Each controller is configurable for use with time slots, Sa4 to Sa8 bits (E1 mode), or the FDL (T1 mode). Each HDLC controller has 128-byte buffers in the transmit and receive paths. When used with time slots, the user can select any time slot or multiple time slots, contiguous or noncontiguous, as well as any specific bits within the time slot(s) to assign to the HDLC controllers.

The user must not map both transmit HDLC controllers to the same Sa bits, time slots or, in T1 mode, map both controllers to the FDL. HDLC #1 and HDLC #2 are identical in operation and therefore the following operational description refers only to a singular controller.

The HDLC controller performs the entire necessary overhead for generating and receiving performance report messages (PRMs) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controller automatically generates and detects flags, generates and checks the CRC check sum, generates and detects abort sequences, stuffs and destuffs zeros, and byte aligns to the data stream. The 128-byte buffers in the HDLC controller are large enough to allow a full PRM to be received or transmitted without host intervention.

The HDLC registers are divided into four groups: control/configuration, status/information, mapping, and FIFOs. [Table 10-12](#) lists these registers by group.

10.17.1 HDLC Configuration

The TR.HxTC and TR.HxRC registers perform the basic configuration of the HDLC controllers. Operating features such as CRC generation, zero stuffer, transmit and receive HDLC mapping options, and idle flags are selected here. These registers also reset the HDLC controllers.

Table 10-12. HDLC Controller Registers

| REGISTER | FUNCTION |
|--|--|
| CONTROL AND CONFIGURATION | |
| TR.H1TC, HDLC #1 Transmit Control Register TR.H2TC, HDLC #2 Transmit Control Register | General control over the transmit HDLC controllers |
| TR.H1RC, HDLC #1 Receive Control Register TR.H2RC, HDLC #2 Receive Control Register | General control over the receive HDLC controllers |
| TR.H1FC, HDLC #1 FIFO Control Register TR.H2FC, HDLC #2 FIFO Control Register | Sets high watermark for receiver and low watermark for transmitter |
| STATUS AND INFORMATION | |
| TR.SR6, HDLC #1 Status Register TR.SR7, HDLC #2 Status Register | Key status information for both transmit and receive directions |
| TR.IMR6, HDLC #1 Interrupt Mask Register TR.IMR7, HDLC #2 Interrupt Mask Register | Selects which bits in the status registers (SR7 and SR8) cause interrupts |
| TR.INFO4, HDLC #1 and #2 Information Register TR.INFO5, HDLC #1 Information Register TR.INFO6, HDLC #2 Information Register | Information about HDLC controller |
| TR.H1RPBA, HDLC #1 Receive Packet Bytes Available TR.H2RPBA, HDLC #2 Receive Packet Bytes Available | Indicates the number of bytes that can be read from the receive FIFO |
| TR.H1TFBA, HDLC #1 Transmit FIFO Buffer Available TR.H2TFBA, HDLC #2 Transmit FIFO Buffer Available | Indicates the number of bytes that can be written to the transmit FIFO |
| MAPPING | |
| TR.H1RCS1, TR.H1RCS2, TR.H1RCS3, TR.H1RCS4, HDLC #1 Receive Channel Select Registers TR.H2RCS1, TR.H2RCS2, TR.H2RCS3, TR.H2RCS4, HDLC #2 Receive Channel Select Registers | Selects which channels are mapped to the receive HDLC controller |
| TR.H1RTSBS, HDLC #1 Receive TS/Sa Bit Select TR.H2RTSBS, HDLC #2 Receive TS/Sa Bit Select | Selects which bits in a channel are used or which Sa bits are used by the receive HDLC controller |
| TR.H1TCS1, TR.H1TCS2, TR.H1TCS3, TR.H1TCS4, HDLC #1 Transmit Channel Select Registers TR.H2TCS1, TR.H2TCS2, TR.H2TCS3, TR.H2TCS4, HDLC #2 Transmit Channel Select Registers | Selects which channels are mapped to the transmit HDLC controller |
| TR.H1TTSBS, HDLC # 1 Transmit TS/Sa Bit Select TR.H2TTSBS, HDLC # 2 Transmit TS/Sa Bit Select | Selects which bits in a channel are used or which Sa bits are used by the transmit HDLC controller |
| FIFOs | |
| TR.H1RF, HDLC #1 Receive FIFO Register TR.H2RF, HDLC #1 Receive FIFO Register | Access to 128-byte receive FIFO |
| TR.H1TF, HDLC #1 Transmit FIFO Register TR.H2TF, HDLC #2 Transmit FIFO Register | Access to 128-byte transmit FIFO |

10.17.2 FIFO Control

The FIFO control register (TR.HxFC) controls and sets the watermarks for the transmit and receive FIFOs. Bits 3, 4, and 5 set the transmit low watermark and the lower 3 bits set the receive high watermark.

When the transmit FIFO empties below the low watermark, the TLWM bit in the appropriate HDLC status register TR.SR6 or TR.SR7 is set. TLWM is a real-time bit and remains set as long as the transmit FIFO's read pointer is below the watermark. If enabled, this condition can also cause an interrupt through the $\overline{\text{INT}}$ pin.

When the receive FIFO fills above the high watermark, the RHWM bit in the appropriate HDLC status register is set. RHWM is a real-time bit and remains set as long as the receive FIFO's write pointer is above the watermark. If enabled, this condition can also cause an interrupt through the $\overline{\text{INT}}$ pin.

10.17.3 HDLC Mapping

The HDLC controllers must be assigned a space in the T1/E1 bandwidth in which they transmit and receive data. The controllers can be mapped to either the FDL (T1), Sa bits (E1), or to channels. If mapped to channels, then any channel or combination of channels, contiguous or not, can be assigned to an HDLC controller. When assigned to a channel(s), any combination of bits within the channel(s) can be avoided.

The TR.HxRCS1–TR.HxRCS4 registers are used to assign the receive controllers to channels 1–24 (T1) or 1–32 (E1) according to the following table:

| REGISTER | CHANNELS |
|-----------|----------|
| TR.HxRCS1 | 1–8 |
| TR.HxRCS2 | 9–16 |
| TR.HxRCS3 | 17–24 |
| TR.HxRCS4 | 25–32 |

The TR.HxTCS1 – TR.HxTCS4 registers are used to assign the transmit controllers to channels 1–24 (T1) or 1–32 (E1) according to the following table.

| REGISTER | CHANNELS |
|-----------|----------|
| TR.HxTCS1 | 1–8 |
| TR.HxTCS2 | 9–16 |
| TR.HxTCS3 | 17–24 |
| TR.HxTCS4 | 25–32 |

10.17.4 FIFO Information

The transmit FIFO buffer-available register indicates the number of bytes that can be written into the transmit FIFO. The count from this register informs the host as to how many bytes can be written into the transmit FIFO without overflowing the buffer.

10.17.5 Receive Packet-Bytes Available

The lower 7 bits of the receive packet-bytes available register indicates the number of bytes (0 through 127) that can be read from the receive FIFO. The value indicated by this register (lower seven bits) informs the host as to how many bytes can be read from the receive FIFO without going past the end of a message. This value refers to one of four possibilities: the first part of a packet, the continuation of a packet, the last part of a packet, or a complete packet. After reading the number of bytes indicated by this register, the host then checks the HDLC information register for detailed message status.

If the value in the TR.HxRPBA register refers to the beginning portion of a message or continuation of a message, then the MSB of the TR.HxRPBA register returns a value of 1. This indicates that the host can safely read the number of bytes returned by the lower seven bits of the TR.HxRPBA register, but there is no need to check the information register since the packet has not yet terminated (successfully or otherwise).

10.17.5.1 Receive HDLC Code Example

The following is an example of a receive HDLC routine:

- 1) Reset receive HDLC controller.
- 2) Set HDLC mode, mapping, and high watermark.
- 3) Start new message buffer.
- 4) Enable RPE and RHWM interrupts.
- 5) Wait for interrupt.
- 6) Disable RPE and RHWM interrupts.
- 7) Read TR.HxRPBA register. N = TR.HxRPBA (lower 7 bits are byte count, MSB is status).
- 8) Read (N and 7Fh) bytes from receive FIFO and store in message buffer.
- 9) Read TR.INFO5 register.
- 10) If PS2, PS1, PS0 = 000, then go to Step 4.
- 11) If PS2, PS1, PS0 = 001, then packet terminated OK, save present message buffer.
- 12) If PS2, PS1, PS0 = 010, then packet terminated with CRC error.
- 13) If PS2, PS1, PS0 = 011, then packet aborted.
- 14) If PS2, PS1, PS0 = 100, then FIFO overflowed.
- 15) Go to Step 3.

10.18 Legacy FDL Support (T1 Mode)

10.18.1 Overview

To provide backward compatibility to the older DS21x52 T1 device, the transceiver maintains the circuitry that existed in the previous generation of the T1 framer. In new applications, it is recommended that the HDLC controllers and BOC controller described in Section [10.14](#) and [10.17](#) are used.

10.18.2 Receive Section

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the receive FDL register (TR.RFDL). Because the TR.RFDL is 8 bits in length, it fills up every 2ms (8 x 250µs). The framer signals an external microcontroller that the buffer has filled through the TR.SR8.3 bit. If enabled through TR.IMR8.3, the $\overline{\text{INT}}$ pin toggles low, indicating that the buffer has filled and needs to be read. The user has 2ms to read this data before it is lost. If the byte in the TR.RFDL matches either of the bytes programmed into the TR.RFDLM1 or TR.RFDLM2 registers, then the TR.SR8.1 bit is set to a 1 and the INT pin toggles low if enabled through TR.IMR8.1. This feature allows an external microcontroller to ignore the FDL or Fs pattern until an important event occurs.

The framer also contains a zero destuffer, which is controlled through the TR.T1RCR2.3 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of an LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled through TR.T1RCR2.3, the device automatically looks for five 1s in a row, followed by a 0. If it finds such a pattern, it automatically removes the zero. If the zero destuffer sees six or more 1s in a row followed by a 0, the 0 is not removed. The TR.T1RCR2.3 bit should always be set to a 1 when the device is extracting the FDL. Refer to *Application Note 335: DS2141A, DS2151 Controlling the FDL* for information about using the device in FDL applications in this legacy support mode.

10.18.3 Transmit Section

The transmit section shifts out into the T1 data stream either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the transmit FDL register (TR.TFDL). When a new value is written to TR.TFDL, it is multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full 8 bits have been shifted out, the framer signals the host microcontroller by setting the TR.SR8.2 bit to a 1 that the buffer is empty and that more data is needed. The INT also toggles low if enabled through TR.IMR8.2. The user has 2ms to update TR.TFDL with a new value. If TR.TFDL is not updated, the old value in TR.TFDL is transmitted once again. The framer also contains a zero stuffer that is controlled through the TR.T1TCR2.5 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of an LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled through TR.T1TCR2.5, the framer automatically looks for five 1s in a row. If it finds such a pattern, it automatically inserts a 0 after the five 1s. The TR.T1TCR2.5 bit should always be set to a 1 when the framer is inserting the FDL.

10.19 D4/SLC-96 Operation

In the D4 framing mode, the framer uses the TR.TFDL register to insert the Fs framing pattern. To allow the device to properly insert the Fs framing pattern, the TR.TFDL register at address C1h must be programmed to 1Ch and the following bits must be programmed as shown:

TR.T1TCR1.2 = 0 (source Fs data from the TR.TFDL register)
TR.T1TCR2.6 = 1 (allow the TR.TFDL register to load on multiframe boundaries)

Since the SLC-96 message fields share the Fs-bit position, the user can access these message fields through the TR.TFDL and TR.RFDL registers. Refer to *Application Note 345: DS2141A, DS2151, DS2152 SLC-96* for a detailed description about implementing an SLC-96 function.

10.20 Line Interface Unit (LIU)

The LIU contains three sections: the receiver that handles clock and data recovery, the transmitter that waveshapes and drives the T1 line, and the jitter attenuator. These three sections are controlled by the line interface control registers (LIC1–LIC4), which are described in the following sections. The LIU has its own T1/E1 mode-select bit and can operate independently of the framer function.

The transceiver can switch between T1 or E1 networks without changing external components on the transmit or receive side. [Figure 10-8](#) shows a network connection using minimal components. In this configuration, the transceiver can connect to T1, J1, or E1 (75Ω or 120Ω) without component changes. The receiver can adjust the 120Ω termination to 100Ω or 75Ω. The transmitter can adjust its output impedance to provide high return-loss characteristics for 120Ω, 100Ω, and 75Ω lines. Other components can be added to this configuration to meet safety and network protection requirements (Section [10.24](#)).

10.20.1 LIU Operation

The analog AMI/HDB3 waveform off the E1 line or the AMI/B8ZS waveform off of the T1 line is transformer-coupled into the RTIP and RRING pins of the device. The user has the option to use internal termination, software selectable for 75Ω/100Ω/120Ω applications, or external termination. The LIU recovers clock and data from the analog signal and passes it through the jitter-attenuation mux outputting the received line clock at RCLKn and bipolar or NRZ data at RPOSO and RNEGO. The transceiver contains an active filter that reconstructs the analog-received signal for the nonlinear losses that occur in transmission. The receive circuitry also is configurable for various monitor applications. The device has a usable receive sensitivity of 0dB to -43dB for E1 and 0dB to -36dB for T1, which allow the device to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6k feet (T1) in length. Data input at TPOSI and TNEGI is sent through the jitter-attenuation mux to the waveshaping circuitry and line driver. The transceiver drives the E1 or T1 line from the TTIP and TRING pins through a coupling transformer. The line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long-haul (CSU) or short-haul (DSX-1) lines for T1.

10.20.2 Receiver

The receiver contains a digital clock recovery system. The device couples to the receive E1 or T1 twisted pair (or coaxial cable in 75Ω E1 applications) through a 1:1 transformer. See [Table 10-13](#) for transformer details. The device has the option of using software-selectable termination requiring only a single fixed pair of termination resistors.

The transceiver's LIU is designed to be fully software selectable for E1 and T1, requiring no change to any external resistors for the receive side. The receive side allows the user to configure the transceiver for 75Ω, 100Ω, or 120Ω receive termination by setting the RT1 (TR.LIC4.1) and RT0 (TR.LIC4.0) bits. When using the internal termination feature, the resistors labeled R in [Figure 10-8](#) should be 60Ω each. If external termination is used, RT1 and RT0 should be set to 0 and the resistors labeled R in [Figure 10-8](#) should be 37.5Ω, 50Ω, or 60Ω each, depending on the line impedance.

There are two ranges of user-selectable receive sensitivity for T1 and E1. The EGL bit of TR.LIC1 (TR.LIC1.4) selects the full or limited sensitivity. The resultant E1 or T1 clock derived from MCLK is multiplied by 16 through an internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16-times over-sampler that is used to recover the clock and data. This over-sampling technique offers outstanding performance to meet jitter tolerance specifications shown in [Figure 10-11](#).

Normally, the clock that is output at the RCLKn pin is the recovered clock from the E1 AMI/HDB3 or T1 AMI/B8ZS waveform presented at the RTIP and RRING inputs. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLKn to an approximate 50% duty cycle. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLKn output can exhibit slightly shorter high cycles of the clock. This is because of the highly over-sampled digital-clock recovery circuitry. See the *Receive AC Timing Characteristics* in Section [14.10](#) for more details. When no signal is present at RTIP and RRING, a receive carrier loss (RCL) condition occurs and the RCLKn is derived from the JACLK source.

10.20.2.1 Receive Level Indicator and Threshold Interrupt

The device reports the signal strength at RTIP and RRING in 2.5dB increments through RL3–RL0 located in Information Register 2 (TR.INFO2). This feature is helpful when trouble-shooting line-performance problems. The device can initiate an interrupt whenever the input falls below a certain level through the input-level under-threshold indicator (TR.SR1.7). Using the RLT0–RLT4 bits of the TR.CCR4 register, the user can set a threshold in 2.5dB increments. The TR.SR1.7 bit is set whenever the input level at RTIP and RRING falls below the threshold set by the value in RLT0–RLT4. The level must remain below the programmed threshold for approximately 50ms for this bit to be set. The accuracy of the receive level indication is ± 1 LSB (2.5dB) from +25°C to +85°C and ± 2 LSBs (5dB) from –40°C to +25°C.

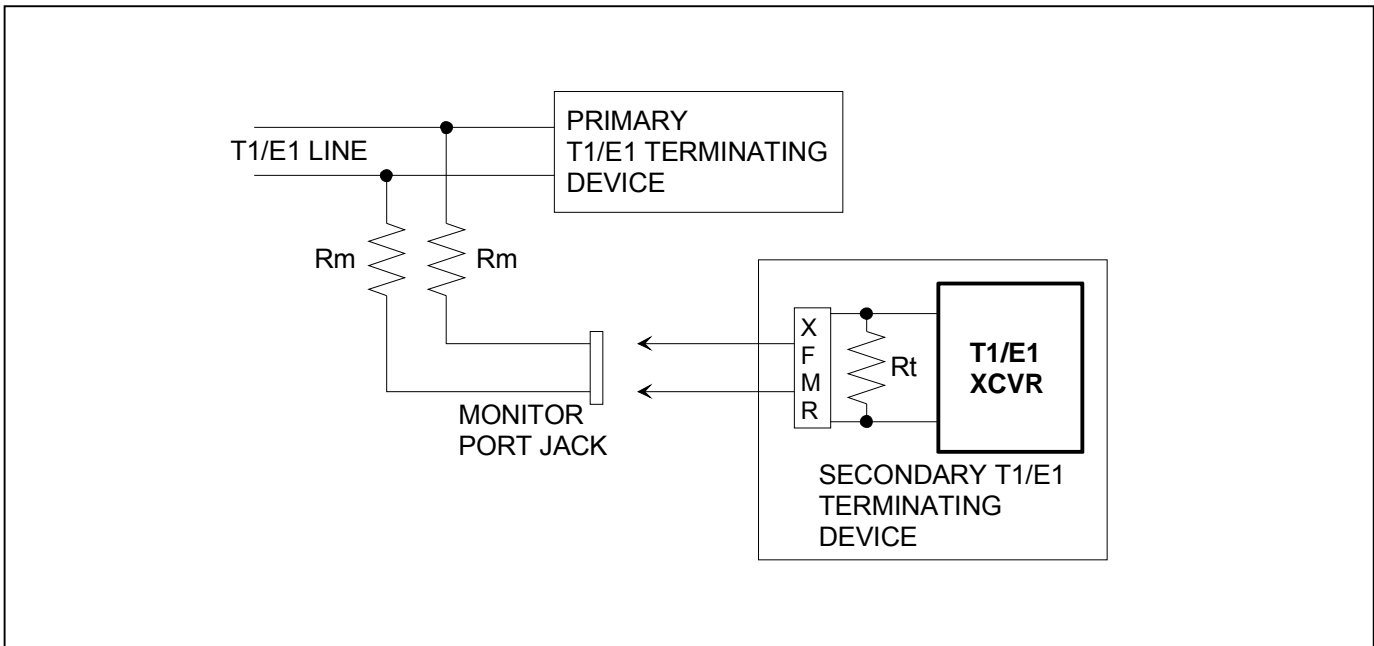
10.20.2.2 Receive G.703 Synchronization Signal (E1 Mode)

The transceiver is capable of receiving a 2.048MHz square-wave synchronization clock as specified in Section 13 of ITU G.703, October 1998. In order to use the device in this mode, set the receive synchronization clock enable (TR.LIC3.2) = 1.

10.20.2.3 Monitor Mode

Monitor applications in both E1 and T1 require various flat gain settings for the receive-side circuitry. The device can be programmed to support these applications through the monitor mode control bits MM1 and MM0 in the TR.LIC3 register ([Figure 10-6](#)).

Figure 10-6. Typical Monitor Application



10.20.3 Transmitter

The transceiver uses a phase-lock loop along with a precision digital-to-analog converter (DAC) to create the waveforms that are transmitted onto the E1 or T1 line. The waveforms created by the device meet the latest ETSI, ITU, ANSI, and AT&T specifications. The user selects which waveform is generated by setting the ETS bit (TR.LIC2.7) for E1 or T1 operation, then programming the L2/L1/L0 bits in register TR.LIC1 for the appropriate application.

A 2.048MHz or 1.544MHz clock is required at TDCLKI for transmitting data presented at TPOSI and TNEGI. Normally these pins are connected to TCLKO, TPOSO, and TNEGO. However, the LIU can operate in an independent fashion. ITU specification G.703 requires an accuracy of ± 50 ppm for both T1 and E1. TR62411 and ANSI specifications require an accuracy of ± 32 ppm for T1 interfaces. The clock can be sourced internally from RCLKn or JACLK. See TR.LIC2.3, TR.LIC4.4, and TR.LIC4.5 for details. Because of the nature of the transmitter's design, very little jitter (less than $0.005U_{I_{P,P}}$ broadband from 10Hz to 100kHz) is added to the jitter present on TCLKT. Also, the waveforms created are independent of the duty cycle of TCLKT. The transmitter in the device couples to the E1 or T1 transmit twisted pair (or coaxial cable in some E1 applications) through a 1:2 step-up transformer. For the device to create the proper waveforms, the transformer used must meet the specifications listed in [Table 10-13](#). The device has the option of using software-selectable transmit termination.

The transmit line drive has two modes of operation: fixed gain or automatic gain. In the fixed gain mode, the transmitter outputs a fixed current into the network load to achieve a nominal pulse amplitude. In the automatic gain mode, the transmitter adjusts its output level to compensate for slight variances in the network load. See the *Transmit Line Build-Out Control (TR.TLBC)* register for details.

10.20.3.1 Transmit Short-Circuit Detector/Limiter

The device has an automatic short-circuit limiter that limits the source current to 50mA (RMS) into a 1Ω load. This feature can be disabled by setting the SCLD bit (TR.LIC2.1) = 1. TCLE (TR.INFO2.5) provides a real-time indication of when the current limiter is activated. If the current limiter is disabled, TCLE indicates that a short-circuit condition exists. Status Register TR.SR1.2 provides a latched version of the information, which can be used to activate an interrupt when enabled by the TR.IMR1 register. The TPD bit (TR.LIC1.0) powers down the transmit line driver and three-states the TTIP and TRING pins.

10.20.3.2 Transmit Open-Circuit Detector

The device can also detect when the TTIP or TRING outputs are open circuited. TOCD (TR.INFO2.4) provides a real-time indication of when an open circuit is detected. TR.SR1 provides a latched version of the information (TR.SR1.1), which can be used to activate an interrupt when enabled by the TR.IMR1 register.

10.20.3.3 Transmit BPV Error Insertion

When IBPV (TR.LIC2.5) is transitioned from a 0 to a 1, the device waits for the next occurrence of three consecutive 1s to insert a BPV. IBPV must be cleared and set again for another BPV error insertion.

10.20.3.4 Transmit G.703 Synchronization Signal (E1 Mode)

The transceiver can transmit the 2.048MHz square-wave synchronization clock as specified in Section 13 of ITU G.703, October 1998. In order to transmit the 2.048MHz clock, when in E1 mode, set the transmit synchronization clock enable (TR.LIC3.1) = 1.

10.21 MCLK Prescaler

A 16.384MHz, 8.192MHz, 4.096MHz, 2.048MHz, or 1.544MHz clock must be applied at MCLK. ITU specification G.703 requires an accuracy of ± 50 ppm for both T1 and E1. TR62411 and ANSI specifications require an accuracy of ± 32 ppm for T1 interfaces. A prescaler divides the 16MHz, 8MHz, or 4MHz clock down to 2.048MHz. There is an on-board PLL for the jitter attenuator, which converts the 2.048MHz clock to a 1.544MHz rate for T1 applications. Setting JAMUX (TR.LIC2.3) to a logic 0 bypasses this PLL.

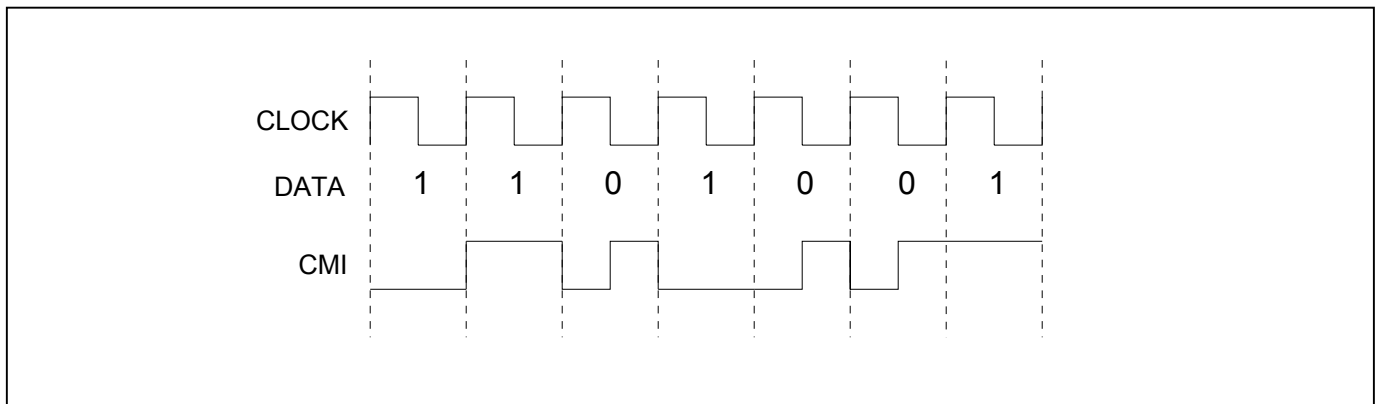
10.22 Jitter Attenuator

The device contains an on-board jitter attenuator that can be set to a depth of either 32 or 128 bits through the JABDS bit (TR.LIC1.2). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay-sensitive applications. The characteristics of the attenuation are shown in [Figure 10-13](#). The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit (TR.LIC1.3). Setting the DJA bit (TR.LIC1.1) disables (in effect, removes) the jitter attenuator. On-board circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLKT pin to create a smooth jitter-free clock that is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLKT pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either $120U_{P,P}$ (buffer depth is 128 bits) or $28U_{P,P}$ (buffer depth is 32 bits), then the transceiver divides the internal nominal 32.768MHz (E1) or 24.704MHz (T1) clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the jitter attenuator limit trip (JALT) bit in Status Register 1 (TR.SR1.4).

10.23 CMI (Code Mark Inversion) Option

The device provides a CMI interface for connection to optical transports. This interface is a unipolar 1T2B signal type. Ones are encoded as either a logical 1 or 0 level for the full duration of the clock period. Zeros are encoded as a 0-to-1 transition at the middle of the clock period.

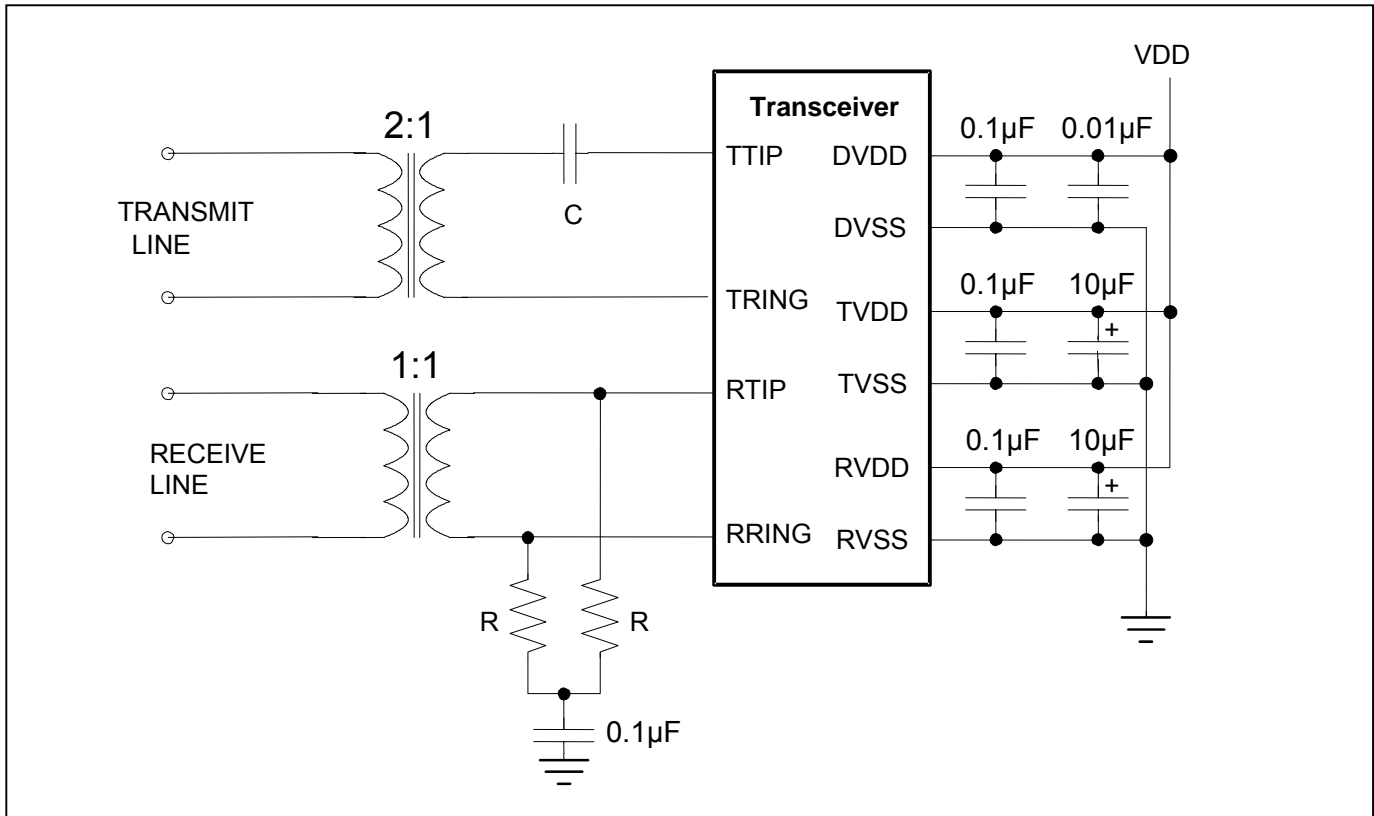
Figure 10-7. CMI Coding



Transmit and receive CMI are enabled through TR.LIC4.7. When this register bit is set, the TTIP pin outputs CMI-coded data at normal levels. This signal can be used to directly drive an optical interface. When CMI is enabled, the user can also use HDB3/B8ZS coding. When this register bit is set, the RTIP pin becomes a unipolar CMI input. The CMI signal is processed to extract and align the clock with data.

10.24 Recommended Circuits

Figure 10-8. Basic Interface



Note 1: All resistor values are $\pm 1\%$.

Note 2: Resistors R should be set to 60Ω each if the internal receive-side termination feature is enabled. When this feature is disabled, $R = 37.5\Omega$ for 75Ω coaxial E1 lines, 60Ω for 120Ω twisted-pair E1 lines, or 50Ω for 100Ω twisted-pair T1 lines.

Note 3: $C = 1\mu\text{F}$ ceramic.

Refer to *Application Note 324: T1/E1 Network Interface Design* for more information on protected interfaces.

Table 10-13. Transformer Specifications

| SPECIFICATION | | RECOMMENDED VALUE |
|------------------------------------|-----------------------|--|
| Turns Ratio 3.3V Applications | | 1:1 (receive) and 1:2 (transmit) $\pm 2\%$ |
| Primary Inductance | | $600\mu\text{H}$ (min) |
| Leakage Inductance | | $1.0\mu\text{H}$ (max) |
| Intertwining Capacitance | | 40pF (max) |
| Transmit Transformer DC Resistance | Primary (Device Side) | 1.0Ω (max) |
| | Secondary | 2.0Ω (max) |
| Receive Transformer DC Resistance | Primary (Device Side) | 1.2Ω (max) |
| | Secondary | 1.2Ω (max) |

Figure 10-9. E1 Transmit Pulse Template

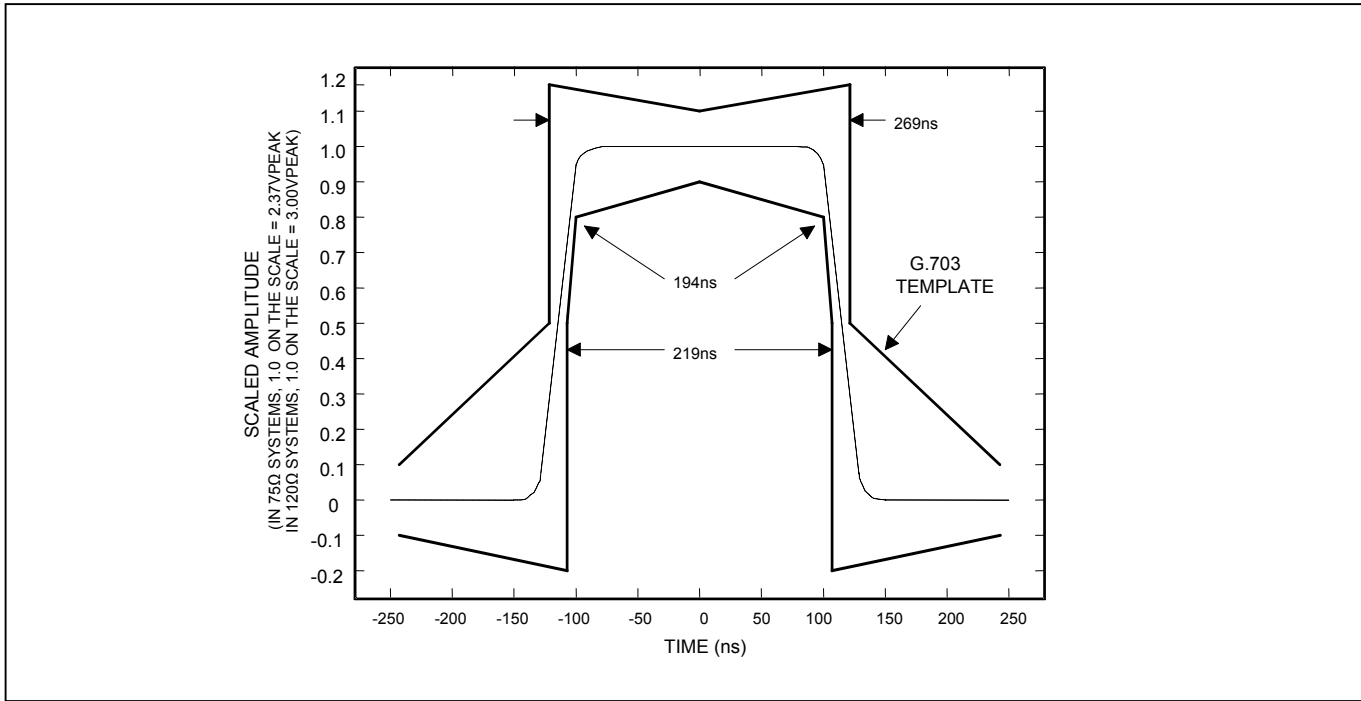


Figure 10-10. T1 Transmit Pulse Template

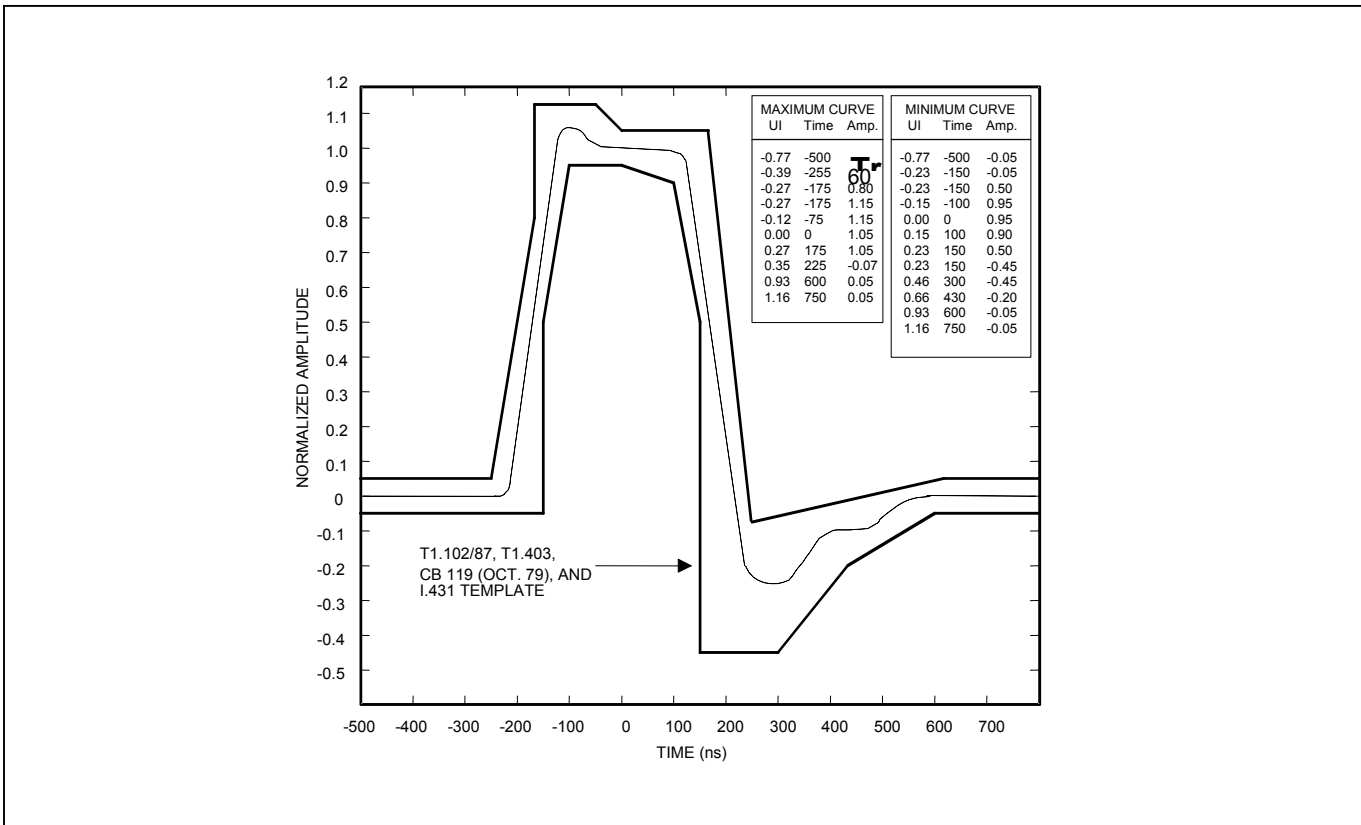


Figure 10-11. Jitter Tolerance

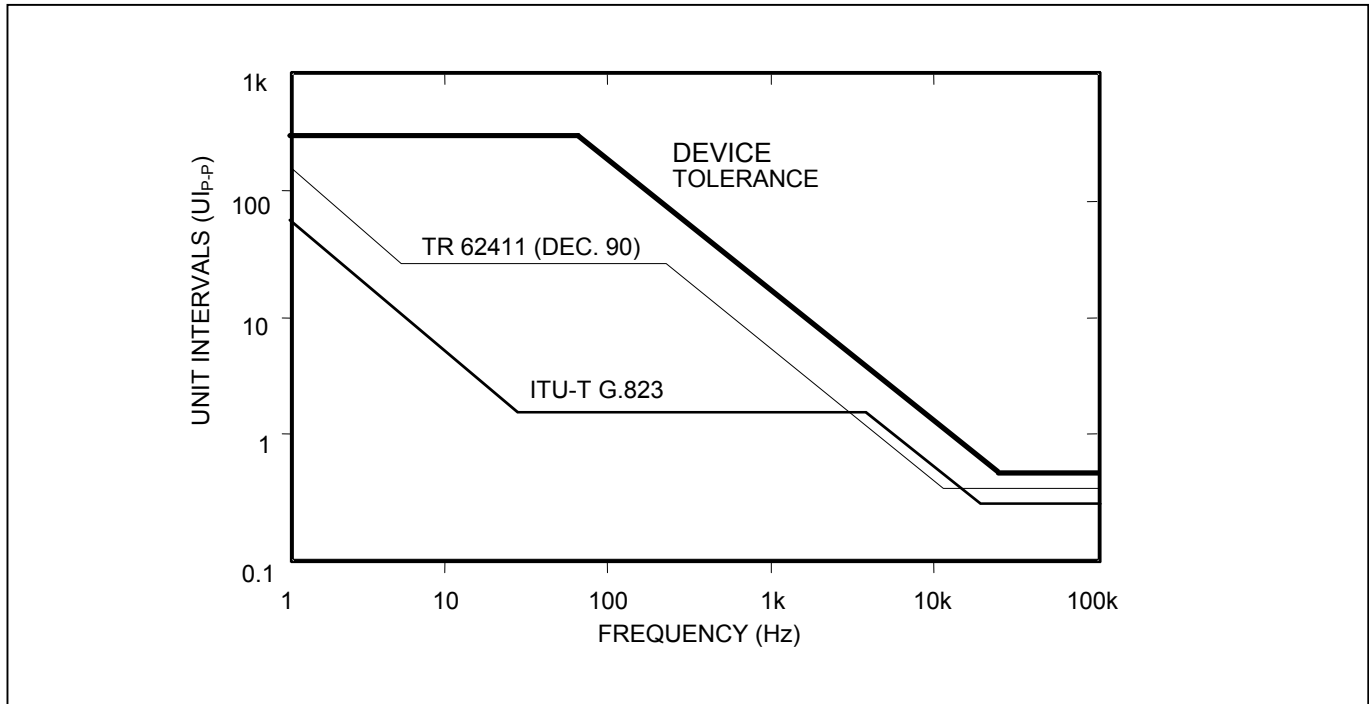


Figure 10-12. Jitter Tolerance (E1 Mode)

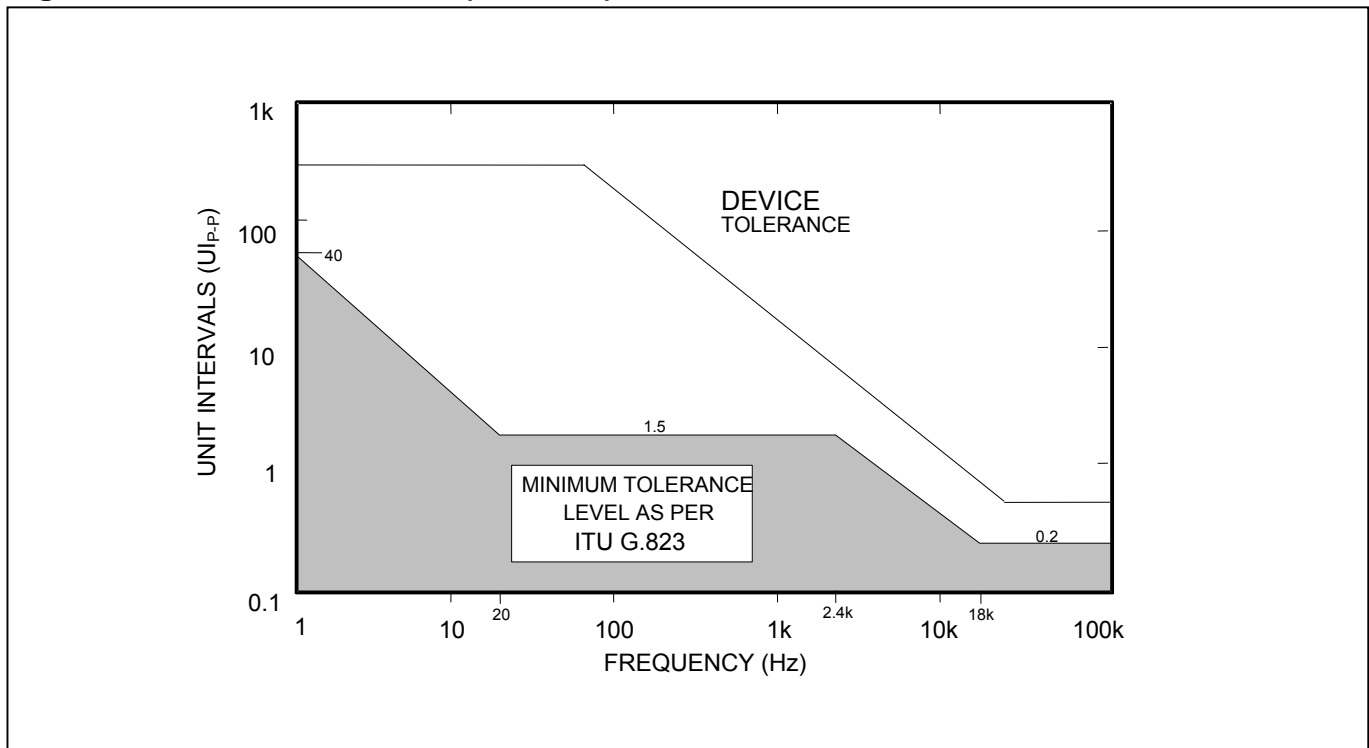


Figure 10-13. Jitter Attenuation (T1 Mode)

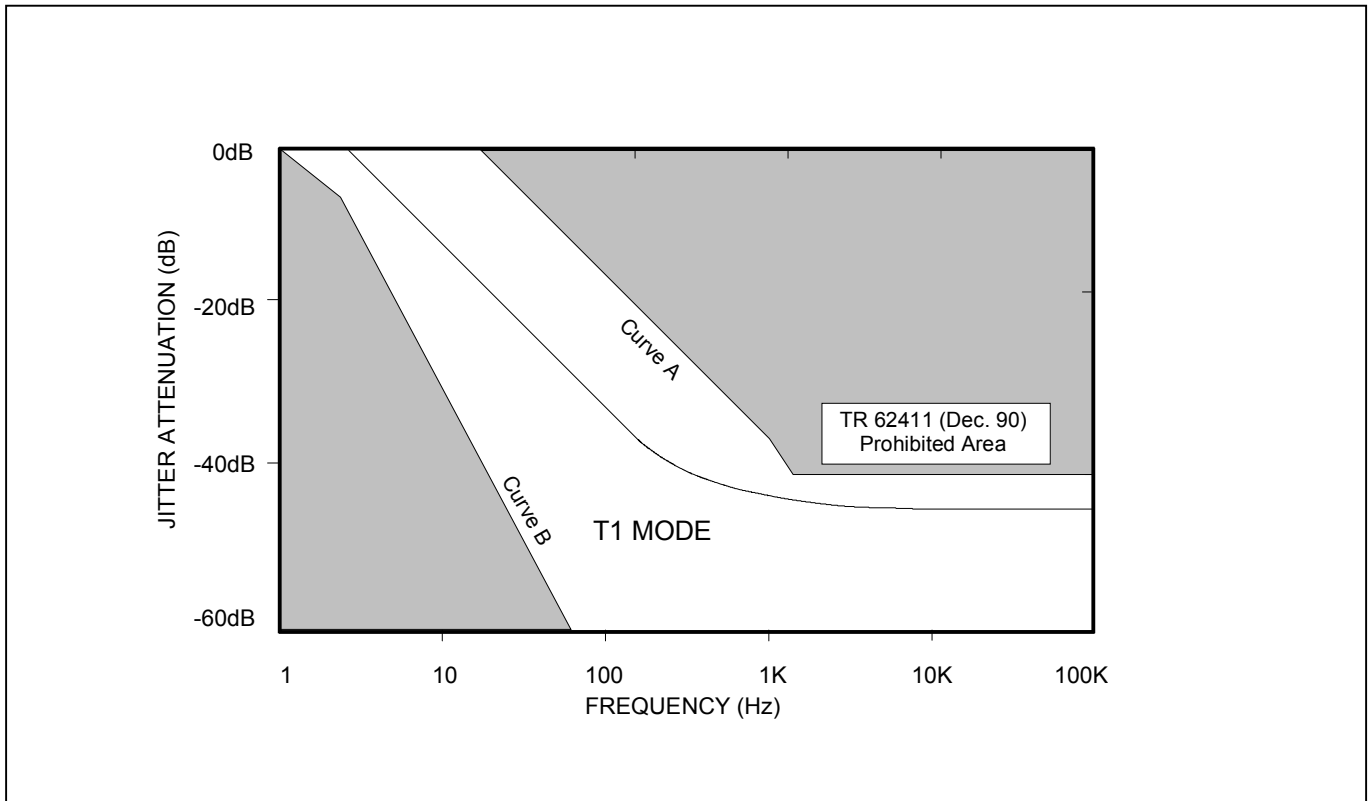


Figure 10-14. Jitter Attenuation (E1 Mode)

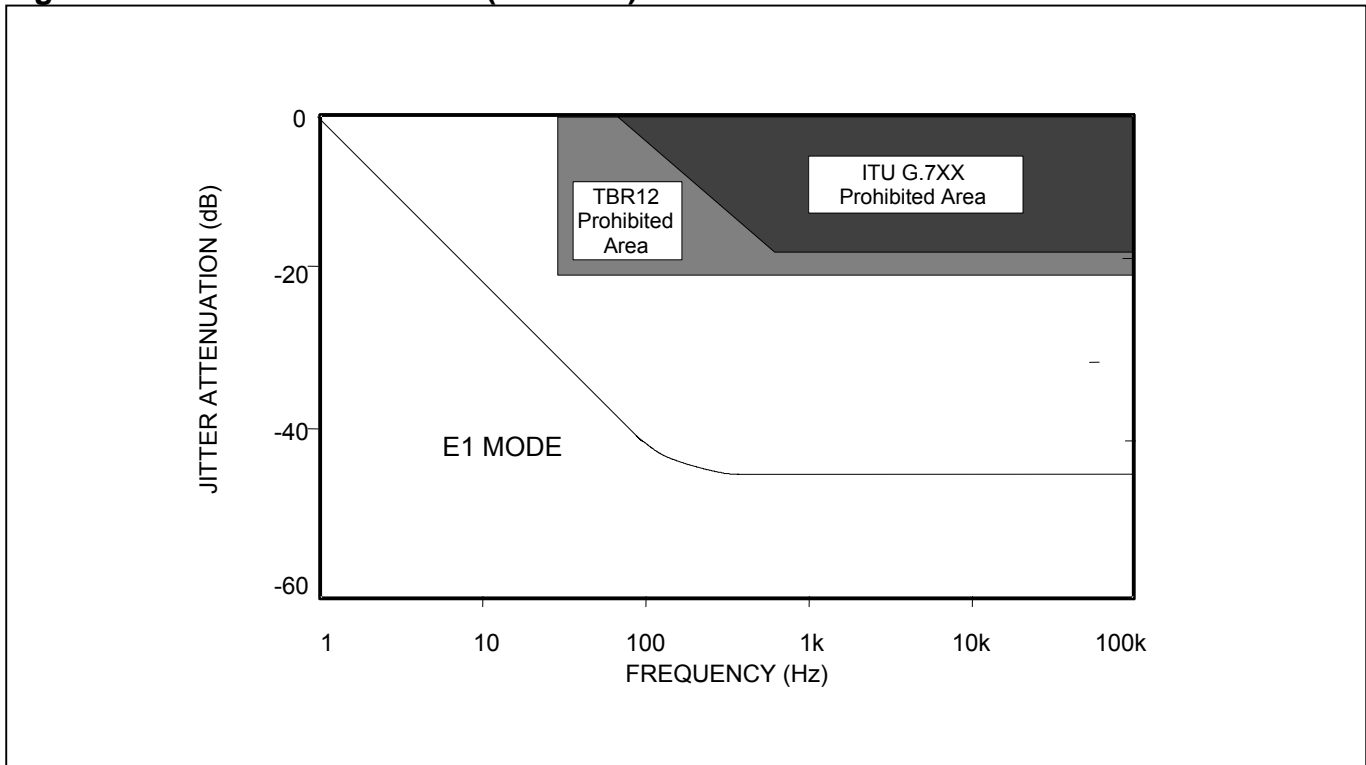
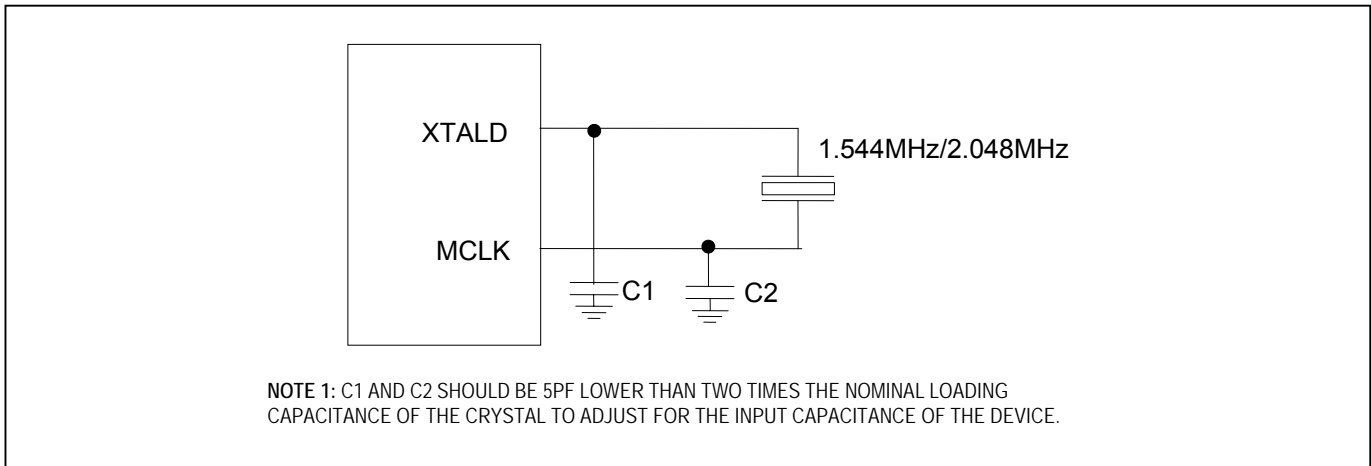


Figure 10-15. Optional Crystal Connections



10.25 T1/E1/J1 Transceiver BERT Function

Each integrated T1/E1 transceiver contains a BERT. The BERT block can generate and detect pseudorandom and repeating bit patterns. It is used to test and stress data communication links, and it is capable of generating and detecting the following patterns:

- The pseudorandom patterns 2E7, 2E11, 2E15, and QRSS
- A repetitive pattern from 1 to 32 bits in length
- Alternating (16-bit) words that flip every 1 to 256 words
- Daly pattern

The BERT receiver has a 32-bit bit counter and a 24-bit error counter. The BERT receiver reports three events: a change in receive synchronizer status, a bit error being detected, and if either the bit counter or the error counter overflows. Each of these events can be masked within the BERT function through the BERT control register 1 (TR.BC1). If the software detects that the BERT has reported an event, then the software must read the BERT information register (BIR) to determine which event(s) has occurred. To activate the BERT block, the host must configure the BERT mux through the TR.BIC register.

10.25.1 BERT Status

TR.SR9 contains the status information on the BERT function. The host can be alerted through this register when there is a BERT change-of-state. A major change-of-state is defined as either a change in the receive synchronization (i.e., the BERT has gone into or out of receive synchronization), a bit error has been detected, or an overflow has occurred in either the bit counter or the error counter. The host must read status register 9 (TR.SR9) to determine the change-of-state.

10.25.2 BERT Mapping

The BERT function can be assigned to the network direction or backplane direction through the direction control bit in the BIC register (TR.BIC.1). See [Figure 10-16](#) and [Figure 10-17](#). The BERT also can be assigned on a per-channel basis. The BERT transmit control selector (BTCS) and BERT receive control selector (BRCS) bits of the per-channel pointer register (TR.PCPR) are used to map the BERT function into time slots of the transmit and receive data streams. In T1 mode, the user can enable mapping into the F-bit position for the transmit and receive directions through the RFUS and TFUS bits in the BERT interface control (TR.BIC) register.

Figure 10-16. Simplified Diagram of BERT in Network Direction

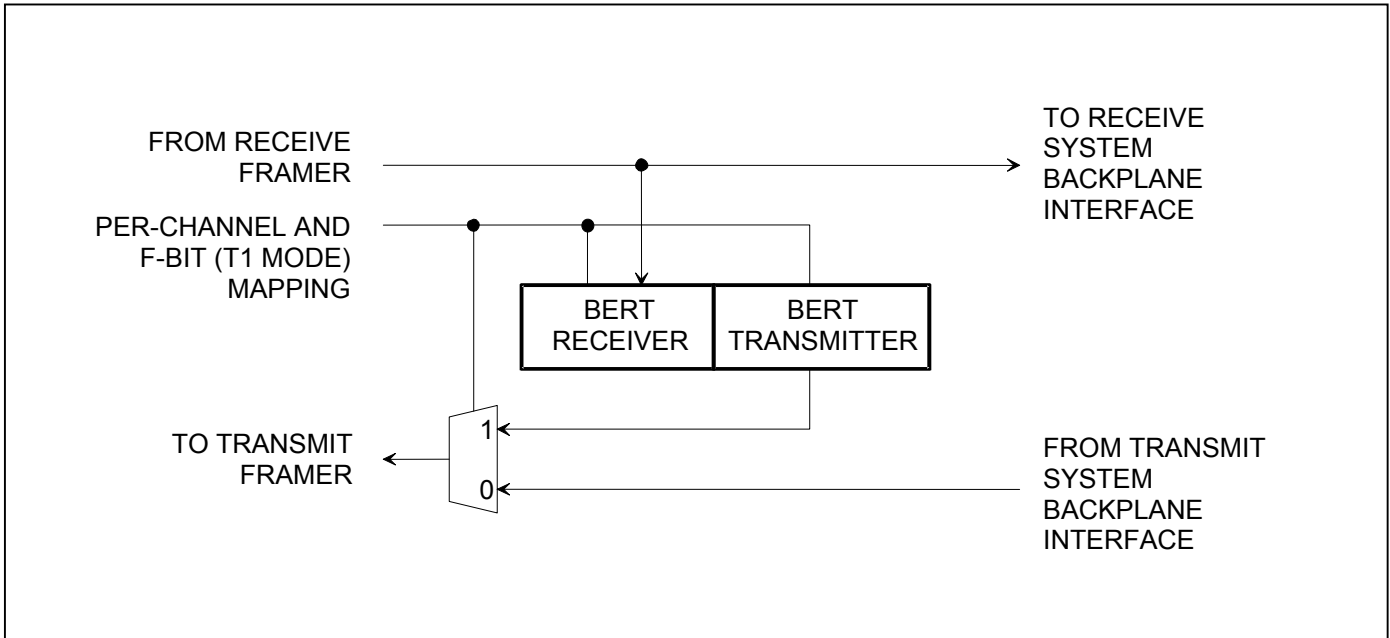
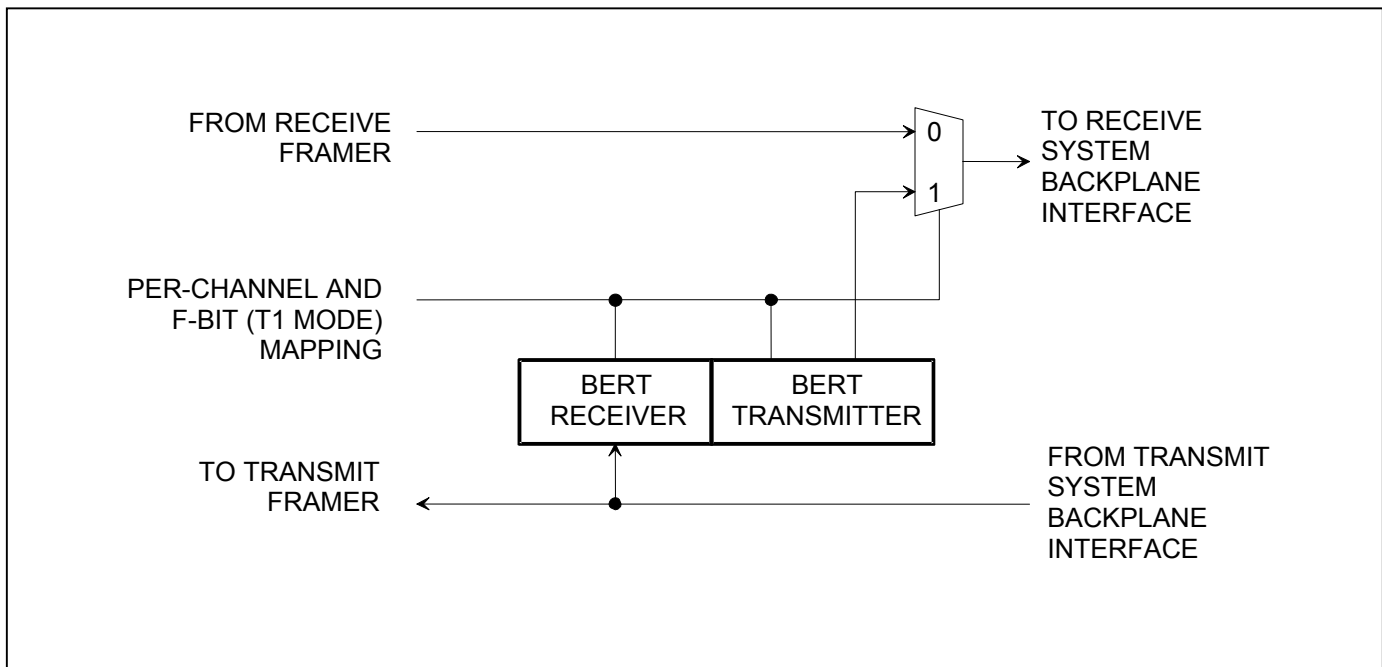


Figure 10-17. Simplified Diagram of BERT in Backplane Direction



10.25.3 BERT Repetitive Pattern Set

These registers must be properly loaded for the BERT to generate and synchronize to a repetitive pattern, a pseudorandom pattern, alternating word pattern, or a Daly pattern. For a repetitive pattern that is fewer than 32 bits, the pattern should be repeated so that all 32 bits are used to describe the pattern. For example, if the pattern was the repeating 5-bit pattern ...01101... (where the rightmost bit is the one sent first and received first), then TR.BRP1 should be loaded with ADh, TR.BRP2 with B5h, TR.BRP3 with D6h, and TR.BRP4 with 5Ah. For a pseudorandom pattern, all four registers should be loaded with all 1s (i.e., FFh). For an alternating word pattern, one word should be placed into TR.BRP1 and TR.BRP2 and the other word should be placed into TR.BRP3 and TR.BRP4. For example, if the DDS stress pattern "7E" is to be described, the user would place 00h in TR.BRP1, 00h in TR.BRP2, 7Eh in TR.BRP3, and 7Eh in TR.BRP4 and the alternating word counter would be set to 50 (decimal) to allow 100 bytes of 00h followed by 100 bytes of 7Eh to be sent and received.

10.25.4 BERT Bit Counter

The BERT Bit Counter is comprised of TR.BBC1, TR.BBC2, TR.BBC3, and TR.BBC4. Once BERT has achieved synchronization, this 32-bit counter increments for each data bit (i.e., clock) received. Toggling the LC control bit in TR.BC1 can clear this counter. This counter saturates when full and sets the BBCO status bit.

10.25.5 BERT Error Counter

The BERT Error Counter is comprised of TR.BEC1, TR.BEC2, and TR.BEC3. Once BERT has achieved synchronization, this 24-bit counter increments for each data bit received in error. Toggling the LC control bit in TR.BC1 can clear this counter. This counter saturates when full and sets the BECO status bit.

10.25.6 BERT Alternating Word-Count Rate

When the BERT is programmed in the alternating word mode, each word repeats for the count loaded into TR.BAWC. One word should be placed into TR.BRP1 and TR.BRP2 and the other word should be placed into TR.BRP3 and TR.BRP4.

10.26 Payload Error-Insertion Function (T1 Mode Only)

An error-insertion function is available in the transceiver and is used to create errors in the payload portion of the T1 frame in the transmit path. This function is only available in T1 mode. Errors can be inserted over the entire frame or the user can select which channels are to be corrupted. Errors are created by inverting the last bit in the count sequence. For example, if the error rate 1 in 16 is selected, the 16th bit is inverted. F-bits are excluded from the count and are never corrupted. Error rate changes occur on frame boundaries. Error-insertion options include continuous and absolute number with both options supporting selectable insertion rates.

Table 10-14. Transmit Error-Insertion Setup Sequence

| STEP | ACTION |
|----------------|--|
| 1 | Enter desired error rate in the TR.ERC register. Note: If TR.ER3 through TR.ER0 = 0, no errors are generated even if the constant error-insertion feature is enabled. |
| 2A or 2B | For constant error insertion, set CE = 1 (TR.ERC.4). For a defined number of errors: <ul style="list-style-type: none"> – Set CE = 0 (TR.ERC.4) – Load TR.NOE1 and TR.NOE2 with the number of errors to be inserted – Toggle WNOE (TR.ERC.7) from 0 to 1 to begin error insertion |

10.26.1 Number-of-Errors Registers

The number-of-error registers determine how many errors are generated. Up to 1023 errors can be generated. The host loads the number of errors to be generated into the TR.NOE1 and TR.NOE2 registers. The host can also update the number of errors to be created by first loading the prescribed value into the TR.NOE registers and then toggling the WNOE bit in the error-rate control registers.

Table 10-15 Error Insertion Examples

| VALUE | WRITE | READ |
|-------|--------------------------|---------------------------------|
| 000h | Do not create any errors | No errors left to be inserted |
| 001h | Create a single error | One error left to be inserted |
| 002h | Create two errors | Two errors left to be inserted |
| 3FFh | Create 1023 errors | 1023 errors left to be inserted |

10.26.2 Number of Errors Left Register

The host can read the NOELx registers at any time to determine how many errors are left to be inserted.

11 INTERLEAVED PCM BUS OPERATION

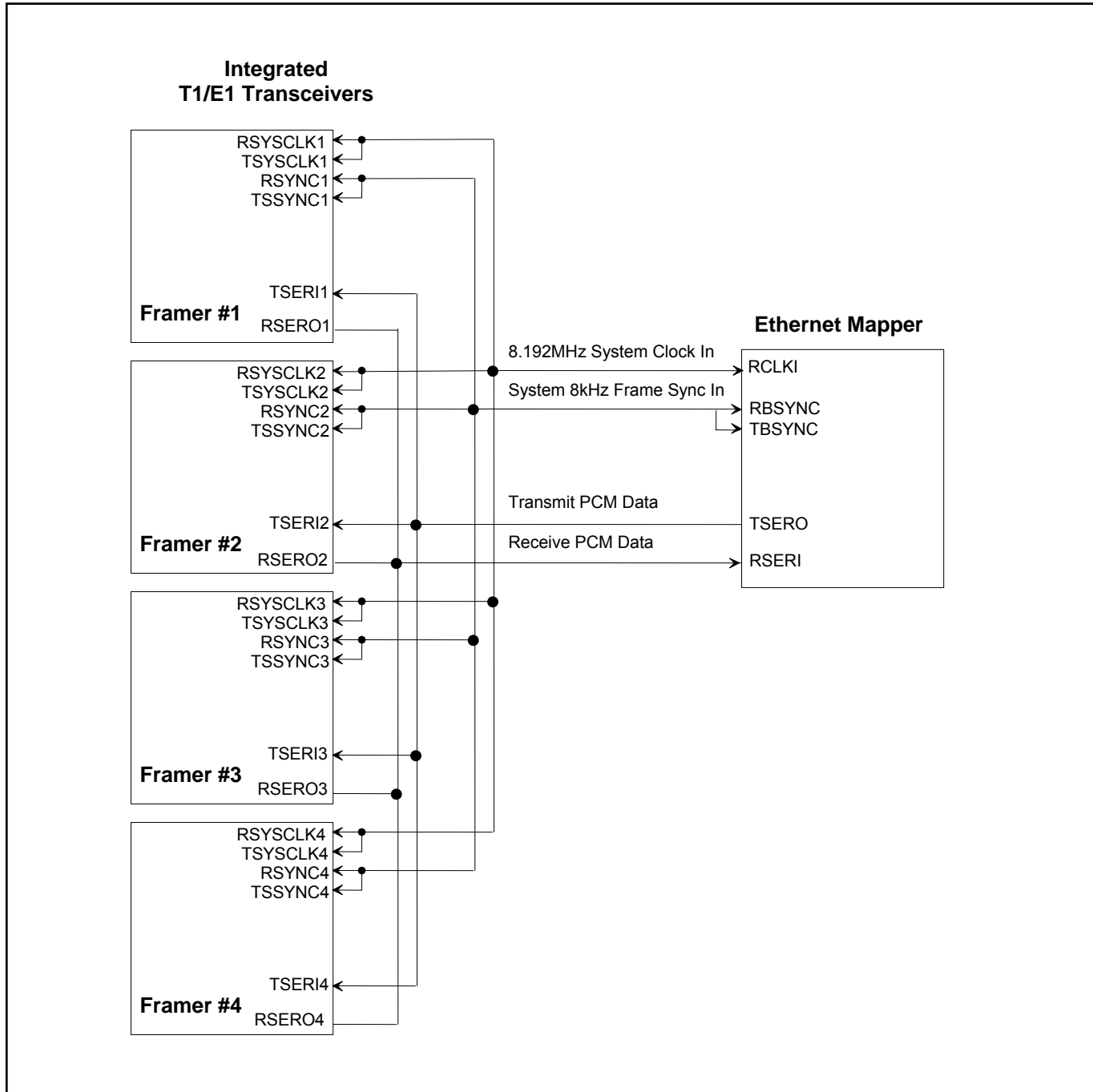
In many architectures, the PCM outputs of individual framers are combined into higher speed PCM buses to simplify transport across the system backplane. The transceiver can be configured to allow PCM data to be multiplexed into higher speed buses eliminating external hardware, saving board space and cost.

The 8.192MHz interleaved PCM bus option (IBO) allows four PCM data streams to share a common bus. See [Figure 11-1](#) for an example of four transceivers sharing a common 8.192MHz PCM bus. The receive elastic stores of each transceiver must be enabled. Via the IBO register the user can configure each transceiver for a specific bus position. For all IBO bus configurations each transceiver is assigned an exclusive position in the high-speed PCM bus. The 8kHz frame sync can be generated from the system backplane or from the first device on the bus. All other devices on the bus must have their frame syncs configured as inputs. Relative to this common frame sync, the devices will await their turn to drive or sample the bus according to the settings of the DA0, DA1, and DA2 bits of the TR.IBOC register.

11.1 Channel Interleave Mode

In channel interleave mode, data is output to the PCM data-out bus one channel at a time from each of the connected devices until all channels of frame n from each device has been placed on the bus. This mode can be used even when the transceivers are operating asynchronous to each other. The elastic stores will manage slip conditions.

Figure 11-1. IBO Interconnection Example



11.2 Programmable Backplane Clock Synthesizer

The transceiver contains an on-chip clock synthesizer that generates a user-selectable clock output on the BPCLK pin, referenced to the recovered receive clock (RCLKn). The synthesizer uses a phase-locked loop to generate low-jitter clocks. Common applications include generation of port and backplane system clocks. The TR.CCR2 register is used to enable (TR.CCR2.0) and select (TR.CCR2.1 and TR.CCR2.2) the clock frequency of the BPCLK pin.

11.3 Fractional T1/E1 Support

Fractional T1/E1 communication is supported on T1/E1 transceivers not being actively used for the transfer of packet data. **The user should take care to fill all unused timeslots on the RSER1 pin with all 1s.**

The T1/E1/J1 transceiver can be programmed to output gapped clocks for selected channels in the receive and transmit paths to simplify connections into a USART or LAPD controller in fractional T1/E1 or ISDN-PRI applications. The receive and transmit paths have independent enables. Channel formats supported include 56kbps and 64kbps. This is accomplished by assigning an alternate function to the RCHCLK and TCHCLK pins. Setting TR.CCR3.0 = 1 causes the RCHCLK pin to output a gapped clock as defined by the receive fractional T1/E1 function of the TR.PCPR register. Setting TR.CCR3.2 = 1 causes the TCHCLK pin to output a gapped clock as defined by the transmit fractional T1/E1 function of the TR.PCPR register. TR.CCR3.1 and TR.CCR3.3 can be used to select between 64kbps and 56kbps operation. See Section [10.2](#) for details about programming the per-channel function. In T1 mode no clock is generated at the F-bit position.

When 56kbps mode is selected, the LSB clock in the channel is omitted. Only the seven most significant bits of the channel have clocks.

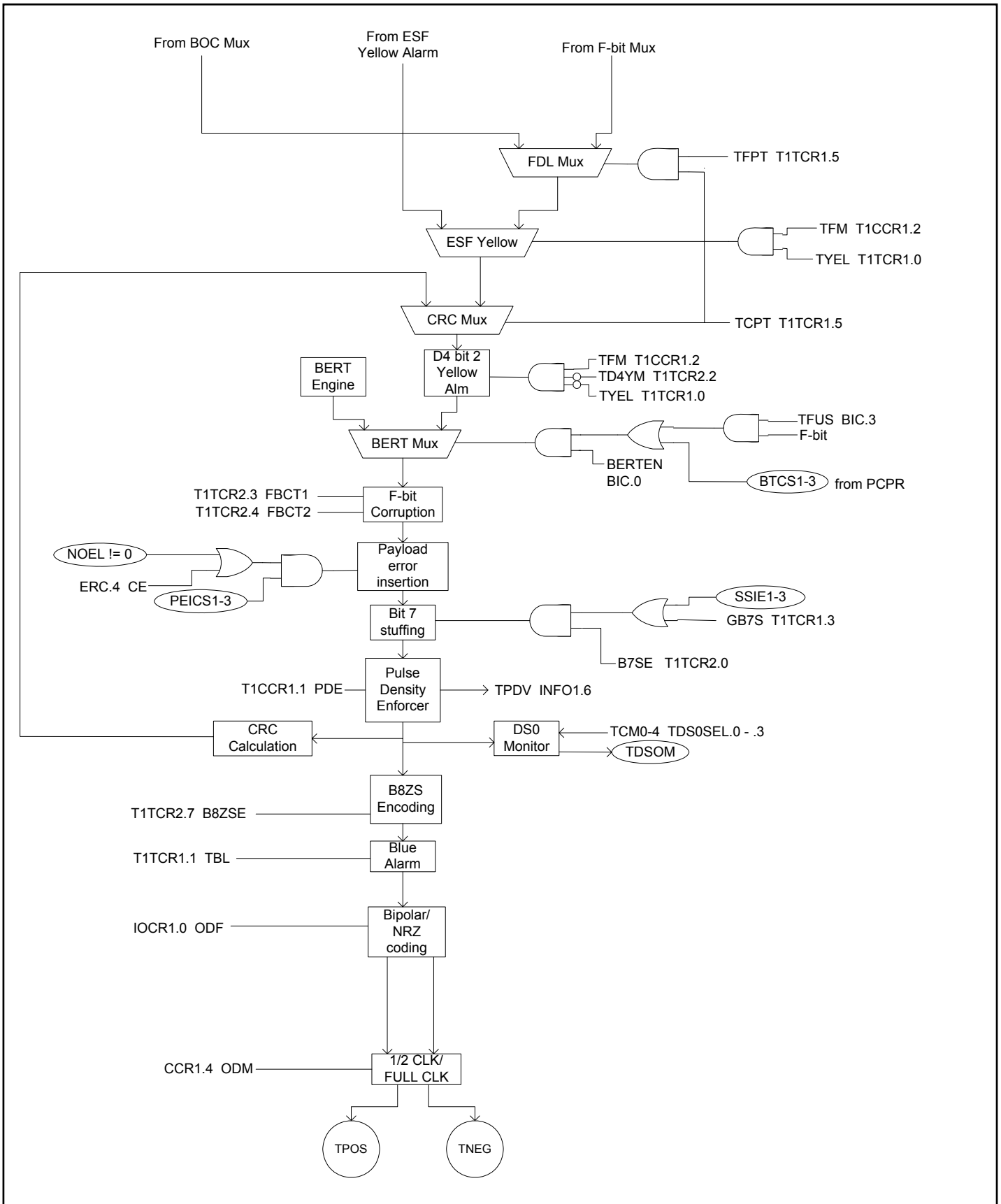
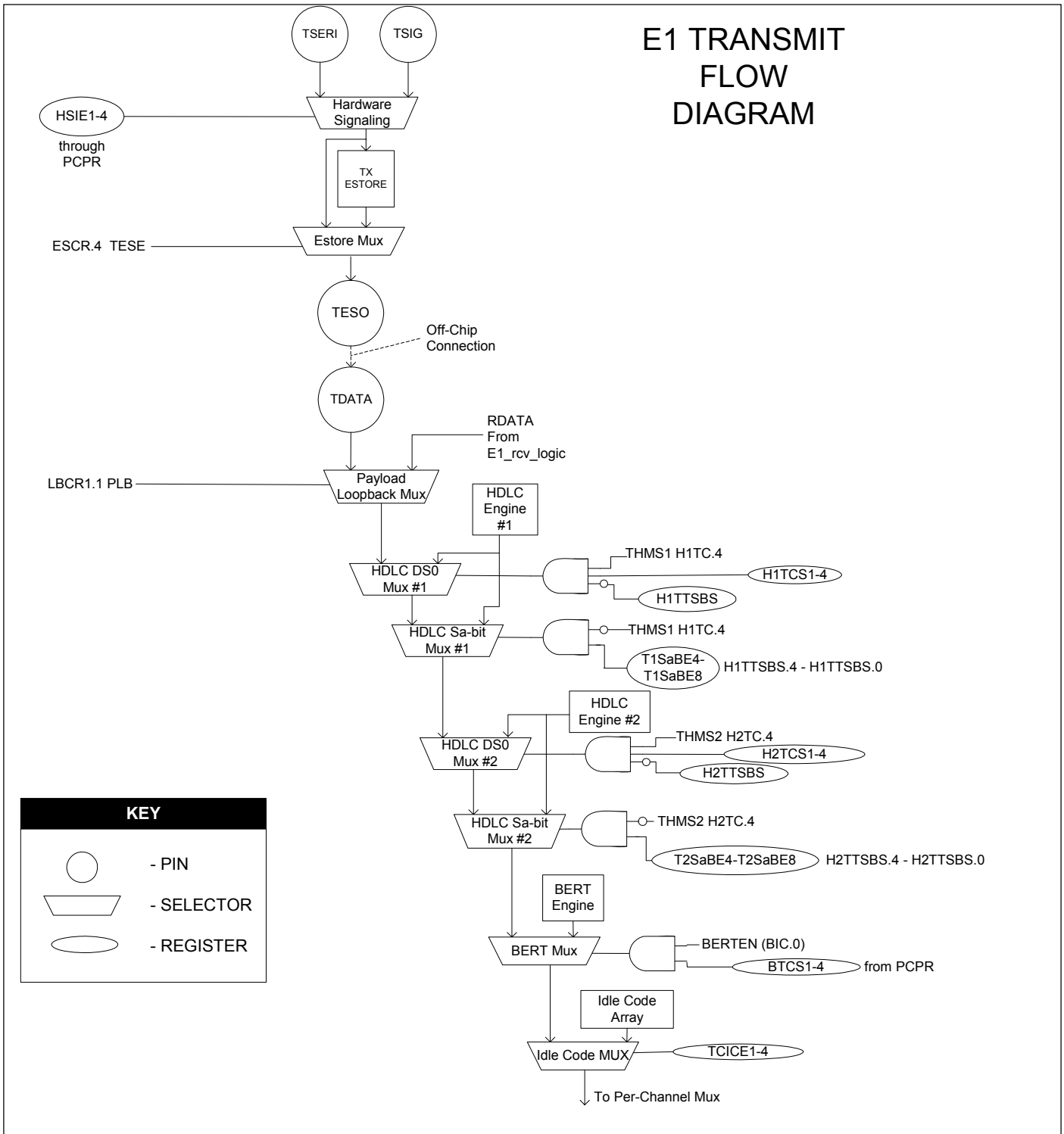
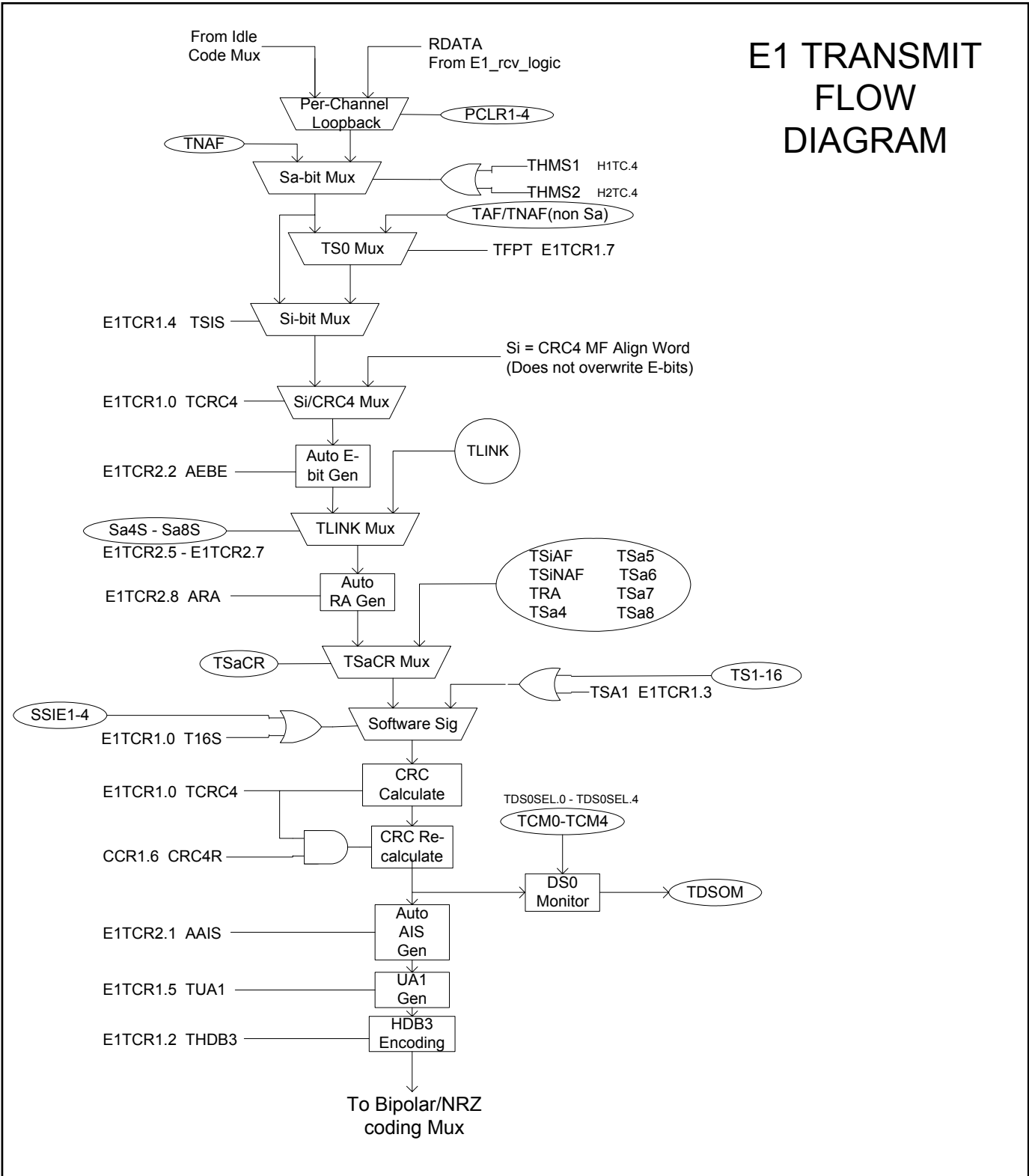


Figure 11-3. E1 Transmit Flow Diagram



E1 TRANSMIT FLOW DIAGRAM



12 DEVICE REGISTERS

Ten address lines are used to address the register space. The register Map for the device is shown in [Table 12-1](#). The addressable range for the device is 0000h to 08FFh. Each Register Section is 64 bytes deep. Global Registers are preserved for software compatibility with multiport devices. The Serial Interface (Line) Registers are used to configure the serial port and the associated transport protocol. The Ethernet Interface (Subscriber) registers are used to control and observe the Ethernet port. The registers associated with the MAC must be configured through indirect register write /read access due to the architecture of the device.

When writing to a register input values for unused bits and registers (those designated with “–”) should be zero unless specifically noted otherwise, as these bits and registers are reserved. When a register is read from, the values of the unused bits and registers should be ignored. A latched status bit is set when an event happens and is cleared when read.

The register details are provided in the following tables.

Table 12-1. Register Address Map

| MAPPER/ PORT | CHIP SELECT | GLOBAL REGISTERS | ARBITER | BERT | SERIAL INTERFACE | ETHERNET INTERFACE | T1/E1/J1 TRANSCEIVERS |
|----------------------|---|---------------------|-----------------|---------------|---------------------|-----------------------|--------------------------|
| Ethernet Mapper | $\overline{CS}=0$, $\overline{CST}=1$ | 0000h– 003Fh | 0040h– 007Fh | | | | |
| Ethernet Mapper | $\overline{CS}=0$, $\overline{CST}=1$ | | | | 00C0h– 013Fh | 0140h– 017Fh | |
| T1/E1/J1 Port 1 * | $\overline{CS}=1$, $\overline{CST}=0$ | | | 0DBh– 0EFh | | | 000h–0FFh |
| T1/E1/J1 Port 2 | $\overline{CS}=1$, $\overline{CST}=0$ | | | 1DBh– 1EFh | | | 100h–1FFh |
| T1/E1/J1 Port 3 | $\overline{CS}=1$, $\overline{CST}=0$ | | | 2DBh– 2EFh | | | 200h–2FFh |
| T1/E1/J1 Port 4 | $\overline{CS}=1$, $\overline{CST}=0$ | | | 3DBh– 3EFh | | | 300h–3FFh |

12.1 Register Bit Maps

Table 12-2, Table 12-3, Table 12-3, Table 12-4, Table 12-5, and Table 12-6 contain the registers of the device. Bits that are reserved are noted with a single dash “—”. All registers not listed are reserved and should be initialized with a value of 00h for proper operation, unless otherwise noted.

12.1.1 Global Register Bit Map

Table 12-2. Global Ethernet Mapper Register Bit Map

| ADDR | Name | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|---------------------------|------------|------------|------------|------------|------------|------------|------------|------------|
| 000h | GL.IDRL | ID07 | ID06 | ID05 | ID04 | ID03 | ID02 | ID01 | ID00 |
| 001h | GL.IDRH | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | ID09 | ID08 |
| 002h | GL.CR1 | — | — | — | — | — | REF_CLKO | INTM | RST |
| 003h | Reserved | — | — | — | — | — | — | — | — |
| 004h | GL.RTCAL | — | — | — | RLCALS1 | — | — | — | TLCALS1 |
| 005h | GL.SRCALS | — | — | — | — | — | — | REFCLKS | SYSCLS |
| 006h | GL.LIE | — | — | — | LIN1TIE | — | — | — | LIN1RIE |
| 007h | GL.LIS | — | — | — | LIN1TIS | — | — | — | LIN1RIS |
| 008h | GL.SIE | — | — | — | — | — | — | — | SUB1IE |
| 009h | GL.SIS | — | — | — | — | — | — | — | SUB1IS |
| 00Ah | GL.TRQIE | — | — | — | TQ1IE | — | — | — | RQ1IE |
| 00Bh | GL.TRQIS | — | — | — | TQ1IS | — | — | — | RQ1IS |
| 00Ch | GL.IBIE | — | — | — | — | — | — | IMUXIE | BIE |
| 00Dh | GL.IBIS | — | — | — | — | — | — | IIS | BIS |
| 00Eh | GL.CON1 | — | — | — | — | — | — | — | LINE1[0] |
| 012h | GL.C1QPR | — | — | — | — | C1MRPR | C1HWPR | C1MHRP | C1HRPR |
| 016h | GL.IMXCN | — | T1E1 | RXE | SENDE | L4 | L3 | L2 | L1 |
| 017h | GL.IMXC | IMXC7 | IMXC6 | IMXC5 | IMXC4 | IMXC3 | IMXC2 | IMXC1 | IMXC0 |
| 018h | GL.IMXSS | ITSYNC4 | ITSYNC3 | ITSYNC2 | ITSYNC1 | IRSYNC4 | IRSYNC3 | IRSYNC2 | IRSYNC1 |
| 019h | GL.IMXSIE | ITSYNCLIE4 | ITSYNCLIE3 | ITSYNCLIE2 | ITSYNCLIE1 | IRSYNCLIE4 | IRSYNCLIE3 | IRSYNCLIE2 | IRSYNCLIE1 |
| 01Ah | GL.IMXSLS | ITSYNCLSL4 | ITSYNCLSL3 | ITSYNCLSL2 | ITSYNCLSL1 | IRSYNCLSL4 | IRSYNCLSL3 | IRSYNCLSL2 | IRSYNCLSL1 |
| 01Bh | GL.IMXDFD | IMUXDFD7 | IMUXDFD6 | IMUXDFD5 | IMUXDFD4 | IMUXDFD3 | IMUXDFD2 | IMUXDFD1 | IMUXDFD0 |
| 01Ch | GL.IMXDIEIE | — | — | — | — | — | — | — | IDDEIE0 |
| 01Dh | GL.IMXDIEELS | — | — | — | — | — | — | — | IDDEELS0 |
| 01Eh | GL.IMXOOFIE | TOOFIE4 | TOOFIE3 | TOOFIE2 | TOOFIE1 | ROOFIE4 | ROOFIE3 | ROOFIE2 | ROOFIE1 |
| 01Fh | GL.IMXOOFSL | TOOFLS4 | TOOFLS3 | TOOFLS2 | TOOFLS1 | ROOFL4 | ROOFL3 | ROOFLS2 | ROOFLS1 |
| 020h | GL.BISTEN | — | — | — | — | — | — | — | BISTE |
| 021h | GL.BISTPF | — | — | — | — | — | — | BISTDN | BISTPF |
| 038h | GL.LSMRRFD | — | — | FD1 | FD0 | LSMRC3 | LSMRC2 | LSMRC1 | LSMRC0 |
| 03Ah | GL.SDMODE1 | — | — | — | — | WT | BL2 | BL1 | BL0 |
| 03Bh | GL.SDMODE2 | — | — | — | — | — | LTMOD2 | LTMOD1 | LTMOD0 |
| 03Ch | GL.SDMODEWS | — | — | — | — | — | — | — | SDMW |
| 03Dh | GL.SDRFTC | SREFT7 | SREFT6 | SREFT5 | SREFT4 | SREFT3 | SREFT2 | SREFT1 | SREFT0 |

Note: All unlisted registers in the range of 000h–03Fh are reserved.

12.1.2 Arbiter Register Bit Map

Table 12-3. Arbiter Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|--------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| 040h | AR.RQSC1 | RQSC1[7] | RQSC1[6] | RQSC1[5] | RQSC1[4] | RQSC1[3] | RQSC1[2] | RQSC1[1] | RQSC1[0] |
| 041h | AR.TQSC1 | TQSC1[7] | TQSC1[6] | TQSC1[5] | TQSC1[4] | TQSC1[3] | TQSC1[2] | TQSC1[1] | TQSC1[0] |

12.1.3 Serial Interface Register Bit Map

Table 12-4. Serial Interface Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|-------------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| 0C0h | Reserved | — | — | — | — | — | — | — | — |
| 0C1h | LI.RSTPD | — | — | — | — | — | — | RESET | — |
| 0C2h | LI.LPBK | — | — | — | — | — | — | — | QLP |
| 0C3h | Reserved | — | — | — | — | — | — | — | — |
| 0C4h | LI.TPPCL | — | — | TFAD | TF16 | TIFV | TSD | TBRE | — |
| 0C5h | LI.TIFGC | TIFG7 | TIFG6 | TIFG5 | TIFG4 | TIFG3 | TIFG2 | TIFG1 | TIFG0 |
| 0C6h | LI.TEPLC | TPEN7 | TPEN6 | TPEN5 | TPEN4 | TPEN3 | TPEN2 | TPEN1 | TPEN0 |
| 0C7h | LI.TEPHC | MEIMS | TPER6 | TPER5 | TPER4 | TPER3 | TPER2 | TPER1 | TPER0 |
| 0C8h | LI.TPPSR | — | — | — | — | — | — | — | <u>TEPE</u> |
| 0C9h | LI.TPPSRL | — | — | — | — | — | — | — | <u>TEPFL</u> |
| 0CAh | LI.TPPSRIE | — | — | — | — | — | — | — | TEPFIE |
| 0CBh | Reserved | — | — | — | — | — | — | — | — |
| 0CCh | LI.TPCR0 | <u>TPC7</u> | <u>TPC6</u> | <u>TPC5</u> | <u>TPC4</u> | <u>TPC3</u> | <u>TPC2</u> | <u>TPC1</u> | <u>TPC0</u> |
| 0CDh | LI.TPCR1 | <u>TPC15</u> | <u>TPC14</u> | <u>TPC13</u> | <u>TPC12</u> | <u>TPC11</u> | <u>TPC10</u> | <u>TPC9</u> | <u>TPC8</u> |
| 0CEh | LI.TPCR2 | <u>TPC23</u> | <u>TPC22</u> | <u>TPC21</u> | <u>TPC20</u> | <u>TPC19</u> | <u>TPC18</u> | <u>TPC17</u> | <u>TPC16</u> |
| 0CFh | Reserved | — | — | — | — | — | — | — | — |
| 0D0h | LI.TBCR0 | <u>TBC7</u> | <u>TBC6</u> | <u>TBC5</u> | <u>TBC4</u> | <u>TBC3</u> | <u>TBC2</u> | <u>TBC1</u> | <u>TBC0</u> |
| 0D1h | LI.TBCR1 | <u>TBC15</u> | <u>TBC14</u> | <u>TBC13</u> | <u>TBC12</u> | <u>TBC11</u> | <u>TBC10</u> | <u>TBC9</u> | <u>TBC8</u> |
| 0D2h | LI.TBCR2 | <u>TBC23</u> | <u>TBC22</u> | <u>TBC21</u> | <u>TBC20</u> | <u>TBC19</u> | <u>TBC18</u> | <u>TBC17</u> | <u>TBC16</u> |
| 0D3h | LI.TBCR3 | <u>TBC31</u> | <u>TBC30</u> | <u>TBC29</u> | <u>TBC28</u> | <u>TBC27</u> | <u>TBC26</u> | <u>TBC25</u> | <u>TBC24</u> |
| 0D4h | LI.TMEI | — | — | — | — | — | — | — | TMEI |
| 0D5h | Reserved | — | — | — | — | — | — | — | — |
| 0D6h | LI.THPMUU | — | — | — | — | — | — | — | TPMUU |
| 0D7h | LI.THPMUS | — | — | — | — | — | — | — | TPMUS |
| 0D8h | LI.TX86EDE | — | — | — | — | — | — | — | X86ED |
| 0D9h | LI.TRX86A | X86TRA7 | X86TRA6 | X86TRA5 | X86TRA4 | X86TRA3 | X86TRA2 | X86TRA1 | X86TRA0 |
| 0DAh | LI.TRX8C | X86TRC7 | X86TRC6 | X86TRC5 | X86TRC4 | X86TRC3 | X86TRC2 | X86TRC1 | X86TRC0 |
| 0DBh | LI.TRX86SAPIH | TRSAPIH7 | TRSAPIH6 | TRSAPIH5 | TRSAPIH4 | TRSAPIH3 | TRSAPIH2 | TRSAPIH1 | TRSAPIH0 |
| 0DCh | LI.TRX86SAPIL | TRSAPIL7 | TRSAPIL6 | TRSAPIL5 | TRSAPIL4 | TRSAPIL3 | TRSAPIL2 | TRSAPIL1 | TRSAPIL0 |
| 0DDh | LI.CIR | CIRE | CIR6 | CIR5 | CIR4 | CIR3 | CIR2 | CIR1 | CIR0 |
| 100h | Reserved | — | — | — | — | — | — | — | — |
| 101h | LI.RPPCL | — | — | RFPD | RF16 | RFED | RDD | RBRE | RCCE |
| 102h | LI.RMPSC | RMX7 | RMX6 | RMX5 | RMX4 | RMX3 | RMX2 | RMX1 | RMX0 |
| 103h | LI.RMPSCH | RMX15 | RMX14 | RMX13 | RMX12 | RMX11 | RMX10 | RMX9 | RMX8 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|-----------------------------|--------|--------|--------|--------|------------|------------|---------|--------|
| 104h | LI.RPPSR | — | — | — | — | — | REPC | RAPC | RSPC |
| 105h | LI.RPPSRL | REPL | RAPL | RIPDL | RSPDL | RLPDL | REPC_L | RAPC_L | RSPC_L |
| 106h | LI.RPPSRIE | REPIE | RAPIE | RIPDIE | RSPDIE | RLPDIE | REPCIE | RAPCIE | RSPCIE |
| 107h | Reserved | — | — | — | — | — | — | — | — |
| 108h | LI.RPCB0 | RPC7 | RPC6 | RPC5 | RPC4 | RPC3 | RPC2 | RPC1 | RPC0 |
| 109h | LI.RPCB1 | RPC15 | RPC14 | RPC13 | RPC12 | RPC11 | RPC10 | RPC09 | RPC08 |
| 10Ah | LI.RPCB2 | RPC23 | RPC22 | RPC21 | RPC20 | RPC19 | RPC18 | RPC17 | RPC16 |
| 10Ch | LI.RFPCB0 | RFPC7 | RFPC6 | RFPC5 | RFPC4 | RFPC3 | RFPC2 | RFPC1 | RFPC0 |
| 10Dh | LI.RFPCB1 | RFPC15 | RFPC14 | RFPC13 | RFPC12 | RFPC11 | RFPC10 | RFPC9 | RFPC8 |
| 10Eh | LI.RFPCB2 | RFPC23 | RFPC22 | RFPC21 | RFPC20 | RFPC19 | RFPC18 | RFPC17 | RFPC16 |
| 10Fh | Reserved | — | — | — | — | — | — | — | — |
| 110h | LI.RAPCB0 | RAPC7 | RAPC6 | RAPC5 | RAPC4 | RAPC3 | RAPC2 | RAPC1 | RAPC0 |
| 111h | LI.RAPCB1 | RAPC15 | RAPC14 | RAPC13 | RAPC12 | RAPC11 | RAPC10 | RAPC9 | RAPC8 |
| 112h | LI.RAPCB2 | RAPC23 | RAPC22 | RAPC21 | RAPC20 | RAPC19 | RAPC18 | RAPC17 | RAPC16 |
| 113h | Reserved | — | — | — | — | — | — | — | — |
| 114h | LI.RSPCB0 | RSPC7 | RSPC6 | RSPC5 | RSPC4 | RSPC3 | RSPC2 | RSPC1 | RSPC0 |
| 115h | LI.RSPCB1 | RSPC15 | RSPC14 | RSPC13 | RSPC12 | RSPC11 | RSPC10 | RSPC9 | RSPC8 |
| 116h | LI.RSPCB2 | RSPC23 | RSPC22 | RSPC21 | RSPC20 | RSPC19 | RSPC18 | RSPC17 | RSPC16 |
| 118h | LI.RBC0 | RBC7 | RBC6 | RBC5 | RBC4 | RBC3 | RBC2 | RBC1 | RBC0 |
| 119h | LI.RBC1 | RBC15 | RBC14 | RBC13 | RBC12 | RBC11 | RBC10 | RBC9 | RBC8 |
| 11Ah | LI.RBC2 | RBC23 | RBC22 | RBC21 | RBC20 | RBC19 | RBC18 | RBC17 | RBC16 |
| 11Bh | LI.RBC3 | RBC31 | RBC30 | RBC29 | RBC28 | RBC27 | RBC26 | RBC25 | RBC24 |
| 11Ch | LI.RAC0 | REBC7 | REBC6 | REBC5 | REBC4 | REBC3 | REBC2 | REBC1 | REBC0 |
| 11Dh | LI.RAC1 | REBC15 | REBC14 | REBC13 | REBC12 | REBC11 | REBC10 | REBC9 | REBC8 |
| 11Eh | LI.RAC2 | REBC23 | REBC22 | REBC21 | REBC20 | REBC19 | REBC18 | REBC17 | REBC16 |
| 11Fh | LI.RAC3 | REBC31 | REBC30 | REBC29 | REBC28 | REBC27 | REBC26 | REBC25 | REBC24 |
| 120h | LI.RHPMUU | — | — | — | — | — | — | — | RPMUU |
| 121h | LI.RHPMUS | — | — | — | — | — | — | — | RPMUUS |
| 122h | LI.RX86S | — | — | — | — | SAPIHNE | SAPILNE | CNE | ANE |
| 123h | LI.RX86LSIE | — | — | — | — | SAPINE01IM | SAPINEFEIM | CNE3LIM | ANE4IM |
| 124h | LI.TQLT | TQLT7 | TQLT6 | TQLT5 | TQLT4 | TQLT3 | TQLT2 | TQLT1 | TQLT0 |
| 125h | LI.TQHT | TQHT7 | TQHT6 | TQHT5 | TQHT4 | TQHT3 | TQHT2 | TQHT1 | TQHT0 |
| 126h | LI.TQTIE | — | — | — | — | TFOVFIE | TQOVFIE | TQHTIE | TQLTIE |
| 127h | LI.TQCTLS | — | — | — | — | TFOVFLS | TQOVFLS | TQHTLS | TQLTLS |

Note: 0DEh–0FFh, 128h–13Fh are reserved.

12.1.4 Ethernet Interface Register Bit Map

Table 12-5. Ethernet Interface Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|----------------------------|----------|----------|----------|---------|---------|---------|---------|---------|
| 140h | SU.MACRADL | MACRA7 | MACRA6 | MACRA5 | MACRA4 | MACRA3 | MACRA2 | MACRA1 | MACRA0 |
| 141h | SU.MACRADH | MACRA15 | MACRA14 | MACRA13 | MACRA12 | MACRA11 | MACRA10 | MACRA09 | MACRA08 |
| 142h | SU.MACRD0 | MACRD7 | MACRD6 | MACRD5 | MACRD4 | MACRD3 | MACRD2 | MACRD1 | MACRD0 |
| 143h | SU.MACRD1 | MACRD15 | MACRD14 | MACRD13 | MACRD12 | MACRD11 | MACRD10 | MACRD9 | MACRD8 |
| 144h | SU.MACRD2 | MACRD23 | MACRD22 | MACRD21 | MACRD20 | MACRD19 | MACRD18 | MACRD17 | MACRD16 |
| 145h | SU.MACRD3 | MACRD31 | MACRD30 | MACRD29 | MACRD28 | MACRD27 | MACRD26 | MACRD25 | MACRD24 |
| 146h | SU.MACWD0 | MACWD7 | MACWD6 | MACWD5 | MACWD4 | MACWD3 | MACWD2 | MACWD1 | MACWD0 |
| 147h | SU.MACWD1 | MACWD15 | MACWD14 | MACWD13 | MACWD12 | MACWD11 | MACWD10 | MACWD09 | MACWD08 |
| 148h | SU.MACWD2 | MACWD23 | MACWD22 | MACWD21 | MACWD20 | MACWD19 | MACWD18 | MACWD17 | MACWD16 |
| 149h | SU.MACWD3 | MACD31 | MACD30 | MACD29 | MACD28 | MACD27 | MACD26 | MACD25 | MACD24 |
| 14Ah | SU.MACAWL | MACAW 7 | MACAW 6 | MACAW 5 | MACAW4 | MACAW3 | MACAW2 | MACAW1 | MACAW0 |
| 14Bh | SU.MACAWH | MACAW 15 | MACAW 14 | MACAW 13 | MACAW12 | MACAW11 | MACAW10 | MACAW9 | MACAW8 |
| 14Ch | SU.MACRWC | — | — | — | — | — | — | MCRW | MCS |
| 14Dh | Reserved | — | — | — | — | — | — | — | — |
| 14Eh | Reserved | — | — | — | — | — | — | — | — |
| 14Fh | SU.LPBK | — | — | — | — | — | — | — | QLP |
| 150h | SU.GCR | — | — | — | — | CRCS | H10S | ATFLOW | JAME |
| 151h | SU.TFRC | — | — | — | — | NCFQ | TPDFCB | TPRHBC | TPRCB |
| 152h | SU.TFSL | UR | EC | LC | ED | LOC | NOC | — | FABORT |
| 153h | SU.TFSH | PR | HBF | CC3 | CC2 | CC1 | CC0 | LCO | DEF |
| 154h | SU.RFSB0 | FL7 | FL6 | FL5 | FL4 | FL3 | FL2 | FL1 | FI0 |
| 155h | SU.RFSB1 | RF | WT | FL13 | FL12 | FL11 | FL10 | FL9 | FI8 |
| 156h | SU.RFSB2 | — | — | CRCE | DB | MIIE | FT | CS | FTL |
| 157h | SU.RFSB3 | MF | — | — | BF | MCF | UF | CF | LE |
| 158h | SU.RMFSRL | RMPS7 | RMPS6 | RMPS5 | RMPS4 | RMPS3 | RMPS2 | RMPS1 | RMPS0 |
| 159h | SU.RMFSRH | RMPS15 | RMPS14 | RMPS13 | RMPS12 | RMPS11 | RMPS10 | RMPS09 | RMPS08 |
| 15Ah | SU.RQLT | RQLT7 | RQLT6 | RQLT5 | RQLT4 | RQLT3 | RQLT2 | RQLT1 | RQLT0 |
| 15Bh | SU.RQHT | RQHT7 | RQHT6 | RQHT5 | RQHT4 | RQHT3 | RQHT2 | RQHT1 | RQHT0 |
| 15Ch | SU.QRIE | — | — | — | — | RFOVFIE | RQVFIE | RQLTIE | RQHTIE |
| 15Dh | SU.QCRLS | — | — | — | — | RFOVFLS | RQOVFLS | RQHTLS | RQLTLS |
| 15Eh | SU.RFRC | — | UCFR | CFRR | LERR | CRCERR | DBR | MIIER | BFR |

Note: 15Fh–17Fh are reserved.

12.1.5 MAC Register Bit Map

Table 12-6. MAC Indirect Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------------------------------------|--------|--------|---------|--------|--------|--------|--------|--------|
| 0000h | SU.MACCR 31:24 | — | — | — | HDB | PS | — | — | — |
| 0001h | 23:16 | DRO | OML1 | OML0 | F | PM | PAM | — | — |
| 0002h | 15:8 | — | — | — | LCC | — | DRTY | — | ASTP |
| 0003h | 7:0 | BOLMT1 | BOLMT0 | DC | — | TE | RE | — | — |
| 0004h | SU.MACAH 31:24 | — | — | — | — | — | — | — | — |
| 0005h | 23:16 | — | — | — | — | — | — | — | — |
| 0006h | 15:8 | PADR47 | PADR46 | PADR45 | PADR44 | PADR43 | PADR42 | PADR41 | PADR40 |
| 0007h | 7:0 | PADR39 | PADR38 | PADR37 | PADR36 | PADR35 | PADR34 | PADR33 | PADR32 |
| 0008h | SU.MACAL 31:24 | PADR31 | PADR30 | PADR29 | PADR28 | PADR27 | PADR26 | PADR25 | PADR24 |
| 0009h | 23:16 | PADR23 | PADR22 | PADR21 | PADR20 | PADR19 | PADR18 | PADR17 | PADR16 |
| 000Ah | 15:8 | PADR15 | PADR14 | PADR13 | PADR12 | PADR11 | PADR10 | PADR09 | PADR08 |
| 000Bh | 7:0 | PADR07 | PADR06 | PADR05 | PADR04 | PADR03 | PADR02 | PADR01 | PADR00 |
| 000Ch | Reserved | — | — | — | — | — | — | — | — |
| 000Dh | Reserved | — | — | — | — | — | — | — | — |
| 000Eh | Reserved | — | — | — | — | — | — | — | — |
| 000Fh | Reserved | — | — | — | — | — | — | — | — |
| 0010h | Reserved | — | — | — | — | — | — | — | — |
| 0011h | Reserved | — | — | — | — | — | — | — | — |
| 0012h | Reserved | — | — | — | — | — | — | — | — |
| 0013h | Reserved | — | — | — | — | — | — | — | — |
| 0014h | SU.MACMIIA 31:24 | — | — | — | — | — | — | — | — |
| 0015h | 23:16 | — | — | — | — | — | — | — | — |
| 0016h | 15:8 | PHYA4 | PHYA3 | PHYA2 | PHYA1 | PHYA0 | MIIA4 | MIIA3 | MIIA2 |
| 0017h | 7:0 | MIIA1 | MIIA0 | — | — | — | — | MIIW | MIIW |
| 0018h | SU.MACMIID 31:24 | — | — | — | — | — | — | — | — |
| 0019h | 23:16 | — | — | — | — | — | — | — | — |
| 001Ah | 15:8 | MIID15 | MIID14 | MIID13 | MIID12 | MIID11 | MIID10 | MIID09 | MIID08 |
| 001Bh | 7:0 | MIID07 | MIID06 | MIID05 | MIID04 | MIID03 | MIID02 | MIID01 | MIID00 |
| 001Ch | SU.MACFCR 31:24 | PT15 | PT14 | PT13 | PT12 | PT11 | PT10 | PT09 | PT08 |
| 001Dh | 23:16 | PT07 | PT06 | PT05 | PT04 | PT03 | PT02 | PT01 | PT00 |
| 001Eh | 15:8 | — | — | — | — | — | — | — | — |
| 001Fh | 7:0 | — | — | — | — | — | PCF | FCE | FCB |
| 100h | SU.MMCCTRL 31:24 | — | — | — | — | — | — | — | — |
| 101h | 23:16 | — | — | — | — | — | — | — | — |
| 102h | 15:8 | — | — | MXFRM10 | MXFRM9 | MXFRM8 | MXFRM7 | MXFRM6 | MXFRM5 |
| 103h | 7:0 | MXFRM4 | MXFRM3 | MXFRM2 | MXFRM1 | MXFRM0 | — | — | — |
| 10Ch | Reserved – initialize to FF | — | — | — | — | — | — | — | — |
| 10Dh | Reserved – initialize to FF | — | — | — | — | — | — | — | — |
| 10Eh | Reserved – initialize to FF | — | — | — | — | — | — | — | — |
| 10Fh | Reserved – initialize to FF | — | — | — | — | — | — | — | — |
| 110h | Reserved – initialize to FF | — | — | — | — | — | — | — | — |

DS33R41 Inverse-Multiplexing Ethernet Mapper with Quad Integrated T1/E1/J1 Transceivers

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|-----------------------------|------------|------------|------------|------------|------------|------------|------------|------------|
| 111h | Reserved – initialize to FF | — | — | — | — | — | — | — | — |
| 112h | Reserved – initialize to FF | — | — | — | — | — | — | — | — |
| 113h | Reserved – initialize to FF | — | — | — | — | — | — | — | — |
| 200h | SU.RxFrmCtr 31:24 | RXFRMC31 | RXFRMC30 | RXFRMC29 | RXFRMC28 | RXFRMC27 | RXFRMC26 | RXFRMC25 | RXFRMC24 |
| 201h | 23:16 | RXFRMC23 | RXFRMC22 | RXFRMC21 | RXFRMC20 | RXFRMC19 | RXFRMC18 | RXFRMC17 | RXFRMC16 |
| 202h | 15:8 | RXFRMC15 | RXFRMC14 | RXFRMC13 | RXFRMC12 | RXFRMC11 | RXFRMC10 | RXFRMC9 | RXFRMC8 |
| 203h | 7:0 | RXFRMC7 | RXFRMC6 | RXFRMC5 | RXFRMC4 | RXFRMC3 | RXFRMC2 | RXFRMC1 | RXFRMC0 |
| 204h | SU.RxFrmOKCtr 31:24 | RXFRMOK31 | RXFRMOK30 | RXFRMOK29 | RXFRMOK28 | RXFRMOK27 | RXFRMOK26 | RXFRMOK25 | RXFRMOK24 |
| 205h | 23:16 | RXFRMOK23 | RXFRMOK22 | RXFRMOK21 | RXFRMOK20 | RXFRMOK19 | RXFRMOK18 | RXFRMOK17 | RXFRMOK16 |
| 206h | 15:8 | RXFRMOK15 | RXFRMOK14 | RXFRMOK13 | RXFRMOK12 | RXFRMOK11 | RXFRMOK10 | RXFRMOK9 | RXFRMOK8 |
| 207h | 7:0 | RXFRMOK7 | RXFRMOK6 | RXFRMOK5 | RXFRMOK4 | RXFRMOK3 | RXFRMOK2 | RXFRMOK1 | RXFRMOK0 |
| 300h | SU.TxFrmCtr | TXFRMC31 | TXFRMC30 | TXFRMC29 | TXFRMC28 | TXFRMC27 | TXFRMC26 | TXFRMC25 | TXFRMC24 |
| 301h | 23:16 | TXFRMC23 | TXFRMC22 | TXFRMC21 | TXFRMC20 | TXFRMC19 | TXFRMC18 | TXFRMC17 | TXFRMC16 |
| 302h | 15:8 | TXFRMC15 | TXFRMC14 | TXFRMC13 | TXFRMC12 | TXFRMC11 | TXFRMC10 | TXFRMC9 | TXFRMC8 |
| 303h | 7:0 | TXFRMC7 | TXFRMC6 | TXFRMC5 | TXFRMC4 | TXFRMC3 | TXFRMC2 | TXFRMC1 | TXFRMC0 |
| 308h | SU.TxBytesCtr | TXBYTEC31 | TXBYTEC30 | TXBYTEC29 | TXBYTEC28 | TXBYTEC27 | TXBYTEC26 | TXBYTEC25 | TXBYTEC24 |
| 309h | 23:16 | TXBYTEC23 | TXBYTEC22 | TXBYTEC21 | TXBYTEC20 | TXBYTEC19 | TXBYTEC18 | TXBYTEC17 | TXBYTEC16 |
| 30Ah | 15:8 | TXBYTEC15 | TXBYTEC14 | TXBYTEC13 | TXBYTEC12 | TXBYTEC11 | TXBYTEC10 | TXBYTEC9 | TXBYTEC8 |
| 30Bh | 7:0 | TXBYTEC7 | TXBYTEC6 | TXBYTEC5 | TXBYTEC4 | TXBYTEC3 | TXBYTEC2 | TXBYTEC1 | TXBYTEC0 |
| 30Ch | SU.TxBytesOkCtr | TXBYTEOK31 | TXBYTEOK30 | TXBYTEOK29 | TXBYTEOK28 | TXBYTEOK27 | TXBYTEOK26 | TXBYTEOK25 | TXBYTEOK24 |
| 30Dh | 23:16 | TXBYTEOK23 | TXBYTEOK22 | TXBYTEOK21 | TXBYTEOK20 | TXBYTEOK19 | TXBYTEOK18 | TXBYTEOK17 | TXBYTEOK16 |
| 30Eh | 15:8 | TXBYTEOK15 | TXBYTEOK14 | TXBYTEOK13 | TXBYTEOK12 | TXBYTEOK11 | TXBYTEOK10 | TXBYTEOK9 | TXBYTEOK8 |
| 30Fh | 7:0 | TXBYTEOK7 | TXBYTEOK6 | TXBYTEOK5 | TXBYTEOK4 | TXBYTEOK3 | TXBYTEOK2 | TXBYTEOK1 | TXBYTEOK0 |
| 334h | SU.TxFrmUndr | TXFRMU31 | TXFRMU30 | TXFRMU29 | TXFRMU28 | TXFRMU27 | TXFRMU26 | TXFRMU25 | TXFRMU24 |
| 335h | 23:16 | TXFRMU23 | TXFRMU22 | TXFRMU21 | TXFRMU20 | TXFRMU19 | TXFRMU18 | TXFRMU17 | TXFRMU16 |
| 336h | 15:8 | TXFRMU15 | TXFRMU14 | TXFRMU13 | TXFRMU12 | TXFRMU11 | TXFRMU10 | TXFRMU9 | TXFRMU8 |
| 337h | 7:0 | TXFRMU7 | TXFRMU6 | TXFRMU5 | TXFRMU4 | TXFRMU3 | TXFRMU2 | TXFRMU1 | TXFRMU0 |
| 338h | SU.TxBdFrmCtr | TXFRMBD31 | TXFRMBD30 | TXFRMBD29 | TXFRMBD28 | TXFRMBD27 | TXFRMBD26 | TXFRMBD25 | TXFRMBD24 |
| 339h | 23:16 | TXFRMBD23 | TXFRMBD22 | TXFRMBD21 | TXFRMBD20 | TXFRMBD19 | TXFRMBD18 | TXFRMBD17 | TXFRMBD16 |
| 33Ah | 15:8 | TXFRMBD15 | TXFRMBD14 | TXFRMBD13 | TXFRMBD12 | TXFRMBD11 | TXFRMBD10 | TXFRMBD9 | TXFRMBD8 |
| 33Bh | 7:0 | TXFRMBD7 | TXFRMBD6 | TXFRMBD5 | TXFRMBD4 | TXFRMBD3 | TXFRMBD2 | TXFRMBD1 | TXFRMBD0 |

Note that the addresses in the table above are the indirect addresses that must be provided to the [SU.MACAWH](#) and [SU.MACAWL](#). All unused and reserved locations must be initialized to zero for proper operation unless specifically noted otherwise.

12.2 T1/E1/J1 Transceiver Register Bit Map

Table 12-7. T1/E1/J1 Transceiver Register Bit Map (Active when CST = 0)

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|----------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| 0 | TR.MSTRREG | — | — | — | — | TEST1 | TEST0 | T1/E1 | SFTRST |
| 1 | TR.IOCR1 | RSMS | RSMS2 | RSMS1 | RSIO | TSDW | TSM | TSIO | ODF |
| 2 | TR.IOCR2 | RCLKINV | TCLKINV | RSYNCINV | TSYNCINV | TSSYNCINV | H100EN | TSCLKM | RSCLKM |
| 3 | TR.T1RCR1 | — | ARC | OOF1 | OOF2 | SYNCC | SYNCT | SYNCE | RESYNC |
| 4 | TR.T1RCR2 | — | RFM | RB8ZS | RSLC96 | RZSE | — | RJC | RD4YM |
| 5 | TR.T1TCR1 | TJC | TFPT | TCPT | TSSE | GB7S | TFDLS | TBL | TYEL |
| 6 | TR.T1TCR2 | TB8ZS | TSLC96 | TZSE | FBCT2 | FBCT1 | TD4YM | Reserved | TB7ZS |
| 7 | TR.T1CCR1 | MCLKS | CRC4R | SIE | TRAI-CI | TAIS-CI | TFM | PDE | TLOOP |
| 8 | TR.SSIE1-T1 TR.SSIE1-E1 | CH8 CH7 | CH7 CH6 | CH6 CH5 | CH5 CH4 | CH4 CH3 | CH3 CH2 | CH2 CH1 | CH1 UCAW |
| 9 | TR.SSIE2-T1 TR.SSIE2-E1 | CH16 CH15 | CH15 CH14 | CH14 CH13 | CH13 CH12 | CH12 CH11 | CH11 CH10 | CH10 CH9 | CH9 CH8 |
| 0A | TR.SSIE3-T1 TR.SSIE3-E1 | CH24 CH22 | CH23 CH21 | CH22 CH20 | CH21 CH19 | CH20 CH18 | CH19 CH17 | CH18 CH16 | CH17 LCAW |
| 0B | TR.SSIE4 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 |
| 0C | TR.T1RDMR1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0D | TR.T1RDMR2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0E | TR.T1RDMR3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0F | TR.IDR | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| 10 | TR.INFO1 | RPDV | TPDV | COFA | 8ZD | 16ZD | SEFE | B8ZS | FBE |
| 11 | TR.INFO2 | BSYNC | BD | TCLE | TOCD | RL3 | RL2 | RL1 | RL0 |
| 12 | TR.INFO3 | — | — | — | — | — | CRCRC | FASRC | CASRC |
| 13 | Reserved | — | — | — | — | — | — | — | — |
| 14 | TR.IIR1 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 |
| 15 | TR.IIR2 | — | — | — | — | — | — | — | SR9 |
| 16 | TR.SR1 | ILUT | TIMER | RSCOS | JALT | LRCL | TCLE | TOCD | LOLITC |
| 17 | TR.IMR1 | ILUT | TIMER | RSCOS | JALT | LRCL | TCLE | TOCD | LOLITC |
| 18 | TR.SR2 | RYELC | RUA1C | FRCLC | RLOSC | RYEL | RUA1 | FRCL | RLOS |
| 19 | TR.IMR2 | RYELC | RUA1C | FRCLC | RLOSC | RYEL | RUA1 | FRCL | RLOS |
| 1A | TR.SR3 | LSPARE | LDN | LUP | LOTC | LORC | V52LNK | RDMA | RRR |
| 1B | TR.IMR3 | LSPARE | LDN | LUP | LOTC | LORC | V52LNK | RDMA | RRR |
| 1C | TR.SR4 | RAIS-CI | RSA1 | RSA0 | TMF | TAF | RMF | RCMF | RAF |
| 1D | TR.IMR4 | RAIS-CI | RSA1 | RSA0 | TMF | TAF | RMF | RCMF | RAF |
| 1E | TR.SR5 | — | — | TESF | TESEM | TSLIP | RESF | RESEM | RSLIP |
| 1F | TR.IMR5 | — | — | TESF | TESEM | TSLIP | RESF | RESEM | RSLIP |
| 20 | TR.SR6 | — | TMEND | RPE | RPS | RHWM | RNE | TLWM | TNF |
| 21 | TR.IMR6 | — | TMEND | RPE | RPS | RHWM | RNE | TLWM | TNF |
| 22 | TR.SR7 | — | TMEND | RPE | RPS | RHWM | RNE | TLWM | TNF |
| 23 | TR.IMR7 | — | TMEND | RPE | RPS | RHWM | RNE | TLWM | TNF |
| 24 | TR.SR8 | — | — | BOCC | RFDLAD | RFDLF | TFDLE | RMTCH | RBOC |
| 25 | TR.IMR8 | — | — | BOCC | RFDLAD | RFDLF | TFDLE | RMTCH | RBOC |
| 26 | TR.SR9 | — | BBED | BBCO | BEC0 | BRA1 | BRA0 | BRLOS | BSYNC |
| 27 | TR.IMR9 | — | BBED | BBCO | BEC0 | BRA1 | BRA0 | BRLOS | BSYNC |
| 28 | TR.PCPR | RSAOICS | RSRCS | RFCS | BRCS | THSCS | PEICS | TFCS | BTCS |
| 29 | TR.PCDR1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 2A | TR.PCDR2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 2B | TR.PCDR3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 2C | TR.PCDR4 | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 2D | TR.INFO4 | — | — | — | — | H2UDR | H2OBT | H1UDR | H1OBT |
| 2E | TR.INFO5 | — | — | EMPTY | TFULL | EMPTY | PS2 | PS1 | PS0 |
| 2F | TR.INFO6 | — | — | EMPTY | TFULL | EMPTY | PS2 | PS1 | PS0 |
| 30 | TR.INFO7 | CSC5 | CSC4 | CSC3 | CSC2 | CSC0 | FASSA | CASSA | CRC4SA |
| 31 | TR.H1RC | RHR | RHMS | — | — | HDLCD | — | — | RSFD |
| 32 | TR.H2RC | RHR | RHMS | — | — | HDLCD | — | — | RSFD |
| 33 | TR.E1RCR1 | RSERC | RSIGM | RHDB3 | RG802 | RCRC4 | FRC | SYNCE | RESYNC |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|------------|---|----------|----------|----------|----------|--------|--------|--------|
| 34 | TR.E1RCR2 | — | — | — | — | — | — | — | RCLA |
| 35 | TR.E1TCR1 | TFPT | T16S | TUA1 | TSiS | TSA1 | THDB3 | TG802 | TCRC4 |
| 36 | TR.E1TCR2 | Reserved | Reserved | Reserved | Reserved | Reserved | AEBE | AAIS | ARA |
| 37 | TR.BOCC | — | — | — | RBOCE | RBR | RBF1 | RBF0 | SBOC |
| 38 | TR.RSINFO1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 39 | TR.RSINFO2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 3A | TR.RSINFO3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 3B | TR.RSINFO4 | — | — | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 3C | TR.RSCSE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 3D | TR.RSCSE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 3E | TR.RSCSE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 3F | TR.RSCSE4 | — | — | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 40 | TR.SIGCR | GRSRE | — | — | RFE | RFF | RCCS | TCCS | FRSAO |
| 41 | TR.ERCNT | — | MECU | ECUS | EAMS | VCRFS | FSBE | MOSCRF | LCVCRF |
| 42 | TR.LCVC1 | LCVC15 | LCVC14 | LCVC13 | LCVC12 | LCVC11 | LCVC10 | LCVC9 | LCCV8 |
| 43 | TR.LCVC2 | LCVC7 | LCVC6 | LCVC5 | LCVC4 | LCVC3 | LCVC2 | LCVC1 | LCVC0 |
| 44 | TR.PCVC1 | PCVC15 | PCVC14 | PCVC13 | PCVC12 | PCVC11 | PCVC10 | PCVC9 | PCVC8 |
| 45 | TR.PCVC2 | PCVC7 | PCVC6 | PCVC5 | PCVC4 | PCVC3 | PCVC2 | PCVC1 | PCVC0 |
| 46 | TR.FOSCR1 | FOS15 | FOS14 | FOS13 | FOS12 | FOS11 | FOS10 | FOS9 | FOS8 |
| 47 | TR.FOSCR2 | FOS7 | FOS6 | FOS5 | FOS4 | FOS3 | FOS2 | FOS1 | FOS0 |
| 48 | TR.EBCR1 | EB15 | EB14 | EB13 | EB12 | EB11 | EB10 | EB9 | EB8 |
| 49 | TR.EBCR2 | EB7 | EB6 | EB5 | EB4 | EB3 | EB2 | EB1 | EB0 |
| 4A | TR.LBCR | LTS | — | — | Reserved | LLB | RLB | PLB | FLB |
| 4B | TR.PCLR1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 4C | TR.PCLR2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 4D | TR.PCLR3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 4E | TR.PCLR4 | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 4F | TR.ESCR | TESALGN | TESR | TESMDM | TESE | RESALGN | RESR | RESMDM | RESE |
| 50 | TR.TS1 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 51 | TR.TS2 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 52 | TR.TS3 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 53 | TR.TS4 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 54 | TR.TS5 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 55 | TR.TS6 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 56 | TR.TS7 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 57 | TR.TS8 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 58 | TR.TS9 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 59 | TR.TS10 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 5A | TR.TS11 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 5B | TR.TS12 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 5C | TR.TS13 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 5D | TR.TS14 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 5E | TR.TS15 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 5F | TR.TS16 | Transmit Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 60 | TR.RS1 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 61 | TR.RS2 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 62 | TR.RS3 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 63 | TR.RS4 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 64 | TR.RS5 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 65 | TR.RS6 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 66 | TR.RS7 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 67 | TR.RS8 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 68 | TR.RS9 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 69 | TR.RS10 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 6A | TR.RS11 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 6B | TR.RS12 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 6C | TR.RS13 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|------------|--|--------|--------|--------|---------|--------|---------|--------|
| 6D | TR.RS14 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 6E | TR.RS15 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 6F | TR.RS16 | Receive Signaling Bit Format Changes With Operating Mode. See Register Definition. | | | | | | | |
| 70 | TR.CCR1 | — | CRC4R | SIE | ODM | — | TCSS1 | TCSS0 | RLOSF |
| 71 | TR.CCR2 | — | — | — | — | — | BPCS1 | BPCS0 | BPEN |
| 72 | TR.CCR3 | — | — | — | — | TDATFMT | TGPKEN | RDATFMT | RGPKEN |
| 73 | TR.CCR4 | RLT3 | RLT2 | RLT1 | RLT0 | — | — | — | — |
| 74 | TR.TDS0SEL | — | — | — | TCM4 | TCM3 | TCM2 | TCM1 | TCM0 |
| 75 | TR.TDS0M | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| 76 | TR.RDS0SEL | — | — | — | RCM4 | RCM3 | RCM2 | RCM1 | RCM0 |
| 77 | TR.RDS0M | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| 78 | TR.LIC1 | L2 | L1 | L0 | EGL | JAS | JABDS | DJA | TPD |
| 79 | TR.LIC2 | ETS | LIRST | IBPV | TUA1 | JAMUX | — | SCLD | CLDS |
| 7A | TR.LIC3 | — | TCES | RCES | MM1 | MM0 | RSCLKE | TSCLKE | TAOZ |
| 7B | TR.LIC4 | CMIE | CMII | MPS1 | MPS0 | TT1 | TT0 | RT1 | RT0 |
| 7C | Reserved | — | — | — | — | — | — | — | — |
| 7D | TR.TLBC | — | AGCD | GC5 | GC4 | GC3 | GC2 | GC1 | GC0 |
| 7E | TR.IAAR | GRIC | GTIC | IAA5 | IAA4 | IAA3 | IAA2 | IAA1 | IAA0 |
| 7F | TR.PCICR | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 80 | TR.TCICE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 81 | TR.TCICE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 82 | TR.TCICE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 83 | TR.TCICE4 | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 84 | TR.RCICE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 85 | TR.RCICE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 86 | TR.RCICE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 87 | TR.RCICE4 | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 88 | TR.RCBR1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 89 | TR.RCBR2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 8A | TR.RCBR3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 8B | TR.RCBR4 | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 8C | TR.TCBR1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 8D | TR.TCBR2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 8E | TR.TCBR3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 8F | TR.TCBR4 | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 90 | TR.H1TC | NOFS | TEOML | THR | THMS | TFS | TEOM | TZSD | TCRCD |
| 91 | TR.H1FC | — | — | TFLWM2 | TFLWM1 | TFLWM0 | RFHWM2 | RFHWM1 | RFHWM0 |
| 92 | TR.H1RCS1 | RHCS8 | RHCS7 | RHCS6 | RHCS5 | RHCS4 | RHCS3 | RHCS2 | RHCS1 |
| 93 | TR.H1RCS2 | RHCS16 | RHCS15 | RHCS14 | RHCS13 | RHCS12 | RHCS11 | RHCS10 | RHCS9 |
| 94 | TR.H1RCS3 | RHCS24 | RHCS23 | RHCS22 | RHCS21 | RHCS20 | RHCS19 | RHCS18 | RHCS17 |
| 95 | TR.H1RCS4 | RHCS32 | RHCS31 | RHCS30 | RHCS29 | RHCS28 | RHCS27 | RHCS26 | RHCS25 |
| 96 | TR.H1RTSBS | RCB8SE | RCB7SE | RCB6SE | RCB5SE | RCB4SE | RCB3SE | RCB2SE | RCB1SE |
| 97 | TR.H1TCS1 | THCS8 | THCS7 | THCS6 | THCS5 | THCS4 | THCS3 | THCS2 | THCS1 |
| 98 | TR.H1TCS2 | THCS16 | THCS15 | THCS14 | THCS13 | THCS12 | THCS11 | THCS10 | THCS9 |
| 99 | TR.H1TCS3 | THCS24 | THCS23 | THCS22 | THCS21 | THCS20 | THCS19 | THCS18 | THCS17 |
| 9A | TR.H1TCS4 | THCS32 | THCS31 | THCS30 | THCS29 | THCS28 | THCS27 | THCS26 | THCS25 |
| 9B | TR.H1TTSBS | TCB8SE | TCB7SE | TCB6SE | TCB5SE | TCB4SE | TCB3SE | TCB2SE | TCB1SE |
| 9C | TR.H1RPBA | MS | RPBA6 | RPBA5 | RPBA4 | RPBA3 | RPBA2 | RPBA1 | RPBA0 |
| 9D | TR.H1TF | THD7 | THD6 | THD5 | THD4 | THD3 | THD2 | THD1 | THD0 |
| 9E | TR.H1RF | RHD7 | RHD6 | RHD5 | RHD4 | RHD3 | RHD2 | RHD1 | RHD0 |
| 9F | TR.H1TFBA | TFBA7 | TFBA6 | TFBA5 | TFBA4 | TFBA3 | TFBA2 | TFBA1 | TFBA0 |
| A0 | TR.H2TC | NOFS | TEOML | THR | THMS | TFS | TEOM | TZSD | TCRCD |
| A1 | TR.H2FC | — | — | TFLWM2 | TFLWM1 | TFLWM0 | RFHWM2 | RFHWM1 | RFHWM0 |
| A2 | TR.H2RCS1 | RHCS8 | RHCS7 | RHCS6 | RHCS5 | RHCS4 | RHCS3 | RHCS2 | RHCS1 |
| A3 | TR.H2RCS2 | RHCS16 | RHCS15 | RHCS14 | RHCS13 | RHCS12 | RHCS11 | RHCS10 | RHCS9 |
| A4 | TR.H2RCS3 | RHCS24 | RHCS23 | RHCS22 | RHCS21 | RHCS20 | RHCS19 | RHCS18 | RHCS17 |
| A5 | TR.H2RCS4 | RHCS32 | RHCS31 | RHCS30 | RHCS29 | RHCS28 | RHCS27 | RHCS26 | RHCS25 |
| A6 | TR.H2RTSBS | RCB8SE | RCB7SE | RCB6SE | RCB5SE | RCB4SE | RCB3SE | RCB2SE | RCB1SE |
| A7 | TR.H2TCS1 | THCS8 | THCS7 | THCS6 | THCS5 | THCS4 | THCS3 | THCS2 | THCS1 |
| A8 | TR.H2TCS2 | THCS16 | THCS15 | THCS14 | THCS13 | THCS12 | THCS11 | THCS10 | THCS9 |

| ADDR | NAME | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------|------------|--|--------|--------|--------|--------|---------|---------|---------|
| A9 | TR.H2TCS3 | THCS24 | THCS23 | THCS22 | THCS21 | THCS20 | THCS19 | THCS18 | THCS17 |
| AA | TR.H2TCS4 | THCS32 | THCS31 | THCS30 | THCS29 | THCS28 | THCS27 | THCS26 | THCS25 |
| AB | TR.H2TTSBS | TCB8SE | TCB7SE | TCB6SE | TCB5SE | TCB4SE | TCB3SE | TCB2SE | TCB1SE |
| AC | TR.H2RPBA | MS | RPBA6 | RPBA5 | RPBA4 | RPBA3 | RPBA2 | RPBA1 | RPBA0 |
| AD | TR.H2TF | THD7 | THD6 | THD5 | THD4 | THD3 | THD2 | THD1 | THD0 |
| AE | TR.H2RF | RHD7 | RHD6 | RHD5 | RHD4 | RHD3 | RHD2 | RHD1 | RHD0 |
| AF | TR.H2TFBA | TFBA7 | TFBA6 | TFBA5 | TFBA4 | TFBA3 | TFBA2 | TFBA1 | TFBA0 |
| B0 | Reserved | — | — | — | — | — | — | — | — |
| B1 | Reserved | — | — | — | — | — | — | — | — |
| B2 | Reserved | — | — | — | — | — | — | — | — |
| B3 | Reserved | — | — | — | — | — | — | — | — |
| B4 | Reserved | — | — | — | — | — | — | — | — |
| B5 | Reserved | — | — | — | — | — | — | — | — |
| B6 | TR.IBCC | TC1 | TC0 | RUP2 | RUP1 | RUP0 | RDN2 | RDN1 | RDN0 |
| B7 | TR.TCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| B8 | TR.TCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| B9 | TR.RUPCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| BA | TR.RUPCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| BB | TR.RDNCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| BC | TR.RDNCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| BD | TR.RSCC | — | — | — | — | — | RSC2 | RSC1 | RSC0 |
| BE | TR.RSCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| BF | TR.RSCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| C0 | TR.RFDL | Bit Definitions Change With BOCC Setting. See Register Definition. | | | | | | | |
| C1 | TR.TFDL | TFDL7 | TFDL6 | TFDL5 | TFDL4 | TFDL3 | TFDL2 | TFDL1 | TFDL0 |
| C2 | TR.RFDLM1 | RFDLM7 | RFDLM6 | RFDLM5 | RFDLM4 | RFDLM3 | RFDLM2 | RFDLM1 | RFDLM0 |
| C3 | TR.RFDLM2 | RFDLM7 | RFDLM6 | RFDLM5 | RFDLM4 | RFDLM3 | RFDLM2 | RFDLM1 | RFDLM0 |
| C4 | — | — | — | — | — | — | — | — | — |
| C5 | TR.IBOC | — | IBS1 | IBS0 | - | IBOEN | DA2 | DA1 | DA0 |
| C6 | TR.RAF | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| C7 | TR.RNAF | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| C8 | TR.RSIAF | SiF0 | SiF2 | SiF4 | SiF6 | SiF8 | SiF10 | SiF12 | SiF14 |
| C9 | TR.RSiNAF | SiF1 | SiF3 | SiF5 | SiF7 | SiF9 | SiF11 | SiF13 | SiF15 |
| CA | TR.RRA | RRAF1 | RRAF3 | RRAF5 | RRAF7 | RRAF9 | RRAF11 | RRAF13 | RRAF15 |
| CB | TR.RSa4 | RSa4F1 | RSa4F3 | RSa4F5 | RSa4F7 | RSa4F9 | RSa4F11 | RSa4F13 | RSa4F15 |
| CC | TR.RSa5 | RSa5F1 | RSa5F3 | RSa5F5 | RSa5F7 | RSa5F9 | RSa5F11 | RSa5F13 | RSa5F15 |
| CD | TR.RSa6 | RSa6F1 | RSa6F3 | RSa6F5 | RSa6F7 | RSa6F9 | RSa6F11 | RSa6F13 | RSa6F15 |
| CE | TR.RSa7 | RSa7F1 | RSa7F3 | RSa7F5 | RSa7F7 | RSa7F9 | RSa7F11 | RSa7F13 | RSa7F15 |
| CF | TR.RSa8 | RSa8F1 | RSa8F3 | RSa8F5 | RSa8F7 | RSa8F9 | RSa8F11 | RSa8F13 | RSa8F15 |
| D0 | TR.TAF | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| D1 | TR.TNAF | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| D2 | TR.TSiAF | TsiF0 | TsiF2 | TsiF4 | TsiF6 | TsiF8 | TsiF10 | TsiF12 | TsiF14 |
| D3 | TR.TSiNAF | TsiF1 | TsiF3 | TsiF5 | TsiF7 | TsiF9 | TsiF11 | TsiF13 | TsiF15 |
| D4 | TR.TRA | TRAF1 | TRAF3 | TRAF5 | TRAF7 | TRAF9 | TRAF11 | TRAF13 | TRAF15 |
| D5 | TR.TSa4 | TSa4F1 | TSa4F3 | TSa4F5 | TSa4F7 | TSa4F9 | TSa4F11 | TSa4F13 | TSa4F15 |
| D6 | TR.TSa5 | TSa5F1 | TSa5F3 | TSa5F5 | TSa5F7 | TSa5F9 | TSa5F11 | TSa5F13 | TSa5F15 |
| D7 | TR.TSa6 | TSa6F1 | TSa6F3 | TSa6F5 | TSa6F7 | TSa6F9 | TSa6F11 | TSa6F13 | TSa6F15 |
| D8 | TR.TSa7 | TSa7F1 | TSa7F3 | TSa7F5 | TSa7F7 | TSa7F9 | TSa7F11 | TSa7F13 | TSa7F15 |
| D9 | TR.TSa8 | TSa8F1 | TSa8F3 | TSa8F5 | TSa8F7 | TSa8F9 | TSa8F11 | TSa8F13 | TSa8F15 |
| DA | TR.TSACR | SiAF | SiNAF | RA | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| DB | TR.BAWC | ACNT7 | ACNT6 | ACNT5 | ACNT4 | ACNT3 | ACNT2 | ACNT1 | ACNT0 |
| DC | TR.BRP1 | RPAT7 | RPAT6 | RPAT5 | RPAT4 | RPAT3 | RPAT2 | RPAT1 | RPAT0 |
| DD | TR.BRP2 | RPAT15 | RPAT14 | RPAT13 | RPAT12 | RPAT11 | RPAT10 | RPAT9 | RPAT8 |
| DE | TR.BRP3 | RPAT23 | RPAT22 | RPAT21 | RPAT20 | RPAT19 | RPAT18 | RPAT17 | RPAT16 |
| DF | TR.BRP4 | RPAT31 | RPAT30 | RPAT29 | RPAT28 | RPAT27 | RPAT26 | RPAT25 | RPAT24 |
| E0 | TR.BC1 | TC | TINV | RINV | PS2 | PS1 | PS0 | LC | RESYNC |
| E1 | TR.BC2 | EIB2 | EIB1 | EIB0 | SBE | RPL3 | RPL2 | RPL1 | RPL0 |
| E2 | Reserved | — | — | — | — | — | — | — | — |
| E3 | TR.BBC1 | BBC7 | BBC6 | BBC5 | BBC4 | BBC3 | BBC2 | BBC1 | BBC0 |
| E4 | TR.BBC2 | BBC15 | BBC14 | BBC13 | BBC12 | BBC11 | BBC10 | BBC9 | BBC8 |

DS33R41 Inverse-Multiplexing Ethernet Mapper with Quad Integrated T1/E1/J1 Transceivers

| ADDR | NAME | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|----------|-------|-------|-------|-------|-------|-------|---------|--------|
| E5 | TR.BBC3 | BBC23 | BBC22 | BBC21 | BBC20 | BBC19 | BBC18 | BBC17 | BBC16 |
| E6 | TR.BBC4 | BBC31 | BBC30 | BBC29 | BBC28 | BBC27 | BBC26 | BBC25 | BBC24 |
| E7 | TR.BEC1 | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |
| E8 | TR.BEC2 | EC15 | EC14 | EC13 | EC12 | EC11 | EC10 | EC9 | EC8 |
| E9 | TR.BEC3 | EC23 | EC22 | EC21 | EC20 | EC19 | EC18 | EC17 | EC16 |
| EA | TR.BIC | — | RFUS | — | TBAT | TFUS | — | BERTDIR | BERTEN |
| EB | TR.ERC | WNOE | — | — | CE | ER3 | ER2 | ER1 | ER0 |
| EC | TR.NOE1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| ED | TR.NOE2 | — | — | — | — | — | — | C9 | C8 |
| EE | TR.NOEL1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| EF | TR.NOEL2 | — | — | — | — | — | — | C9 | C8 |
| F1 | TR.PSA1 | — | — | AGCT2 | SRR1 | AGCT1 | SRR0 | AGCT0 | SRIB0 |
| F2 | TR.PSA2 | SRIA4 | — | — | — | SRIA3 | — | — | — |
| F0– FF | Reserved | — | — | — | — | — | — | — | — |

Note: Address locations above are for T1/E1/J1 Transceiver 1. Transceiver 2 has a base address of 100h, Transceiver 3 has a base address of 200h, and Transceiver 3 has a base address of 300h.

12.3 Global Register Definitions for Ethernet Mapper

Functions contained in the global registers include: framer reset, LIU reset, device ID, BERT interrupt status, framer interrupt status, IBO configuration, MCLK configuration, and BPCLK configuration. These registers are preserved to provide code compatibility with the multiport devices in this product family. The global registers bit descriptions are presented below.

Register Name: **GL.IDRL**
 Register Description: **Global ID Low Register**
 Register Address: **00h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Name | <u>ID07</u> | <u>ID06</u> | <u>ID05</u> | <u>ID04</u> | <u>ID03</u> | <u>ID02</u> | <u>ID01</u> | <u>ID00</u> |
| Default | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

Bit 7: ID07. Reserved for future use.

Bit 6: ID06. Reserved for future use.

Bit 5: ID05. If this bit is set the device contains a RMII interface

Bit 4: ID04. If this bit is set the device contains a MII interface.

Bit 3: ID03. If this bit is set the device contains an Ethernet PHY.

Bits 2 to 0: ID02 to ID00. A 3-bit count that is equal to 000b for the first die revision, and is incremented with each successive die revision. May not match the two-letter die revision code on the top brand of the device.

Register Name: **GL.IDRH**
 Register Description: **Global ID High Register**
 Register Address: **01h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Name | <u>ID15</u> | <u>ID14</u> | <u>ID13</u> | <u>ID12</u> | <u>ID11</u> | <u>ID10</u> | <u>ID09</u> | <u>ID08</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

Bits 7 to 5: ID15 to ID13. Number of ports in the device – 1.

Bit 4: ID12. If this bit is set the device has LIU functionality.

Bit 3: ID11. If this bit is set the device has a framer.

Bit 2: ID10. Reserved for future use.

Bit 1: ID09. If this bit is set the device has HDLC or X.86 encapsulation.

Bit 0: ID08. If this bit is set the device has inverse multiplexing functionality.

Register Name: **GL.CR1**
 Register Description: **Global Control Register 1**
 Register Address: **02h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|----------|------|-----|
| Name | — | — | — | — | — | REF_CLKO | INTM | RST |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2: REF_CLKO OFF (REF_CLKO). This bit determines the REF_CLKO output mode.

1 = REF_CLKO is disabled and outputs an active low signal.

0 = REF_CLKO is active and in accordance with RMII/MII Selection.

Bit 1: $\overline{\text{INT}}$ Pin Mode (INTM). This bit determines the inactive mode of the $\overline{\text{INT}}$ pin. The $\overline{\text{INT}}$ pin always drives low when active.

1 = Pin is high impedance when not active.

0 = Pin drives high when not active.

Bit 0: Reset (RST). When this bit is set to 1, all of the internal data path and status and control registers (except this RST bit), on all ports, are reset to their default state. This bit must be set high for a minimum of 100ns.

0 = Normal operation.

1 = Reset and force all internal registers to their default values.

Register Name: **GL.RTCAL**
 Register Description: **Global Receive and Transmit Serial Port Clock Activity Latched Status**
 Register Address: **04h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|--------|---|---|---|--------|
| Name | — | — | — | RLCAL1 | — | — | — | TLCAL1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Receive Serial Interface Clock Activity Latched Status 1 (RLCAL1). This bit is set to 1 if the receive clock for Serial Interface 1 has activity. This bit is cleared upon read.

Bit 0: Transmit Serial Interface Clock Activity Latched Status 1 (TLCAL1). This bit is set to 1 if the transmit clock for Serial Interface 1 has activity. This bit is cleared upon read.

Register Name: **GL.SRCALS**
 Register Description: **Global SDRAM Reference Clock Activity Latched Status**
 Register Address: **05h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---------|--------|
| Name | — | — | — | — | — | — | REFCLKS | SYSCLS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 1: Reference Clock Activity Latched Status (REFCLKS). This bit is set to 1 if REF_CLK has activity. This bit is cleared upon read.

Bit 0: System Clock Input Latched Status (SYSCLS). This bit is set to 1 if SYSCCLKI has activity. This bit is cleared upon read.

Register Name: **GL.LIE**
 Register Description: **Global Serial Interface Interrupt Enable**
 Register Address: **06h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---------|---|---|---|---------|
| Name | — | — | — | LIN1TIE | — | — | — | LIN1RIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Serial Interface 1 TX Interrupt Enable (LINE1TIE). Setting this bit to 1 enables an interrupt on LIN1TIS.

Bit 0: Serial Interface 1 RX Interrupt Enable (LINE1RIE). Setting this bit to 1 enables an interrupt on LIN1RIS.

Register Name: **GL.LIS**
 Register Description: **Global Serial Interface Interrupt Status**
 Register Address: **07h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---------|---|---|---|---------|
| Name | — | — | — | LIN1TIS | — | — | — | LIN1RIS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Serial Interface 1 TX Interrupt Status (LIN1TIS). This bit is set if Serial Interface 1 Transmit has an enabled interrupt generating event. Serial Interface interrupts consist of HDLC interrupts and X.86 interrupts.

Bit 0: Serial Interface 1 RX Interrupt Status (LIN1RIS). This bit is set if Serial Interface 1 Receive has an enabled interrupt generating event. Serial Interface interrupts consist of HDLC interrupts and X.86 interrupts.

Register Name: **GL.SIE**
 Register Description: **Global Ethernet Interface Interrupt Enable**
 Register Address: **08h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|--------|
| Name | — | — | — | — | — | — | — | SUB1IE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Ethernet Interface 1 Interrupt Enable (SUB1IE). Setting this bit to 1 enables an interrupt on SUB1S.

Register Name: **GL.SIS**
 Register Description: **Global Ethernet Interface Interrupt Status**
 Register Address: **09h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|--------|
| Name | — | — | — | — | — | — | — | SUB1IS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Ethernet Interface 1 Interrupt Status (SUB1IS). This bit is set to 1 if Ethernet Interface 1 has an enabled interrupt generating event. The Ethernet Interface consists of the MAC and The RMII/MII port.

Register Name: **GL.TRQIE**
 Register Description: **Global Transmit Receive Queue Interrupt Enable**
 Register Address: **0Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|---|---|---|-------|
| Name | — | — | — | TQ1IE | — | — | — | RQ1IE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Transmit Queue 1 Interrupt Enable (TQ1IE). Setting this bit to 1 enables an interrupt on TQ1IS.

Bit 0: Receive Queue 1 Interrupt Enable (RQ1IE). Setting this bit to 1 enables an interrupt on RQ1IS.

Register Name: **GL.TRQIS**
 Register Description: **Global Transmit Receive Queue Interrupt Status**
 Register Address: **0Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|---|---|---|-------|
| Name | — | — | — | TQ1IS | — | — | — | RQ1IS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Transmit Queue 1 Interrupt Status (TQ1IS). If this bit is set to 1, the Transmit Queue 1 has interrupt status event. Transmit queue events are transmit queue crossing thresholds and queue overflows.

Bit 0: Receive Queue 1 Interrupt Status (RQ1IS). If this bit is set to 1, the Receive Queue 1 has interrupt status event. Receive queue events are transmit queue crossing thresholds and queue overflows.

Register Name: **GL.IBIE**
 Register Description: **Global IMUX and BERT Interrupt Enable**
 Register Address: **0Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|--------|-----|
| Name | — | — | — | — | — | — | IMUXIE | BIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 1: IMUX Interrupt Enable (IMUXIE). Setting this bit to 1 enables an interrupt on IIS.

Bit 0: BERT Interrupt Enable (BIE). Setting this bit to 1 enables an interrupt on BIS.

Register Name: **GL.IBIS**
 Register Description: **Global IMUX and BERT Interrupt Status**
 Register Address: **0Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|-----|-----|
| Name | — | — | — | — | — | — | IIS | BIS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 1: IMUX Interrupt Status (IIS). This bit is set to 1 if the IMUX has an enabled interrupt generating event.

Bit 0: BERT Interrupt Status (BIS). This bit is set to 1 if the BERT has an enabled interrupt generating event.

Register Name: **GL.CON1**
 Register Description: **Connection Register for Ethernet Interface 1**
 Register Address: **0Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|----------|
| Name | — | — | — | — | — | — | — | LINE1[0] |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Bit 0: LINE1[0]. This bit is preserved to provide software compatibility with multiport devices. The LINE1[0] bit selects the Ethernet port that is to be connected to the Serial Interface. Note that bidirectional connection is assumed between the Serial and Ethernet Interfaces. The connection register and corresponding queue size must be defined for proper operation. Writing a 0 to this register will disconnect the connection. When a connection is disconnected, “1”s are sourced to the Serial Interface transmit and to the HDLC receiver and the clocks to the HDLC transmitter/receiver are disabled.

Register Name: **GL.C1QPR**
 Register Description: **Connection 1 Queue Pointer Reset**
 Register Address: **12h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|--------|--------|--------|--------|
| Name | — | — | — | — | C1MRPR | C1HWPR | C1MHPR | C1HRPR |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: MAC Read Pointer Reset (C1MRPR). Setting this bit to 1 resets the receive queue read pointer for connection 1. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 2: HDLC Write Pointer Reset (C1HWPR). Setting this bit to 1 resets the receive queue write pointer for connection 1. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 1: HDLC Read Pointer Reset (C1MHPR). Setting this bit to 1 resets the transmit queue read pointer for connection 1. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 0: MAC Transmit Write Pointer Reset (C1HRPR). Setting this bit to 1 resets the transmit queue write pointer for connection 1. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Register Name: **GL.IMXCN**
 Register Description: **Inverse MUX Configuration Register**
 Register Address: **16h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|-----|-------|----|----|----|----|
| Name | — | T1E1 | RXE | SENDE | L4 | L3 | L2 | L1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: T1E1 Mode (T1E1). This bit determines if the IMUX operation is for T1 or E1 Mode.

0 = T1 Mode
 1 = E1 Mode

Bit 5: Receive Enable (RXE). If this bit is set to 1, data will be received from the Serial Interface and passed to the packet processor. If equal to 0, no data will be sent to the packet processor.

Bit 4: SEND Enable (SENDE). If this bit is set to 1, the data will be transmitted on the Serial Interface. If equal to 0, data is blocked.

Bit 3: Link 4 (L4). If this bit is set to 1, link number four is participating in the communication. If this bit is equal to 0, the link does not participate.

Bit 2: Link 3 (L3). If this bit is set to 1, link number three is participating in the communication. If this bit is equal to 0, the link does not participate.

Bit 1: Link 2 (L2). If this bit is set to 1, link number two is participating in the communication. If this bit is equal to 0, the link does not participate.

Bit 0: Link 1 (L1.) If this bit is set to 1, link number one is participating in the communication. If this bit is equal to 0, the link does not participate.

Register Name: **GL.IMXC**
 Register Description: **Inverse MUX Command Register**
 Register Address: **17h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | IMUXC7 | IMUXC6 | IMUXC5 | IMUXC4 | IMUXC3 | IMUXC2 | IMUXC1 | IMUXC0 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Bits 7 to 0: Inverse Multiplexing Command (IMUXC[7:0]). This byte is used to issue IMUX commands.

Table 12-8. Available IMUX User Commands

| VALUE | COMMAND | COMMENT |
|------------|------------|--|
| 1111 1111b | NOP | No operation to perform. |
| 1000 0010b | Link Start | Establish Link with the distant end. Upon reception of this message, this distant end begins searching for three consecutive sequence numbers. |

The user must send a link start command. The NOP command may be written to this register after the link start command is written. All values other than those listed above will be ignored.

Register Name: **GL.IMXSS**
 Register Description: **Inverse MUX Sync Status**
 Register Address: **18h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Name | ITSYNC4 | ITSYNC3 | ITSYNC2 | ITSYNC1 | IRSYNC4 | IRSYNC3 | IRSYNC2 | IRSYNC1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: IMUX Transmit Sync 4 (ITSYNC4). If this bit is set to 1, the device has received a rsync command for the fourth portion of the 8.192Mbps link from the distant node. This status bit indicates that the distant end is in sync.

Bit 6: IMUX Transmit Sync 3 (ITSYNC3). If this bit is set to 1, the device has received a rsync command for the third portion of the 8.192Mbps link from the distant node. This status bit indicates that the distant end is in sync.

Bit 5: IMUX Transmit Sync 2 (ITSYNC2). If this bit is set to 1, the device has received a rsync command for the second portion of the 8.192Mbps link from the distant node. This status bit indicates that the distant end is in sync.

Bit 4: IMUX Transmit Sync 1 (ITSYNC1). If this bit is set to 1, the device has received a rsync command for the first portion of the 8.192Mbps link from the distant node. This status bit indicates that the distant end is in sync.

Bit 3: IMUX Receive Sync 4 (IRSYNC4). If this bit is set to 1, the local end is in sync for the fourth portion of the 8.192Mbps link. The command states that the local end is in sync.

Bit 2: IMUX Receive Sync 3 (IRSYNC3). If this bit is set to 1, the local end is in sync for the third portion of the 8.192Mbps link. The command states that the local end is in sync.

Bit 1: IMUX Receive Sync 2 (IRSYNC2). If this bit is set to 1, the local end is in sync for the second portion of the 8.192Mbps link. The command states that the local end is in sync.

Bit 0: IMUX Receive Sync 1 (IRSYNC1). If this bit is set to 1, the local end is in sync for the first portion of the 8.192Mbps link. The command states that the local end is in sync.

Register Name: **GL.IMXSIE**
 Register Description: **Inverse Mux Sync Interrupt Enable**
 Register Address: **19h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------------|------------|------------|------------|------------|------------|------------|------------|
| Name | ITSYNCLIE4 | ITSYNCLIE3 | ITSYNCLIE2 | ITSYNCLIE1 | IRSYNCLIE4 | IRSYNCLIE3 | IRSYNCLIE2 | IRSYNCLIE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: IMUX Transmit Sync Interrupt Enable 4 (ITSYNCLIE4). Setting this bit to 1 enables an interrupt on ITSYNCLS4.

Bit 6: IMUX Transmit Sync Interrupt Enable 3 (ITSYNCLIE3). Setting this bit to 1 enables an interrupt on ITSYNCLS3.

Bit 5: IMUX Transmit Sync Interrupt Enable 2 (ITSYNCLIE2). Setting this bit to 1 enables an interrupt on ITSYNCLS2.

Bit 4: IMUX Transmit Sync Interrupt Enable 1 (ITSYNCLIE1). Setting this bit to 1 enables an interrupt on ITSYNCLS1.

Bit 3: IMUX Receive Sync Interrupt Enable 4 (IRSYNCLIE4). Setting this bit to 1 enables an interrupt on IRSYNCLS4.

Bit 2: IMUX Receive Sync Interrupt Enable 3 (IRSYNCLIE3). Setting this bit to 1 enables an interrupt on IRSYNCLS3.

Bit 1: IMUX Receive Sync Interrupt Enable 2 (IRSYNCLIE2). Setting this bit to 1 enables an interrupt on IRSYNCLS2.

Bit 0: IMUX Receive Sync Interrupt Enable 1 (IRSYNCLIE1). Setting this bit to 1 enables an interrupt on IRSYNCLS1.

Register Name: **GL.IMXSLS**
 Register Description: **Inverse MUX Sync Latched Status**
 Register Address: **1Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Name | ITSYNCLS4 | ITSYNCLS3 | ITSYNCLS2 | ITSYNCLS1 | IRSYNCLS4 | IRSYNCLS3 | IRSYNCLS2 | IRSYNCLS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: IMUX Transmit Sync Latched Status 4 (ITSYNCLS4). This is a latched status bit for ITSYNCL4.

Bit 6: IMUX Transmit Sync Latched Status 3 (ITSYNCLS3). This is a latched status bit for ITSYNCL3.

Bit 5: IMUX Transmit Sync Latched Status 2 (ITSYNCLS2). This is a latched status bit for ITSYNCL2.

Bit 4: IMUX Transmit Sync Latched Status 1 (ITSYNCLS1). This is a latched status bit for ITSYNCL1.

Bit 3: IMUX Receive Sync Latched Status 4 (IRSYNCLS4). This is a latched status bit for IRSYNCL4.

Bit 2: IMUX Receive Sync Latched Status 3 (IRSYNCLS3). This is a latched status bit for IRSYNCL3.

Bit 1: IMUX Receive Sync Latched Status 2 (IRSYNCLS2). This is a latched status bit for IRSYNCL2.

Bit 0: IMUX Receive Sync Latched Status 1 (IRSYNCLS1). This is a latched status bit for IRSYNCL1.

Register Name: **GL.IMXDFD**
 Register Description: **Inverse MUX Diff delay**
 Register Address: **1Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Name | IMUXDFD7 | IMUXDFD6 | IMUXDFD5 | IMUXDFD4 | IMUXDFD3 | IMUXDFD2 | IMUXDFD1 | IMUXDFD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: IMUX Differential Delay. These 8 bits provide the IMUX differential delay. The maximum differential delay that can be measured is 64ms.

Register Name: **GL.IMXDIE**
 Register Description: **Inverse MUX Diff delay Error Interrupt Enable**
 Register Address: **1Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|--------|
| Name | — | — | — | — | — | — | — | IDDEIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: IMUX Differential Delay Error Interrupt Enable (IDDEIE). Setting this bit to 1 enables an interrupt on IDDELS0.

Register Name: **GL.IMXDDELS**
 Register Description: **Inverse MUX Diff delay Error Latched Status**
 Register Address: **1Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---------|
| Name | — | — | — | — | — | — | — | IDDELS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: IMUX Differential Delay Error latched Status (IDDELS0). This bit provides the differential delay error latched status. It is set to 1 when the differential delay has exceeded 7.75ms.

Register Name: **GL.IMXOOFIE**
 Register Description: **Inverse MUX OOF Interrupt Enable**
 Register Address: **1Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Name | TOOFIE4 | TOOFIE3 | TOOFIE2 | TOOFIE1 | ROOFIE4 | ROOFIE3 | ROOFIE2 | ROOFIE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: IMUX Transmit OOF Interrupt Enable 4 (TOOFIE4). Setting this bit to 1 enables an interrupt on TOOFLS4.

Bit 6: IMUX Transmit OOF Interrupt Enable 3 (TOOFIE3). Setting this bit to 1 enables an interrupt on TOOFLS3.

Bit 5: IMUX Transmit OOF Interrupt Enable 2 (TOOFIE2). Setting this bit to 1 enables an interrupt on TOOFLS2.

Bit 4: IMUX Transmit OOF Interrupt Enable 1 (TOOFIE1). Setting this bit to 1 enables an interrupt on TOOFLS1.

Bit 3: IMUX Receive OOF Interrupt Enable 4 (ROOFIE4). Setting this bit to 1 enables an interrupt on ROOFLS4.

Bit 2: IMUX Receive OOF Interrupt Enable 3 (ROOFIE3). Setting this bit to 1 enables an interrupt on ROOFLS3.

Bit 1: IMUX Receive OOF Interrupt Enable 2 (ROOFIE2). Setting this bit to 1 enables an interrupt on ROOFLS2.

Bit 0: IMUX Receive OOF Interrupt Enable 1 (ROOFIE1). Setting this bit to 1 enables an interrupt on ROOFLS1.

Register Name: **GL.IMXOOFLS**
 Register Description: **Inverse MUX Out Of Frame Latched Status**
 Register Address: **1Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|--------|---------|---------|--------|--------|---------|---------|
| Name | TOOFLS4 | OOFLS3 | TOOFLS2 | TOOFLS1 | ROOFL4 | ROOFL3 | ROOFLS2 | ROOFLS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: IMUX Transmit OOF Latched Status 4 (TOOFLS4). This is a latched bit for Transmit OOF, this bit is set if the distant end is out of frame.

Bit 6: IMUX Transmit OOF Latched Status 3 (TOOFLS3). This is a latched bit for Transmit OOF, this bit is set if the distant end is out of frame.

Bit 5: IMUX Transmit Sync Latched Status 2 (TOOFLS2). This is a latched bit for Transmit OOF, this bit is set if the distant end is out of frame.

Bit 4: IMUX Transmit Sync Latched Status 1 (TOOFLS1). This is a latched bit for Transmit OOF, this bit is set if the distant end is out of frame.

Bit 3: IMUX Receive Sync Latched Status 4 (ROOFLS4). This is a latched bit for Receiver OOF, this bit is set if the receiver end is out of frame.

Bit 2: IMUX Receive Sync Latched Status 3 (ROOFLS3). This is a latched bit for Receiver OOF, this bit is set if the receiver end is out of frame.

Bit 1: IMUX Receive Sync Latched Status 2 (ROOFLS2). This is a latched bit for Receiver OOF, this bit is set if the receiver end is out of frame.

Bit 0: IMUX Receive Sync Latched Status 1 (ROOFLS1). This is a latched bit for Receiver OOF, this bit is set if the receiver end is out of frame.

Note that the user must clear the [GL.IMXCN.SENDE](#) bit to stop data transmission when an OOF condition is detected. The user must re-initiate the handshaking procedure for re-establishment of communication.

Register Name: **GL.BISTEN**
 Register Description: **BIST Enable**
 Register Address: **20h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|-------|
| Name | — | — | — | — | — | — | — | BISTE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: BIST Enable (BISTE). If this bit is set the device performs BIST test on the SDRAM. Normal data communication is halted while BIST enable is high. The user must reset the device after completion of BIST test before normal dataflow can begin.

Register Name: **GL.BISTPF**
 Register Description: **BIST PassFail**
 Register Address: **21h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|--------|--------|
| Name | — | — | — | — | — | — | BISTDN | BISTPF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 1: BIST DONE (BISTDN). If this bit is set to 1, the device has completed the BIST Test initiated by BISTE. The pass-fail result is available in BISTPF.

Bit 0: BIST PassFail (BISTPF). This bit is equal to 0 after the device performs BIST testing on the SDRAM and the test passes. This bit is set to 1 if the test failed. This bit is valid only after the BIST test is complete and the BIST DN bit is set. If set this bit can only be cleared by resetting the device.

Register Name: **GL.LSMRRFD**
 Register Description: **Global Local Synchronization Machine Reset and Receive Frame Delay**
 Register Address: **38h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-----|-----|--------|--------|--------|--------|
| Name | — | — | FD1 | FD0 | LSMRC3 | LSMRC2 | LSMRC1 | LSMRC0 |
| Default | 0 | — | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 5 and 4: Frame Delay (FD[1:0]). Configures the delay that the frames are stored in the differential delay compensation RAM before being sent to the HDLC. The default value is 0 for a frame delay of 2 frames. A value of "01" = 3 frames, "10" = 4 frames, and "11" = 5 frames.

Bit 3: Local Machine Reset 3 (LSRMC3). Setting this bit to 1 resets the local IMUX state machine for link 4. Clear for normal operation.

Bit 2: Local Machine Reset 2 (LSRMC2). Setting this bit to 1 resets the local IMUX state machine for link 3. Clear for normal operation.

Bit 1: Local Machine Reset 1 (LSRMC1). Setting this bit to 1 resets the local IMUX state machine for link 2. Clear for normal operation.

Bit 0: Local Machine Reset 0 (LSRMC0). Setting this bit to 1 resets the local IMUX state machine for link 1. Clear for normal operation.

Register Name: **GL.SDMODE1**
 Register Description: **Global SDRAM Mode Register 1**
 Register Address: **3Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|----|-----|-----|-----|
| Name | — | — | — | — | WT | BL2 | BL1 | BL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

Bit 3: Wrap Type (WT). This bit is used to configure the wrap mode.
 0 = Sequential
 1 = Interleave

Bits 2 to 0: Burst Length 2 through 0 (BL2 to BL0). These bits are used to determine the Burst Length.

Note: This register has a non-zero default value. This should be taken into consideration when initializing the device.

Note: After changing the value of this register, the user must toggle the GL.SDMODEWS.SDMW bit to write the new values to the SDRAM.

Register Name: **GL.SDMODE2**
 Register Description: **Global SDRAM Mode Register 2**
 Register Address: **3Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|--------|--------|--------|
| Name | — | — | — | — | — | LTMOD2 | LTMOD1 | LTMOD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Bits 2 to 0: CAS Latency Mode (LTMOD2 to LTMOD0). These bits are used to setup CAS Latency. Note: Only CAS Latency of 2 or 3 is allowed.

Note: This register has a non-zero default value. This should be taken into consideration when initializing the device.

Note: After changing the value of this register, the user must toggle the GL.SDMODEWS.SDMW bit to write the new values to the SDRAM.

Register Name: **GL.SDMODEWS**
 Register Description: **Global SDRAM Mode Register Write Status**
 Register Address: **3Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|------|
| Name | — | — | — | — | — | — | — | SDMW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: SDRAM Mode Write (SDMW). Setting this bit to 1 will write the current values of the mode control and refresh time control registers to the SDRAM. The user must clear this bit and set it again for subsequent write operations.

Register Name: **GL.SDRFTC**
 Register Description: **Global SDRAM Refresh Time Control**
 Register Address: **3Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | SREFT7 | SREFT6 | SREFT5 | SREFT4 | SREFT3 | SREFT2 | SREFT1 | SREFT0 |
| Default | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

Bits 7 to 0: SDRAM Refresh Time Control (SREFT7 to SREFT0). These 8 bits are used to control the SDRAM refresh frequency. The refresh rate will be equal to this register value x 8 x 100MHz.

Note: This register has a non-zero default value. This should be taken into consideration when initializing the device.

Note: After changing the value of this register, the user must toggle the GL.SDMODEWS.SDMW bit to write the new values to the SDRAM.

12.4 Arbiter Registers

The Arbiter manages the transport between the Ethernet port and the Serial Interface. It is responsible for queuing and dequeuing data to an external SDRAM. The arbiter handles requests from the HDLC and MAC to transfer data to/from the SDRAM. The base address of the Arbiter register space is 0040h.

12.4.1 Arbiter Register Bit Descriptions

Register Name: **AR.RQSC1**
 Register Description: **Arbiter Receive Queue Size Connection 1**
 Register Address: **40h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RQSC7 | RQSC6 | RQSC5 | RQSC4 | RQSC3 | RQSC2 | RQSC1 | RQSC0 |
| Default | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |

Bits 7 to 0: Receive Queue Size (RQSC[7:0]). These 7 bits of the size of receive queue associated with the connection. Receive queue is for data arriving from the MAC to be sent to the WAN. The Queue address size is defined in increments of 32 x 2048 bytes. The queue size is AR.RQSC1 multiplied by 32 to determine the number of 2048 byte packets that can be stored in the queue. This queue is constructed in the external SDRAM. **Note: Queue size of 0 is not allowed and should never be set.**

Register Name: **AR.TQSC1**
 Register Description: **Arbiter Transmit Queue Size Connection 1**
 Register Address: **41h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TQSC7 | TQSC6 | TQSC5 | TQSC4 | TQSC3 | TQSC2 | TQSC1 | TQSC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

Bits 7 to 0: Transmit Queue Size (TQSC[7:0]). This is size of transmit queue associated with the connection. The queue address size is defined in increments of 32 packets. The range of bytes will depend on the external SDRAM connected to the device. Transmit queue is the data queue for data arriving on the WAN that is sent to the MAC. **Note that queue size of 0 is not allowed and should never be set.**

12.5 Serial Interface Registers

The Serial Interface contains the Serial HDLC transport circuitry and the associated serial port. The Serial Interface register map consists of registers that are common functions, transmit functions, and receive functions.

Bits that are underlined are read-only; all other bits can be written. All reserved registers and bits with “—” designation should be written to zero, unless specifically noted in the register definition. When read, the information from reserved registers and bits designated with “—” should be discarded.

Counter registers are updated by asserting (low to high transition) the associated performance monitoring update signal (xxPMU). During the counter register update process, the associated performance monitoring status signal (xxPMS) is deasserted. The counter register update process consists of loading the counter register with the current count, resetting the counter, forcing the zero count status indication low for one clock cycle, and then asserting xxPMS. No events are missed during this update procedure.

A latched bit is set when the associated event occurs, and remains set until it is cleared by reading. Once cleared, a latched bit will not be set again until the associated event occurs again. Reserved configuration bits and registers should be written to zero.

12.5.1 Serial Interface Transmit and Common Registers

Serial Interface Transmit Registers are used to control the HDLC transmitter associated with each Serial Interface. The register map is shown in the following table. Note that throughout this document the HDLC Processor is also referred to as a “packet processor.”

12.5.2 Serial Interface Transmit Register Bit Descriptions

Register Name: **LI.RSTPD**
 Register Description: **Serial Interface Reset Register**
 Register Address: **0C1h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|-------|---|
| Name | — | — | — | — | — | — | RESET | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 1: RESET If this bit set to 1, the Data Path and Control and Status for this interface are reset. The Serial Interface is held in Reset as long as this bit is high. This bit must be high for a minimum of 200ns for a valid reset to occur.

Register Name: **LI.LPBK**
 Register Description: **Serial Interface Loopback Control Register**
 Register Address: **0C2h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|-----|
| Name | — | — | — | — | — | — | — | QLP |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Queue Loopback Enable (QLP) If this bit set to 1, data received on the Serial Interface is looped back to the Serial Interface transmitter. Received data will not be sent from the Serial Interface to the Ethernet Interface. Buffered packet data will remain in queue until the loopback is removed.

12.5.3 Transmit HDLC Processor Registers

Register Name: **LI.TPPCL**
 Register Description: **Transmit Packet Processor Control Low Register**
 Register Address: **0C4h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|------|------|-----|------|-------|
| Name | — | — | TFAD | TF16 | TIFV | TSD | TBRE | TIAEI |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: The user should take care not to modify this register value during packet error insertion.

Bit 5: Transmit FCS Append Disable (TFAD). This bit controls whether or not an FCS is appended to the end of each packet. When equal to 0, the calculated FCS bytes are appended to packets. When set to 1, packets are transmitted without FCS. In X.86 Mode, FCS is always 32 bits and is always appended to the packet.

Bit 4: Transmit FCS-16 Enable (TF16). When 0, the FCS processing uses a 32-bit FCS. When 1, the FCS processing uses a 16-bit FCS. In X.86 Mode, 32-bit FCS processing is enabled.

Bit 3: Transmit Bit Synchronous Inter-Frame Fill Value (TIFV). When 0, inter-frame fill is done with the flag sequence (7Eh). When 1, inter-frame fill is done with all '1's. This bit is ignored in byte synchronous mode. In X.86 mode the interframe flag is always 7E.

Bit 2: Transmit Scrambling Disable (TSD). When equal to 0, $X^{43}+1$ scrambling is performed. When set to 1, scrambling is disabled. Note that in hardware mode, transmit scrambling is controlled by the SCD hardware pin.

Bit 1: Transmit Bit Reordering Enable (TBRE). When equal to 0, bit reordering is disabled (The first bit transmitted is from the MSB of the transmit FIFO byte TFD [7]). When set to 1, bit reordering is enabled (The first bit transmitted is from the LSB of the transmit FIFO byte TFD [0]). Note that this function can be controlled in Hardware mode with the BREO hardware pin.

Bit 0: Transmit Initiate Automatic Error Insertion (TIAEI). This write-only bit initiates error insertion. See the LI.TEPHC register definition for details of usage.

Register Name: **LI.TIFGC**
 Register Description: **Transmit Inter-Frame Gapping Control Register**
 Register Address: **0C5h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TIFG7 | TIFG6 | TIFG5 | TIFG4 | TIFG3 | TIFG2 | TIFG1 | TIFG0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Bits 7 to 0: Transmit Inter-Frame Gapping (TIFG[7:0]). These eight bits indicate the number of additional flags and bytes of inter-frame fill to be inserted between packets. The number of flags and bytes of inter-frame fill between packets is at least the value of TIFG[7:0] plus 1. Note: If inter-frame fill is set to all 1s, a TIFG value of 2 or 3 will result in a flag, two bytes of 1s, and an additional flag between packets.

Register Name: **LI.TEPLC**
 Register Description: **Transmit Errored Packet Low Control Register**
 Register Address: **0C6h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TPEN7 | TPEN6 | TPEN5 | TPEN4 | TPEN3 | TPEN2 | TPEN1 | TPEN0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Errored Packet Insertion Number (TPEN[7:0]). These eight bits indicate the total number of errored packets to be transmitted when triggered by TIAEI. Error insertion will end after this number of errored packets have been transmitted. A value of FFh results in continuous errored packet insertion at the specified rate.

Register Name: **LI.TEPHC**
 Register Description: **Transmit Errored Packet High Control Register**
 Register Address: **0C7h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | MEIMS | TPER6 | TPER5 | TPER4 | TPER3 | TPER2 | TPER1 | TPER0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Manual Error Insert Mode Select (MEIMS). When 0, the transmit manual error insertion signal (TMEI) will not cause errors to be inserted. When 1, TMEI will cause an error to be inserted when it transitions from 0 to 1. Note: Enabling TMEI does not disable error insertion using TCER[6:0] and TCEN[7:0].

Bits 6 to 0: Transmit Errored Packet Insertion Rate (TPER[6:0]). These seven bits indicate the rate at which errored packets are to be output. One out of every $x * 10^y$ packets is to be an errored packet. TPER[3:0] is the value x, and TPER[6:4] is the value y which has a maximum value of 6. If TPER[3:0] has a value of 0h errored packet insertion is disabled. If TPER[6:4] has a value of 6xh or 7xh the errored packet rate is $x * 10^6$. A TPER[6:0] value of 01h results in every packet being errored. A TPER[6:0] value of 0Fh results in every 15th packet being errored. A TPER[6:0] value of 11h results in every 10th packet being errored.

To initiate automatic error insertion, use the following routine:

- 1) Configure LI.TEPLC and LI.TEPHC for the desired error insertion mode.
- 2) Write the LI.TPPCL.TIAEI bit to 1. Note that this bit is write-only.
- 3) If not using continuous error insertion (LI.TPELC is not equal to FFh), the user should monitor the LI.TPPSR.TEPF bit for completion of the error insertion. If interrupt on completion of error insertion is enabled (LI.TPPSR.TEPFIE = 1), the user only needs to wait for the interrupt condition.
- 4) Proceed with the cleanup routine listed below.

Cleanup routine:

- 1) Write LI.TEPLC and LI.TEPHC each to 00h.
- 2) Write the LI.TPPCL.TIAEI bit to 0.

Register Name: **LI.TPPSR**
 Register Description: **Transmit Packet Processor Status Register**
 Register Address: **0C8h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|-------------|
| Name | — | — | — | — | — | — | — | <u>TEPF</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Transmit Errored Packet Insertion Finished (TEPF). This bit is set when the number of errored packets indicated by the TPEN[7:0] bits in the TEPC register have been transmitted. This bit is cleared when errored packet insertion is disabled, or a new errored packet insertion process is initiated.

Register Name: **LI.TPPSRL**
 Register Description: **Transmit Packet Processor Status Register Latched**
 Register Address: **0C9h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|--------------|
| Name | — | — | — | — | — | — | — | <u>TEPFL</u> |
| Default | | | | | | | | |

Bit 0: Transmit Errored Packet Insertion Finished Latched (TEPFL). This bit is set when the TEPF bit in the TPPSR register transitions from 0 to 1.

Register Name: **LI.TPPSRIE**
 Register Description: **Transmit Packet Processor Status Register Interrupt Enable**
 Register Address: **0CAh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|--------|
| Name | — | — | — | — | — | — | — | TEPFIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Transmit Errored Packet Insertion Finished Interrupt Enable (TEPFIE). This bit enables an interrupt if the TEPFL bit in the LI.TPPSRL register is set.

0 = interrupt disabled

1 = interrupt enabled

Register Name: **LI.TPCR0**
 Register Description: **Transmit Packet Count Byte 0**
 Register Address: **0CCh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Name | <u>TPC7</u> | <u>TPC6</u> | <u>TPC5</u> | <u>TPC4</u> | <u>TPC3</u> | <u>TPC2</u> | <u>TPC1</u> | <u>TPC0</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Packet Count (TPC[7:0]). Eight bits of 24-bit value. Register description below.

Register Name: **LI.TPCR1**
 Register Description: **Transmit Packet Count Byte 1**
 Register Address: **0CDh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| Name | <u>TPC15</u> | <u>TPC14</u> | <u>TPC13</u> | <u>TPC12</u> | <u>TPC11</u> | <u>TPC10</u> | <u>TPC9</u> | <u>TPC8</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Packet Count (TPC[15:8]). Eight bits of 24-bit value. Register description below.

Register Name: **LI.TPCR2**
 Register Description: **Transmit Packet Count Byte 2**
 Register Address: **0CEh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Name | <u>TPC23</u> | <u>TPC22</u> | <u>TPC21</u> | <u>TPC20</u> | <u>TPC19</u> | <u>TPC18</u> | <u>TPC17</u> | <u>TPC16</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Packet Count (TPC[23:16]). These 24 bits indicate the number of packets extracted from the Transmit FIFO and output in the outgoing data stream.

Register Name: **LI.TBCR0**
 Register Description: **Transmit Byte Count Byte 0**
 Register Address: **0D0h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Name | <u>TBC7</u> | <u>TBC6</u> | <u>TBC5</u> | <u>TBC4</u> | <u>TBC3</u> | <u>TBC2</u> | <u>TBC1</u> | <u>TBC0</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Byte Count (TBC[7:0]). Eight bits of 32-bit value. Register description below.

Register Name: **LI.TBCR1**
 Register Description: **Transmit Byte Count Byte 1**
 Register Address: **0D1h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| Name | <u>TBC15</u> | <u>TBC14</u> | <u>TBC13</u> | <u>TBC12</u> | <u>TBC11</u> | <u>TBC10</u> | <u>TBC9</u> | <u>TBC8</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Byte Count (TBC[15:8]). Eight bits of 32-bit value. Register description below.

Register Name: **LI.TBCR2**
 Register Description: **Transmit Byte Count Byte 2**
 Register Address: **0D2h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Name | <u>TBC23</u> | <u>TBC22</u> | <u>TBC21</u> | <u>TBC20</u> | <u>TBC19</u> | <u>TBC18</u> | <u>TBC17</u> | <u>TBC16</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Byte Count (TBC[23:16]). Eight bits of 32-bit value. Register description below.

Register Name: **LI.TBCR3**
 Register Description: **Transmit Byte Count Byte 3**
 Register Address: **0D3h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Name | <u>TBC31</u> | <u>TBC30</u> | <u>TBC29</u> | <u>TBC28</u> | <u>TBC27</u> | <u>TBC26</u> | <u>TBC25</u> | <u>TBC24</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Byte Count (TBC[31:24]). These 32 bits indicate the number of packet bytes inserted in the outgoing data stream.

Register Name: **LI.TMEI**
 Register Description: **Transmit Manual Error Insertion**
 Register Address: **0D4h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|------|
| Name | — | — | — | — | — | — | — | TMEI |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Transmit Manual Error Insertion (TMEI). A 0-to-1 transition inserts a single error in the Transmit direction.

Register Name: **LI.THPMUU**
 Register Description: **Serial Interface Transmit HDLC PMU Update Register**
 Register Address: **0D6h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|-------|
| Name | — | — | — | — | — | — | — | TPMUU |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Transmit PMU Update (TPMUU). This signal causes the transmit cell/packet processor block performance monitoring registers (counters) to be updated. A 0-to-1 transition causes the performance monitoring registers to be updated with the latest data, and the counters reset (0 or 1). This update updates performance monitoring counters for the Serial Interface.

Register Name: **LI.THPMUS**
 Register Description: **Serial Interface Transmit HDLC PMU Update Status Register**
 Register Address: **0D7h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|-------|
| Name | — | — | — | — | — | — | — | TPMUS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Transmit PMU Update Status (TPMUS). This bit is set when the Transmit PMU Update is completed. This bit is cleared when TPMUU is reset.

12.5.4 X.86 Registers

X.86 transmit and common registers are used to control the operation of the X.86 encoder and decoder.

Register Name: **LI.TX86EDE**
 Register Description: **X.86 Encoding Decoding Enable**
 Register Address: **0D8h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|-------|
| Name | — | — | — | — | — | — | — | X86ED |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: X.86 Encoding Decoding (X86ED). If this bit is set to 1, X.86 encoding and decoding is enabled for the Transmit and Receive paths. The MAC Frame is encapsulated in the X.86 Frame for Transmit and the X.86 headers are checked for in the received data. If X.86 functionality is selected, the X.86 receiver byte boundary is provided by the RSYNC signal and the device provides the transmit byte synchronization TSYNC. No HDLC encapsulation is performed.

Register Name: **LI.TRX86A**
 Register Description: **Transmit Receive X.86 Address**
 Register Address: **0D9h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Name | X86TRA7 | X86TRA6 | X86TRA5 | X86TRA4 | X86TRA3 | X86TRA2 | X86TRA1 | X86TRA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

Bits 7 to 0: X86 Transmit Receive Address (X86TRA7 to X86TRA0). This is the address field for the X.86 transmitter and for the receiver. The register default value is 0x04.

Register Name: **LI.TRX8C**
 Register Description: **Transmit Receive X.86 Control**
 Register Address: **0DAh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Name | X86TRC7 | X86TRC6 | X86TRC5 | X86TRC4 | X86TRC3 | X86TRC2 | X86TRC1 | X86TRC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

Bits 7 to 0: X86 Transmit Receive Control (X86TRC7 to X86TRC0). This is the control field for the X.86 transmitter and expected value for the receiver. The register is reset to 0x03

Register Name: **LI.TRX86SAPIH**
 Register Description: **Transmit Receive X.86 SAPIH**
 Register Address: **0DBh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Name | TRSAPIH7 | TRSAPIH6 | TRSAPIH5 | TRSAPIH4 | TRSAPIH3 | TRSAPIH2 | TRSAPIH1 | TRSAPIH0 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

Bits 7 to 0: X86 Transmit Receive Address (TRSAPIH7 to TRSAPIH0). This is the address field for the X.86 transmitter and expected for the receiver. The register is reset to 0xfe.

Register Name: **LI.TRX86SAPIL**
 Register Description: **Transmit Receive X.86 SAPIL**
 Register Address: **0DCh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Name | TRSAPIL7 | TRSAPIL6 | TRSAPIL5 | TRSAPIL4 | TRSAPIL3 | TRSAPIL2 | TRSAPIL1 | TRSAPIL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Bits 7 to 0: X86 Transmit Receive Control (TRSAPIL7 to TRSAPIL0). This is the address field for the X.86 transmitter and expected value for the receiver. The register is reset to 0x01

Register Name: **LI.CIR**
 Register Description: **Committed Information Rate**
 Register Address: **0DDh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CIRE | CIR6 | CIR5 | CIR4 | CIR3 | CIR2 | CIR1 | CIR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Bit 7: Committed Information Rate Enable (CIRE). Set this bit to 1 to enable the Committed Information Rate Controller feature.

Bits 6 to 0: Committed Information Rate (CIR6 to CIR0). These bits provide the value for the committed information rate. The value is multiplied by 500kbps to get the CIR value. The user must ensure that the CIR value is less than or equal to the maximum Serial Interface transmit rate. The valid range is from 1 to 104. Any values outside this range will result in unpredictable behavior. Note that a value of 104 translates to a 52Mbps line rate. Hence if the CIR is above the line rate, the rate is not restricted by the CIR. For instance, if using a T1 line and the CIR is programmed with a value of 104, it has no effect in restricting the rate.

12.5.5 Receive Serial Interface

Serial Receive Registers are used to control the HDLC Receiver associated with each Serial Interface. Note that throughout this document HDLC Processor is also referred to as “Packet Processor.” The receive packet processor block has 17 registers.

Register Name: **LI.RPPCL**
 Register Description: **Receive Packet Processor Control Low Register**
 Register Address: **101h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|------|------|-----|------|------|
| Name | — | — | RFPD | RF16 | RFED | RDD | RBRE | RCCE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Receive FCS Processing Disable (RFPD). When equal to 0, FCS processing is performed and FCS is appended to packets. When set to 1, FCS processing is disabled (the packets do not have an FCS appended). In X.86 mode, FCS processing is always enabled.

Bit 4: Receive FCS-16 Enable (RF16). When 0, the error checking circuit uses a 32-bit FCS. When 1, the error checking circuit uses a 16-bit FCS. This bit is ignored when FCS processing is disabled. In X.86 mode, the FCS is always 32 bits.

Bit 3: Receive FCS Extraction Disable (RFED). When 0, the FCS bytes are discarded. When 1, the FCS bytes are passed on. This bit is ignored when FCS processing is disabled. In X.86 mode, FCS bytes are discarded.

Bit 2: Receive Descrambling Disable (RDD). When equal to 0, $X^{43} + 1$ descrambling is performed. When set to 1, descrambling is disabled.

Bit 1: Receive Bit Reordering Enable (RBRE). When equal to 0, reordering is disabled and the first bit received is expected to be the MSB DT [7] of the byte. When set to 1, bit reordering is enabled and the first bit received is expected to be the LSB DT [0] of the byte. Note that function is controlled by the BREO in Hardware Mode.

Bit 0: Receive Clear Channel Enable (RCCE). When equal to 0, packet processing is enabled. When set to 1, the device is in clear channel mode and all packet-processing functions except descrambling and bit reordering are disabled.

Register Name: **LI.RMPSCCL**
 Register Description: **Receive Maximum Packet Size Control Low Register**
 Register Address: **102h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | RMX7 | RMX6 | RMX5 | RMX4 | RMX3 | RMX2 | RMX1 | RMX0 |
| Default | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Maximum Packet Size (RMX[7:0]). Eight bits of a 16-bit value. Register description below.

Register Name: **LI.RMPSCH**
 Register Description: **Receive Maximum Packet Size Control High Register**
 Register Address: **103h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|------|------|
| Name | RMX15 | RMX14 | RMX13 | RMX12 | RMX11 | RMX10 | RMX9 | RMX8 |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

Bits 7 to 0: Receive Maximum Packet Size (RMX[15:8]) These 16 bits indicate the maximum allowable packet size in bytes. The size includes the FCS bytes, but excludes bit/byte stuffing. Note: If the maximum packet size is less than the minimum packet size, all packets are discarded. When packet processing is disabled, these sixteen bits indicate the "packet" size the incoming data is to be broken into.

The maximum packet size allowable is 2016 bytes plus the FCS bytes. Any values programmed that are greater than 2016 + FCS will have the same effect as 2016+ FCS value.

In X.86 mode, the X.86 encapsulation bytes are included in maximum size control.

Register Name: **LI.RPPSR**
 Register Description: **Receive Packet Processor Status Register**
 Register Address: **104h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|------|------|------|
| Name | — | — | | — | | REPC | RAPC | RSPC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2: Receive FCS Errored Packet Count (REPC). This read-only bit indicates that the receive FCS errored packet count is non-zero.

Bit 1: Receive Aborted Packet Count (RAPC). This read-only bit indicates that the receive aborted packet count is non-zero.

Bit 0: Receive Size Violation Packet Count (RSPC). This read-only bit indicates that the receive size violation packet count is non-zero.

Register Name: **LI.RPPSRL**
 Register Description: **Receive Packet Processor Status Register Latched**
 Register Address: **105h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Name | <u>REPL</u> | <u>RAPL</u> | <u>RIPDL</u> | <u>RSPDL</u> | <u>RLPDL</u> | <u>REPCL</u> | <u>RAPCL</u> | <u>RSPCL</u> |
| Default | — | — | — | — | — | — | — | — |

Bit 7: Receive FCS Errored Packet Latched (REPL). This bit is set when a packet with an errored FCS is detected.

Bit 6: Receive Aborted Packet Latched (RAPL). This bit is set when a packet with an abort indication is detected.

Bit 5: Receive Invalid Packet Detected Latched (RIPDL). This bit is set when a packet with a non-integer number of bytes is detected.

Bit 4: Receive Small Packet Detected Latched (RSPDL). This bit is set when a packet smaller than the minimum packet size is detected.

Bit 3: Receive Large Packet Detected Latched (RLPDL). This bit is set when a packet larger than the maximum packet size is detected.

Bit 2: Receive FCS Errored Packet Count Latched (REPCL). This bit is set when the REPC bit in the RPPSR register transitions from zero to one.

Bit 1: Receive Aborted Packet Count Latched (RAPCL). This bit is set when the RAPC bit in the RPPSR register transitions from zero to one.

Bit 0: Receive Size Violation Packet Count Latched (RSPCL). This bit is set when the RSPC bit in the RPPSR register transitions from zero to one.

Register Name: **LI.RPPSRIE**
 Register Description: **Receive Packet Processor Status Register Interrupt Enable**
 Register Address: **106h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|--------|--------|--------|--------|--------|--------|
| Name | REPIE | RAPIE | RIPDIE | RSPDIE | RLPDIE | REPCIE | RAPCIE | RSPCIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive FCS Errored Packet Interrupt Enable (REPIE). This bit enables an interrupt if the REPL bit in the [LI.RPPSRL](#) register is set.

0 = interrupt disabled
 1 = interrupt enabled

Bit 6: Receive Aborted Packet Interrupt Enable (RAPIE). This bit enables an interrupt if the RAPL bit in the LI.RPPSRL register is set.

0 = interrupt disabled
 1 = interrupt enabled

Bit 5: Receive Invalid Packet Detected Interrupt Enable (RIPDIE). This bit enables an interrupt if the RIPDL bit in the LI.RPPSRL register is set.

0 = interrupt disabled
 1 = interrupt enabled

Bit 4: Receive Small Packet Detected Interrupt Enable (RSPDIE). This bit enables an interrupt if the RSPDL bit in the LI.RPPSRL register is set.

0 = interrupt disabled
 1 = interrupt enabled

Bit 3: Receive Large Packet Detected Interrupt Enable (RLPDIE) This bit enables an interrupt if the RLPDL bit in the LI.RPPSRL register is set.

0 = interrupt disabled
 1 = interrupt enabled

Bit 2: Receive FCS Errored Packet Count Interrupt Enable (REPCIE). This bit enables an interrupt if the REPC bit in the LI.RPPSRL register is set. Must be set low when the packets do not have an FCS appended.

0 = interrupt disabled
 1 = interrupt enabled

Bit 1: Receive Aborted Packet Count Interrupt Enable (RAPCIE). This bit enables an interrupt if the RAPCL bit in the LI.RPPSRL register is set.

0 = interrupt disabled
 1 = interrupt enabled

Bit 0: Receive Size Violation Packet Count Interrupt Enable (RSPCIE). This bit enables an interrupt if the RSPCL bit in the LI.RPPSRL register is set.

0 = interrupt disabled
 1 = interrupt enabled

Register Name: **LI.RPCB0**
 Register Description: **Receive Packet Count Byte 0 Register**
 Register Address: **108h**

| | | | | | | | | |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | <u>RPC7</u> | <u>RPC6</u> | <u>RPC5</u> | <u>RPC4</u> | <u>RPC3</u> | <u>RPC2</u> | <u>RPC1</u> | <u>RPC0</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Packet Count (RPC[7:0]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RPCB1**
 Register Description: **Receive Packet Count Byte 1 Register**
 Register Address: **109h**

| | | | | | | | | |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | <u>RPC15</u> | <u>RPC14</u> | <u>RPC13</u> | <u>RPC12</u> | <u>RPC11</u> | <u>RPC10</u> | <u>RPC09</u> | <u>RPC08</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Packet Count (RPC[15:8]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RPCB2**
 Register Description: **Receive Packet Count Byte 2 Register**
 Register Address: **10Ah**

| | | | | | | | | |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | <u>RPC23</u> | <u>RPC22</u> | <u>RPC21</u> | <u>RPC20</u> | <u>RPC19</u> | <u>RPC18</u> | <u>RPC17</u> | <u>RPC16</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Packet Count (RPC[23:16]). These 24 bits indicate the number of packets stored in the receive FIFO without an abort indication. Note: Packets discarded due to system loopback or an overflow condition are included in this count. This register is valid when clear channel is enabled.

Register Name: **LI.RFPCB0**
 Register Description: **Receive FCS Errored Packet Count Byte 0 Register**
 Register Address: **10Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Name | <u>RFPC7</u> | <u>RFPC6</u> | <u>RFPC5</u> | <u>RFPC4</u> | <u>RFPC3</u> | <u>RFPC2</u> | <u>RFPC1</u> | <u>RFPC0</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive FCS Errored Packet Count (RFPC[7:0]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RFPCB1**
 Register Description: **Receive FCS Errored Packet Count Byte 1 Register**
 Register Address: **10Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| Name | <u>RFPC15</u> | <u>RFPC14</u> | <u>RFPC13</u> | <u>RFPC12</u> | <u>RFPC11</u> | <u>RFPC10</u> | <u>RFPC9</u> | <u>RFPC8</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive FCS Errored Packet Count (RFPC[15:8]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RFPCB2**
 Register Description: **Receive FCS Errored Packet Count Byte 2 Register**
 Register Address: **10Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Name | <u>RFPC23</u> | <u>RFPC22</u> | <u>RFPC21</u> | <u>RFPC20</u> | <u>RFPC19</u> | <u>RFPC18</u> | <u>RFPC17</u> | <u>RFPC16</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive FCS Errored Packet Count (RFPC[23:16]). These 24 bits indicate the number of packets received with an FCS error. The byte count for these packets is included in the receive aborted byte count register REBCR.

Register Name: **LI.RAPCB0**
 Register Description: **Receive Aborted Packet Count Byte 0 Register**
 Register Address: **110h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Name | <u>RAPC7</u> | <u>RAPC6</u> | <u>RAPC5</u> | <u>RAPC4</u> | <u>RAPC3</u> | <u>RAPC2</u> | <u>RAPC1</u> | <u>RAPC0</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Aborted Packet Count (RAPC [7:0]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RAPCB1**
 Register Description: **Receive Aborted Packet Count Byte 1 Register**
 Register Address: **111h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| Name | <u>RAPC15</u> | <u>RAPC14</u> | <u>RAPC13</u> | <u>RAPC12</u> | <u>RAPC11</u> | <u>RAPC10</u> | <u>RAPC9</u> | <u>RAPC8</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Aborted Packet Count (RAPC[15:8]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RAPCB2**
 Register Description: **Receive Aborted Packet Count Byte 2 Register**
 Register Address: **112h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Name | <u>RAPC23</u> | <u>RAPC22</u> | <u>RAPC21</u> | <u>RAPC20</u> | <u>RAPC19</u> | <u>RAPC18</u> | <u>RAPC17</u> | <u>RAPC16</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Aborted Packet Count (RAPC[23:16]). The 24-bit value from these three registers indicates the number of packets received with a packet abort indication. The byte count for these packets is included in the receive aborted byte count register REBCR.

Register Name: **LI.RSPCB0**
 Register Description: **Receive Size Violation Packet Count Byte 0 Register**
 Register Address: **114h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Name | <u>RSPC7</u> | <u>RSPC6</u> | <u>RSPC5</u> | <u>RSPC4</u> | <u>RSPC3</u> | <u>RSPC2</u> | <u>RSPC1</u> | <u>RSPC0</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Size Violation Packet Count (RSPC[7:0]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RSPCB1**
 Register Description: **Receive Size Violation Packet Count Byte 1 Register**
 Register Address: **115h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| Name | <u>RSPC15</u> | <u>RSPC14</u> | <u>RSPC13</u> | <u>RSPC12</u> | <u>RSPC11</u> | <u>RSPC10</u> | <u>RSPC9</u> | <u>RSPC8</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Size Violation Packet Count (RSPC[15:8]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RSPCB2**
 Register Description: **Receive Size Violation Packet Count Byte 2 Registers**
 Register Address: **116h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Name | <u>RSPC23</u> | <u>RSPC22</u> | <u>RSPC21</u> | <u>RSPC20</u> | <u>RSPC19</u> | <u>RSPC18</u> | <u>RSPC17</u> | <u>RSPC16</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Size Violation Packet Count (RSPC[23:16]). These 24 bits indicate the number of packets received with a packet size violation (below minimum, above maximum, or non-integer number of bytes). The byte count for these packets is included in the receive aborted byte count register REBCR.

Register Name: **LI.RBC0**
 Register Description: **Receive Byte Count 0 Register**
 Register Address: **118h**

| | | | | | | | | |
|---------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | <u>RBC7</u> | <u>RBC6</u> | <u>RBC5</u> | <u>RBC4</u> | <u>RBC3</u> | <u>RBC2</u> | <u>RBC1</u> | <u>RBC0</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Byte Count (RBC[7:0]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RBC1**
 Register Description: **Receive Byte Count 1 Register**
 Register Address: **119h**

| | | | | | | | | |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | <u>RBC15</u> | <u>RBC14</u> | <u>RBC13</u> | <u>RBC12</u> | <u>RBC11</u> | <u>RBC10</u> | <u>RBC9</u> | <u>RBC8</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Byte Count (RBC[15:8]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RBC2**
 Register Description: **Receive Byte Count 2 Register**
 Register Address: **11Ah**

| | | | | | | | | |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | <u>RBC23</u> | <u>RBC22</u> | <u>RBC21</u> | <u>RBC20</u> | <u>RBC19</u> | <u>RBC18</u> | <u>RBC17</u> | <u>RBC16</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Byte Count (RBC[23:16]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RBC3**
 Register Description: **Receive Byte Count 3 Register**
 Register Address: **11Bh**

| | | | | | | | | |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | <u>RBC31</u> | <u>RBC30</u> | <u>RBC29</u> | <u>RBC28</u> | <u>RBC27</u> | <u>RBC26</u> | <u>RBC25</u> | <u>RBC24</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Byte Count (RBC[31:24]). These 32 bits indicate the number of bytes contained in packets stored in the receive FIFO without an abort indication. Note: Bytes discarded due to FCS extraction, system loopback, FIFO reset, or an overflow condition may be included in this count.

Register Name: **LI.RAC0**
 Register Description: **Receive Aborted Byte Count 0 Register**
 Register Address: **11Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Name | <u>REBC7</u> | <u>REBC6</u> | <u>REBC5</u> | <u>REBC4</u> | <u>REBC3</u> | <u>REBC2</u> | <u>REBC1</u> | <u>REBC0</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Aborted Byte Count (RBC[7:0]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RAC1**
 Register Description: **Receive Aborted Byte Count 1 Register**
 Register Address: **11Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| Name | <u>REBC15</u> | <u>REBC14</u> | <u>REBC13</u> | <u>REBC12</u> | <u>REBC11</u> | <u>REBC10</u> | <u>REBC9</u> | <u>REBC8</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Aborted Byte Count (RBC[15:8]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RAC2**
 Register Description: **Receive Aborted Byte Count 2 Register**
 Register Address: **11Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Name | <u>REBC23</u> | <u>REBC22</u> | <u>REBC21</u> | <u>REBC20</u> | <u>REBC19</u> | <u>REBC18</u> | <u>REBC17</u> | <u>REBC16</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Aborted Byte Count (RBC[23:16]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RAC3**
 Register Description: **Receive Aborted Byte Count 3 Register**
 Register Address: **11Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Name | <u>REBC31</u> | <u>REBC30</u> | <u>REBC29</u> | <u>REBC28</u> | <u>REBC27</u> | <u>REBC26</u> | <u>REBC25</u> | <u>REBC24</u> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Aborted Byte Count (REBC[31:24]). These 32 bits indicate the number of bytes contained in packets stored in the receive FIFO with an abort indication. Note: Bytes discarded due to FCS extraction, system loopback, FIFO reset, or an overflow condition may be included in this count.

Register Name: **LI.RHPMUU**
 Register Description: **Serial Interface Receive HDLC PMU Update Register**
 Register Address: **120h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|-------|
| Name | — | — | — | — | — | — | — | RPMUU |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Receive PMU Update (RPMUU). This signal causes the receive cell/packet processor block performance monitoring registers to be updated. A 0 to 1 transition causes the performance monitoring registers to be updated with the latest data, and resets the associated counters. This bit updates performance monitoring counters for the Serial Interface.

Register Name: **LI.RHPMUS**
 Register Description: **Serial Interface Receive HDLC PMU Update Status Register**
 Register Address: **121h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|--------|
| Name | — | — | — | — | — | — | — | RPMUUS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Receive PMU Update Status (RPMUUS). This bit is set when the Transmit PMU Update is completed. This bit is cleared when RPMUU is set to 0.

Register Name: **LI.RX86S**
 Register Description: **Receive X.86 Latched Status Register**
 Register Address: **122h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---------|---------|-----|-----|
| Name | — | — | — | — | SAPIHNE | SAPILNE | CNE | ANE |
| Default | — | — | — | — | — | — | — | — |

Bit 3: SAPI High Not Equal to [LI.TRX86SAPIH](#) Latched Status (SAPIHNE). This latched status bit is set if SAPIH is not equal to LI.TRX86SAPIH. This latched status bit is cleared upon read.

Bit 2: SAPI Low Not Equal to [LI.TRX86SAPIL](#) Latched Status (SAPILNE). This latched status bit is set if SAPIL is not equal to LI.TRX86SAPIL. This latched status bit is cleared upon read.

Bit 1: Control Not Equal to [LI.TRX8C](#) (CNE). This latched status bit is set if the control field is not equal to LI.TRX8C. This latched status bit is cleared upon read.

Bit 0: Address Not Equal to [LI.TRX86A](#) (ANE). This latched status bit is set if the X.86 Address field is not equal to LI.TRX86A. This latched status bit is cleared upon read.

Register Name: **LI.RX86LSIE**
 Register Description: **Receive X.86 Interrupt Enable**
 Register Address: **123h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------------|------------|---------|--------|
| Name | — | — | — | — | SAPINE01IM | SAPINEFEIM | CNE3LIM | ANE4IM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: SAPI Octet Not Equal to [LI.TRX86SAPIH](#) Interrupt Enable (SAPINE01IM). If this bit is set to 1, LI.RX86S.SAPIHNE generates an interrupt.

Bit 2: SAPI Octet Not Equal to [LI.TRX86SAPIL](#) Interrupt Enable (SAPINEFEIM). If this bit is set to 1, LI.RX86S.SAPILNE generates an interrupt.

Bit 1: Control Not Equal to [LI.TRX8C](#) Interrupt Enable (CNE3LIM). If this bit is set to 1, LI.RX86S.CNE generates an interrupt.

Bit 0: Address Not Equal to [LI.TRX86A](#) Interrupt Enable (ANE4IM). If this bit is set to 1, LI.RX86S.ANE generates an interrupt.

Register Name: **LI.TQLT**
 Register Description: **Serial Interface Transmit Queue Low Threshold (Watermark)**
 Register Address: **124h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TQLT7 | TQLT6 | TQLT5 | TQLT4 | TQLT3 | TQLT2 | TQLT1 | TQLT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Queue Low Threshold (TQLT[7:0]). The transmit queue low threshold for the connection, in increments of 32 packets of 2048 bytes each. The value of this register is multiplied by 32 x 2048 bytes to determine the byte location of the threshold. Note that the transmit queue is for data that was received from the Serial Interface to be sent to the Ethernet Interface.

Register Name: **LI.TQHT**
 Register Description: **Serial Interface Transmit Queue High Threshold (Watermark)**
 Register Address: **125h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TQHT7 | TQHT6 | TQHT5 | TQHT4 | TQHT3 | TQHT2 | TQHT1 | TQHT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Queue High Threshold (TQHT[7:0]). The transmit queue high threshold for the connection, in increments of 32 packets of 2048 bytes each. The value of this register is multiplied by 32 x 2048 bytes to determine the byte location of the threshold. Note that the transmit queue is for data that was received from the Serial Interface to be sent to the Ethernet Interface.

Register Name: **LI.TQTIE**
 Register Description: **Serial Interface Transmit Queue Cross Threshold Interrupt Enable**
 Register Address: **126h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|---------|---------|--------|--------|
| Name | --- | --- | --- | --- | TFOVFIE | TQOVFIE | TQHTIE | TQLTIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: Transmit FIFO Overflow for Connection Interrupt Enable (TFOVFIE). If this bit is set, the watermark interrupt is enabled for TFOVFLS.

Bit 2: Transmit Queue Overflow for Connection Interrupt Enable (TQOVFIE). If this bit is set, the watermark interrupt is enabled for TQOVFLS.

Bit 1: Transmit Queue for Connection High Threshold Interrupt Enable (TQHTIE). If this bit is set, the watermark interrupt is enabled for TQHTS.

Bit 0: Transmit Queue for Connection Low Threshold Interrupt Enable (TQLTIE). If this bit is set, the watermark interrupt is enabled for TQLTS.

Register Name: **LI.TQCTLS**
 Register Description: **Serial Interface Transmit Queue Cross Threshold Latched Status**
 Register Address: **127h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|---------|---------|--------|--------|
| Name | --- | --- | --- | --- | TFOVFLS | TQOVFLS | TQHTLS | TQLTLS |
| Default | --- | --- | --- | --- | --- | --- | --- | --- |

Bit 3: Transmit Queue FIFO Overflowed Latched Status (TFOVFLS). This bit is set if the transmit queue FIFO has overflowed. This register is cleared after a read. This FIFO is for data to be transmitted from the HDLC to be sent to the SDRAM.

Bit 2: Transmit Queue Overflow Latched Status (TQOVFLS). This bit is set if the transmit queue has overflowed. This register is cleared after a read.

Bit 1: Transmit Queue for Connection Exceeded High Threshold Latched Status (TQHTLS). This bit is set if the transmit queue crosses the high watermark. This register is cleared after a read.

Bit 0: Transmit Queue for Connection Exceeded Low Threshold Latched Status (TQLTLS). This bit is set if the transmit queue crosses the low watermark. This register is cleared after a read.

12.6 Ethernet Interface Registers

The Ethernet Interface registers are used to configure RMII/MII bus operation and establish the MAC parameters as required by the user. The MAC Registers cannot be addressed directly from the processor port. The registers below are used to perform indirect read or write operations to the MAC registers. The MAC Status Registers are shown in [Table 12-6](#). Accessing the MAC Registers is described in Section [9.13](#).

12.6.1 Ethernet Interface Register Bit Descriptions

Register Name: **SU.MACRADL**
 Register Description: **MAC Read Address Low Register**
 Register Address: **140h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | MACRA7 | MACRA6 | MACRA5 | MACRA4 | MACRA3 | MACRA2 | MACRA1 | MACRA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Read Address (MACRA7 to MACRA0). Low byte of the MAC address. Used only for read operations.

Register Name: **SU.MACRADH**
 Register Description: **MAC Read Address High Register**
 Register Address: **141h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|--------|--------|
| Name | MACRA15 | MACRA14 | MACRA13 | MACRA12 | MACRA11 | MACRA10 | MACRA9 | MACRA8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Read Address (MACRA15 to MACRA0). High byte of the MAC address. Used only for read operations.

Register Name: **SU.MACRD0**
 Register Description: **MAC Read Data Byte 0**
 Register Address: **142h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | MACRD7 | MACRD6 | MACRD5 | MACRD4 | MACRD3 | MACRD2 | MACRD1 | MACRD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Read Data 0 (MACRD7 to MACRD0). One of four bytes of data read from the MAC. Valid after a read command has been issued and the [SU.MACRWC.MCS](#) bit is zero.

Register Name: **SU.MACRD1**
 Register Description: **MAC Read Data Byte 1**
 Register Address: **143h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|--------|--------|
| Name | MACRD15 | MACRD14 | MACRD13 | MACRD12 | MACRD11 | MACRD10 | MACRD9 | MACRD8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Read Data 1 (MACRD15 to MACRD0). One of four bytes of data read from the MAC. Valid after a read command has been issued and the [SU.MACRWC.MCS](#) bit is zero.

Register Name: **SU.MACRD2**
 Register Description: **MAC Read Data Byte 2**
 Register Address: **144h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Name | MACRD23 | MACRD22 | MACRD21 | MACRD20 | MACRD19 | MACRD18 | MACRD17 | MACRD16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Read Data 2 (MACRD23 to MACRD16). One of four bytes of data read from the MAC. Valid after a read command has been issued and the [SU.MACRWC](#).MCS bit is zero.

Register Name: **SU.MACRD3**
 Register Description: **MAC Read Data Byte 3**
 Register Address: **145h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Name | MACRD31 | MACRD30 | MACRD29 | MACRD28 | MACRD27 | MACRD26 | MACRD25 | MACRD24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Read Data 3 (MACRD31 to MACRD24). One of four bytes of data read from the MAC. Valid after a read command has been issued and the [SU.MACRWC](#).MCS bit is zero.

Register Name: **SU.MACWD0**
 Register Description: **MAC Write Data 0**
 Register Address: **146h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | MACWD7 | MACWD6 | MACWD5 | MACWD4 | MACWD3 | MACWD2 | MACWD1 | MACWD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Write Data 0 (MACWD7 to MACWD0). One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the [SU.MACRWC](#).MCS bit is zero.

Register Name: **SU.MACWD1**
 Register Description: **MAC Write Data 1**
 Register Address: **147h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Name | MACWD15 | MACWD14 | MACWD13 | MACWD12 | MACWD11 | MACWD10 | MACWD09 | MACWD08 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Write Data 1 (MACWD15 to MACWD8). One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the [SU.MACRWC](#).MCS bit is zero.

Register Name: **SU.MACWD2**
 Register Description: **MAC Write Data 2**
 Register Address: **148h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Name | MACWD23 | MACWD22 | MACWD21 | MACWD20 | MACWD19 | MACWD18 | MACWD17 | MACWD16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Write Data 2 (MACWD23 to MACWD16). One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the [SU.MACRWC](#).MCS bit is zero.

Register Name: **SU.MACWD3**
 Register Description: **MAC Write Data 3**
 Register Address: **149h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | MACD31 | MACD30 | MACD29 | MACD28 | MACD27 | MACD26 | MACD25 | MACD24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Write Data 3 (MACD31 to MACD24). One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the [SU.MACRWC.MCS](#) bit is zero.

Register Name: **SU.MACAWL**
 Register Description: **MAC Address Write Low**
 Register Address: **14Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | MACAW7 | MACAW6 | MACAW5 | MACAW4 | MACAW3 | MACAW2 | MACAW1 | MACAW0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Write Address (MACAW7 to MACAW0). Low byte of the MAC address. Used only for write operations.

Register Name: **SU.MACAWH**
 Register Description: **MAC Address Write High**
 Register Address: **14Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | MACAW1 | MACAW1 | MACAW1 | MACAW1 | MACAW1 | MACAW1 | MACAW9 | MACAW8 |
| | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: MAC Write Address (MACAW15 to MACAW8). High byte of the MAC address. Used only for write operations.

Register Name: **SU.MACRWC**
 Register Description: **MAC Read Write Command Status**
 Register Address: **14Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|------|-----|
| Name | — | — | — | — | — | — | MCRW | MCS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 1: MAC Command RW (MCRW). If this bit is written to 1, a read is performed from the MAC. If this bit is written to 0, a write operation is performed. Address information for write operations must be located in [SU.MACAWH](#) and [SU.MACAWL](#). Address information for read operations must be located in [SU.MACRADH](#) and [SU.MACRADL](#). The user must also write a 1 to the MCS bit, and the device will clear MCS when the operation is complete.

Bit 0: MAC Command Status (MCS). Setting MCS in conjunction with MCRW will initiate a read or write to the MAC registers. Upon completion of the read or write this bit is cleared. Once a read or write command has been initiated the host must poll this bit to see when the operation is complete.

Register Name: **SU.LPBK**
 Register Description: **Ethernet Interface Loopback Control Register**
 Register Address: **14Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|-----|
| Name | — | — | — | — | — | — | — | QLP |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Queue Loopback Enable (QLP). If this bit is set to 1, data from the Ethernet Interface receive queue is looped back to the transmit queue. Buffered data from the serial interface will remain until the loopback is removed.

Register Name: **SU.GCR**
 Register Description: **Ethernet Interface General Control Register**
 Register Address: **150h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|--------|------|
| Name | — | — | — | — | CRCS | H10S | ATFLOW | JAME |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Bit 3: CRCS. If this bit is zero (default), the received MAC or Ethernet Frame CRC is stripped before the data is encapsulated and transmitted on the serial interface. Data received from the serial interface is decapsulated, a CRC is recalculated and appended to the packet for transmission to the Ethernet interface. If this bit is set to 1, the CRC is not stripped from received packets prior to encapsulation and transmission to the serial interface, and data received from the serial interface is decapsulated directly. No CRC recalculation is performed on data received from the serial interface. Note that the maximum packet size supported by the Ethernet interface is still 2016 (this includes the 4 bytes of CRC).

Bit 2: H10S This bit controls the 10/100 selection for RMII and DCE Mode. **When in RMII mode**, setting this bit to 1 will cause the MAC will operate at 100 Mbps and setting this bit to zero will cause the MAC to operate at 10 Mbps. **When in DCE mode**, the bit function is inverted – setting this bit to 1 will cause the MAC to operate at 10 Mbps. In DTE and MII mode, the MAC determines the data rate from the incoming TX_CLK and RX_CLK.

Bit 1: Automatic Flow Control Enable (ATFLOW). If this bit is set to 1, automatic flow control is enabled based on the connection receive queue size and high watermarks. Pause frames are sent automatically in full duplex mode. The pause time must be programmed through [SU.MACFCR](#). The jam sequence will not be sent automatically in half duplex mode unless the JAME bit is set. This bit is applicable only in software mode.

Bit 0: Jam Enable (JAME.) If this bit is set to 1, a Jam sequence is sent for a duration of 4 bytes. This function is only valid in half duplex mode, and will only function if Automatic Flow Control is disabled. Note that if the receive queue size is less than receive high threshold, setting a JAME will JAM one received frame. If JAME is set and the receiver queue size is higher than the high threshold, all received frames are jammed until the queue empties below the threshold.

Note that [SU.GCR](#) is only valid in the software mode. In hardware mode, pins are used to control Automatic flow control and 100/10-speed selection.

Register Name: **SU.TFRC**
 Register Description: **Transmit Frame Resend Control**
 Register Address: **151h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|--------|--------|-------|
| Name | — | — | — | — | NCFQ | TPDFCB | TPRHBC | TPRCB |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: No Carrier Queue Flush Bar (NCFQ). If this bit is set to 1, the queue for data passing from Serial Interface to Ethernet Interface will not be flushed when loss of carrier is detected.

Bit 2: Transmit Packet Deferred Fail Control Enable (TPDFCB). If this bit is set to 1, the current frame is transmitted immediately instead of being deferred. If this bit is set to 0, the frame is deferred if CRS is asserted and sent when the CRS is unasserted indicating the media is idle.

Bit 1: Transmit Packet HB Fail Control Bar (TPRHBC). If this bit is set to 1, the current frame will not be retransmitted if a heartbeat failure is detected.

Bit 0: Transmit Packet Resend Control Bar (TPRCB). If this bit is set to 1, the current frame will not be retransmitted if any of the following errors have occurred:

- Jabber timeout
- Loss of carrier
- Excessive deferral
- Late collision
- Excessive collisions
- Under run
- Collision

Note that blocking retransmission due to collision (applicable in MII/Half Duplex Mode) can result in unpredictable system level behavior.

Register Name: **SU.TFSL**
 Register Description: **Transmit Frame Status Low**
 Register Address: **152h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|-----|-----|---|--------|
| Name | UR | EC | LC | ED | LOC | NOC | — | FABORT |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Under Run (UR). When this bit is set to 1, the frame was aborted due to a data under run condition of the transmit buffer.

Bit 6: Excessive Collisions (EC). When this bit is set to 1, a frame has been aborted after 16 successive collisions while attempting to transmit the current frame. If the Disable Retry bit is set to 1, then Excessive Collisions will be set to 1 after the first collision.

Bit 5: Late Collision (LC). When this bit is set to 1, a frame was aborted by collision after the 64 bit collision window. Not valid if an under run has occurred.

Bit 4: Excessive Deferral (ED). When this bit is set to 1, a frame was aborted due to excessive deferral.

Bit 3: Loss Of Carrier (LOC). When this bit is set to 1, a frame was aborted due to loss of carrier for one or more bit times. Valid only for non-collided frames. Valid only in half-duplex operation.

Bit 2: No Carrier (NOC). When this bit is set to 1, a frame was aborted because no carrier was found for transmission.

Bit 1: Reserved.

Bit 0: Frame Abort (FABORT). When this bit is set to 1, the MAC has aborted a frame for one of the above reasons. When this bit is clear, the previous frame has been transmitted successfully.

Register Name: **SU.TFSH**
 Register Description: **Transmit Frame Status High**
 Register Address: **153h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|-----|-----|-----|-----|-----|-----|-----|
| Name | PR | HBF | CC3 | CC2 | CC1 | CC0 | LCO | DEF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Packet Resend (PR). When this bit is set, the current packet must be retransmitted due to a collision.

Bit 6: Heartbeat Failure (HBF). When this bit is set, the device failed to detect a heart beat after transmission. This bit is not valid if an under run has occurred.

Bits 5 to 2: Collision Count (CC3 to CC0). These four bits indicate the number of collisions that occurred prior to successful transmission of the previous frame. Not valid if Excessive Collisions is set to 1.

Bit 1: Late Collision (LCO). When set to 1, the MAC observed a collision after the 64-byte collision window.

Bit 0: Deferred Frame (DEF). When set to 1, the current frame was deferred due to carrier assertion by another node after being ready to transmit.

Register Name: **SU.RFSB0**
 Register Description: **Receive Frame Status Byte 0**
 Register Address: **154h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | FL7 | FL6 | FL5 | FL4 | FL3 | FL2 | FL1 | FL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Frame Length (FL[7:0]). These eight bits are the low byte of the length (in bytes) of the received frame, with FCS and Padding. If Automatic Pad Stripping is enabled, this value is the length of the received packet without PCS or Pad bytes. The upper six bits are contained in SU.RFSB1.

Register Name: **SU.RFSB1**
 Register Description: **Receive Frame Status Byte 1**
 Register Address: **155h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|------|------|------|------|-----|-----|
| Name | RF | WT | FL13 | FL12 | FL11 | FL10 | FL9 | FL8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Runt Frame (RF). This bit is set to 1 if the received frame was altered by a collision or terminated within the collision window.

Bit 6: Watchdog Timeout (WT). This bit is set to 1 if a packet receive time exceeds 2048 byte times. After 2048 byte times the receiver is disabled and the received frame will fail CRC check.

Bits 5 to 0: Frame Length (FL[13:8]). These six bits are the upper bits of the length (in bytes) of the received frame, with FCS and Padding. If Automatic Pad Stripping is enabled, this value is the length of the received packet without PCS or Pad bytes.

Register Name: **SU.RFSB2**
 Register Description: **Receive Frame Status Byte 2**
 Register Address: **156h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|----|------|----|----|-----|
| Name | — | — | CRCE | DB | MIIE | FT | CS | FTL |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: CRC Error (CRCE). This bit is set to 1 if the received frame does not contain a valid CRC value.

Bit 4: Dribbling Bit (DB). This bit is set to 1 if the received frame contains a non-integer multiple of 8 bits. It does not indicate that the frame is invalid. This bit is not valid for runt or collided frames.

Bit 3: MII Error (MIIE). This bit is set to 1 if an error was found on the MII bus.

Bit 2: Frame Type (FT). This bit is set to 1 if the received frame exceeds 1536 bytes. It is equal to zero if the received frame is an 802.3 frame. This bit is not valid for runt frames.

Bit 1: Collision Seen (CS). This bit is set to 1 if a late collision occurred on the received packet. A late collision is one that occurs after the 64-byte collision window.

Bit 0: Frame Too Long (FTL). This bit is set to 1 if a frame exceeds the 1518 byte maximum standard Ethernet frame. This bit is only an indication, and causes no frame truncation.

Register Name: **SU.RFSB3**
 Register Description: **Receive Frame Status Byte 3**
 Register Address: **157h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|----|-----|----|----|----|
| Name | MF | — | — | BF | MCF | UF | CF | LE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Missed Frame (MF). This bit is set to 1 if the packet is not successfully received from the MAC by the packet Arbiter.

Bit 4: Broadcast Frame (BF). This bit is set to 1 if the current frame is a broadcast frame.

Bit 3: Multicast Frame (MCF). This bit is set to 1 if the current frame is a multicast frame.

Bit 2: Unsupported Control Frame (UF). This bit is set to 1 if the frame received is a control frame with an opcode that is not supported. If the Control Frame bit is set, and the Unsupported Control Frame bit is clear, then a pause frame has been received and the transmitter is paused.

Bit 1: Control Frame (CF). This bit is set to 1 when the current frame is a control frame. This bit is only valid in full-duplex mode.

Bit 0: Length Error (LE). This bit is set to 1 when the frames length field and the actual byte count are unequal. This bit is only valid for 802.3 frames.

Register Name: **SU.RMFSRL**
 Register Description: **Receiver Maximum Frame Low Register**
 Register Address: **158h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RMPS7 | RMPS6 | RMPS5 | RMPS4 | RMPS3 | RMPS2 | RMPS1 | RMPS0 |
| Default | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receiver Maximum Frame (RMPS[7:0]). Eight bits of a 16-bit value. Register description below.

Register Name: **SU.RMFSRH**
 Register Description: **Receiver Maximum Frame High Register**
 Register Address: **159h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Name | RMPS15 | RMPS14 | RMPS13 | RMPS12 | RMPS11 | RMPS10 | RMPS9 | RMPS8 |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

Bits 7 to 0: Receiver Maximum Frame (RMPS[15:8]). This value is the receiver's maximum frame size (in bytes), up to a maximum of 2016 bytes. Any frame received greater than this value is rejected. The frame size includes destination address, source address, type/length, data and crc-32. The frame size is not the same as the frame length encoded within the IEEE 802.3 frame. **Any values programmed that are greater than 2016 will have unpredictable behavior and should be avoided.**

Register Name: **SU.RQLT**
 Register Description: **Receive Queue Low Threshold (Watermark)**
 Register Address: **15Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RQLT7 | RQLT6 | RQLT5 | RQLT4 | RQLT3 | RQLT2 | RQLT1 | RQLT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Queue Low Threshold (RQLT[7:0]). The receive queue low threshold for the connection, in increments of 32 packets of 2048 bytes each. The value of this register is multiplied by 32 x 2048 bytes to determine the byte location of the threshold. Note that the receive queue is for data that was received from the Ethernet Interface to be sent to the Serial Interface.

Register Name: **SU.RQHT**
 Register Description: **Receive Queue High Threshold (Watermark)**
 Register Address: **15Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RQHT7 | RQHT6 | RQHT5 | RQHT4 | RQHT3 | RQHT2 | RQHT1 | RQHT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Queue High Threshold (RQHT[7:0]). The receive queue high threshold for the connection, in increments of 32 packets of 2048 bytes each. The value of this register is multiplied by 32 x 2048 bytes to determine the byte location of the threshold. Note that the receive queue is for data that was received from the Ethernet Interface to be sent to the Serial Interface.

Register Name: **SU.QRIE**
 Register Description: **Receive Queue Cross Threshold Enable**
 Register Address: **15Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---------|--------|--------|--------|
| Name | — | — | — | — | RFOVFIE | RQVFIE | RQLTIE | RQHTIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: Receive FIFO Overflow Interrupt Enable (RFOVFIE). If this bit is set, the interrupt is enabled for RFOVFLS.

Bit 2: Receive Queue Overflow Interrupt Enable (RQVFIE). If this bit is set, the interrupt is enabled for RQOVFLS.

Bit 1: Receive Queue Crosses Low Threshold Interrupt Enable (RQLTIE). If this bit is set, the watermark interrupt is enabled for RQLTS.

Bit 0: Receive Queue Crosses High Threshold Interrupt Enable (RQHTIE). If this bit is set, the watermark interrupt is enabled for RQHTS.

Register Name: **SU.QCRLS**
 Register Description: **Queue Cross Threshold Latched Status**
 Register Address: **15Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---------|---------|--------|--------|
| Name | — | — | — | — | RFOVFLS | RQOVFLS | RQHTLS | RQLTLS |
| Default | — | — | — | — | — | — | — | — |

Bit 3: Receive FIFO Overflow latched Status (RFOVFLS). This bit is set if the receive FIFO overflows for the data to be transmitted from the MAC to the SDRAM.

Bit 2: Receive Queue Overflow Latched Status (RQOVFLS). This bit is set if the receive queue has overflowed. This register is cleared after a read.

Bit 1: Receive Queue for Connection Crossed High Threshold Latched Status (RQHTLS). This bit is set if the receive queue crosses the high Watermark. This register is cleared after a read.

Bit 0: Receive Queue for Connection Crossed Low Threshold latched status (RQLTLS). This bit is set if the receive queue crosses the low Watermark. This register is cleared after a read.

Note the bit order differences in the high/low threshold indications in SU.QCRLS and the interrupt enables in SU.QRIE.

Register Name: **SU.RFRC**
 Register Description: **Receive Frame Rejection Control**
 Register Address: **15Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|------|--------|-----|-------|-----|
| Name | — | UCFR | CFRR | LERR | CRCERR | DBR | MIIER | BFR |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Uncontrolled Control Frame Reject (UCFR). When set to 1, Control Frames other than Pause Frames are allowed. When this bit is equal to zero, non-pause control frames are rejected.

Bit 5: Control Frame Reject (CFRR). When set to 1, control frames are allowed. When this bit is equal to zero, all control frames are rejected.

Bit 4: Length Error Reject (LERR). When set to 1, frames with an unmatched frame length field and actual number of bytes received are allowed. When equal to zero, only frames with matching length fields and actual bytes received will be allowed.

Bit 3: CRC Error Reject (CRCERR). When set to 1, frames received with a CRC error or MII error are allowed. When equal to zero, frames with CRC or MII errors are rejected.

Bit 2: Dribbling Bit Reject (DBR). When set to 1, frames with lengths of non-integer multiples of 8 bits are allowed. When equal to zero, frames with dribbling bits are rejected. The dribbling bit setting is only valid only if there is not a collision or runt frame.

Bit 1: MII Error Reject (MIIER). When set to 1, frames are allowed with MII Receive Errors. When equal to zero, frames with MII errors are rejected.

Bit 0: Broadcast Frame Reject (BFR). When set to 1, broadcast frames are allowed. When equal to zero, broadcast frames are rejected.

12.6.2 MAC Registers

The control Registers related to the control of the individual MACs are shown in the following table. The device keeps statistics for the packet traffic sent and received. The register address map is shown in the following table. Note that the addresses listed are the indirect addresses that must be provided to [SU.MACRADH/SU.MACRADL](#) or [SU.MACAWH/SU.MACAWL](#).

Register Name: **SU.MACCR**
 Register Description: **MAC Control Register**
 Register Address: **0000h (indirect)**

0000h:

| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---------|----------|----------|----------|-----|----|----------|----------|----------|
| Name | Reserved | Reserved | Reserved | HDB | PS | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0001h:

| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---------|-----|----------|------|----|----|-----|----------|----------|
| Name | DRO | Reserved | OML0 | F | PM | PAM | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0002h:

| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---------|----------|----------|----------|-----|----------|------|----------|------|
| Name | Reserved | Reserved | Reserved | LCC | Reserved | DRTY | Reserved | ASTP |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0003h:

| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---------|--------|--------|----|----------|----|----|----------|----------|
| Name | BOLMT1 | BOLMT0 | DC | Reserved | TE | RE | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 28: Heartbeat Disable (HDB). When set to 1, the heartbeat (SQE) function is disabled. This bit should be set to 1 when operating in MII mode.

Bit 27: Port Select (PS). This bit should be equal to 0 for proper operation.

Bit 23: Disable Receive Own (DRO). When set to 1, the MAC disables the reception of frames while TX_EN is asserted. When this bit equals zero, transmitted frames are also received by the MAC. This bit should be cleared when operating in full-duplex mode.

Bit 21: Loopback Operating Mode (OMLO). When set to 1, data is looped from the transmit side, back to the receive side, without being transmitted to the PHY.

Bit 20: Full-Duplex Mode Select (F). When set to 1, the MAC transmits and receives data simultaneously. When in full-duplex mode, the heartbeat check is disabled and the heartbeat fail status should be ignored.

Bit 19: Promiscuous Mode (PM) When set to 1, the MAC is in Promiscuous Mode and forwards all frames. Note that the default value is 1.

Bit 18: Pass All Multicast (PAM) When set to 1, the MAC forwards Multicast Frames.

Bit 12: Late Collision Control (LCC). When set to 1, enables retransmission of a collided packet even after the collision period. When this bit is clear, retransmission of late collisions is disabled.

Bit 10: Disable Retry (DRTY). When set to 1, the MAC makes only a single attempt to transmit each frame. If a collision occurs, the MAC ignores the current frame and proceeds to the next frame. When this bit equals 0, the MAC will retry collided packets 16 times before signaling a retry error.

Bit 8: Automatic Pad Stripping (ASTP). When set to 1, all incoming frames with less than 46 byte length are automatically stripped of the pad characters and FCS.

Bits 7 and 6: Back-Off Limit (BOLMT[1:0]). These two bits allow the user to set the back-off limit used for the maximum retransmission delay for collided packets. Default operation limits the maximum delay for retransmission to a countdown of 10 bits from a random number generator. The user can reduce the maximum number of counter bits as described in the table below. See IEEE 802.3 for details of the back-off algorithm.

| Bit 7 | Bit 6 | Random Number Generator Bits Used |
|-------|-------|-----------------------------------|
| 0 | 0 | 10 |
| 0 | 1 | 8 |
| 1 | 0 | 4 |
| 1 | 1 | 1 |

Bit 5: Deferral Check (DC). When set to 1, the MAC will abort packet transmission if it has deferred for more than 24,288 bit times. The deferral counter starts when the transmitter is ready to transmit a packet, but is prevented from transmission because CRS is active. If the MAC begins transmission but a collision occurs after the beginning of transmission, the deferral counter is reset again. If this bit is equal to zero, then the MAC will defer indefinitely.

Bit 3: Transmitter Enable (TE). When set to 1, packet transmission is enabled. When equal to zero, transmission is disabled.

Bit 2: Receiver Enable (RE). When set to 1, packet reception is enabled. When equal to zero, packets are not received.

Register Name: **SU.MACAH**
 Register Description: **MAC Address High Register**
 Register Address: **0004h (indirect)**

0004h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

0005h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

0006h:

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | PADR47 | PADR46 | PADR45 | PADR44 | PADR43 | PADR42 | PADR41 | PADR40 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

0007h:

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | PADR39 | PADR38 | PADR37 | PADR36 | PADR35 | PADR34 | PADR33 | PADR32 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Bits 31 to 00: PADR[32:47:32]. These 32 bits should be initialized with the upper 4 bytes of the Physical Address for this MAC device.

Register Name: **SU.MACAL**
 Register Description: **MAC Address Low Register**
 Register Address: **0008h (indirect)**

0008h:

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | PADR31 | PADR30 | PADR29 | PADR28 | PADR27 | PADR26 | PADR25 | PADR24 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

0009h:

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | PADR23 | PADR22 | PADR21 | PADR20 | PADR19 | PADR18 | PADR17 | PADR16 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

000Ah:

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | PADR15 | PADR14 | PADR13 | PADR12 | PADR11 | PADR10 | PADR09 | PADR08 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

000Bh:

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | PADR07 | PADR06 | PADR05 | PADR04 | PADR03 | PADR02 | PADR01 | PADR00 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Bits 31 to 00: PADR[31:00]. These 32 bits should be initialized with the lower 4 bytes of the Physical Address for this MAC device.

Register Name: **SU.MACMIIA**
 Register Description: **MAC MII Management (MDIO) Address Register**
 Register Address: **0014h (indirect)**

0014h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0015h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0016h:

| | | | | | | | | |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | PHYA4 | PHYA3 | PHYA2 | PHYA1 | PHYA0 | MIIA4 | MIIA3 | MIIA2 |
| Default | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

0017h:

| | | | | | | | | |
|---------|-------|-------|----------|----------|----------|----------|------|------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | MIIA1 | MIIA0 | Reserved | Reserved | Reserved | Reserved | MIIW | MIIB |
| Default | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 15 to 11: PHY Address (PHYA[4:0]). These 5 bits select one of the 32 available PHY address locations to access through the PHY management (MDIO) bus.

Bits 10 to 6: MII Address (MIIA[4:0]). These 5 bits are the address location within the PHY that is being accessed.

Bit 1: MII Write (MIIW). Write this bit to 1 in order to execute a write instruction over the MDIO interface. Write the bit to zero to execute a read instruction.

Bit 0: MII Busy (MIIB). This bit is set to 1 by the device during execution of a MII management instruction through the MDIO interface, and is set to zero when the device has completed the instruction. The user should read this bit and ensure that it is equal to zero prior to beginning a MDIO instruction.

Register Name: **SU.MACMIID**
 Register Description: **MAC MII (MDIO) Data Register**
 Register Address: **0018h (indirect)**

0018h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0019h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

001Ah:

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | MIID15 | MIID14 | MIID13 | MIID12 | MIID11 | MIID10 | MIID09 | MIID08 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

001Bh:

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | MIID07 | MIID06 | MIID05 | MIID04 | MIID03 | MIID02 | MIID01 | MIID00 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 15 to 0: MII (MDIO) Data (MIID[15:00]). These two bytes contain the data to be written to or the data read from the MII management interface (MDIO).

Register Name: **SU.MACFCR**
 Register Description: **MAC Flow Control Register**
 Register Address: **001Ch (indirect)**

001Ch:

| | | | | | | | | |
|---------|------|------|------|------|------|------|------|------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | PT15 | PT14 | PT13 | PT12 | PT11 | PT10 | PT09 | PT08 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

001Dh:

| | | | | | | | | |
|---------|------|------|------|------|------|------|------|------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | PT07 | PT06 | PT05 | PT04 | PT03 | PT02 | PT01 | PT00 |
| Default | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

001Eh:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

001Fh:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|-----|-----|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | FCE | FCB |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Bits 31 to 16: Pause Time (PT[15:00]). These bits are used for the Pause Time Field in transmitted Pause Frames. This value is the number of time slots the remote node should wait prior to transmission.

Bit 1: Flow Control Enable (FCE). When set to 1, the MAC automatically detects pause frames and will disable the transmitter for the requested pause time.

Bit 0: Flow Control Busy (FCB). The host can set this bit to 1 in order to initiate transmission of a pause frame. During transmission of a pause frame, this bit remains set. The device will clear this bit when transmission of the pause frame has been completed. The user should read this bit and ensure that this bit is equal to zero prior to initiating a pause frame.

Register Name: **SU.MMCCTRL**
 Register Description: **MAC MMC Control Register**
 Register Address: **0100h (indirect)**

0100h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0101h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0102h:

| | | | | | | | | |
|---------|----------|----------|---------|--------|--------|--------|--------|--------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | Reserved | Reserved | MXFRM10 | MXFRM9 | MXFRM8 | MXFRM7 | MXFRM6 | MXFRM5 |
| Default | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

0103h:

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|----------|----------|----------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | MXFRM4 | MXFRM3 | MXFRM2 | MXFRM1 | MXFRM0 | Reserved | Reserved | Reserved |
| Default | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |

Bits 13 to 3: Maximum Frame Size (MXFRM[10:0]). These bits indicate the maximum packet size value. All transmitted frames larger than this value are counted as long frames.

Bit 1: Reserved. Note that this bit must be written to a "1" for proper operation.

Register Name: **Reserved**
 Register Description: **MAC Reserved Control Register**
 Register Address: **010Ch (indirect)**

010Ch:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

010Dh:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

010Eh:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

010Fh:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Addresses 10Ch through 10Fh must each be initialized with all 1s (FFh) for proper software-mode operation.

Register Name: **Reserved**
 Register Description: **MAC Reserved Control Register**
 Register Address: **0110h (indirect)**

0110h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0111h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0112h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0113h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Addresses 110h through 113h must each be initialized with all 1s (FFh) for proper software-mode operation.

Register Name: **SU.RxFrmCtr**
 Register Description: **MAC All Frames Received Counter**
 Register Address: **0200h (indirect)**

0200h:

| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Name | RXFRMC31 | RXFRMC30 | RXFRMC29 | RXFRMC28 | RXFRMC27 | RXFRMC26 | RXFRMC25 | RXFRMC24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0201h:

| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Name | RXFRMC23 | RXFRMC22 | RXFRMC21 | RXFRMC20 | RXFRMC19 | RXFRMC18 | RXFRMC17 | RXFRMC16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0202h:

| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---------|----------|----------|----------|----------|----------|----------|---------|---------|
| Name | RXFRMC15 | RXFRMC14 | RXFRMC13 | RXFRMC12 | RXFRMC11 | RXFRMC10 | RXFRMC9 | RXFRMC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0203h:

| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Name | RXFRMC7 | RXFRMC6 | RXFRMC5 | RXFRMC4 | RXFRMC3 | RXFRMC2 | RXFRMC1 | RXFRMC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 31 to 0: All Frames Received Counter (RXFRMC[31:0]). 32-bit value indicating the number of frames received. Each time a frame is received, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment $2^{32}-1$ times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a rollover to occur.

Register Name: **SU.RxFrmOkCtr**
 Register Description: **MAC Frames Received OK Counter**
 Register Address: **0204h (indirect)**

0204h:

| | | | | | | | | |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | RXFRMOK31 | RXFRMOK30 | RXFRMOK29 | RXFRMOK28 | RXFRMOK27 | RXFRMOK26 | RXFRMOK25 | RXFRMOK24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0205h:

| | | | | | | | | |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | RXFRMOK23 | RXFRMOK22 | RXFRMOK21 | RXFRMOK20 | RXFRMOK19 | RXFRMOK18 | RXFRMOK17 | RXFRMOK16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0206h:

| | | | | | | | | |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | RXFRMOK15 | RXFRMOK14 | RXFRMOK13 | RXFRMOK12 | RXFRMOK11 | RXFRMOK10 | RXFRMOK9 | RXFRMOK8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0207h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | RXFRMOK7 | RXFRMOK6 | RXFRMOK5 | RXFRMOK4 | RXFRMOK3 | RXFRMOK2 | RXFRMOK1 | RXFRMOK0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 31 to 0: Frames Received OK Counter (RXFRMOK[31:0]). 32-bit value indicating the number of frames received and determined to be valid. Each time a valid frame is received, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment $2^{32}-1$ times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a rollover to occur.

Register Name: **SU.TxFrmCtr**
 Register Description: **MAC All Frames Transmitted Counter**
 Register Address: **0300h (indirect)**

0300h:

| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Name | TXFRMC31 | TXFRMC30 | TXFRMC29 | TXFRMC28 | TXFRMC27 | TXFRMC26 | TXFRMC25 | TXFRMC24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0301h:

| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Name | TXFRMC23 | TXFRMC22 | TXFRMC21 | TXFRMC20 | TXFRMC19 | TXFRMC18 | TXFRMC17 | TXFRMC16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0302h:

| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---------|----------|----------|----------|----------|----------|----------|---------|---------|
| Name | TXFRMC15 | TXFRMC14 | TXFRMC13 | TXFRMC12 | TXFRMC11 | TXFRMC10 | TXFRMC9 | TXFRMC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0303h:

| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Name | TXFRMC7 | TXFRMC6 | TXFRMC5 | TXFRMC4 | TXFRMC3 | TXFRMC2 | TXFRMC1 | TXFRMC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 31 to 0: All Frames Transmitted Counter (TXFRMC[31:0]). 32-bit value indicating the number of frames transmitted. Each time a frame is transmitted, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment $2^{32}-1$ times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a rollover to occur.

Register Name: **SU.TxBytesCtr**
 Register Description: **MAC All Bytes Transmitted Counter**
 Register Address: **0308h (indirect)**

0308h:

| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Name | TXBYTEC31 | TXBYTEC30 | TXBYTEC29 | TXBYTEC28 | TXBYTEC27 | TXBYTEC26 | TXBYTEC25 | TXBYTEC24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0309h:

| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Name | TXBYTEC23 | TXBYTEC22 | TXBYTEC21 | TXBYTEC20 | TXBYTEC19 | TXBYTEC18 | TXBYTEC17 | TXBYTEC16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

030Ah:

| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| Name | TXBYTEC15 | TXBYTEC14 | TXBYTEC13 | TXBYTEC12 | TXBYTEC11 | TXBYTEC10 | TXBYTEC9 | TXBYTEC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

030Bh:

| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Name | TXBYTEC7 | TXBYTEC6 | TXBYTEC5 | TXBYTEC4 | TXBYTEC3 | TXBYTEC2 | TXBYTEC1 | TXBYTEC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 31 to 0: All Bytes Transmitted Counter (TXBYTEC[31:0]). 32-bit value indicating the number of bytes transmitted. Each time a byte is transmitted, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment $2^{32}-1$ times at the maximum data rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a rollover to occur.

Register Name: **SU.TxBytesOkCtr**
 Register Description: **MAC Bytes Transmitted OK Counter**
 Register Address: **030Ch (indirect)**

030Ch:

| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---------|------------|------------|------------|------------|------------|------------|------------|------------|
| Name | TXBYTEOK31 | TXBYTEOK30 | TXBYTEOK29 | TXBYTEOK28 | TXBYTEOK27 | TXBYTEOK26 | TXBYTEOK25 | TXBYTEOK24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

030Dh:

| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---------|------------|------------|------------|------------|------------|------------|------------|------------|
| Name | TXBYTEOK23 | TXBYTEOK22 | TXBYTEOK21 | TXBYTEOK20 | TXBYTEOK19 | TXBYTEOK18 | TXBYTEOK17 | TXBYTEOK16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

030Eh:

| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
|---------|------------|------------|------------|------------|------------|------------|-----------|-----------|
| Name | TXBYTEOK15 | TXBYTEOK14 | TXBYTEOK13 | TXBYTEOK12 | TXBYTEOK11 | TXBYTEOK10 | TXBYTEOK9 | TXBYTEOK8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

030Fh:

| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Name | TXBYTEOK7 | TXBYTEOK6 | TXBYTEOK5 | TXBYTEOK4 | TXBYTEOK3 | TXBYTEOK2 | TXBYTEOK1 | TXBYTEOK0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 31 to 0: Bytes Transmitted OK Counter (TXBYTEOK[31:0]). 32-bit value indicating the number of bytes transmitted and determined to be valid. Each time a valid byte is transmitted, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment $2^{32}-1$ times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a rollover to occur.

Register Name: **SU.TXFRMUNDR**
 Register Description: **MAC Transmit Frame Under Run Counter**
 Register Address: **0334h (indirect)**

0334h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | TXFRMU31 | TXFRMU30 | TXFRMU29 | TXFRMU28 | TXFRMU27 | TXFRMU26 | TXFRMU25 | TXFRMU24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0335h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | TXFRMU23 | TXFRMU22 | TXFRMU21 | TXFRMU20 | TXFRMU19 | TXFRMU18 | TXFRMU17 | TXFRMU16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0336h:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|---------|---------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | TXFRMU15 | TXFRMU14 | TXFRMU13 | TXFRMU12 | TXFRMU11 | TXFRMU10 | TXFRMU9 | TXFRMU8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0337h:

| | | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | TXFRMU7 | TXFRMU6 | TXFRMU5 | TXFRMU4 | TXFRMU3 | TXFRMU2 | TXFRMU1 | TXFRMU0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 31 to 0: Frames Aborted Due to FIFO Underrun Counter (TXFRMU[31:0]). 32-bit value indicating the number of frames aborted due to FIFO under run. Each time a frame is aborted due to FIFO under run, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment $2^{32}-1$ times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a rollover to occur.

Register Name: **SU.TxBdFrmCtr**
 Register Description: **MAC All Frames Aborted Counter**
 Register Address: **0338h (indirect)**

0338h:

| | | | | | | | | |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit # | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Name | TXFRMBD31 | TXFRMBD30 | TXFRMBD29 | TXFRMBD28 | TXFRMBD27 | TXFRMBD26 | TXFRMBD25 | TXFRMBD24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

0339h:

| | | | | | | | | |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit # | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Name | TXFRMBD23 | TXFRMBD22 | TXFRMBD21 | TXFRMBD20 | TXFRMBD19 | TXFRMBD18 | TXFRMBD17 | TXFRMBD16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

033Ah:

| | | | | | | | | |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 |
| Name | TXFRMBD15 | TXFRMBD14 | TXFRMBD13 | TXFRMBD12 | TXFRMBD11 | TXFRMBD10 | TXFRMBD9 | TXFRMBD8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

033Bh:

| | | | | | | | | |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Name | TXFRMBD7 | TXFRMBD6 | TXFRMBD5 | TXFRMBD4 | TXFRMBD3 | TXFRMBD2 | TXFRMBD1 | TXFRMBD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 31 to 0: All Frames Aborted Counter (TXFRMBD[31:0]). 32-bit value indicating the number of frames aborted due to any reason. Each time a frame is aborted, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment $2^{32}-1$ times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a rollover to occur.

12.7 Transceiver Registers

Register Name: **TR.MSTRREG**
 Register Description: **Master Mode Register**
 Register Address: **00h**

| | | | | | | | | |
|---------|---|---|---|---|-------|-------|-------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | TEST1 | TEST0 | T1/E1 | SFTRST |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 3 and 2: Test Mode Bits (TEST1 and TEST0). Test modes are used to force the output pins of the transceiver into known states. This can facilitate the checkout of assemblies during the manufacturing process and also be used to isolate devices from shared buses.

| TEST1 | TEST0 | Effect On Output Pins |
|-------|-------|--|
| 0 | 0 | Operate normally |
| 0 | 1 | Force all output pins into tri-state (including all I/O pins and parallel port pins) |
| 1 | 0 | Force all output pins low (including all I/O pins except parallel port pins) |
| 1 | 1 | Force all output pins high (including all I/O pins except parallel port pins) |

Bit 1: Transceiver Operating Mode (T1/E1). Used to select the operating mode of the framer/formatter (digital) portion of the transceiver. The operating mode of the LIU must also be programmed.

0 = T1 operation

1 = E1 operation

Bit 0: Software-Issued Reset (SFTRST). A 0-to-1 transition causes the register space in the T1/E1/J1 transceiver to be cleared. A reset clears all configuration and status registers. The bit automatically clears itself when the reset has completed.

Register Name: **TR.IOCR1**
 Register Description: **I/O Configuration Register 1**
 Register Address: **01h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-------|------|------|-----|------|-----|
| Name | RSMS | RSMS2 | RSMS1 | RSIO | TSDW | TSM | TSIO | ODF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: RSYNC Multiframe Skip Control (RSMS). Useful in framing format conversions from D4 to ESF. This function is not available when the receive-side elastic store is enabled. RSYNC must be set to output multiframe pulses (TR.IOCR1.5 = 1 and TR.IOCR1.4 = 0).

- 0 = RSYNC outputs a pulse at every multiframe
- 1 = RSYNC outputs a pulse at every other multiframe

Bit 6: RSYNC Mode Select 2 (RSMS2)

T1 Mode: RSYNC pin must be programmed in the output frame mode (TR.IOCR1.5 = 0, TR.IOCR1.4 = 0).

- 0 = do not pulse double-wide in signaling frames
- 1 = do pulse double-wide in signaling frames

E1 Mode: RSYNC pin must be programmed in the output multiframe mode (TR.IOCR1.5 = 1, TR.IOCR1.4 = 0).

- 0 = RSYNC outputs CAS multiframe boundaries
- 1 = RSYNC outputs CRC4 multiframe boundaries

Bit 5: RSYNC Mode Select 1 (RSMS1). Selects frame or multiframe pulse when RSYNC pin is in output mode. In input mode (elastic store must be enabled), multiframe mode is only useful when receive signaling reinsertion is enabled. See the timing diagrams in Section [13](#).

- 0 = frame mode
- 1 = multiframe mode

Bit 4: RSYNC I/O Select (RSIO). This bit must be set to 0 when TR.ESCR.0 = 0.

- 0 = RSYNC is an output
- 1 = RSYNC is an input (only valid if elastic store enabled)

Bit 3: TSYNC Double-Wide (TSDW). This bit must be set to 0 when TR.IOCR1.2 = 1 or when TR.IOCR1.1 = 0.

- 0 = do not pulse double-wide in signaling frames
- 1 = do pulse double-wide in signaling frames

Bit 2: TSYNC Mode Select (TSM). Selects frame or multiframe mode for the TSYNC pin. See the timing diagrams in Section [13](#).

- 0 = frame mode
- 1 = multiframe mode

Bit 1: TSYNC I/O Select (TSIO)

- 0 = TSYNC is an input
- 1 = TSYNC is an output

Bit 0: Output Data Format (ODF)

- 0 = bipolar data at TPOSO and TNEGO
- 1 = NRZ data at TPOSO; TNEGO = 0

Register Name: **TR.IOCR2**
 Register Description: **I/O Configuration Register 2**
 Register Address: **02h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|----------|----------|-----------|--------|--------|--------|
| Name | RCLKINV | TCLKINV | RSYNCINV | TSYNCINV | TSSYNCINV | H100EN | TSCLKM | RSCLKM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: RCLKn Invert (RCLKINV)

0 = no inversion
 1 = inverts signal on RCLKn output.

Bit 6: TCLKT Invert (TCLKINV)

0 = no inversion
 1 = inverts signal on TCLKT input.

Bit 5: RSYNC Invert (RSYNCINV)

0 = no inversion
 1 = invert

Bit 4: TSYNC Invert (TSYNCINV)

0 = no inversion
 1 = invert

Bit 3: TSSYNC Invert (TSSYNCINV)

0 = no inversion
 1 = invert

Bit 2 : H.100 SYNC Mode (H100EN)

0 = normal operation
 1 = SYNC shift

Bit 1: TSYCLK Mode Select (TSCLKM)

0 = if TSYCLK is 1.544MHz
 1 = if TSYCLK is 2.048MHz

Bit 0: RSYCLK Mode Select (RSCLKM)

0 = if RSYCLK is 1.544MHz
 1 = if RSYCLK is 2.048MHz

Register Name: **TR.T1RCR1**
 Register Description: **T1 Receive Control Register 1**
 Register Address: **03h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-----|------|------|-------|-------|-------|--------|
| Name | — | ARC | OOF1 | OOF2 | SYNCC | SYNCT | SYNCE | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Auto Resync Criteria (ARC)

0 = resync on OOF or RCL event
 1 = resync on OOF only

Bits 5 and 4: Out-of-Frame Select Bits (OOF1 and OOF2)

| OOF2 | OOF1 | Out-Of-Frame Criteria |
|------|------|-------------------------|
| 0 | 0 | 2/4 frame bits in error |
| 0 | 1 | 2/5 frame bits in error |
| 1 | 0 | 2/6 frame bits in error |
| 1 | 1 | 2/6 frame bits in error |

Bit 3: Sync Criteria (SYNCC)

In D4 Framing Mode:

0 = search for Ft pattern, then search for Fs pattern
 1 = cross couple Ft and Fs pattern

In ESF Framing Mode:

0 = search for FPS pattern only
 1 = search for FPS and verify with CRC6

Bit 2: Sync Time (SYNCT)

0 = qualify 10 bits
 1 = qualify 24 bits

Bit 1: Sync Enable (SYNCE)

0 = auto resync enabled
 1 = auto resync disabled

Bit 0: Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the receive-side framer is initiated. Must be cleared and set again for a subsequent resync.

Register Name: **TR.T1RCR2**
 Register Description: **T1 Receive Control Register 2**
 Register Address: **04h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-----|-------|--------|------|---|-----|-------|
| Name | — | RFM | RB8ZS | RSLC96 | RZSE | — | RJC | RD4YM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Receive Frame Mode Select (RFM)

0 = D4 framing mode
 1 = ESF framing mode

Bit 5: Receive B8ZS Enable (RB8ZS)

0 = B8ZS disabled
 1 = B8ZS enabled

Bit 4: Receive SLC-96 Enable (RSLC96). Only set this bit to a 1 in D4/SLC-96 framing applications. See Section [10.19](#) for details.

0 = SLC-96 disabled
 1 = SLC-96 enabled

Bit 3: Receive FDL Zero-Destuffer Enable (RZSE). Set this bit to 0 if using the internal HDLC/BOC controller instead of the legacy support for the FDL. See Section [10.18](#) for details.

0 = zero destuffer disabled
 1 = zero destuffer enabled

Bit 2: Reserved. Set to zero for proper operation.

Bit 1: Receive Japanese CRC6 Enable (RJC)

0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation)
 1 = use Japanese standard JT-G704 CRC6 calculation

Bit 0: Receive-Side D4 Yellow Alarm Select (RD4YM)

0 = 0s in bit 2 of all channels
 1 = a 1 in the S-bit position of frame 12 (J1 Yellow Alarm Mode)

Register Name: **TR.T1TCR1**
 Register Description: **T1 Transmit Control Register 1**
 Register Address: **05h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|------|------|------|------|-------|-----|------|
| Name | TJC | TFPT | TCPT | TSSE | GB7S | TFDLS | TBL | TYEL |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Japanese CRC6 Enable (TJC)

- 0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation)
- 1 = use Japanese standard JT-G704 CRC6 calculation

Bit 6: Transmit F-Bit Pass-Through (TFPT)

- 0 = F bits sourced internally
- 1 = F bits sampled at TSERI

Bit 5: Transmit CRC Pass-Through (TCPT)

- 0 = source CRC6 bits internally
- 1 = CRC6 bits sampled at TSERI during F-bit time

Bit 4: Transmit Software Signaling Enable (TSSE)

- 0 = do not source signaling data from the TR.TSx registers regardless of the TR.SSIEx registers. The TR.SSIEx registers still define which channels are to have B7 stuffing preformed.
- 1 = source signaling data as enabled by the TR.SSIEx registers

Bit 3: Global Bit 7 Stuffing (GB7S)

- 0 = allow the SSIEx registers to determine which channels containing all 0s are to be bit 7 stuffed
- 1 = force bit 7 stuffing in all 0-byte channels regardless of how the TR.SSIEx registers are programmed

Bit 2: TFDL Register Select (TFDLS)

- 0 = source FDL or Fs-bits from the internal TR.TFDL register (legacy FDL support mode)
- 1 = source FDL or Fs-bits from the internal HDLC controller

Bit 1: Transmit Blue Alarm (TBL)

- 0 = transmit data normally
- 1 = transmit an unframed all-ones code at TPOS and TNEG

Bit 0: Transmit Yellow Alarm (TYEL)

- 0 = do not transmit yellow alarm
- 1 = transmit yellow alarm

Register Name: **TR.T1TCR2**
 Register Description: **T1 Transmit Control Register 2**
 Register Address: **06h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|--------|------|-------|-------|-------|---|-------|
| Name | TB8ZS | TSLC96 | TZSE | FBCT2 | FBCT1 | TD4YM | — | TB7ZS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit B8ZS Enable (TB8ZS)

0 = B8ZS disabled
 1 = B8ZS enabled

Bit 6: Transmit SLC-96/Fs-Bit Insertion Enable (TSLC96). Only set this bit to a 1 in D4 framing applications. Must be set to 1 to source the Fs pattern from the TR.TFDL register. See Section [10.19](#) for details.

0 = SLC-96/Fs-bit insertion disabled
 1 = SLC-96/Fs-bit insertion enabled

Bit 5: Transmit FDL Zero-Stuffer Enable (TZSE). Set this bit to 0 if using the internal HDLC controller instead of the legacy support for the FDL.

0 = zero stuffer disabled
 1 = zero stuffer enabled

Bit 4: F-Bit Corruption Type 2 (FBCT2). Setting this bit high enables the corruption of one Ft (D4 framing mode) or FPS (ESF framing mode) bit in every 128 Ft or FPS bits as long as the bit remains set.

Bit 3: F-Bit Corruption Type 1 (FBCT1). A low-to-high transition of this bit causes the next three consecutive Ft (D4 framing mode) or FPS (ESF framing mode) bits to be corrupted causing the remote end to experience a loss of synchronization.

Bit 2: Transmit-Side D4 Yellow Alarm Select (TD4YM)

0 = 0s in bit 2 of all channels
 1 = a 1 in the S-bit position of frame 12

Bit 0: Transmit-Side Bit 7 Zero-Suppression Enable (TB7ZS)

0 = no stuffing occurs
 1 = bit 7 forced to a 1 in channels with all 0s

Register Name: **TR.T1CCR1**
 Register Description: **T1 Common Control Register 1**
 Register Address: **07h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-----|---------|---------|-----|-----|-------|
| Name | MCLKS | CRC4R | SIE | TRAI-CI | TAIS-CI | TFM | PDE | TLOOP |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: MCLK Source Select (MCLKS). Selects the source of MCLK.

- 0 = MCLK is sourced from the MCLK pin.
- 1 = MCLK is sourced from the TSYSCLK pin.

Bit 6: CRC-4 Recalculate (E1 Mode Only) (CRC4R).

- 0 = Transmit CRC-4 Generation and Insertion operates in normal mode.
- 1 = Transmit CRC-4 operation according to G.706 Intermediate Path Recalculation Method.

BIT 5: Signaling Integration Enable (SIE).

- 0 = Signaling changes of state are reported upon any change in selected channels.
- 1 = Signaling must be stable for three multiframes before a change of state is reported.

Bit 4: Transmit RAI-CI Enable (TRAI-CI). Setting this bit causes the ESF RAI-CI code to be transmitted in the FDL bit position.

- 0 = do not transmit the ESF RAI-CI code
- 1 = transmit the ESF RAI-CI code

Bit 3: Transmit AIS-CI Enable (TAIS-CI). Setting this bit and the TBL bit (TR.T1TCR1.1) causes the AIS-CI code to be transmitted at TPOSO and TNEGO, as defined in ANSI T1.403.

- 0 = do not transmit the AIS-CI code
- 1 = transmit the AIS-CI code (TR.T1TCR1.1 must also be set = 1)

Bit 2: Transmit Frame Mode Select (TFM)

- 0 = D4 framing mode
- 1 = ESF framing mode

Bit 1: Pulse Density Enforcer Enable (PDE). The framer always examines the transmit and receive data streams for violations of these, which are required by ANSI T1.403: No more than 15 consecutive 0s and at least N 1s in each and every time window of $8 \times (N + 1)$ bits, where N = 1 through 23. Violations for the transmit and receive data streams are reported in the TR.INFO1.6 and TR.INFO1.7 bits, respectively. When this bit is set to 1, the T1/E1/J1 transceiver forces the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, this bit should be set to 0 since B8ZS encoded data streams cannot violate the pulse density requirements.

- 0 = disable transmit pulse density enforcer
- 1 = enable transmit pulse density enforcer

Bit 0: Transmit Loop-Code Enable (TLOOP). See Section [10.20](#) for details.

- 0 = transmit data normally
- 1 = replace normal transmitted data with repeating code as defined in registers TR.TCD1 and TR.TCD2

Register Name: **TR.SSIE1 (T1 Mode)**
 Register Description: **Software Signaling Insertion Enable 1**
 Register Address: **08h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Software Signaling Insertion Enable for Channels 8 to 1 (CH8 to CH1). These bits determine which channels are to have signaling inserted from the transmit signaling registers.

0 = do not source signaling data from the TR.TSx registers for this channel

1 = source signaling data from the TR.TSx registers for this channel

Register Name: **TR.SSIE1 (E1 Mode)**
 Register Description: **Software Signaling Insertion Enable 1**
 Register Address: **08h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|------|
| Name | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | UCAW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 1: Software Signaling-Insertion Enable for Channels 7 to 1 (CH7 to CH1). These bits determine which channels are to have signaling inserted from the transmit signaling registers.

0 = do not source signaling data from the TR.TSx registers for this channel

1 = source signaling data from the TR.TSx registers for this channel

Bit 0: Upper CAS Align/Alarm Word (UCAW). Selects the upper CAS align/alarm pattern (0000) to be sourced from the upper 4 bits of the TS1 register.

0 = do not source the upper CAS align/alarm pattern from the TR.TS1 register

1 = source the upper CAS align/alarm pattern from the TR.TS1 register

Register Name: **TR.SSIE2 (T1 Mode)**
 Register Description: **Software Signaling-Insertion Enable 2**
 Register Address: **09h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|-----|
| Name | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Software Signaling Insertion Enable for Channels 16 to 9 (CH16 to CH9). These bits determine which channels are to have signaling inserted from the transmit signaling registers.

0 = do not source signaling data from the TR.TSx registers for this channel

1 = source signaling data from the TR.TSx registers for this channel

Register Name: **TR.SSIE2 (E1 Mode)**
 Register Description: **Software Signaling Insertion Enable 2**
 Register Address: **09h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|-----|-----|
| Name | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Software Signaling Insertion Enable for Channels 15 to 8 (CH15 to CH8). These bits determine which channels are to have signaling inserted from the transmit signaling registers.

0 = do not source signaling data from the TR.TSx registers for this channel

1 = source signaling data from the TR.TSx registers for this channel

Register Name: **TR.SSIE3 (T1 Mode)**
 Register Description: **Software Signaling-Insertion Enable 3**
 Register Address: **0Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Software Signaling Insertion Enable for Channels 24 to 17 (CH24 to CH17). These bits determine which channels are to have signaling inserted from the transmit signaling registers.

0 = do not source signaling data from the TR.TSx registers for this channel

1 = source signaling data from the TR.TSx registers for this channel

Register Name: **TR.SSIE3 (E1 Mode)**
 Register Description: **Software Signaling Insertion Enable 3**
 Register Address: **0Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | LCAW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 1: Software Signaling Insertion Enable for LCAW and Channels 22 to 16 (CH22 to CH16). These bits determine which channels are to have signaling inserted from the transmit signaling registers.

0 = do not source signaling data from the TR.TSx registers for this channel

1 = source signaling data from the TR.TSx registers for this channel

Bit 0: Lower CAS Align/Alarm Word (LCAW). Selects the lower CAS align/alarm bits (xyxx) to be sourced from the lower 4 bits of the TS1 register.

0 = do not source the lower CAS align/alarm bits from the TR.TS1 register

1 = source the lower CAS alarm align/bits from the TR.TS1 register

Register Name: **TR.SSIE4**
 Register Description: **Software Signaling Insertion Enable 4**
 Register Address: **0Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Software Signaling Insertion Enable for Channels 30 to 23 (CH30 to CH23). These bits determine which channels are to have signaling inserted from the transmit signaling registers.

0 = do not source signaling data from the TR.TSx registers for this channel

1 = source signaling data from the TR.TSx registers for this channel

Register Name: **TR.T1RDMR1**
 Register Description: **T1 Receive Digital-Milliwatt Enable Register 1**
 Register Address: **0Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Digital-Milliwatt Enable for Channels 8 to 1 (CH8 to CH1)

0 = do not affect the receive data associated with this channel

1 = replace the receive data associated with this channel with digital-milliwatt code

Register Name: **TR.T1RDMR2**
 Register Description: **T1 Receive Digital-Milliwatt Enable Register 2**
 Register Address: **0Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|-----|
| Name | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Digital-Milliwatt Enable for Channels 16 to 9 (CH16 to CH9)

0 = do not affect the receive data associated with this channel

1 = replace the receive data associated with this channel with digital-milliwatt code

Register Name: **TR.T1RDMR3**
 Register Description: **T1 Receive Digital-Milliwatt Enable Register 3**
 Register Address: **0Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Digital-Milliwatt Enable for Channels 24 to 17 (CH24 to CH17)

0 = do not affect the receive data associated with this channel

1 = replace the receive data associated with this channel with digital-milliwatt code

Register Name: **TR.IDR**
 Register Description: **Device Identification Register**
 Register Address: **0Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| Default | 1 | 0 | 0 | 0 | X | X | X | X |

Bits 7 to 4: Device ID (ID7 to ID4). The upper four bits of TR.IDR are used to display the transceiver ID.

Bits 3 to 0: Chip Revision Bits (ID3 to ID0). The lower four bits of TR.IDR are used to display the die revision of the chip. ID0 is the LSB of a decimal code that represents the chip revision.

Register Name: **TR.INFO1**
 Register Description: **Information Register 1**
 Register Address: **10h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|-----|------|------|------|-----|
| Name | RPDV | TPDV | COFA | 8ZD | 16ZD | SEFE | B8ZS | FBE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Pulse-Density Violation Event (RPDV). Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.

Bit 6: Transmit Pulse-Density Violation Event (TPDV). Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.

Bit 5: Change-of-Frame Alignment Event (COFA). Set when the last resync resulted in a change-of-frame or multiframe alignment.

Bit 4: Eight Zero-Detect Event (8ZD). Set when a string of at least eight consecutive 0s (regardless of the length of the string) have been received at RPOSI and RNEGI.

Bit 3: Sixteen Zero-Detect Event (16ZD). Set when a string of at least 16 consecutive 0s (regardless of the length of the string) have been received at RPOSI and RNEGI.

Bit 2: Severely Errored Framing Event (SEFE). Set when two out of six framing bits (Ft or FPS) are received in error.

Bit 1: B8ZS Codeword Detect Event (B8ZS). Set when a B8ZS codeword is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not by TR.T1TCR2.7. Useful for automatically setting the line coding.

Bit 0: Frame Bit-Error Event (FBE). Set when an Ft (D4) or FPS (ESF) framing bit is received in error.

Register Name: **TR.INFO2**
 Register Description: **Information Register 2**
 Register Address: **11h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|----|------|------|-----|-----|-----|-----|
| Name | BSYNC | BD | TCLE | TOCD | RL3 | RL2 | RL1 | RL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: BERT Real-Time Synchronization Status (BSYNC). Real-time status of the synchronizer (this bit is not latched). This bit is set when the incoming pattern matches for 32 consecutive bit positions. It is cleared when six or more bits out of 64 are received in error. Refer to BSYNC in the BERT status register, TR.SR9, for an interrupt-generating version of this signal.

Bit 6: BOC Detected (BD). A real-time bit that is set high when the BOC detector is presently seeing a valid sequence and set low when no BOC is currently being detected.

Bit 5: Transmit Current-Limit Exceeded (TCLE). A real-time bit that is set when the 50mA (RMS) current limiter is activated, whether the current limiter is enabled or not.

Bit 4: Transmit Open-Circuit Detect (TOCD). A real-time bit that is set when the device detects that the TTIP and TRING outputs are open-circuited.

Bits 3 to 0: Receive Level Bits (RL3 to RL0). Real-time bits.

| RL3 | RL2 | RL1 | RL0 | Receive Level (dB) |
|-----|-----|-----|-----|--------------------|
| 0 | 0 | 0 | 0 | Greater than -2.5 |
| 0 | 0 | 0 | 1 | -2.5 to -5.0 |
| 0 | 0 | 1 | 0 | -5.0 to -7.5 |
| 0 | 0 | 1 | 1 | -7.5 to -10.0 |
| 0 | 1 | 0 | 0 | -10.0 to -12.5 |
| 0 | 1 | 0 | 1 | -12.5 to -15.0 |
| 0 | 1 | 1 | 0 | -15.0 to -17.5 |
| 0 | 1 | 1 | 1 | -17.5 to -20.0 |
| 1 | 0 | 0 | 0 | -20.0 to -22.5 |
| 1 | 0 | 0 | 1 | -22.5 to -25.0 |
| 1 | 0 | 1 | 0 | -25.0 to -27.5 |
| 1 | 0 | 1 | 1 | -27.5 to -30.0 |
| 1 | 1 | 0 | 0 | -30.0 to -32.5 |
| 1 | 1 | 0 | 1 | -32.5 to -35.0 |
| 1 | 1 | 1 | 0 | -35.0 to -37.5 |
| 1 | 1 | 1 | 1 | Less than -37.5 |

Note: RL0 through RL3 only indicate the signal range as specified by the EGL bit in TR.LIC1. Example: if EGL = 1 and in T1 mode, RL0 through RL3 will only indicate a signal range of >-2.5dB to -15dB even if the signal is < -15dB.

Register Name: **TR.INFO3**
 Register Description: **Information Register 3**
 Register Address: **12h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|-------|-------|-------|
| Name | — | — | — | — | — | CRCRC | FASRC | CASRC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2: CRC Resync Criteria Met Event (CRCRC). Set when 915/1000 codewords are received in error.

Bit 1: FAS Resync Criteria Met Event (FASRC). Set when three consecutive FAS words are received in error. Note: During a CRC resync the FAS synchronizer is brought online to verify the FAS alignment. If during this process an FAS emulator exists, the FAS synchronizer may temporarily align to the emulator. The FASRC will go active indicating a search for a valid FAS has been activated.

Bit 0: CAS Resync Criteria Met Event (CASRC). Set when two consecutive CAS MF alignment words are received in error.

Register Name: **TR.IIR1**
 Register Description: **Interrupt Information Register 1**
 Register Address: **14h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Status Register 8 to 1 (SR[8:1]). When set to 1, these bits indicate that an enabled interrupt is active in the associated T1/E1/J1 status register.

Register Name: **TR.IIR2**
 Register Description: **Interrupt Information Register 2**
 Register Address: **15h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|-----|
| Name | — | — | — | — | — | — | — | SR9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 0: Status Register 9 (SR9). When set to 1, this bit indicates that an enabled interrupt is active in the associated T1/E1/J1 status register.

Register Name: **TR.SR1**
 Register Description: **Status Register 1**
 Register Address: **16h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-------|------|------|------|------|--------|
| Name | ILUT | TIMER | RSCOS | JALT | LRCL | TCLE | TOCD | LOLITC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Input Level Under Threshold (ILUT). This bit is set whenever the input level at RTIP and RRING falls below the threshold set by the value in TR.CCR4.4 through TR.CCR4.7. The level must remain below the programmed threshold for approximately 50ms for this bit to be set. This is a double interrupt bit (Section 9.6).

Bit 6: Timer Event (TIMER). Follows the error-counter update interval as determined by the ECUS bit in the error-counter configuration register (TR.ERCNT).

T1: set on increments of 1 second or 42ms based on RCLKn

E1: set on increments of 1 second or 62.5ms based on RCLKn

Bit 5: Receive Signaling Change-of-State Event (RSCOS). Set when any channel selected by the receive signaling change-of-state interrupt-enable registers (TR.RSCSE1 through TR.RSCSE4) changes signaling state.

Bit 4: Jitter Attenuator Limit Trip Event (JALT). Set when the jitter attenuator FIFO reaches to within 4 bits of its useful limit. This bit is cleared when read. Useful for debugging jitter attenuation operation.

Bit 3: Line Interface Receive Carrier Loss Condition (LRCL). Set when the carrier signal is lost. This is a double interrupt bit (Section 9.6).

Bit 2: Transmit Current-Limit Exceeded Condition (TCLE). Set when the 50mA (RMS) current limiter is activated, whether the current limiter is enabled or not. This is a double interrupt bit (Section 9.6).

Bit 1: Transmit Open-Circuit Detect Condition (TOCD). Set when the device detects that the TTIP and TRING outputs are open-circuited. This is a double interrupt bit (Section 9.6).

Bit 0: Loss of Line Interface Transmit Clock Condition (LOLITC). Set when TDCLKI has not transitioned for one channel time. This is a double interrupt bit (Section 9.6).

Register Name: **TR.IMR1**
 Register Description: **Interrupt Mask Register 1**
 Register Address: **17h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-------|------|------|------|------|--------|
| Name | ILUT | TIMER | RSCOS | JALT | LRCL | TCLE | TOCD | LOLITC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Input Level Under Threshold (ILUT)

0 = interrupt masked
 1 = interrupt enabled

Bit 6: Timer Event (TIMER)

0 = interrupt masked
 1 = interrupt enabled

Bit 5: Receive Signaling Change-of-State Event (RSCOS)

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Jitter Attenuator Limit Trip Event (JALT)

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Line Interface Receive Carrier-Loss Condition (LRCL)

0 = interrupt masked
 1 = interrupt enabled—generates interrupts on rising and falling edges

Bit 2: Transmit Current-Limit Exceeded Condition (TCLE)

0 = interrupt masked
 1 = interrupt enabled—generates interrupts on rising and falling edges

Bit 1: Transmit Open-Circuit Detect Condition (TOCD)

0 = interrupt masked
 1 = interrupt enabled—generates interrupts on rising and falling edges

Bit 0: Loss-of-Transmit Clock Condition (LOLITC)

0 = interrupt masked
 1 = interrupt enabled—generates interrupts on rising and falling edges

Register Name: **TR.SR2**
 Register Description: **Status Register 2**
 Register Address: **18h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|------|------|------|------|
| Name | RYELC | RUA1C | FRCLC | RLOSC | RYEL | RUA1 | FRCL | RLOS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Yellow Alarm Clear Event (RYELC) (T1 Only). Set when the receive Yellow Alarm condition is no longer detected.

Bit 6: Receive Unframed All-Ones Clear Event (RUA1C). Set when the unframed all 1s condition is no longer detected.

Bit 5: Framer Receive Carrier-Loss Clear Event (FRCLC). Set when the carrier loss condition at RPOSI and RNEGI is no longer detected.

Bit 4: Receive Loss-of-Sync Clear Event (RLOSC). Set when the framer achieves synchronization; remains set until read.

Bit 3: Receive Yellow Alarm Condition (RYEL) (T1 Only). Set when a Yellow Alarm is received at RPOSI and RNEGI.

Bit 2: Receive Unframed All-Ones (T1 Blue Alarm, E1 AIS) Condition (RUA1). Set when an unframed all 1s code is received at RPOSI and RNEGI.

Bit 1: Framer Receive Carrier-Loss Condition (FRCL). Set when 255 (or 2048 if TR.E1RCR2.0 = 1) E1 mode or 192 T1 mode consecutive 0s have been detected at RPOSI and RNEGI.

Bit 0: Receive Loss-of-Sync Condition (RLOS). Set when the transceiver is not synchronized to the received data stream.

Register Name: **TR.IMR2**
 Register Description: **Interrupt Mask Register 2**
 Register Address: **19h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|------|------|------|------|
| Name | RYELC | RUA1C | FRCLC | RLOSC | RYEL | RUA1 | FRCL | RLOS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Yellow Alarm Clear Event (RYELC)

0 = interrupt masked
 1 = interrupt enabled

Bit 6: Receive Unframed All-Ones Condition Clear Event (RUA1C)

0 = interrupt masked
 1 = interrupt enabled

Bit 5: Framer Receive Carrier Loss Condition Clear (FRCLC)

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Receive Loss-of-Sync Clear Event (RLOSC)

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Receive Yellow Alarm Condition (RYEL)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising edge only

Bit 2: Receive Unframed All-Ones (Blue Alarm) Condition (RUA1)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising edge only

Bit 1: Framer Receive Carrier Loss Condition (FRCL)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising edge only

Bit 0: Receive Loss-of-Sync Condition (RLOS)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising edge only

Register Name: **TR.SR3**
 Register Description: **Status Register 3**
 Register Address: **1Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|-----|-----|------|------|--------|------|-----|
| Name | LSPARE | LDN | LUP | LOTC | LORC | V52LNK | RDMA | RRA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Spare Code Detected Condition (LSPARE) (T1 Only). Set when the spare code as defined in the TR.RSCD1/2 registers is being received. This is a double interrupt bit. See Section [9.6](#).

Bit 6: Loop-Down Code Detected Condition (LDN) (T1 Only). Set when the loop down code as defined in the TR.RDNC1/2 register is being received. This is a double interrupt bit. See Section 9.6.

Bit 5: Loop-Up Code Detected Condition (LUP) (T1 Only). Set when the loop-up code as defined in the TR.RUPCD1/2 register is being received. This is a double interrupt bit. See Section 9.6.

Bit 4: Loss-of-Transmit Clock Condition (LOTC). Set when the TCLKT pin has not transitioned for one channel time. Forces the LOTC pin high if enabled by TR.CCR1.0. This is a double interrupt bit. See Section 9.6.

Bit 3: Loss-of-Receive Clock Condition (LORC). Set when the RCLKI pin has not transitioned for one channel time. This is a double interrupt bit. See Section 9.6.

Bit 2: V5.2 Link Detected Condition (V52LNK) (E1 Only). Set on detection of a V5.2 link identification signal (G.965). This is a double interrupt bit. See Section 9.6.

Bit 1: Receive Distant MF Alarm Condition (RDMA) (E1 Only). Set when bit 6 of time slot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode. This is a double interrupt bit. See Section 9.6.

Bit 0: Receive Remote Alarm Condition (RRA) (E1 Only). Set when a remote alarm is received at RPOSI and RNEGI. This is a double interrupt bit. See Section 9.6.

Register Name: **TR.IMR3**
 Register Description: **Interrupt Mask Register 3**
 Register Address: **1Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|-----|-----|------|------|--------|------|-----|
| Name | LSPARE | LDN | LUP | LOTG | LORC | V52LNK | RDMA | RRA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Spare Code Detected Condition (LSPARE)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 6: Loop-Down Code-Detected Condition (LDN)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 5: Loop-Up Code-Detected Condition (LUP)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 4: Loss-of-Transmit Clock Condition (LOTG)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 3: Loss-of-Receive Clock Condition (LORC)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 2: V5.2 Link Detected Condition (V52LNK)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 1: Receive Distant MF Alarm Condition (RDMA)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 0: Receive Remote Alarm Condition (RRA)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Register Name: **TR.SR4**
 Register Description: **Status Register 4**
 Register Address: **1Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|------|-------|-----|-----|-----|------|-----|
| Name | RAIS-CI | RSAO | RS AZ | TMF | TAF | RMF | RCMF | RAF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive AIS-CI Event (RAIS-CI) (T1 Only). Set when the receiver detects the AIS-CI pattern as defined in ANSI T1.403.

Bit 6: Receive Signaling All-Ones Event (RSAO) (E1 Only). Set when the contents of time slot 16 contains fewer than three 0s over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.

Bit 5: Receive Signaling All-Zeros Event (RS AZ) (E1 Only). Set when over a full MF, time slot 16 contains all 0s.

Bit 4: Transmit Multiframe Event (TMF)

E1 Mode: Set every 2ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.

T1 Mode: Set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries.

Bit 3: Transmit Align Frame Event (TAF) (E1 Only). Set every 250 μ s at the beginning of align frames. Used to alert the host that the TR.TAF and TR.TNAF registers need to be updated.

Bit 2: Receive Multiframe Event (RMF)

E1 Mode: Set every 2ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.

T1 Mode: Set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries.

Bit 1: Receive CRC4 Multiframe Event (RCMF) (E1 Only). Set on CRC4 multiframe boundaries; continues to set every 2ms on an arbitrary boundary if CRC4 is disabled.

Bit 0: Receive Align Frame Event (RAF) (E1 Only). Set every 250 μ s at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the TR.RAF and TR.RNAF registers.

Register Name: **TR.IMR4**
 Register Description: **Interrupt Mask Register 4**
 Register Address: **1Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|------|------|-----|-----|-----|------|-----|
| Name | RAIS-CI | RSAO | RSAZ | TMF | TAF | RMF | RCMF | RAF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive AIS-CI Event (RAIS-CI)

0 = interrupt masked
 1 = interrupt enabled

Bit 6: Receive Signaling All-Ones Event (RSAO)

0 = interrupt masked
 1 = interrupt enabled

Bit 5: Receive Signaling All-Zeros Event (RSAZ)

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Transmit Multiframe Event (TMF)

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Transmit Align Frame Event (TAF)

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Receive Multiframe Event (RMF)

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Receive CRC4 Multiframe Event (RCMF)

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Receive Align Frame Event (RAF)

0 = interrupt masked
 1 = interrupt enabled

Register Name: **TR.SR5**
 Register Description: **Status Register 5**
 Register Address: **1Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|-------|-------|------|-------|-------|
| Name | — | — | TESF | TESEM | TSLIP | RESF | RESEM | RSLIP |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Transmit Elastic Store Full Event (TESF). Set when the transmit elastic store buffer fills and a frame is deleted.

Bit 4: Transmit Elastic Store Empty Event (TESEM). Set when the transmit elastic store buffer empties and a frame is repeated.

Bit 3: Transmit Elastic Store Slip-Occurrence Event (TSLIP). Set when the transmit elastic store has either repeated or deleted a frame.

Bit 2: Receive Elastic Store Full Event (RESF). Set when the receive elastic store buffer fills and a frame is deleted.

Bit 1: Receive Elastic Store Empty Event (RESEM). Set when the receive elastic store buffer empties and a frame is repeated.

Bit 0: Receive Elastic Store Slip-Occurrence Event (RSLIP). Set when the receive elastic store has either repeated or deleted a frame.

Register Name: **TR.IMR5**
 Register Description: **Interrupt Mask Register 5**
 Register Address: **1Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|-------|-------|------|-------|-------|
| Name | — | — | TESF | TESEM | TSLIP | RESF | RESEM | RSLIP |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Transmit Elastic Store Full Event (TESF)

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Transmit Elastic Store Empty Event (TESEM)

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Transmit Elastic Store Slip-Occurrence Event (TSLIP)

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Receive Elastic Store Full Event (RESF)

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Receive Elastic Store Empty Event (RESEM)

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Receive Elastic Store Slip-Occurrence Event (RSLIP)

0 = interrupt masked
 1 = interrupt enabled

Register Name: **TR.SR6, TR.SR7**
 Register Description: **HDLC #1 Status Register 6**
HDLC #2 Status Register 7
 Register Address: **20h, 22h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-------|-----|-----|------|-----|------|-----|
| Name | — | TMEND | RPE | RPS | RHWM | RNE | TLWM | TNF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Transmit Message-End Event (TMEND). Set when the transmit HDLC controller has finished sending a message. This is a latched bit and is cleared when read.

Bit 5: Receive Packet-End Event (RPE). Set when the HDLC controller detects either the finish of a valid message (i.e., CRC check complete) or when the controller has experienced a message fault such as a CRC checking error, or an overrun condition, or an abort has been seen. This is a latched bit and is cleared when read.

Bit 4: Receive Packet-Start Event (RPS). Set when the HDLC controller detects an opening byte. This is a latched bit and is cleared when read.

Bit 3: Receive FIFO Above High-Watermark Condition (RHWM). Set when the receive 128-byte FIFO fills beyond the high watermark as defined by the receive high-watermark register (TR.RHWMR).

Bit 2: Receive FIFO Not Empty Condition (RNE). Set when the receive 128-byte FIFO has at least 1 byte available for a read.

Bit 1: Transmit FIFO Below Low-Watermark Condition (TLWM). Set when the transmit 128-byte FIFO empties beyond the low watermark as defined by the transmit low-watermark register (TR.TLWMR).

Bit 0: Transmit FIFO Not Full Condition (TNF). Set when the transmit 128-byte FIFO has at least 1 byte available.

Register Name: **TR.IMR6, TR.IMR7**
 Register Description: **HDLC # 1 Interrupt Mask Register 6**
HDLC # 2 Interrupt Mask Register 7
 Register Address: **21h, 23h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-------|-----|-----|------|-----|------|-----|
| Name | — | TMEND | RPE | RPS | RHWM | RNE | TLWM | TNF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Transmit Message-End Event (TMEND)

0 = interrupt masked
 1 = interrupt enabled

Bit 5: Receive Packet-End Event (RPE)

0 = interrupt masked
 1 = interrupt enabled

Bit 4: Receive Packet-Start Event (RPS)

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Receive FIFO Above High-Watermark Condition (RHWM)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising edge only

Bit 2: Receive FIFO Not Empty Condition (RNE)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising edge only

Bit 1: Transmit FIFO Below Low-Watermark Condition (TLWM)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising edge only

Bit 0: Transmit FIFO Not Full Condition (TNF)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising edge only

Register Name: **TR.INFO5, TR.INFO6**
 Register Description: **HDLC #1 Information Register**
HDLC #2 Information Register
 Register Address: **2Eh, 2Fh**

| | | | | | | | | |
|---------|---|---|-------|-------|-------|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | EMPTY | TFULL | EMPTY | PS2 | PS1 | PS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Transmit FIFO Empty (EMPTY). A real-time bit that is set high when the FIFO is empty.

Bit 4: Transmit FIFO Full (TFULL). A real-time bit that is set high when the FIFO is full.

Bit 3: Receive FIFO Empty (EMPTY). A real-time bit that is set high when the receive FIFO is empty.

Bits 2 to 0: Receive Packet Status (PS0 to PS2). These are real-time bits indicating the status as of the last read of the receive FIFO.

| PS2 | PS1 | PS0 | Packet Status |
|-----|-----|-----|--|
| 0 | 0 | 0 | In Progress |
| 0 | 0 | 1 | Packet OK: Packet ended with correct CRC codeword |
| 0 | 1 | 0 | CRC Error: A closing flag was detected, preceded by a corrupt CRC codeword |
| 0 | 1 | 1 | Abort: Packet ended because an abort signal was detected (seven or more 1s in a row). |
| 1 | 0 | 0 | Overrun: HDLC controller terminated reception of packet because receive FIFO is full. |

Register Name: **TR.INFO4**
 Register Description: **HDLC Event Information Register #4**
 Register Address: **2Dh**

| | | | | | | | | |
|---------|---|---|---|---|-------|-------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | H2UDR | H2OBT | H1UDR | H1OBT |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: HDLC #2 Transmit FIFO Underrun Event (H2UDR). Set when the transmit FIFO empties out without having seen the TMEND bit set. An abort is automatically sent. This bit is latched and is cleared when read.

Bit 2: HDLC #2 Opening Byte Event (H2OBT). Set when the next byte available in the receive FIFO is the first byte of a message.

Bit 1: HDLC #1 Transmit FIFO Underrun Event (H1UDR). Set when the transmit FIFO empties out without having seen the TMEND bit set. An abort is automatically sent. This bit is latched and is cleared when read.

Bit 0: HDLC #1 Opening Byte Event (H1OBT). Set when the next byte available in the receive FIFO is the first byte of a message.

Register Name: **TR.SR8**
 Register Description: **Status Register 8**
 Register Address: **24h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|--------|-------|-------|-------|------|
| Name | — | — | BOCC | RFDLAD | RFDLF | TFDLE | RMTCH | RBOC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: BOC Clear Event (BOCC). Set when 30 FDL bits occur without an abort sequence.

Bit 4: RFDL Abort Detect Event (RFDLAD). Set when eight consecutive 1s are received on the FDL.

Bit 3: RFDL Register Full Event (RFDLF). Set when the receive FDL buffer (TR.RFDL) fills to capacity.

Bit 2: TFDL Register Empty Event (TFDLE). Set when the transmit FDL buffer (TR.TFDL) empties.

Bit 1: Receive FDL Match Event (RMTCH). Set whenever the contents of the TR.RFDL register matches TR.RFDLM1 or TR.RFDLM2.

Bit 0: Receive BOC Detector Change-of-State Event (RBOC). Set whenever the BOC detector sees a change of state to a valid BOC. The setting of this bit prompts the user to read the TR.RFDL register.

Register Name: **TR.IMR8**
 Register Description: **Interrupt Mask Register 8**
 Register Address: **25h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|--------|-------|-------|-------|------|
| Name | — | — | BOCC | RFDLAD | RFDLF | TFDLE | RMTCH | RBOC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: BOC Clear Event (BOCC)

0 = interrupt masked
 1 = interrupt enabled

Bit 4: RFDL Abort Detect Event (RFDLAD)

0 = interrupt masked
 1 = interrupt enabled

Bit 3: RFDL Register Full Event (RFDLF)

0 = interrupt masked
 1 = interrupt enabled

Bit 2: TFDL Register Empty Event (TFDLE)

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Receive FDL Match Event (RMTCH)

0 = interrupt masked
 1 = interrupt enabled

Bit 0: Receive BOC Detector Change-of-State Event (RBOC)

0 = interrupt masked
 1 = interrupt enabled

Register Name: **TR.SR9**
 Register Description: **Status Register 9**
 Register Address: **26h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|------|------|------|-------|-------|
| Name | — | BBED | BBCO | BECO | BRA1 | BRA0 | BRLOS | BSYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: BERT Bit-Error Detected (BED) Event (BBED). A latched bit that is set when a bit error is detected. The receive BERT must be in synchronization for it to detect bit errors. Cleared when read.

Bit 5: BERT Bit-Counter Overflow Event (BBCO). A latched bit that is set when the 32-bit BERT bit counter (BBC) overflows. Cleared when read and is not set again until another overflow occurs.

Bit 4: BERT Error-Counter Overflow (BECO) Event (BECO). A latched bit that is set when the 24-bit BERT error counter (BEC) overflows. Cleared when read and is not set again until another overflow occurs.

Bit 3: BERT Receive All-Ones Condition (BRA1). A latched bit that is set when 32 consecutive 1s are received. Allowed to be cleared once a 0 is received. This is a double interrupt bit (Section [9.6](#)).

Bit 2: BERT Receive All-Zeros Condition (BRA0). A latched bit that is set when 32 consecutive 0s are received. Allowed to be cleared once a 1 is received. This is a double interrupt bit (Section [9.6](#)).

Bit 1: BERT Receive Loss-of-Synchronization Condition (BRLOS). A latched bit that is set whenever the receive BERT begins searching for a pattern. Once synchronization is achieved, this bit remains set until read. This is a double interrupt bit (Section [9.6](#)).

Bit 0: BERT in Synchronization Condition (BSYNC). Set when the incoming pattern matches for 32 consecutive bit positions. Refer to BSYNC in the TR.INFO2 register for a real-time version of this bit. This is a double interrupt bit (Section [9.6](#)).

Register Name: **TR.IMR9**
 Register Description: **Interrupt Mask Register 9**
 Register Address: **27h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|------|------|------|-------|-------|
| Name | — | BBED | BBCO | BECO | BRA1 | BRA0 | BRLOS | BSYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Bit-Error Detected Event (BBED)

0 = interrupt masked
 1 = interrupt enabled

Bit 5: BERT Bit-Counter Overflow Event (BBCO)

0 = interrupt masked
 1 = interrupt enabled

Bit 4: BERT Error-Counter Overflow Event (BECO)

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Receive All-Ones Condition (BRA1)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 2: Receive All-Zeros Condition (BRA0)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 1: Receive Loss-of-Synchronization Condition (BRLOS)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Bit 0: BERT in Synchronization Condition (BSYNC)

0 = interrupt masked
 1 = interrupt enabled—interrupts on rising and falling edges

Register Name: **TR.PCPR**
 Register Description: **Per-Channel Pointer Register**
 Register Address: **28h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|-------|------|------|-------|-------|------|------|
| Name | RSAOICS | RSRCS | RFCS | BRCS | THSCS | PEICS | TFCS | BTCS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Signaling All-Ones Insertion Channel Select (RSAOICS)

Bit 6: Receive Signaling Reinsertion Channel Select (RSRCS)

Bit 5: Receive Fractional Channel Select (RFCS)

Bit 4: Bert Receive Channel Select (BRCS)

Bit 3: Transmit Hardware Signaling Channel Select (THSCS)

Bit 2: Payload Error Insert Channel Select (PEICS)

Bit 1: Transmit Fractional Channel Select (TFCS)

Bit 0: Bert Transmit Channel Select (BTCS)

See Section [10.2](#) for a general overview of per-channel operation. See Section [10.10](#) for more information on per-channel idle code generation. See Section 10.2 for more information on per-channel loopback operation.

Register Name: **TR.PCDR1**
 Register Description: **Per-Channel Data Register 1**
 Register Address: **29h**

| | | | | | | | | |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | — | — | — |
| Default | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |

Register Name: **TR.PCDR2**
 Register Description: **Per-Channel Data Register 2**
 Register Address: **2Ah**

| | | | | | | | | |
|---------|------|------|------|------|------|------|------|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | — | — | — |
| Default | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |

Register Name: **TR.PCDR3**
 Register Description: **Per-Channel Data Register 3**
 Register Address: **2Bh**

| | | | | | | | | |
|---------|------|------|------|------|------|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | — | — | — |
| Default | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |

Register Name: **TR.PCDR4**
 Register Description: **Per-Channel Data Register 4**
 Register Address: **2Ch**

| | | | | | | | | |
|---------|------|------|------|------|------|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | — | — | — |
| Default | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |

See Section [10.2](#) for a general overview of per-channel operation. See Section [10.10](#) for more information on per-channel idle code generation. See Section 10.2 for more information on per-channel loopback operation.

Register Name: **TR.INFO7**
 Register Description: **Information Register 7 (Real-Time, Non-Latched Register)**
 Register Address: **30h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|-------|-------|--------|
| Name | CSC5 | CSC4 | CSC3 | CSC2 | CSC0 | FASSA | CASSA | CRC4SA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 3: CRC4 Sync Counter Bits (CSC5 to CSC2, CSC0). The CRC4 sync counter increments each time the 8ms CRC4 multiframe search times out. The counter is cleared when the framer has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (TR.E1RCR1.3 = 0). This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC4 level. ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400ms, then the search should be abandoned and proper action taken. The CRC4 sync counter rolls over. CSC0 is the LSB of the 6-bit counter. (Note: The bit next to LSB is not accessible. CSC1 is omitted to allow resolution to >400ms using 5 bits.) These are read-only, non-latched, real-time bits. It is not necessary to precede the read of these bits with a write.

Bit 2: FAS Sync Active (FASSA). Set while the synchronizer is searching for alignment at the FAS level. This is a read-only, non-latched, real-time bit. It is not necessary to precede the read of this bit with a write.

Bit 1: CAS MF Sync Active (CASSA). Set while the synchronizer is searching for the CAS MF alignment word. This is a read-only, non-latched, real-time bit. It is not necessary to precede the read of this bit with a write.

Bit 0: CRC4 MF Sync Active (CRC4SA). Set while the synchronizer is searching for the CRC4 MF alignment word. This is a read-only, non-latched, real-time bit. It is not necessary to precede the read of this bit with a write.

Register Name: **TR.H1RC, TR.H2RC**
 Register Description: **HDLC #1 Receive Control
 HDLC #2 Receive Control**
 Register Address: **31h, 32h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|------|---|---|---|---|---|------|
| Name | RHR | RHMS | — | — | — | — | — | RSFD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive HDLC Reset (RHR). Resets the receive HDLC controller and flushes the receive FIFO. Must be cleared and set again for a subsequent reset.

0 = normal operation

1 = reset receive HDLC controller and flush the receive FIFO

Bit 6: Receive HDLC Mapping Select (RHMS)

0 = receive HDLC assigned to channels

1 = receive HDLC assigned to FDL (T1 mode), Sa bits (E1 mode)

Bits 5 to 1: Unused, must be set to 0 or proper operation.

Bit 0: Receive SS7 Fill-In Signal Unit Delete (RSFD)

0 = normal operation; all FISUs are stored in the receive FIFO and reported to the host.

1 = When a consecutive FISU having the same BSN the previous FISU is detected, it is deleted without host intervention.

Register Name: **TR.E1RCR1**
 Register Description: **E1 Receive Control Register 1**
 Register Address: **33h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-----|-------|--------|
| Name | RSERC | RSIGM | RHDB3 | RG802 | RCRC4 | FRC | SYNCE | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: RSERO Control (RSERC)

0 = allow RSERO to output data as received under all conditions
 1 = force RSERO to 1 under loss-of-frame alignment conditions

Bit 6: Receive Signaling Mode Select (RSIGM)

0 = CAS signaling mode
 1 = CCS signaling mode

Bit 5: Receive HDB3 Enable (RHDB3)

0 = HDB3 disabled
 1 = HDB3 enabled

Bit 4: Receive G.802 Enable (RG802). See Section [10.10](#) for details.

0 = do not force RCHBLK high during bit 1 of time slot 26
 1 = force RCHBLK high during bit 1 of time slot 26

Bit 3: Receive CRC4 Enable (RCRC4)

0 = CRC4 disabled
 1 = CRC4 enabled

Bit 2: Frame Resync Criteria (FRC)

0 = resync if FAS received in error three consecutive times
 1 = resync if FAS or bit 2 of non-FAS is received in error three consecutive times

Bit 1: Sync Enable (SYNCE)

0 = auto resync enabled
 1 = auto resync disabled

Bit 0: Resync (RESYNC). When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

Register Name: **TR.E1RCR2**
 Register Description: **E1 Receive Control Register 2**
 Register Address: **34h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|------|
| Name | — | — | — | — | — | — | — | RCLA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Receive Carrier-Loss (RCL) Alternate Criteria (RCLA). Defines the criteria for a receive carrier-loss condition for both the framer and LIU.

0 = RCL declared upon 255 consecutive 0s (125 μ s)
 1 = RCL declared upon 2048 consecutive 0s (1ms)

Register Name: **TR.E1TCR1**
 Register Description: **E1 Transmit Control Register 1**
 Register Address: **35h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|-------|-------|-------|
| Name | TFPT | T16S | TUA1 | TSiS | TSA1 | THDB3 | TG802 | TCRC4 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Time Slot 0 Pass-Through (TFPT)

0 = FAS bits/Sa bits/remote alarm sourced internally from the TR.TAF and TR.TNAF registers
 1 = FAS bits/Sa bits/remote alarm sourced from TSERI

Bit 6: Transmit Time Slot 16 Data Select (T16S). See Section [10.10](#) for details.

0 = time slot 16 determined by the TR.SSiEx registers and the THSCS function in the TR.PCPR register
 1 = source time slot 16 from TR.TS1 to TR.TS16 registers

Bit 5: Transmit Unframed All Ones (TUA1)

0 = transmit data normally
 1 = transmit an unframed all-ones code at TPOSO and TNEGO

Bit 4: Transmit International Bit Select (TSiS)

0 = sample Si bits at TSERI pin
 1 = source Si bits from TR.TAF and TR.TNAF registers (in this mode, TR.E1TCR1.7 must be set to 0)

Bit 3: Transmit Signaling All Ones (TSA1)

0 = normal operation
 1 = force time slot 16 in every frame to all ones

Bit 2: Transmit HDB3 Enable (THDB3)

0 = HDB3 disabled
 1 = HDB3 enabled

Bit 1: Transmit G.802 Enable (TG802). See Section [10.10](#) for details.

0 = do not force TCHBLK high during bit 1 of time slot 26
 1 = force TCHBLK high during bit 1 of time slot 26

Bit 0: Transmit CRC4 Enable (TCRC4)

0 = CRC4 disabled
 1 = CRC4 enabled

Register Name: **TR.E1TCR2**
 Register Description: **E1 Transmit Control Register 2**
 Register Address: **36h**

| | | | | | | | | |
|---------|---|---|---|---|---|------|------|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | AEBE | AAIS | ARA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2: Automatic E-Bit Enable (AEBE)

0 = E-bits not automatically set in the transmit direction
 1 = E-bits automatically set in the transmit direction

Bit 1: Automatic AIS Generation (AAIS)

0 = disabled
 1 = enabled

Bit 0: Automatic Remote Alarm Generation (ARA)

0 = disabled
 1 = enabled

Register Name: **TR.BOCC**
 Register Description: **BOC Control Register**
 Register Address: **37h**

| | | | | | | | | |
|---------|---|---|---|-------|-----|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | RBOCE | RBR | RBF1 | RBF0 | SBOC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Receive BOC Enable (RBOCE). Enables the receive BOC function. The TR.RFDL register reports the received BOC code and two information bits when this bit is set.

0 = receive BOC function disabled
 1 = receive BOC function enabled; the TR.RFDL register reports BOC messages and information

Bit 3: Receive BOC Reset (RBR). A 0-to-1 transition resets the BOC circuitry. Must be cleared and set again for a subsequent reset.

Bits 2 and 1: Receive BOC Filter Bits (RBF1, RBF0). The BOC filter sets the number of consecutive patterns that must be received without error prior to an indication of a valid message.

| RBF1 | RBF0 | Consecutive BOC Codes for Valid Sequence Identification |
|------|------|---|
| 0 | 0 | None |
| 0 | 1 | 3 |
| 1 | 0 | 5 |
| 1 | 1 | 7 |

Bit 0: Send BOC (SBOC). Set = 1 to transmit the BOC code placed in bits 0 to 5 of the TR.TFDL register.

Register Name: **TR.RSINFO1, TR.RSINFO2, TR.RSINFO3, TR.RSINFO4**
 Register Description: **Receive Signaling Change-of-State Information**
 Register Address: **38h, 39h, 3Ah, 3Bh**

| (MSB) | | | | | | | (LSB) | |
|-------|------|------|------|------|------|------|-------|---------|
| CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RSINFO1 |
| CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RSINFO2 |
| CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RSINFO3 |
| | | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | RSINFO4 |

When a channel's signaling data changes state, the respective bit in registers TR.RSINFO1–4 is set. An interrupt is generated if the channel was also enabled as an interrupt source by setting the appropriate bit in TR.RSCSE1–4. The bit remains set until read.

Register Name: **TR.RSCSE1, TR.RSCSE2, TR.RSCSE3, TR.RSCSE4**
 Register Description: **Receive Signaling Change-of-State Interrupt Enable**
 Register Address: **3Ch, 3Dh, 3Eh, 3Fh**

| (MSB) | | | | | | | (LSB) | |
|-------|------|------|------|------|------|------|-------|--------|
| CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RSCSE1 |
| CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RSCSE2 |
| CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RSCSE3 |
| | | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | RSCSE4 |

Setting any of the CH1–CH30 bits in the TR.RSCSE1–TR.RSCSE4 registers causes an interrupt when that channel's signaling data changes state.

Register Name: **TR.SIGCR**
 Register Description: **Signaling Control Register**
 Register Address: **40h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|---|---|-----|-----|------|------|-------|
| Name | GRSRE | — | — | RFE | RFF | RCCS | TCCS | FRSAO |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Global Receive Signaling Reinsertion Enable (GRSRE). This bit allows the user to reinsert all signaling channels without programming all channels through the per-channel function.

- 0 = do not reinsert all signaling
- 1 = reinsert all signaling

Bit 4: Receive Freeze Enable (RFE). See Section [10.9.2.3](#) for details.

- 0 = no freezing of receive signaling data occurs
- 1 = allow freezing of receive signaling data at RSIG (and RSERO if receive signaling reinsertion is enabled)

Bit 3: Receive Force Freeze (RFF). Freezes receive-side signaling at RSIG (and RSERO if receive signaling reinsertion is enabled); overrides receive freeze enable (RFE). See Section [10.9.2.3](#) for details.

- 0 = do not force a freeze event
- 1 = force a freeze event

Bit 2: Receive Time Slot Control for CAS Signaling (RCCS). Controls the order that signaling is placed into the receive signaling registers. This bit should be set = 0 in T1 mode.

- 0 = signaling data is CAS format
- 1 = signaling data is CCS format

Bit 1: Transmit Time Slot Control for CAS Signaling (TCCS). Controls the order that signaling is transmitted from the transmit signaling registers. This bit should be set = 0 in T1 mode.

- 0 = signaling data is CAS format
- 1 = signaling data is CCS format

Bit 0: Force Receive Signaling All Ones (FRSAO). In T1 mode, this bit forces all signaling data at the RSIG and RSERO pin to all ones. This bit has no effect in E1 mode.

- 0 = normal signaling data at RSIG and RSERO
- 1 = force signaling data at RSIG and RSERO to all ones

Register Name: **TR.ERCNT**
 Register Description: **Error-Counter Configuration Register**
 Register Address: **41h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|------|-------|------|--------|--------|
| Name | — | MECU | ECUS | EAMS | VCRFS | FSBE | MOSCRF | LCVCRF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Manual Error-Counter Update (MECU). When enabled by TR.ERCNT.4, the changing of this bit from a 0 to a 1 allows the next clock cycle to load the error-counter registers with the latest counts and reset the counters. The user must wait a minimum of 1.5 RCLKn clock periods before reading the error count registers to allow for proper update.

Bit 5: Error-Counter Update Select (ECUS)

T1 Mode:

- 0 = update error counters once a second
- 1 = update error counters every 42ms (333 frames)

E1 Mode:

- 0 = update error counters once a second
- 1 = update error counters every 62.5ms (500 frames)

Bit 4: Error-Accumulation Mode Select (EAMS)

- 0 = TR.ERCNT.5 determines accumulation time
- 1 = TR.ERCNT.6 determines accumulation time

Bit 3: E1 Line-Code Violation Count Register Function Select (VCRFS)

- 0 = count bipolar violations (BPVs)
- 1 = count code violations (CVs)

Bit 2: PCVCR Fs-Bit Error-Report Enable (FSBE)

- 0 = do not report bit errors in Fs-bit position; only Ft-bit position
- 1 = report bit errors in Fs-bit position as well as Ft-bit position

Bit 1: Multiframe Out-of-Sync Count Register Function Select (MOSCRF)

- 0 = count errors in the framing bit position
- 1 = count the number of multiframes out-of-sync

Bit 0: T1 Line-Code Violation Count Register Function Select (LCVCRF)

- 0 = do not count excessive 0s
- 1 = count excessive 0s

Register Name: **TR.LCVCR1**
 Register Description: **Line-Code Violation Count Register 1**
 Register Address: **42h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Name | LCVC15 | LCVC14 | LCVC13 | LCVC12 | LCVC11 | LCVC10 | LCVC9 | LCCV8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Line-Code Violation Counter Bits 15 to 8 (LCVC15 to LCVC8). LCV15 is the MSB of the 16-bit code violation count.

Register Name: **TR.LCVCR2**
 Register Description: **Line-Code Violation Count Register 2**
 Register Address: **43h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | LCVC7 | LCVC6 | LCVC5 | LCVC4 | LCVC3 | LCVC2 | LCVC1 | LCVC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Line-Code Violation Counter Bits 7 to 0 (LCVC7 to LCVC0). LCV0 is the LSB of the 16-bit code violation count.

Register Name: **TR.PCVC1**
 Register Description: **Path Code Violation Count Register 1**
 Register Address: **44h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Name | PCVC15 | PCVC14 | PCVC13 | PCVC12 | PCVC11 | PCVC10 | PCVC9 | PCVC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Path Code Violation Counter Bits 15 to 8 (PCVC15 to PCVC8). PCVC15 is the MSB of the 16-bit path code violation count.

Register Name: **TR.PCVC2**
 Register Description: **Path Code Violation Count Register 2**
 Register Address: **45h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | PCVC7 | PCVC6 | PCVC5 | PCVC4 | PCVC3 | PCVC2 | PCVC1 | PCVC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Path Code Violation Counter Bits 7 to 0 (PCVC7 to PCVC0). PCVC0 is the LSB of the 16-bit path code violation count.

Register Name: **TR.FOSCR1**
 Register Description: **Frames Out-of-Sync Count Register 1**
 Register Address: **46h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|------|------|
| Name | FOS15 | FOS14 | FOS13 | FOS12 | FOS11 | FOS10 | FOS9 | FOS8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Frames Out-of-Sync Counter Bits 15 to 8 (FOS15 to FOS8). FOS15 is the MSB of the 16-bit frames out-of-sync count.

Register Name: **TR.FOSCR2**
 Register Description: **Frames Out-of-Sync Count Register 2**
 Register Address: **47h**

| | | | | | | | | |
|---------|------|------|------|------|------|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FOS7 | FOS6 | FOS5 | FOS4 | FOS3 | FOS2 | FOS1 | FOS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Frames Out-of-Sync Counter Bits 7 to 0 (FOS7 to FOS0). FOS0 is the LSB of the 16-bit frames out-of-sync count.

Register Name: **TR.EBCR1**
 Register Description: **E-Bit Count Register 1**
 Register Address: **48h**

| | | | | | | | | |
|---------|------|------|------|------|------|------|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | EB15 | EB14 | EB13 | EB12 | EB11 | EB10 | EB9 | EB8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: E-Bit Counter Bits 15 to 8 (EB15 to EB8). EB15 is the MSB of the 16-bit E-bit count.

Register Name: **TR.EBCR2**
 Register Description: **E-Bit Count Register 2**
 Register Address: **49h**

| | | | | | | | | |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | EB7 | EB6 | EB5 | EB4 | EB3 | EB2 | EB1 | EB0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: E-Bit Counter Bits 7 to 0 (EB7 to EB0). EB0 is the LSB of the 16-bit E-bit count.

Register Name: **TR.LBCR**
 Register Description: **Loopback Control Register**
 Register Address: **4Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|----------|-----|-----|-----|-----|
| Name | — | — | — | Reserved | LLB | RLB | PLB | FLB |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Reserved. This bit should be set to 0 for proper operation.

Bit 3: Local Loopback (LLB). When this bit is set to 1, data continues to be transmitted as normal through the transmit side of the transceiver. Data being received at RTIP and RRING are replaced with the data being transmitted. Data in this loopback passes through the jitter attenuator. See [Figure 6-3](#) for more details.

Bit 2: Remote Loopback (RLB). When this bit is set to 1, data input by the RPOSI and RNEGI pins is transmitted back to the TPOSO and TNEGO pins. Data continues to pass through the receive-side framer of the transceiver as it would normally. Data from the transmit-side formatter is ignored. See Figure 6-3 for more details.

Bit 1: Payload Loopback (PLB). When set to 1, payload loopback is enabled and the following occurs:

- 1) Data is transmitted from the TPOSO and TNEGO pins synchronous with RCLKn instead of TCLKT.
- 2) All the receive side signals continue to operate normally.
- 3) Data at the TSERI and TSIG pins is ignored.

T1 Mode: Normally, this loopback is only enabled when ESF framing is being performed but can also be enabled in D4 framing applications. The transceiver loops the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back; they are reinserted by the transceiver.

E1 Mode: The transceiver loops the 248 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The transmit section modifies the payload as if it was input at TSERI. The FAS word; Si, Sa, and E bits; and CRC4 are not looped back; they are reinserted by the transceiver.

Bit 0: Framer Loopback (FLB). When this bit is set to 1, the transceiver loops data from the transmit side back to the receive side. When FLB is enabled, the following occurs:

- 1) T1 Mode: An unframed all-ones code is transmitted at TPOSO and TNEGO.
E1 Mode: Normal data is transmitted at TPOSO and TNEGO.
- 2) Data at RPOSI and RNEGI is ignored.
- 3) All receive-side signals take on timing synchronous with TCLKT instead of RCLKI.

Please note that it is not acceptable to have RCLKn connected to TCLKT during this loopback because this causes an unstable condition.

Register Name: **TR.PCLR1**
 Register Description: **Per-Channel Loopback Enable Register 1**
 Register Address: **4Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Per-Channel Loopback Enable for Channels 8 to 1 (CH8 to CH1)

0 = loopback disabled

1 = enable loopback; source data from the corresponding receive channel

Register Name: **TR.PCLR2**
 Register Description: **Per-Channel Loopback Enable Register 2**
 Register Address: **4Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|-----|
| Name | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Per-Channel Loopback Enable for Channels 16 to 9 (CH16 to CH9)

0 = loopback disabled

1 = enable loopback; source data from the corresponding receive channel

Register Name: **TR.PCLR3**
 Register Description: **Per-Channel Loopback Enable Register 3**
 Register Address: **4Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Per-Channel Loopback Enable for Channels 24 to 17 (CH24 to CH17)

0 = loopback disabled

1 = enable loopback; source data from the corresponding receive channel

Register Name: **TR.PCLR4**
 Register Description: **Per-Channel Loopback Enable Register 4**
 Register Address: **4Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Per-Channel Loopback Enable for Channels 32 to 25 (CH32 to CH25)

0 = loopback disabled

1 = enable loopback; source data from the corresponding receive channel

Register Name: **TR.ESCR**
 Register Description: **Elastic Store Control Register**
 Register Address: **4Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|------|--------|------|---------|------|--------|------|
| Name | TESALGN | TESR | TESMDM | TESE | RESALGN | RESR | RESMDM | RESE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Elastic Store Align (TESALGN). Setting this bit from a 0 to a 1 forces the transmit elastic store's write/read pointers to a minimum separation of half a frame. No action is taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command is executed and the data is disrupted. It should be toggled after TSYCLK has been applied and is stable. It must be cleared and set again for a subsequent align. See Section [10.12.3](#) for details.

Bit 6: Transmit Elastic Store Reset (TESR). Setting this bit from a 0 to a 1 forces the read and write pointers into opposite frames, maximizing the delay through the transmit elastic store. Transmit data is lost during the reset. It should be toggled after TSYCLK has been applied and is stable. See Section [10.12.3](#) for details. Do not leave this bit set HIGH.

Bit 5: Transmit Elastic Store Minimum-Delay Mode (TESMDM). See Section [10.12.3.1](#) for details.

0 = elastic stores operate at full two-frame depth

1 = elastic stores operate at 32-bit depth

Bit 4: Transmit Elastic Store Enable (TESE)

0 = elastic store is bypassed

1 = elastic store is enabled

Bit 3: Receive Elastic Store Align (RESALGN). Setting this bit from a 0 to a 1 forces the receive elastic store's write/read pointers to a minimum separation of half a frame. No action is taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command is executed and the data is disrupted. It should be toggled after RSYCLK has been applied and is stable. Must be cleared and set again for a subsequent align. See Section [10.12.3](#) for details.

Bit 2: Receive Elastic Store Reset (RESR). Setting this bit from a 0 to a 1 forces the read and write pointers into opposite frames, maximizing the delay through the receive elastic store. It should be toggled after RSYCLK has been applied and is stable. See Section [10.12.3](#) for details. Do not leave this bit set HIGH.

Bit 1: Receive Elastic Store Minimum-Delay Mode (RESMDM). See Section [10.12.3.1](#) for details.

0 = elastic stores operate at full two-frame depth

1 = elastic stores operate at 32-bit depth

Bit 0: Receive Elastic Store Enable (RESE)

0 = elastic store is bypassed

1 = elastic store is enabled

Register Name: **TR.TS1 to TR.TS16**
 Register Description: **Transmit Signaling Registers (E1 Mode, CAS Format)**
 Register Address: **50h to 5Fh**

| (MSB) | | | | | | | (LSB) | |
|--------|--------|--------|--------|--------|--------|--------|--------|------|
| 0 | 0 | 0 | 0 | X | Y | X | X | TS1 |
| CH2-A | CH2-B | CH2-C | CH2-D | CH1-A | CH1-B | CH1-C | CH1-D | TS2 |
| CH4-A | CH4-B | CH4-C | CH4-D | CH3-A | CH3-B | CH3-C | CH3-D | TS3 |
| CH6-A | CH6-B | CH6-C | CH6-D | CH5-A | CH5-B | CH5-C | CH5-D | TS4 |
| CH8-A | CH8-B | CH8-C | CH8-D | CH7-A | CH7-B | CH7-C | CH7-D | TS5 |
| CH10-A | CH10-B | CH10-C | CH10-D | CH9-A | CH9-B | CH9-C | CH9-D | TS6 |
| CH12-A | CH12-B | CH12-C | CH12-D | CH11-A | CH11-B | CH11-C | CH11-D | TS7 |
| CH14-A | CH14-B | CH14-C | CH14-D | CH13-A | CH13-B | CH13-C | CH13-D | TS8 |
| CH16-A | CH16-B | CH16-C | CH16-D | CH15-A | CH15-B | CH15-C | CH15-D | TS9 |
| CH18-A | CH18-B | CH18-C | CH18-D | CH17-A | CH17-B | CH17-C | CH17-D | TS10 |
| CH20-A | CH20-B | CH20-C | CH20-D | CH19-A | CH19-B | CH19-C | CH19-D | TS11 |
| CH22-A | CH22-B | CH22-C | CH22-D | CH21-A | CH21-B | CH21-C | CH21-D | TS12 |
| CH24-A | CH24-B | CH24-C | CH24-D | CH23-A | CH23-B | CH23-C | CH23-D | TS13 |
| CH26-A | CH26-B | CH26-C | CH26-D | CH25-A | CH25-B | CH25-C | CH25-D | TS14 |
| CH28-A | CH28-B | CH28-C | CH28-D | CH27-A | CH27-B | CH27-C | CH27-D | TS15 |
| CH30-A | CH30-B | CH30-C | CH30-D | CH29-A | CH29-B | CH29-C | CH29-D | TS16 |

Register Name: **TR.TS1 to TR.TS16**
 Register Description: **Transmit Signaling Registers (E1 Mode, CCS Format)**
 Register Address: **50h to 5Fh**

| (MSB) | | | | | | | (LSB) | |
|--------------|-----|-----|-----|-----|-----|-----|--------------|------|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | TS1 |
| 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | TS2 |
| 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | TS3 |
| 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | TS4 |
| 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | TS5 |
| 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | TS6 |
| 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | TS7 |
| 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | TS8 |
| 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | TS9 |
| 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | TS10 |
| 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | TS11 |
| 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | TS12 |
| 97 | 98 | 99 | 100 | 101 | 102 | 103 | 104 | TS13 |
| 105 | 106 | 107 | 108 | 109 | 110 | 111 | 112 | TS14 |
| 113 | 114 | 115 | 116 | 117 | 118 | 119 | 120 | TS15 |
| 121 | 122 | 123 | 124 | 125 | 126 | 127 | 128 | TS16 |

Register Name: **TR.TS1 to TR.TS12**
 Register Description: **Transmit Signaling Registers (T1 Mode, ESF Format)**
 Register Address: **50h to 5Bh**

| (MSB) | | | | | | | (LSB) | |
|--------------|--------|--------|--------|--------|--------|--------|--------------|------|
| CH2-A | CH2-B | CH2-C | CH2-D | CH1-A | CH1-B | CH1-C | CH1-D | TS1 |
| CH4-A | CH4-B | CH4-C | CH4-D | CH3-A | CH3-B | CH3-C | CH3-D | TS2 |
| CH6-A | CH6-B | CH6-C | CH6-D | CH5-A | CH5-B | CH5-C | CH5-D | TS3 |
| CH8-A | CH8-B | CH8-C | CH8-D | CH7-A | CH7-B | CH7-C | CH7-D | TS4 |
| CH10-A | CH10-B | CH10-C | CH10-D | CH9-A | CH9-B | CH9-C | CH9-D | TS5 |
| CH12-A | CH12-B | CH12-C | CH12-D | CH11-A | CH11-B | CH11-C | CH11-D | TS6 |
| CH14-A | CH14-B | CH14-C | CH14-D | CH13-A | CH13-B | CH13-C | CH13-D | TS7 |
| CH16-A | CH16-B | CH16-C | CH16-D | CH15-A | CH15-B | CH15-C | CH15-D | TS8 |
| CH18-A | CH18-B | CH18-C | CH18-D | CH17-A | CH17-B | CH17-C | CH17-D | TS9 |
| CH20-A | CH20-B | CH20-C | CH20-D | CH19-A | CH19-B | CH19-C | CH19-D | TS10 |
| CH22-A | CH22-B | CH22-C | CH22-D | CH21-A | CH21-B | CH21-C | CH21-D | TS11 |
| CH24-A | CH24-B | CH24-C | CH24-D | CH23-A | CH23-B | CH23-C | CH23-D | TS12 |

Register Name: **TR.TS1 to TR.TS12**
 Register Description: **Transmit Signaling Registers (T1 Mode, D4 Format)**
 Register Address: **50h to 5Bh**

| (MSB) | | | | | | | (LSB) | |
|--------------|--------|---------------|---------------|--------|--------|---------------|---------------|------|
| CH2-A | CH2-B | CH2-A | CH2-B | CH1-A | CH1-B | CH1-A | CH1-B | TS1 |
| CH4-A | CH4-B | CH4-A | CH4-B | CH3-A | CH3-B | CH3-A | CH3-B | TS2 |
| CH6-A | CH6-B | CH6-A | CH6-B | CH5-A | CH5-B | CH5-A | CH5-B | TS3 |
| CH8-A | CH8-B | CH8-A | CH8-B | CH7-A | CH7-B | CH7-A | CH7-B | TS4 |
| CH10-A | CH10-B | CH10-A | CH10-B | CH9-A | CH9-B | CH9-A | CH9-B | TS5 |
| CH12-A | CH12-B | CH12-A | CH12-B | CH11-A | CH11-B | CH11-A | CH11-B | TS6 |
| CH14-A | CH14-B | CH14-A | CH14-B | CH13-A | CH13-B | CH13-A | CH13-B | TS7 |
| CH16-A | CH16-B | CH16-A | CH16-B | CH15-A | CH15-B | CH15-A | CH15-B | TS8 |
| CH18-A | CH18-B | CH18-A | CH18-B | CH17-A | CH17-B | CH17-A | CH17-B | TS9 |
| CH20-A | CH20-B | CH20-A | CH20-B | CH19-A | CH19-B | CH19-A | CH19-B | TS10 |
| CH22-A | CH22-B | CH22-A | CH22-B | CH21-A | CH21-B | CH21-A | CH21-B | TS11 |
| CH24-A | CH24-B | CH24-A | CH24-B | CH23-A | CH23-B | CH23-A | CH23-B | TS12 |

Note: In D4 format, TR.TS1–TR.TS12 contain signaling data for two frames. Bold type indicates data for second frame.

Register Name: **TR.RS1 to TR.RS12**
 Register Description: **Receive Signaling Registers (T1 Mode, ESF Format)**
 Register Address: **60h to 6Bh**

| (MSB) | | | | | | | (LSB) | |
|--------------|--------|--------|--------|--------|--------|--------|--------------|------|
| CH2-A | CH2-B | CH2-C | CH2-D | CH1-A | CH1-B | CH1-C | CH1-D | RS1 |
| CH4-A | CH4-B | CH4-C | CH4-D | CH3-A | CH3-B | CH3-C | CH3-D | RS2 |
| CH6-A | CH6-B | CH6-C | CH6-D | CH5-A | CH5-B | CH5-C | CH5-D | RS3 |
| CH8-A | CH8-B | CH8-C | CH8-D | CH7-A | CH7-B | CH7-C | CH7-D | RS4 |
| CH10-A | CH10-B | CH10-C | CH10-D | CH9-A | CH9-B | CH9-C | CH9-D | RS5 |
| CH12-A | CH12-B | CH12-C | CH12-D | CH11-A | CH11-B | CH11-C | CH11-D | RS6 |
| CH14-A | CH14-B | CH14-C | CH14-D | CH13-A | CH13-B | CH13-C | CH13-D | RS7 |
| CH16-A | CH16-B | CH16-C | CH16-D | CH15-A | CH15-B | CH15-C | CH15-D | RS8 |
| CH18-A | CH18-B | CH18-C | CH18-D | CH17-A | CH17-B | CH17-C | CH17-D | RS9 |
| CH20-A | CH20-B | CH20-C | CH20-D | CH19-A | CH19-B | CH19-C | CH19-D | RS10 |
| CH22-A | CH22-B | CH22-C | CH22-D | CH21-A | CH21-B | CH21-C | CH21-D | RS11 |
| CH24-A | CH24-B | CH24-C | CH24-D | CH23-A | CH23-B | CH23-C | CH23-D | RS12 |

Register Name: **TR.RS1 to TR.RS12**
 Register Description: **Receive Signaling Registers (T1 Mode, D4 Format)**
 Register Address: **60h to 6Bh**

| (MSB) | | | | | | | (LSB) | |
|--------------|--------|---------------|---------------|--------|--------|---------------|---------------|------|
| CH2-A | CH2-B | CH2-A | CH2-B | CH1-A | CH1-B | CH1-A | CH1-B | RS1 |
| CH4-A | CH4-B | CH4-A | CH4-B | CH3-A | CH3-B | CH3-A | CH3-B | RS2 |
| CH6-A | CH6-B | CH6-A | CH6-B | CH5-A | CH5-B | CH5-A | CH5-B | RS3 |
| CH8-A | CH8-B | CH8-A | CH8-B | CH7-A | CH7-B | CH7-A | CH7-B | RS4 |
| CH10-A | CH10-B | CH10-A | CH10-B | CH9-A | CH9-B | CH9-A | CH9-B | RS5 |
| CH12-A | CH12-B | CH12-A | CH12-B | CH11-A | CH11-B | CH11-A | CH11-B | RS6 |
| CH14-A | CH14-B | CH14-A | CH14-B | CH13-A | CH13-B | CH13-A | CH13-B | RS7 |
| CH16-A | CH16-B | CH16-A | CH16-B | CH15-A | CH15-B | CH15-A | CH15-B | RS8 |
| CH18-A | CH18-B | CH18-A | CH18-B | CH17-A | CH17-B | CH17-A | CH17-B | RS9 |
| CH20-A | CH20-B | CH20-A | CH20-B | CH19-A | CH19-B | CH19-A | CH19-B | RS10 |
| CH22-A | CH22-B | CH22-A | CH22-B | CH21-A | CH21-B | CH21-A | CH21-B | RS11 |
| CH24-A | CH24-B | CH24-A | CH24-B | CH23-A | CH23-B | CH23-A | CH23-B | RS12 |

Note: In D4 format, TR.TS1–TR.TS12 contain signaling data for two frames. Bold type indicates data for second frame.

Register Name: **TR.RS1 to TR.RS16**
 Register Description: **Receive Signaling Registers (E1 Mode, CAS Format)**
 Register Address: **60h to 6Fh**

| (MSB) | | | | | | | (LSB) | |
|--------|--------|--------|--------|--------|--------|--------|--------|------|
| 0 | 0 | 0 | 0 | X | Y | X | X | RS1 |
| CH2-A | CH2-B | CH2-C | CH2-D | CH1-A | CH1-B | CH1-C | CH1-D | RS2 |
| CH4-A | CH4-B | CH4-C | CH4-D | CH3-A | CH3-B | CH3-C | CH3-D | RS3 |
| CH6-A | CH6-B | CH6-C | CH6-D | CH5-A | CH5-B | CH5-C | CH5-D | RS4 |
| CH8-A | CH8-B | CH8-C | CH8-D | CH7-A | CH7-B | CH7-C | CH7-D | RS5 |
| CH10-A | CH10-B | CH10-C | CH10-D | CH9-A | CH9-B | CH9-C | CH9-D | RS6 |
| CH12-A | CH12-B | CH12-C | CH12-D | CH11-A | CH11-B | CH11-C | CH11-D | RS7 |
| CH14-A | CH14-B | CH14-C | CH14-D | CH13-A | CH13-B | CH13-C | CH13-D | RS8 |
| CH16-A | CH16-B | CH16-C | CH16-D | CH15-A | CH15-B | CH15-C | CH15-D | RS9 |
| CH18-A | CH18-B | CH18-C | CH18-D | CH17-A | CH17-B | CH17-C | CH17-D | RS10 |
| CH20-A | CH20-B | CH20-C | CH20-D | CH19-A | CH19-B | CH19-C | CH19-D | RS11 |
| CH22-A | CH22-B | CH22-C | CH22-D | CH21-A | CH21-B | CH21-C | CH21-D | RS12 |
| CH24-A | CH24-B | CH24-C | CH24-D | CH23-A | CH23-B | CH23-C | CH23-D | RS13 |
| CH26-A | CH26-B | CH26-C | CH26-D | CH25-A | CH25-B | CH25-C | CH25-D | RS14 |
| CH28-A | CH28-B | CH28-C | CH28-D | CH27-A | CH27-B | CH27-C | CH27-D | RS15 |
| CH30-A | CH30-B | CH30-C | CH30-D | CH29-A | CH29-B | CH29-C | CH29-D | RS16 |

Register Name: **TR.RS1 to TR.RS16**
 Register Description: **Receive Signaling Registers (E1 Mode, CCS Format)**
 Register Address: **60h to 6Fh**

| (MSB) | | | | | | | (LSB) | |
|-------|-----|-----|-----|-----|-----|-----|-------|------|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | RS1 |
| 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | RS2 |
| 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | RS3 |
| 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | RS4 |
| 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | RS5 |
| 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | RS6 |
| 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | RS7 |
| 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | RS8 |
| 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | RS9 |
| 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | RS10 |
| 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | RS11 |
| 89 | 90 | 91 | 92 | 93 | 94 | 95 | 96 | RS12 |
| 97 | 98 | 99 | 100 | 101 | 102 | 103 | 104 | RS13 |
| 105 | 106 | 107 | 108 | 109 | 110 | 111 | 112 | RS14 |
| 113 | 114 | 115 | 116 | 117 | 118 | 119 | 120 | RS15 |
| 121 | 122 | 123 | 124 | 125 | 126 | 127 | 128 | RS16 |

Register Name: **TR.CCR1**
 Register Description: **Common Control Register 1**
 Register Address: **70h**

| | | | | | | | | |
|---------|-------|-------|-----|-----|-------|-------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MCLKS | CRC4R | SIE | ODM | DICAI | TCSS1 | TCSS0 | RLOSF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: MCLK Source (MCLKS). Selects the source of MCLK.

- 0 = MCLK is source from the MCLK pin
- 1 = MCLK is source from the TSYSCLK pin

Bit 6: CRC-4 Recalculate (CRC4R)

- 0 = transmit CRC-4 generation and insertion operates in normal mode
- 1 = transmit CRC-4 generation operates according to G.706 intermediate path recalculation method

Bit 5: Signaling Integration Enable (SIE)

- 0 = signaling changes of state reported on any change in selected channels
- 1 = signaling must be stable for three multiframes in order for a change of state to be reported

Bit 4: Output Data Mode (ODM)

- 0 = pulses at TPOSO and TNEGO are one full TCLKO period wide
- 1 = pulses at TPOSO and TNEGO are one-half TCLKO period wide

Bit 3: Disable Idle Code Auto Increment (DICAI). Selects/deselects the auto-increment feature for the transmit and receive idle code array address register. See Section [10.10](#).

- 0 = addresses in TR.IAAR register automatically increment on every read/write operation to the TR.PCICR register
- 1 = addresses in TR.IAAR register do not automatically increment

Bit 2: Transmit Clock Source Select Bit 0 (TCSS1)

| TCSS1 | TCSS0 | Transmit Clock Source |
|-------|-------|---|
| 0 | 0 | The TCLKT pin is always the source of transmit clock. |
| 0 | 1 | Switch to the clock present at RCLKn when the signal at the TCLKT pin fails to transition after 1 channel time. |
| 1 | 0 | Use the scaled signal present at MCLK as the transmit clock. The TCLKT pin is ignored. |
| 1 | 1 | Use the signal present at RCLKn as the transmit clock. The TCLKT pin is ignored. |

Bit 1: Transmit Clock Source Select Bit 0 (TCSS0)

Bit 0: Function of the RLOS/LOTIC Output (RLOSF)

- 0 = receive loss of sync (RLOS)
- 1 = loss-of-transmit clock (LOTIC)

Register Name: **TR.CCR2**
 Register Description: **Common Control Register 2**
 Register Address: **71h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|-------|-------|------|
| Name | — | — | — | — | — | BPCS1 | BPCS0 | BPEN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 2 and 1: Backplane Clock Selects (BPCS1 and BPCS0)

| BPCS1 | BPCS0 | BPCLK Frequency (MHz) |
|-------|-------|-----------------------|
| 0 | 0 | 16.384 |
| 0 | 1 | 8.192 |
| 1 | 0 | 4.096 |
| 1 | 1 | 2.048 |

Bit 0: Backplane Clock Enable (BPEN)

0 = disable BPCLK pin (pin held at logic 0)

1 = enable BPCLK pin

Note: The backplane clock settings in TR.CCR2 are only active for Port 1 and Port 2 in the DS33R41 register map and correspond to the output pins BPCLK1 and BPCLK2, respectively.

Register Name: **TR.CCR3**
 Register Description: **Common Control Register 3**
 Register Address: **72h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|--------|---|---|---------|---------|---------|---------|
| Name | TMSS | INTDIS | — | — | TDATFMT | TGPCKEN | RDATFMT | RGPCKEN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Multiframe Sync Source (TMSS). Should be set = 0 only when transmit hardware signaling is enabled.

0 = elastic store is source of multiframe sync

1 = framer or TSYNC pin is source of multiframe sync

Bit 6: Interrupt Disable (INTDIS). This bit is convenient for disabling interrupts without altering the various interrupt mask register settings.

0 = interrupts are enabled according to the various mask register settings

1 = interrupts are disabled regardless of the mask register settings

Bit 3: Transmit Channel-Data Format (TDATFMT)

0 = 64kbps (data contained in all 8 bits)

1 = 56kbps (data contained in seven out of the 8 bits)

Bit 2: Transmit Gapped-Clock Enable (TGPCKEN)

0 = TCHCLK functions normally

1 = enable gapped bit-clock output on TCHCLK

Bit 1: Receive Channel-Data Format (RDATFMT)

0 = 64kbps (data contained in all 8 bits)

1 = 56kbps (data contained in seven out of the 8 bits)

Bit 0: Receive Gapped-Clock Enable (RGPKEN)

0 = RCHCLK functions normally

1 = enable gapped bit-clock output on RCHCLK

Register Name: **TR.CCR4**
 Register Description: **Common Control Register 4**
 Register Address: **73h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|---|---|---|---|
| Name | RLT3 | RLT2 | RLT1 | RLT0 | — | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 4: Receive Level Threshold Bits (RLT3 to RLT0)

| RLT3 | RLT2 | RLT1 | RLT0 | Receive Level (dB) |
|------|------|------|------|--------------------|
| 0 | 0 | 0 | 0 | Greater than -2.5 |
| 0 | 0 | 0 | 1 | -2.5 |
| 0 | 0 | 1 | 0 | -5.0 |
| 0 | 0 | 1 | 1 | -7.5 |
| 0 | 1 | 0 | 0 | -10.0 |
| 0 | 1 | 0 | 1 | -12.5 |
| 0 | 1 | 1 | 0 | -15.0 |
| 0 | 1 | 1 | 1 | -17.5 |
| 1 | 0 | 0 | 0 | -20.0 |
| 1 | 0 | 0 | 1 | -22.5 |
| 1 | 0 | 1 | 0 | -25.0 |
| 1 | 0 | 1 | 1 | -27.5 |
| 1 | 1 | 0 | 0 | -30.0 |
| 1 | 1 | 0 | 1 | -32.5 |
| 1 | 1 | 1 | 0 | -35.0 |
| 1 | 1 | 1 | 1 | Less than -37.5 |

Register Name: **TR.TDS0SEL**
 Register Description: **Transmit Channel Monitor Select**
 Register Address: **74h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|------|------|------|------|------|
| Name | — | — | — | TCM4 | TCM3 | TCM2 | TCM1 | TCM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 4 to 0: Transmit Channel Monitor Bits (TCM4 to TCM0). TCM0 is the LSB of a 5-bit channel select that determines which transmit channel data appear in the TR.TDS0M register.

Register Name: **TR.TDS0M**
 Register Description: **Transmit DS0 Monitor Register**
 Register Address: **75h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit DS0 Channel Bits (B1 to B8). Transmit channel data that has been selected by the transmit channel monitor select register. B8 is the LSB of the DS0 channel (last bit to be transmitted).

Register Name: **TR.RDS0SEL**
 Register Description: **Receive Channel Monitor Select**
 Register Address: **76h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|------|------|------|------|------|
| Name | — | — | — | RCM4 | RCM3 | RCM2 | RCM1 | RCM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 4 to 0: Receive Channel Monitor Bits (RCM4 to RCM0). RCM0 is the LSB of a 5-bit channel select that determines which receive DS0 channel data appear in the TR.RDS0M register.

Register Name: **TR.RDS0M**
 Register Description: **Receive DS0 Monitor Register**
 Register Address: **77h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive DS0 Channel Bits (B1 to B8). Receive channel data that has been selected by the receive channel monitor select register. B8 is the LSB of the DS0 channel (last bit to be received).

Register Name: **TR.LIC1**
 Register Description: **Line Interface Control 1**
 Register Address: **78h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|-----|-----|-------|-----|-----|
| Name | L2 | L1 | L0 | EGL | JAS | JABDS | DJA | TPD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 5: Line Build-Out Select (L2 to L0). These bits select the output waveshape. See [Table 12-10](#), [Table 12-11](#), [Table 12-12](#), and [Table 12-13](#) for the correct register settings for specific applications. In E1 mode, when using the internal termination, the user needs only to select 000 for 75Ω operation or 001 for 120Ω operation. Using TT0 and TT1 of the LICR4 register, users can then select the proper internal source termination. Line build-outs 100 and 101 are provided for backward compatibility with older products only.

Bit 4: Receive Equalizer Gain Limit (EGL). This bit controls the sensitivity of the receive equalizer.

T1 Mode

0 = -36dB (long haul)

1 = -15dB (limited long haul)

E1 Mode

0 = -12dB (short haul)

1 = -43dB (long haul)

Bit 3: Jitter Attenuator Select (JAS)

0 = place the jitter attenuator on the receive side

1 = place the jitter attenuator on the transmit side

Bit 2: Jitter Attenuator Buffer Depth Select (JABDS)

0 = 128 bits

1 = 32 bits (use for delay-sensitive applications)

Bit 1: Disable Jitter Attenuator (DJA)

0 = jitter attenuator enabled

1 = jitter attenuator disabled

Bit 0: Transmit Power-Down (TPD) This bit along with the TPD pin and the LTS (TR.LBCR.7) bit controls the transmit power-down function.

0 = powers down the transmitter and tri-states the TTIP and TRING pins

1 = normal transmitter operation

Table 12-9. TPD Control

| TR.LBCR. 7 (LTS) | TPD PIN | TR.LIC1.0 (TPD) | FUNCTION |
|------------------------|------------|--------------------|---|
| 0 | X | 0 | Transmitter in power-down mode, TTIP and TRING tri-stated |
| 0 | X | 1 | Transmitter enabled |
| 1 | 0 | 0 | Transmitter in power-down mode, TTIP and TRING tri-stated |
| 1 | 0 | 1 | Transmitter enabled |
| 1 | 1 | 0 | Transmitter in power-down mode, TTIP and TRING tri-stated |
| 1 | 1 | 1 | Transmitter in power-down mode, TTIP and TRING tri-stated |

Table 12-10. E1 Mode With Automatic Gain Control Mode Enabled (TLBC.6 = 0)

| APPLICATION | LIC1.7 (L2) | LIC1.6 (L1) | LIC1.5 (L0) | PSA1 (F1h) | PSA2 (F2h) | RETURN LOSS | Rt (1) |
|-----------------------------|-------------|-------------|-------------|------------|------------|-------------|--------|
| 75Ω Normal | 0 | 0 | 0 | 20h | 08h | N.M.** | 0 |
| 120Ω Normal | 0 | 0 | 1 | 20h | 00h | N.M. | 0 |
| 75Ω with High Return Loss* | 1 | 0 | 0 | 00h | 00h | 21dB | 6.2Ω |
| 120Ω with High Return Loss* | 1 | 0 | 1 | 20h | 00h | 21dB | 11.6Ω |

Table 12-11. E1 Mode With Automatic Gain Control Mode Disabled (TLBC.6 = 1)

| APPLICATION | LIC1.7 (L2) | LIC1.6 (L1) | LIC1.5 (L0) | PSA1 (F1h) | PSA2 (F2h) | RETURN LOSS | Rt (1) |
|-----------------------------|-------------|-------------|-------------|------------|------------|-------------|--------|
| 75Ω Normal | 0 | 0 | 0 | 20h | 08h | N.M. | 0 |
| 120Ω Normal | 0 | 0 | 1 | 00h | 00h | N.M. | 0 |
| 75Ω with High Return Loss* | 1 | 0 | 0 | 00h | 00h | 21dB | 6.2Ω |
| 120Ω with High Return Loss* | 1 | 0 | 1 | 00h | 00h | 21dB | 11.6Ω |

Table 12-12. T1 Mode With Automatic Gain Control Mode Enabled (TLBC.6 = 0)

| APPLICATION | LIC1.7 (L2) | LIC1.6 (L1) | LIC1.5 (L0) | PSA1 (F1h) | PSA2 (F2h) | RETURN LOSS | Rt (1) |
|-------------------------------|-------------|-------------|-------------|------------|------------|-------------|--------|
| 0dB CSU | 0 | 0 | 0 | 00h | 00h | N.M. | 0 |
| DSX-1 (0 to 133 feet)/0dB CSU | 0 | 0 | 0 | 00h | 00h | N.M. | 0 |
| DSX-1 (133 to 266 feet) | 0 | 0 | 1 | 0Ah | 00h | N.M. | 0 |
| DSX-1 (266 to 399 feet) | 0 | 1 | 0 | 0Ah | 00h | N.M. | 0 |
| DSX-1 (399 to 533 feet) | 0 | 1 | 1 | 00h | 00h | N.M. | 0 |
| DSX-1 (533 to 655 feet) | 1 | 0 | 0 | 0Ah | 00h | N.M. | 0 |
| -7.5dB CSU | 1 | 0 | 1 | 00h | 00h | N.M. | 0 |
| -15dB CSU | 1 | 1 | 0 | 00h | 00h | N.M. | 0 |
| -22.5dB CSU | 1 | 1 | 1 | 00h | 00h | N.M. | 0 |

Table 12-13. T1 Mode With Automatic Gain Control Mode Disabled (TLBC.6 = 1)

| APPLICATION | LIC1.7 (L2) | LIC1.6 (L1) | LIC1.5 (L0) | PSA1 (F1h) | PSA2 (F2h) | RETURN LOSS | Rt (1) |
|-------------------------------|-------------|-------------|-------------|------------|------------|-------------|--------|
| 0dB CSU | 0 | 0 | 0 | 00h | 00h | N.M. | 0 |
| DSX-1 (0 to 133 feet)/0dB CSU | 0 | 0 | 0 | 00h | 00h | N.M. | 0 |
| DSX-1 (133 to 266 feet) | 0 | 0 | 1 | 00h | 00h | N.M. | 0 |
| DSX-1 (266 to 399 feet) | 0 | 1 | 0 | 00h | 00h | N.M. | 0 |
| DSX-1 (399 to 533 feet) | 0 | 1 | 1 | 00h | 00h | N.M. | 0 |
| DSX-1 (533 to 655 feet) | 1 | 0 | 0 | 00h | 00h | N.M. | 0 |
| -7.5dB CSU | 1 | 0 | 1 | 00h | 00h | N.M. | 0 |
| -15dB CSU | 1 | 1 | 0 | 00h | 00h | N.M. | 0 |
| -22.5dB CSU | 1 | 1 | 1 | 00h | 00h | N.M. | 0 |

*TT0 and TT1 of the LIC4 register must be set to zero in this configuration.

**N.M. = not meaningful.

Register Name: **TR.TLBC**
 Register Description: **Transmit Line Build-Out Control**
 Register Address: **7Dh**

| | | | | | | | | |
|---------|---|------|-----|-----|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | AGCE | GC5 | GC4 | GC3 | GC2 | GC1 | GC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Automatic Gain Control Enable (AGCE)

0 = use Transmit AGC, TR.TLBC bits 0–5 are “don’t care”

1 = do not use Transmit AGC, TR.TLBC bits 0–5 set nominal level

Bits 5 to 0: Gain Control Bits (GC5 to GC0). The GC0 through GC5 bits control the gain setting automatic gain control is disabled. Use the tables below for setting the recommended values. The LB (line build-out) column refers to the value in the L0–L2 bits in TR.LIC1 (Line Interface Control 1) register.

| NETWORK MODE | LB | GC5 | GC4 | GC3 | GC2 | GC1 | GC0 |
|--------------------------------|----|-----|-----|-----|-----|-----|-----|
| T1, Impedance Match Off | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| | 2 | 0 | 1 | 1 | 0 | 1 | 0 |
| | 3 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 4 | 1 | 0 | 0 | 1 | 1 | 1 |
| | 5 | 1 | 0 | 0 | 1 | 1 | 1 |
| | 6 | 0 | 1 | 0 | 0 | 1 | 1 |
| | 7 | 1 | 1 | 1 | 1 | 1 | 1 |
| T1, Impedance Match On | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | 2 | 0 | 1 | 0 | 1 | 0 | 1 |
| | 3 | 0 | 1 | 1 | 0 | 1 | 0 |
| | 4 | 1 | 0 | 0 | 0 | 1 | 0 |
| | 5 | 1 | 0 | 0 | 0 | 0 | 0 |
| | 6 | 0 | 0 | 1 | 1 | 0 | 0 |
| | 7 | 1 | 1 | 1 | 1 | 1 | 1 |
| E1, Impedance Match Off | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| | 4 | 1 | 0 | 1 | 0 | 1 | 0 |
| | 5 | 1 | 0 | 1 | 0 | 0 | 0 |
| E1, Impedance Match On | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

Register Name: **TR.LIC2**
 Register Description: **Line Interface Control 2**
 Register Address: **79h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-------|------|------|-------|---|------|------|
| Name | ETS | LIRST | IBPV | TUA1 | JAMUX | — | SCLD | CLDS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: E1/T1 Select (ETS)

0 = T1 mode selected
 1 = E1 mode selected

Bit 6: Line Interface Reset (LIRST). Setting this bit from a 0 to a 1 initiates an internal reset that resets the clock recovery state machine and re-centers the jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.

Bit 5: Insert BPV (IBPV). A 0-to-1 transition on this bit causes a single BPV to be inserted into the transmit data stream. Once this bit has been toggled from a 0 to a 1, the device waits for the next occurrence of three consecutive 1s to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted.

Bit 4: Transmit Unframed All Ones (TUA1). The polarity of this bit is set such that the device transmits an all-ones pattern on power-up or device reset. This bit must be set to a 1 to allow the device to transmit data. The transmission of this data pattern is always timed off of the JACLK.

0 = transmit all ones at TTIP and TRING
 1 = transmit data normally

Bit 3: Jitter Attenuator Mux (JAMUX). Controls the source for JACLK.

0 = JACLK sourced from MCLK (2.048MHz or 1.544MHz at MCLK)
 1 = JACLK sourced from internal PLL (2.048MHz at MCLK)

Bit 1: Short-Circuit Limit Disable (ETS = 1) (SCLD). Controls the 50mA (RMS) current limiter.

0 = enable 50mA current limiter
 1 = disable 50mA current limiter

Bit 0: Custom Line Driver Select (CLDS). Setting this bit to a 1 redefines the operation of the transmit line driver. When this bit is set to a 1 and TR.LIC1.5 = TR.LIC1.6 = TR.LIC1.7 = 0, the device generates a square wave at the TTIP and TRING outputs instead of a normal waveform. When this bit is set to a 1 and TR.LIC1.5 = TR.LIC1.6 = TR.LIC1.7 ≠ 0, the device forces TTIP and TRING outputs to become open-drain drivers instead of their normal push-pull operation. This bit should be set to 0 for normal operation of the device.

Register Name: **TR.LIC3**
 Register Description: **Line Interface Control 3**
 Register Address: **7Ah**

| | | | | | | | | |
|---------|---|------|------|-----|-----|--------|--------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | TCES | RCES | MM1 | MM0 | RSCLKE | TSCLKE | TAOZ |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Transmit-Clock Edge Select (TCES). Selects which TDCLKI edge to sample TPOSI and TNEGI.
 0 = sample TPOSI and TNEGI on falling edge of TDCLKI
 1 = sample TPOSI and TNEGI on rising edge of TDCLKI

Bit 5: Receive-Clock Edge Select (RCES). Selects which RCLKOn edge to update RPOSO and RNEGO.
 0 = update RPOSO and RNEGO on rising edge of RCLKOn
 1 = update RPOSO and RNEGO on falling edge of RCLKOn

Bits 3 and 4: Monitor Mode (MM1 and MM0)

| MM1 | MM0 | Internal Linear Gain Boost (dB) |
|-----|-----|---------------------------------|
| 0 | 0 | Normal operation (no boost) |
| 0 | 1 | 20 |
| 1 | 0 | 26 |
| 1 | 1 | 32 |

Bit 2: Receive Synchronization G.703 Clock Enable (RSCLKE)
 0 = disable 1.544MHz (T1)/2.048MHz (E1) synchronization receive mode
 1 = enable 1.544MHz (T1)/2.048MHz (E1) synchronization receive mode

Bit 1: Transmit Synchronization G.703 Clock Enable (TSCLKE)
 0 = disable 1.544MHz (T1)/2.048MHz (E1) transmit synchronization clock
 1 = enable 1.544MHz (T1)/2.048MHz (E1) transmit synchronization clock

Bit 0: Transmit Alternate Ones and Zeros (TAOZ). Transmit a ...101010... pattern (customer disconnect indication signal) at TTIP and TRING. The transmission of this data pattern is always timed off of TCLKT.
 0 = disabled
 1 = enabled

Register Name: **TR.LIC4**
 Register Description: **Line Interface Control 4**
 Register Address: **7Bh**

| | | | | | | | | |
|---------|------|------|------|------|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CMIE | CMII | MPS1 | MPS0 | TT1 | TT0 | RT1 | RT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: CMI Enable (CMIE)

0 = disable CMI mode
 1 = enable CMI mode

Bit 6: CMI Invert (CMII)

0 = CMI normal at TTIP and RTIP
 1 = invert CMI signal at TTIP and RTIP

Bits 5 and 4: MCLK Prescaler (MPS1 and MPS0)

T1 Mode:

| MCLK (MHz) | MPS1 | MPS0 | JAMUX (TR.LIC2.3) |
|------------|------|------|-------------------|
| 1.544 | 0 | 0 | 0 |
| 3.088 | 0 | 1 | 0 |
| 6.176 | 1 | 0 | 0 |
| 12.352 | 1 | 1 | 0 |
| 2.048 | 0 | 0 | 1 |
| 4.096 | 0 | 1 | 1 |
| 8.192 | 1 | 0 | 1 |
| 16.384 | 1 | 1 | 1 |

E1 Mode:

| MCLK (MHz) | MPS1 | MPS0 | JAMUX (TR.LIC2.3) |
|------------|------|------|-------------------|
| 2.048 | 0 | 0 | 0 |
| 4.096 | 0 | 1 | 0 |
| 8.192 | 1 | 0 | 0 |
| 16.384 | 1 | 1 | 0 |

Bits 3 and 2: Transmit Termination Select (TT1 and TT0)

| TT1 | TT0 | Internal Transmit-Termination Configuration |
|-----|-----|---|
| 0 | 0 | Internal transmit-side termination disabled |
| 0 | 1 | Internal transmit -side 75Ω enabled |
| 1 | 0 | Internal transmit -side 100Ω enabled |
| 1 | 1 | Internal transmit -side 120Ω enabled |

Bits 1 and 0: Receive Termination Select (RT1 and RT0)

| RT1 | RT0 | Internal Receive-Termination Configuration |
|-----|-----|--|
| 0 | 0 | Internal receive-side termination disabled |
| 0 | 1 | Internal receive-side 75Ω enabled |
| 1 | 0 | Internal receive-side 100Ω enabled |
| 1 | 1 | Internal receive-side 120Ω enabled |

Register Name: **TR.PSA1**
 Register Description: **Pulse Shape Adjustment 1**
 Register Address: **F1h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-------|------|-------|------|-------|-------|
| Name | — | — | AGCT2 | SRR1 | AGCT1 | SRR0 | AGCT0 | SRIB0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 and 6: Set to zero for normal operation.

Bits 5, 3, 1: Automatic Gain Control Target Bits 2, 1, 0 (AGCT2, AGCT1, AGCT0). These three bits adjust the target amplitude of the waveform when using Automatic Gain Control (AGCE = 0). The adjustment for each setting is listed below:

Standard Settings for non-automatic gain mode:

| AGCT2 | AGCT1 | AGCT0 | AGCAC (in hex) | % change in amplitude |
|-------|-------|-------|----------------|-----------------------|
| 0 | 0 | 0 | 00h | 0% (default) |
| 0 | 0 | 1 | 02h | - 23% |
| 0 | 1 | 0 | 08h | - 15% |
| 0 | 1 | 1 | 0Ah | - 8% |
| 1 | 0 | 0 | 20h | + 6% |
| 1 | 0 | 1 | 22h | + 10% |
| 1 | 1 | 0 | 28h | + 15% |
| 1 | 1 | 1 | 2Ah | + 35% |

Bits 4 and 2: Slew Rate Reduction Control Bits 1 and 0 (SRR1 and SRR0). These bits are a binary weighted array that can be set to make the waveform "colder" (i.e., increase rise time, reduce overshoot).

Bit 0: Slew Rate Increase "B" (SRIB0). This bit, when set, makes the waveform a bit hotter (different method than Group 1). Not much effect from this bit should be expected.

Register Name: **TR.PSA2**
 Register Description: **Pulse Shape Adjustment 2**
 Register Address: **F2h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|---|---|---|-------|---|---|---|
| Name | SRIA4 | — | — | — | SRIA3 | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 6, 5, 4, 2, 1, and 0: Unused, must be set to zero for proper operation.

Bits 7 and 3: Slew Rate Increase "A" Control Bits 4 and 3 (SRIA4 and SRIA3). These bits (together with the SRIA0–SRIA2 in the SRC1 register) form a 5-bit binary weighted array used to increase the slew rate of the output waveform. However, SRIA3 and SRIA4 have the same weighting. SRIA4 (F2h, bit 7) is the MSB, and SRIA0 (F0h, bit 5) is the LSB. The more of this array that is set, the "hotter" (i.e., faster rise times, more overshoot) the waveform.

Register Name: **TR.IAAR**
 Register Description: **Idle Array Address Register**
 Register Address: **7Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | GRIC | GTIC | IAA5 | IAA4 | IAA3 | IAA2 | IAA1 | IAA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Global Receive-Idle Code (GRIC). Setting this bit causes all receive channels to be set to the idle code written to the TR.PCICR register. This bit must be set = 0 for read operations. The value in bits IAA0–IAA5 must be a valid transmit channel (01h to 20h for E1 mode; 01h to 18h for T1 mode).

Bit 6: Global Transmit-Idle Code (GTIC). Setting this bit causes all transmit channels to be set to the idle code written to the PCICR register. This bit must be set = 0 for read operations. The value in bits IAA0–IAA5 must be a valid transmit channel (01h to 20h for E1 mode; 01h to 18h for T1 mode).

| GRIC | GTIC | FUNCTION |
|------|------|--|
| 0 | 0 | Updates a single transmit or receive channel |
| 0 | 1 | Updates all transmit channels |
| 1 | 0 | Updates all receive channels |
| 1 | 1 | Updates all transmit and receive channels |

Bits 5 to 0: Channel Pointer Address Bits (IAA5 to IAA0). These bits select the channel to be programmed with the idle code defined in the TR.PCICR register. IAA0 is the LSB of the 5-bit channel code. Channel 1 is 01h.

Register Name: **TR.PCICR**
 Register Description: **Per-Channel Idle Code Register**
 Register Address: **7Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Per-Channel Idle-Code Bits (C7 to C0). This register defines the idle code to be programmed in the channel selected by the TR.IAAR register. C0 is the LSB of the idle code (this bit is transmitted last).

Register Name: **TR.TCICE1**
 Register Description: **Transmit-Channel Idle-Code Enable Register 1**
 Register Address: **80h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Channels 8 to 1 Code Insertion Control Bits (CH8 to CH1)

0 = do not insert data from the idle-code array into the transmit data stream

1 = insert data from the idle-code array into the transmit data stream

Register Name: **TR.TCICE2**
 Register Description: **Transmit-Channel Idle-Code Enable Register 2**
 Register Address: **81h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|-----|
| Name | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Channels 16 to 9 Code Insertion Control Bits (CH16 to CH9)

0 = do not insert data from the idle-code array into the transmit data stream

1 = insert data from the idle code-array into the transmit data stream

Register Name: **TR.TCICE3**
 Register Description: **Transmit-Channel Idle-Code Enable Register 3**
 Register Address: **82h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Channels 24 to 17 Code Insertion Control Bits (CH24 to CH17)

0 = do not insert data from the idle-code array into the transmit data stream

1 = insert data from the idle code-array into the transmit data stream

Register Name: **TR.TCICE4**
 Register Description: **Transmit-Channel Idle-Code Enable Register 4**
 Register Address: **83h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Channels 32 to 25 Code Insertion Control Bits (CH32 to CH25)

0 = do not insert data from the idle-code array into the transmit data stream

1 = insert data from the idle-code array into the transmit data stream

Register Name: **TR.RCICE1**
 Register Description: **Receive-Channel Idle-Code Enable Register 1**
 Register Address: **84h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Channels 8 to 1 Code Insertion Control Bits (CH8 to CH1)

0 = do not insert data from the idle-code array into the receive data stream

1 = insert data from the idle-code array into the receive data stream

Register Name: **TR.RCICE2**
 Register Description: **Receive-Channel Idle-Code Enable Register 2**
 Register Address: **85h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|-----|
| Name | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Channels 16 to 9 Code Insertion Control Bits (CH16 to CH9)

0 = do not insert data from the idle-code array into the receive data stream
 1 = insert data from the idle-code array into the receive data stream

Register Name: **TR.RCICE3**
 Register Description: **Receive-Channel Idle-Code Enable Register 3**
 Register Address: **86h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Channels 24 to 17 Code Insertion Control Bits (CH24 to CH17)

0 = do not insert data from the idle-code array into the receive data stream
 1 = insert data from the idle-code array into the receive data stream

Register Name: **TR.RCICE4**
 Register Description: **Receive-Channel Idle-Code Enable Register 4**
 Register Address: **87h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Channels 32 to 25 Code Insertion Control Bits (CH32 to CH25)

0 = do not insert data from the idle-code array into the receive data stream
 1 = insert data from the idle-code array into the receive data stream

Register Name: **TR.RCBR1**
 Register Description: **Receive Channel Blocking Register 1**
 Register Address: **88h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Channels 8 to 1 Channel Blocking Control Bits (CH8 to CH1)

0 = force the RCHBLK pin to remain low during this channel time
 1 = force the RCHBLK pin high during this channel time

Register Name: **TR.RCBR2**
 Register Description: **Receive Channel Blocking Register 2**
 Register Address: **89h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|-----|
| Name | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Channels 16 to 9 Channel Blocking Control Bits (CH16 to CH9)

0 = force the RCHBLK pin to remain low during this channel time

1 = force the RCHBLK pin high during this channel time

Register Name: **TR.RCBR3**
 Register Description: **Receive Channel Blocking Register 3**
 Register Address: **8Ah**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Channels 24 to 17 Channel Blocking Control Bits (CH24 to CH17)

0 = force the RCHBLK pin to remain low during this channel time

1 = force the RCHBLK pin high during this channel time

Register Name: **TR.RCBR4**
 Register Description: **Receive Channel Blocking Register 4**
 Register Address: **8Bh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Channels 32 to 25 Channel Blocking Control Bits (CH32 to CH25)

0 = force the RCHBLK pin to remain low during this channel time

1 = force the RCHBLK pin high during this channel time

Register Name: **TR.TCBR1**
 Register Description: **Transmit Channel Blocking Register 1**
 Register Address: **8Ch**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Channels 8 to 1 Channel Blocking Control Bits (CH8 to CH1)

0 = force the TCHBLK pin to remain low during this channel time
 1 = force the TCHBLK pin high during this channel time

Register Name: **TR.TCBR2**
 Register Description: **Transmit Channel Blocking Register 2**
 Register Address: **8Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|-----|
| Name | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Channels 16 to 9 Channel Blocking Control Bits (CH16 to CH9)

0 = force the TCHBLK pin to remain low during this channel time
 1 = force the TCHBLK pin high during this channel time

Register Name: **TR.TCBR3**
 Register Description: **Transmit Channel Blocking Register 3**
 Register Address: **8Eh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Channels 24 to 17 Channel Blocking Control Bits (CH24 to CH17)

0 = force the TCHBLK pin to remain low during this channel time
 1 = force the TCHBLK pin high during this channel time

Register Name: **TR.TCBR4**
 Register Description: **Transmit Channel Blocking Register 4**
 Register Address: **8Fh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit Channels 32 to 25 Channel Blocking Control Bits (CH32 to CH25)

0 = force the TCHBLK pin to remain low during this channel time
 1 = force the TCHBLK pin high during this channel time

Register Name: **TR.H1TC, TR.H2TC**
 Register Description: **HDLC #1 Transmit Control**
HDLC #2 Transmit Control
 Register Address: **90h, A0h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-----|------|-----|------|------|-------|
| Name | NOFS | TEOML | THR | THMS | TFS | TEOM | TZSD | TCRCD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Number of Flags Select (NOFS)

- 0 = send one flag between consecutive messages
- 1 = send two flags between consecutive messages

Bit 6: Transmit End of Message and Loop (TEOML). To loop on a message, this bit should be set to a 1 just before the last data byte of an HDLC packet is written into the transmit FIFO. The message repeats until the user clears this bit or a new message is written to the transmit FIFO. If the host clears the bit, the looping message completes, then flags are transmitted until a new message is written to the FIFO. If the host terminates the loop by writing a new message to the FIFO, the loop terminates, one or two flags are transmitted, and the new message starts. If not disabled through TCRCD, the transmitter automatically appends a 2-byte CRC code to the end of all messages. This is useful for transmitting consecutive SS7 FISUs without host intervention.

Bit 5: Transmit HDLC Reset (THR). Resets the transmit HDLC controller and flushes the transmit FIFO. An abort followed by 7Eh or FFh flags/idle is transmitted until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent reset.

- 0 = normal operation
- 1 = reset transmit HDLC controller and flush the transmit FIFO

Bit 4: Transmit HDLC Mapping Select (THMS)

- 0 = transmit HDLC assigned to channels
- 1 = transmit HDLC assigned to FDL (T1 mode), Sa bits (E1 mode)

Bit 3: Transmit Flag/Idle Select (TFS). This bit selects the intermessage fill character after the closing and before the opening flags (7Eh).

- 0 = 7Eh
- 1 = FFh

Bit 2: Transmit End of Message (TEOM). Should be set to a 1 just before the last data byte of an HDLC packet is written into the transmit FIFO at HxTF. If not disabled through TCRCD, the transmitter automatically appends a 2-byte CRC code to the end of the message.

Bit 1: Transmit Zero-Stuffer Defeat (TZSD). The zero-stuffer function automatically inserts a 0 in the message field (between the flags) after five consecutive 1s to prevent the emulation of a flag or abort sequence by the data pattern. The receiver automatically removes (destuffs) any 0 after five 1s in the message field.

- 0 = enable the zero stuffer (normal operation)
- 1 = disable the zero stuffer

Bit 0: Transmit CRC Defeat (TCRCD). A 2-byte CRC code is automatically appended to the outbound message. This bit can be used to disable the CRC function.

- 0 = enable CRC generation (normal operation)
- 1 = disable CRC generation

Register Name: **TR.H1FC, TR.H2FC**
 Register Description: **HDLC #1 FIFO Control**
HDLC #2 FIFO Control
 Register Address: **91h, A1h**

| | | | | | | | | |
|---------|---|---|--------|--------|--------|--------|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | TFLWM2 | TFLWM1 | TFLWM0 | RFHWM2 | RFHWM1 | RFHWM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 5 to 3: Transmit FIFO Low-Watermark Select (TFLWM2 to TFLWM0)

| TFLWM2 | TFLWM1 | TFLWM0 | Transmit FIFO Watermark (bytes) |
|--------|--------|--------|---------------------------------|
| 0 | 0 | 0 | 4 |
| 0 | 0 | 1 | 16 |
| 0 | 1 | 0 | 32 |
| 0 | 1 | 1 | 48 |
| 1 | 0 | 0 | 64 |
| 1 | 0 | 1 | 80 |
| 1 | 1 | 0 | 96 |
| 1 | 1 | 1 | 112 |

Bits 2 to 0: Receive FIFO High-Watermark Select (RFHWM2 to RFHWM0)

| RFHWM2 | RFHWM1 | RFHWM0 | Receive FIFO Watermark (bytes) |
|--------|--------|--------|--------------------------------|
| 0 | 0 | 0 | 4 |
| 0 | 0 | 1 | 16 |
| 0 | 1 | 0 | 32 |
| 0 | 1 | 1 | 48 |
| 1 | 0 | 0 | 64 |
| 1 | 0 | 1 | 80 |
| 1 | 1 | 0 | 96 |
| 1 | 1 | 1 | 112 |

Register Name: **TR.H1RCS1, TR.H1RCS2, TR.H1RCS3, TR.H1RCS4
TR.H2RCS1, TR.H2RCS2, TR.H2RCS3, TR.H2RCS4**

Register Description: **HDLC #1 Receive Channel Select
HDLC #2 Receive Channel Select**

Register Address: **92h, 93h, 94h, 95h
A2h, A3h, A4h, A5h**

| (MSB) | | | | | | | (LSB) | |
|--------------|--------|--------|--------|--------|--------|--------|--------------|----------------|
| RHCS8 | RHCS7 | RHCS6 | RHCS5 | RHCS4 | RHCS3 | RHCS2 | RHCS1 | H1RCS1 |
| RHCS16 | RHCS15 | RHCS14 | RHCS13 | RHCS12 | RHCS11 | RHCS10 | RHCS9 | H1RCS2 |
| RHCS24 | RHCS23 | RHCS22 | RHCS21 | RHCS20 | RHCS19 | RHCS18 | RHCS17 | H1RCS3 |
| RHCS32 | RHCS31 | RHCS30 | RHCS29 | RHCS28 | RHCS27 | RHCS26 | RHCS25 | H1RCS4 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Default |

Setting a bit to 1 will enable that channel's data to be sent to the Receive HDLC Controller. Multiple bits may be selected for each of the two HDLC controllers in the integrated T1/E1 transceiver.

Register Name: **TR.H1RTSBS, TR.H2RTSBS**
 Register Description: **HDLC #1 Receive Time Slot Bits/Sa Bits Select**
HDLC #2 Receive Time Slot Bits/Sa Bits Select
 Register Address: **96h, A6h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | RCB8SE | RCB7SE | RCB6SE | RCB5SE | RCB4SE | RCB3SE | RCB2SE | RCB1SE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Channel Bit 8 Suppress Enable (RCB8SE). MSB of the channel. Set to 1 to stop this bit from being used.

Bit 6: Receive Channel Bit 7 Suppress Enable (RCB7SE). Set to 1 to stop this bit from being used.

Bit 5: Receive Channel Bit 6 Suppress Enable (RCB6SE). Set to 1 to stop this bit from being used.

Bit 4: Receive Channel Bit 5 Suppress Enable/Sa4 Bit Enable (RCB5SE). Set to 1 to stop this bit from being used.

Bit 3: Receive Channel Bit 4 Suppress Enable/Sa5 Bit Enable (RCB4SE). Set to 1 to stop this bit from being used.

Bit 2: Receive Channel Bit 3 Suppress Enable/Sa6 Bit Enable (RCB3SE). Set to 1 to stop this bit from being used.

Bit 1: Receive Channel Bit 2 Suppress Enable/Sa7 Bit Enable (RCB2SE). Set to 1 to stop this bit from being used.

Bit 0: Receive Channel Bit 1 Suppress Enable/Sa8 Bit Enable (RCB1SE). LSB of the channel. Set to 1 to stop this bit from being used.

Register Name: **TR.H1TCS1, TR.H1TCS2, TR.H1TCS3, TR.H1TCS4
TR.H2TCS1, TR.H2TCS2, TR.H2TCS3, TR.H2TCS4**
 Register Description: **HDLC #1 Transmit Channel Select
HDLC #2 Transmit Channel Select**
 Register Address: **97h, 98h, 99h, 9Ah
A7h, A8h, A9h, AAh**

| (MSB) | | | | | | | (LSB) | |
|--------------|--------|--------|--------|--------|--------|--------|--------------|----------------|
| THCS8 | THCS7 | THCS6 | THCS5 | THCS4 | THCS3 | THCS2 | THCS1 | H1TCS1 |
| THCS16 | THCS15 | THCS14 | THCS13 | THCS12 | THCS11 | THCS10 | THCS9 | H1TCS2 |
| THCS24 | THCS23 | THCS22 | THCS21 | THCS20 | THCS19 | THCS18 | THCS17 | H1TCS3 |
| THCS32 | THCS31 | THCS30 | THCS29 | THCS28 | THCS27 | THCS26 | THCS25 | H1TCS4 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Default |

Setting a bit to 1 will enable data from the Transmit HDLC Controller to be sent on that channel. Multiple bits may be selected for each of the two HDLC controllers in the integrated T1/E1 transceiver.

Register Name: **TR.H1TTSBS, TR.H2TTSBS**
 Register Description: **HDLC #1 Transmit Time Slot Bits/Sa Bits Select**
HDLC #2 Transmit Time Slot Bits/Sa Bits Select
 Register Address: **9Bh, ABh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | TCB8SE | TCB7SE | TCB6SE | TCB5SE | TCB4SE | TCB3SE | TCB2SE | TCB1SE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Channel Bit 8 Suppress Enable (TCB1SE). MSB of the channel. Set to 1 to stop this bit from being used.

Bit 6: Transmit Channel Bit 7 Suppress Enable (TCB1SE). Set to 1 to stop this bit from being used.

Bit 5: Transmit Channel Bit 6 Suppress Enable (TCB1SE). Set to 1 to stop this bit from being used.

Bit 4: Transmit Channel Bit 5 Suppress Enable/Sa4 Bit Enable (TCB1SE). Set to 1 to stop this bit from being used.

Bit 3: Transmit Channel Bit 4 Suppress Enable/Sa5 Bit Enable (TCB1SE). Set to 1 to stop this bit from being used.

Bit 2: Transmit Channel Bit 3 Suppress Enable/Sa6 Bit Enable (TCB1SE). Set to 1 to stop this bit from being used.

Bit 1: Transmit Channel Bit 2 Suppress Enable/Sa7 Bit Enable (TCB1SE). Set to 1 to stop this bit from being used.

Bit 0: Transmit Channel Bit 1 Suppress Enable/Sa8 Bit Enable (TCB1SE). LSB of the channel. Set to 1 to stop this bit from being used.

Register Name: **TR.H1RPBA, TR.H2RPBA**
 Register Description: **HDLC #1 Receive Packet Bytes Available**
HDLC #2 Receive Packet Bytes Available
 Register Address: **9Ch, ACh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|-------|-------|-------|-------|-------|-------|-------|
| Name | MS | RPBA6 | RPBA5 | RPBA4 | RPBA3 | RPBA2 | RPBA1 | RPBA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Message Status (MS)

0 = bytes indicated by RPBA0 through RPBA6 are the end of a message. Host must check the INFO5 or INFO6 register for details.

1 = bytes indicated by RPBA0 through RPBA6 are the beginning or continuation of a message. The host does not need to check the INFO5 or INFO6 register.

Bits 6 to 0: Receive FIFO Packet Bytes Available Count (RPBA6 to RPBA0). RPBA0 is the LSB.

Register Name: **TR.H1TF, TR.H2TF**
 Register Description: **HDLC #1 Transmit FIFO**
HDLC #2 Transmit FIFO
 Register Address: **9Dh, ADh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | THD7 | THD6 | THD5 | THD4 | THD3 | THD2 | THD1 | THD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit HDLC Data Bit 7 (THD7). MSB of an HDLC packet data byte.

Bit 6: Transmit HDLC Data Bit 6 (THD6)

Bit 5: Transmit HDLC Data Bit 5 (THD5)

Bit 4: Transmit HDLC Data Bit 4 (THD4)

Bit 3: Transmit HDLC Data Bit 3 (THD3)

Bit 2: Transmit HDLC Data Bit 2 (THD2)

Bit 1: Transmit HDLC Data Bit 1 (THD1)

Bit 0: Transmit HDLC Data Bit 0 (THD0). LSB of an HDLC packet data byte.

Register Name: **TR.H1RF, TR.H2RF**
 Register Description: **HDLC #1 Receive FIFO**
HDLC #2 Receive FIFO
 Register Address: **9Eh, AEh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | RHD7 | RHD6 | RHD5 | RHD4 | RHD3 | RHD2 | RHD1 | RHD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive HDLC Data Bit 7 (RHD7). MSB of an HDLC packet data byte.

Bit 6: Receive HDLC Data Bit 6 (RHD6)

Bit 5: Receive HDLC Data Bit 5 (RHD5)

Bit 4: Receive HDLC Data Bit 4 (RHD4)

Bit 3: Receive HDLC Data Bit 3 (RHD3)

Bit 2: Receive HDLC Data Bit 2 (RHD2)

Bit 1: Receive HDLC Data Bit 1 (RHD1)

Bit 0: Receive HDLC Data Bit 0 (RHD0). LSB of an HDLC packet data byte.

Register Name: **TR.H1TFBA, TR.H2TFBA**
 Register Description: **HDLC #1 Transmit FIFO Buffer Available**
HDLC #2 Transmit FIFO Buffer Available
 Register Address: **9Fh, AFh**

| | | | | | | | | |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | TFBA7 | TFBA6 | TFBA5 | TFBA4 | TFBA3 | TFBA2 | TFBA1 | TFBA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit FIFO Bytes Available (TFBA7 to TFBA0). TFBA0 is the LSB.

Register Name: **TR.IBCC**
 Register Description: **In-Band Code Control Register**
 Register Address: **B6h**

| | | | | | | | | |
|---------|-----|-----|------|------|------|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | TC1 | TC0 | RUP2 | RUP1 | RUP0 | RDN2 | RDN1 | RDN0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 and 6: Transmit Code Length Definition Bits (TC1 and TC0)

| TC1 | TC0 | Length Selected (bits) |
|-----|-----|------------------------|
| 0 | 0 | 5 |
| 0 | 1 | 6/3 |
| 1 | 0 | 7 |
| 1 | 1 | 16/8/4/2/1 |

Bits 5 to 3: Receive Up-Code Length Definition Bits (RUP2 to RUP1)

| RUP2 | RUP1 | RUP0 | Length Selected (bits) |
|------|------|------|------------------------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8/16 |

Bits 2 to 0: Receive Down-Code Length Definition Bits (RDN2 to RDN0)

| RDN2 | RDN1 | RDN0 | Length Selected (bits) |
|------|------|------|------------------------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8/16 |

Register Name: **TR.TCD1**
 Register Description: **Transmit Code-Definition Register 1**
 Register Address: **B7h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Code-Definition Bit 7 (C7). First bit of the repeating pattern.

Bits 6 to 3: Transmit Code-Definition Bits 6 to 3 (C6 to C3)

Bit 2: Transmit Code-Definition Bit 2 (C2). A don't care if a 5-bit length is selected.

Bit 1: Transmit Code-Definition Bit 1 (C1). A don't care if a 5-bit or 6-bit length is selected.

Bit 0: Transmit Code-Definition Bit 0 (C0). A don't care if a 5-, 6-, or 7-bit length is selected.

Register Name: **TR.TCD2**
 Register Description: **Transmit Code Definition Register 2**
 Register Address: **B8h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Least significant byte of 16 bit code.

Bits 7 to 0: Transmit Code-Definition Bits 7 to 0 (C7 to C0). A don't care if a 5-, 6-, or 7-bit length is selected.

Register Name: **TR.RUPCD1**
 Register Description: **Receive Up-Code Definition Register 1**
 Register Address: **B9h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Writing this register resets the detector's integration period.

Bit 7: Receive Up-Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Receive Up-Code Definition Bit 6 (C6). A don't care if a 1-bit length is selected.

Bit 5: Receive Up-Code Definition Bit 5 (C5). A don't care if a 1-bit or 2-bit length is selected.

Bit 4: Receive Up-Code Definition Bit 4 (C4). A don't care if a 1-bit to 3-bit length is selected.

Bit 3: Receive Up-Code Definition Bit 3 (C3). A don't care if a 1-bit to 4-bit length is selected.

Bit 2: Receive Up-Code Definition Bit 2 (C2). A don't care if a 1-bit to 5-bit length is selected.

Bit 1: Receive Up-Code Definition Bit 1 (C1). A don't care if a 1-bit to 6-bit length is selected.

Bit 0: Receive Up-Code Definition Bit 0 (C0). A don't care if a 1-bit to 7-bit length is selected.

Register Name: **TR.RUPCD2**
 Register Description: **Receive Up-Code Definition Register 2**
 Register Address: **BAh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Up-Code Definition Bits 7 to 0 (C7 to C0). A don't care if a 1-bit to 7-bit length is selected.

Register Name: **TR.RDNCD1**
 Register Description: **Receive Down-Code Definition Register 1**
 Register Address: **BBh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Writing this register resets the detector's integration period.

Bit 7: Receive Down-Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Receive Down-Code Definition Bit 6 (C6). A don't care if a 1-bit length is selected.

Bit 5: Receive Down-Code Definition Bit 5 (C5). A don't care if a 1-bit or 2-bit length is selected.

Bit 4: Receive Down-Code Definition Bit 4 (C4). A don't care if a 1-bit to 3-bit length is selected.

Bit 3: Receive Down-Code Definition Bit 3 (C3). A don't care if a 1-bit to 4-bit length is selected.

Bit 2: Receive Down-Code Definition Bit 2 (C2). A don't care if a 1-bit to 5-bit length is selected.

Bit 1: Receive Down-Code Definition Bit 1 (C1). A don't care if a 1-bit to 6-bit length is selected.

Bit 0: Receive Down-Code Definition Bit 0 (C0). A don't care if a 1-bit to 7-bit length is selected.

Register Name: **TR.RDNCD2**
 Register Description: **Receive Down-Code Definition Register 2**
 Register Address: **BCh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Down-Code Definition Bits 7 to 0 (C7 to C0). A don't care if a 1-bit to 7-bit length is selected.

Register Name: **TR.RSCC**
 Register Description: **In-Band Receive Spare Control Register**
 Register Address: **BDh**

| | | | | | | | | |
|---------|---|---|---|---|---|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | RSC2 | RSC1 | RSC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 3: Unused, must be set to 0 for proper operation

Bits 2 to 0: Receive Spare Code Length Definition Bits (RSC2 to RSC0)

| RSC2 | RSC1 | RSC0 | Length Selected (bits) |
|------|------|------|------------------------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8/16 |

Register Name: **TR.RSCD1**
 Register Description: **Receive Spare-Code Definition Register 1**
 Register Address: **BEh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Writing this register resets the detector's integration period.

Bit 7: Receive Spare-Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Receive Spare-Code Definition Bit 6 (C6). A don't care if a 1-bit length is selected.

Bit 5: Receive Spare-Code Definition Bit 5 (C5). A don't care if a 1-bit or 2-bit length is selected.

Bit 4: Receive Spare-Code Definition Bit 4 (C4). A don't care if a 1-bit to 3-bit length is selected.

Bit 3: Receive Spare-Code Definition Bit 3 (C3). A don't care if a 1-bit to 4-bit length is selected.

Bit 2: Receive Spare-Code Definition Bit 2 (C2). A don't care if a 1-bit to 5-bit length is selected.

Bit 1: Receive Spare-Code Definition Bit 1 (C1). A don't care if a 1-bit to 6-bit length is selected.

Bit 0: Receive Spare-Code Definition Bit 0 (C0). A don't care if a 1-bit to 7-bit length is selected.

Register Name: **TR.RSCD2**
 Register Description: **Receive Spare Code Definition Register 2**
 Register Address: **BFh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive Spare-Code Definition Bits 7 to 0 (C7 to C0). A don't care if a 1-bit to 7-bit length is selected.

Register Name: **TR.RFDL (TR.BOCC.4 = 1)**
 Register Description: **Receive FDL Register**
 Register Address: **C0h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-------|-------|-------|-------|-------|-------|
| Name | — | — | RBOC5 | RBOC4 | RBOC3 | RBOC2 | RBOC1 | RBOC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RFDL register bit definitions when TR.BOCC.4 = 1:

Bit 5: BOC Bit 5 (RBOC5)

Bit 4: BOC Bit 4 (RBOC4)

Bit 3: BOC Bit 3 (RBOC3)

Bit 2: BOC Bit 2 (RBOC2)

Bit 1: BOC Bit 1 (RBOC1)

Bit 0: BOC Bit 0 (RBOC0)

Register Name: **TR.RFDL (TR.BOCC.4 = 0)**
 Register Description: **Receive FDL Register**
 Register Address: **C0h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RFDL7 | RFDL6 | RFDL5 | RFDL4 | RFDL3 | RFDL2 | RFDL1 | RFDL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The receive FDL register (TR.RFDL) reports the incoming FDL or the incoming Fs bits. The LSB is received first.

Bit 7: Receive FDL Bit 7 (RFDL7). MSB of the received FDL code.

Bit 6: Receive FDL Bit 6 (RFDL6)

Bit 5: Receive FDL Bit 5 (RFDL5)

Bit 4: Receive FDL Bit 4 (RFDL4)

Bit 3: Receive FDL Bit 3 (RFDL3)

Bit 2: Receive FDL Bit 2 (RFDL2)

Bit 1: Receive FDL Bit 1 (RFDL1)

Bit 0: Receive FDL Bit 0 (RFDL0). LSB of the received FDL code.

Register Name: **TR.TFDL**
 Register Description: **Transmit FDL Register**
 Register Address: **C1h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TFDL7 | TFDL6 | TFDL5 | TFDL4 | TFDL3 | TFDL2 | TFDL1 | TFDL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Also used to insert Fs framing pattern in D4 framing mode.

The transmit FDL register (TR.TFDL) contains the FDL information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first.

Bit 7: Transmit FDL Bit 7 (TFDL7). MSB of the transmit FDL code.

Bit 6: Transmit FDL Bit 6 (TFDL6)

Bit 5: Transmit FDL Bit 5 (TFDL5)

Bit 4: Transmit FDL Bit 4 (TFDL4)

Bit 3: Transmit FDL Bit 3 (TFDL3)

Bit 2: Transmit FDL Bit 2 (TFDL2)

Bit 1: Transmit FDL Bit 1 (TFDL1)

Bit 0: Transmit FDL Bit 0 (TFDL0). LSB of the transmit FDL code.

Register Name: **TR.RFDLM1, TR.RFDLM2**
 Register Description: **Receive FDL Match Register 1**
Receive FDL Match Register 2
 Register Address: **C2h, C3h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | RFDLM7 | RFDLM6 | RFDLM5 | RFDLM4 | RFDLM3 | RFDLM2 | RFDLM1 | RFDLM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive FDL Match Bit 7 (RFDLM7). MSB of the FDL match code.

Bit 6: Receive FDL Match Bit 6 (RFDLM6)

Bit 5: Receive FDL Match Bit 5 (RFDLM5)

Bit 4: Receive FDL Match Bit 4 (RFDLM4)

Bit 3: Receive FDL Match Bit 3 (RFDLM3)

Bit 2: Receive FDL Match Bit 2 (RFDLM2)

Bit 1: Receive FDL Match Bit 1 (RFDLM1)

Bit 0: Receive FDL Match Bit 0 (RFDLM0). LSB of the FDL match code.

Register Name: **TR.IBOC**
 Register Description: **Interleave Bus Operation Control Register**
 Register Address: **C5h**

| | | | | | | | | |
|---------|---|------|------|---|-------|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | IBS1 | IBS0 | — | IBOEN | DA2 | DA1 | DA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 and 4: Reserved, must be set to zero for proper operation.

Bits 6 and 5: IBO Bus Size Bit 1 (IBS1 and IBS0). Indicates how many devices are on the bus.

| IBS1 | IBS0 | BUS SIZE |
|------|------|---------------------|
| 0 | 1 | Four Devices on Bus |

Bit 3: Interleave Bus Operation Enable (IBOEN). THIS BIT MUST BE SET TO 1.

0 = Interleave Bus Operation disabled—allowed for application-specific requirements.

1 = Interleave Bus Operation enabled—normal operation.

Bits 2 to 0: Device Assignment Bits (DA2 to DA0)

| DA2 | DA1 | DA0 | DEVICE POSITION |
|-----|-----|-----|-------------------|
| 0 | 0 | 0 | 1st device on bus |
| 0 | 0 | 1 | 2nd device on bus |
| 0 | 1 | 0 | 3rd device on bus |
| 0 | 1 | 1 | 4th device on bus |

Register Name: **TR.RAF**
 Register Description: **Receive Align Frame Register**
 Register Address: **C6h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|---|---|---|---|---|
| Name | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: International Bit (Si)

Bit 6: Frame Alignment Signal Bit (0)

Bit 5: Frame Alignment Signal Bit (0)

Bit 4: Frame Alignment Signal Bit (1)

Bit 3: Frame Alignment Signal Bit (1)

Bit 2: Frame Alignment Signal Bit (0)

Bit 1: Frame Alignment Signal Bit (1)

Bit 0: Frame Alignment Signal Bit (1)

Register Name: **TR.RNAF**
 Register Description: **Receive Nonalign Frame Register**
 Register Address: **C7h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|-----|-----|-----|-----|-----|
| Name | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: International Bit (Si)

Bit 6: Frame Nonalignment Signal Bit (1)

Bit 5: Remote Alarm (A)

Bit 4: Additional Bit 4 (Sa4)

Bit 3: Additional Bit 5 (Sa5)

Bit 2: Additional Bit 6 (Sa6)

Bit 1: Additional Bit 7 (Sa7)

Bit 0: Additional Bit 8 (Sa8)

Register Name: **TR.RSiAF**
 Register Description: **Received Si Bits of the Align Frame**
 Register Address: **C8h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|-------|-------|-------|
| Name | SiF0 | SiF2 | SiF4 | SiF6 | SiF8 | SiF10 | SiF12 | SiF14 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Si Bit of Frame 0 (SiF0)

Bit 6: Si Bit of Frame 2 (SiF2)

Bit 5: Si Bit of Frame 4 (SiF4)

Bit 4: Si Bit of Frame 6 (SiF6)

Bit 3: Si Bit of Frame 8 (SiF8)

Bit 2: Si Bit of Frame 10 (SiF10)

Bit 1: Si Bit of Frame 12 (SiF12)

Bit 0: Si Bit of Frame 14 (SiF14)

Register Name: **TR.RSiNAF**
 Register Description: **Received Si Bits of the Nonalign Frame**
 Register Address: **C9h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|-------|-------|-------|
| Name | SiF1 | SiF3 | SiF5 | SiF7 | SiF9 | SiF11 | SiF13 | SiF15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Si Bit of Frame 1 (SiF1)

Bit 6: Si Bit of Frame 3 (SiF3)

Bit 5: Si Bit of Frame 5 (SiF5)

Bit 4: Si Bit of Frame 7 (SiF7)

Bit 3: Si Bit of Frame 9 (SiF9)

Bit 2: Si Bit of Frame 11 (SiF11)

Bit 1: Si Bit of Frame 13 (SiF13)

Bit 0: Si Bit of Frame 15 (SiF15)

Register Name: **TR.RRA**
 Register Description: **Received Remote Alarm**
 Register Address: **CAh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|--------|--------|--------|
| Name | RRAF1 | RRAF3 | RRAF5 | RRAF7 | RRAF9 | RRAF11 | RRAF13 | RRAF15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Remote Alarm Bit of Frame 1 (RRAF1)

Bit 6: Remote Alarm Bit of Frame 3 (RRAF3)

Bit 5: Remote Alarm Bit of Frame 5 (RRAF5)

Bit 4: Remote Alarm Bit of Frame 7 (RRAF7)

Bit 3: Remote Alarm Bit of Frame 9 (RRAF9)

Bit 2: Remote Alarm Bit of Frame 11 (RRAF11)

Bit 1: Remote Alarm Bit of Frame 13 (RRAF13)

Bit 0: Remote Alarm Bit of Frame 15 (RRAF15)

Register Name: **TR.RSa4**
 Register Description: **Received Sa4 Bits**
 Register Address: **CBh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | RSa4F1 | RSa4F3 | RSa4F5 | RSa4F7 | RSa4F9 | RSa4F11 | RSa4F13 | RSa4F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa4 Bit of Frame 1 (RSa4F1)

Bit 6: Sa4 Bit of Frame 3 (RSa4F3)

Bit 5: Sa4 Bit of Frame 5 (RSa4F5)

Bit 4: Sa4 Bit of Frame 7 (RSa4F7)

Bit 3: Sa4 Bit of Frame 9 (RSa4F9)

Bit 2: Sa4 Bit of Frame 11 (RSa4F11)

Bit 1: Sa4 Bit of Frame 13 (RSa4F13)

Bit 0: Sa4 Bit of Frame 15 (RSa4F15)

Register Name: **TR.RSa5**
 Register Description: **Received Sa5 Bits**
 Register Address: **CCh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | RSa5F1 | RSa5F3 | RSa5F5 | RSa5F7 | RSa5F9 | RSa5F11 | RSa5F13 | RSa5F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa5 Bit of Frame 1 (RSa5F1)

Bit 6: Sa5 Bit of Frame 3 (RSa5F3)

Bit 5: Sa5 Bit of Frame 5 (RSa5F5)

Bit 4: Sa5 Bit of Frame 7 (RSa5F7)

Bit 3: Sa5 Bit of Frame 9 (RSa5F9)

Bit 2: Sa5 Bit of Frame 11 (RSa5F11)

Bit 1: Sa5 Bit of Frame 13 (RSa5F13)

Bit 0: Sa5 Bit of Frame 15 (RSa5F15)

Register Name: **TR.RSa6**
 Register Description: **Received Sa6 Bits**
 Register Address: **CDh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | RSa6F1 | RSa6F3 | RSa6F5 | RSa6F7 | RSa6F9 | RSa6F11 | RSa6F13 | RSa6F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa6 Bit of Frame 3(RSa6F3)

Bit 6: Sa6 Bit of Frame 4 (RSa6F4)

Bit 5: Sa6 Bit of Frame 5 (RSa6F5)

Bit 4: Sa6 Bit of Frame 7 (RSa6F7)

Bit 3: Sa6 Bit of Frame 9 (RSa6F9)

Bit 2: Sa6 Bit of Frame 11 (RSa6F11)

Bit 1: Sa6 Bit of Frame 13 (RSa6F13)

Bit 0: Sa6 Bit of Frame 15 (RSa6F15)

Register Name: **TR.RSa7**
 Register Description: **Received Sa7 Bits**
 Register Address: **CEh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | RSa7F1 | Rsa7F3 | RSa7F5 | RSa7F7 | RSa7F9 | RSa7F11 | RSa7F13 | RSa7F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa7 Bit of Frame 1 (RSa4F1)

Bit 6: Sa7 Bit of Frame 3 (RSa7F3)

Bit 5: Sa7 Bit of Frame 5 (RSa7F5)

Bit 4: Sa7 Bit of Frame 7 (RSa7F7)

Bit 3: Sa7 Bit of Frame 9 (RSa7F9)

Bit 2: Sa7 Bit of Frame 11 (RSa7F11)

Bit 1: Sa7 Bit of Frame 13 (RSa7F13)

Bit 0: Sa7 Bit of Frame 15 (RSa7F15)

Register Name: **TR.RSa8**
 Register Description: **Received Sa8 Bits**
 Register Address: **CFh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | RSa8F1 | RSa8F3 | RSa8F5 | RSa8F7 | RSa8F9 | RSa8F11 | RSa8F13 | RSa8F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa8 Bit of Frame 1 (RSa8F1)

Bit 6: Sa8 Bit of Frame 3 (RSa8F3)

Bit 5: Sa8 Bit of Frame 5 (RSa8F5)

Bit 4: Sa8 Bit of Frame 7 (RSa8F7)

Bit 3: Sa8 Bit of Frame 9 (RSa8F9)

Bit 2: Sa8 Bit of Frame 11 (RSa8F11)

Bit 1: Sa8 Bit of Frame 13 (RSa8F13)

Bit 0: Sa8 Bit of Frame 15 (RSa8F15)

Register Name: **TR.TAF**
 Register Description: **Transmit Align Frame Register**
 Register Address: **D0h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|---|---|---|---|---|
| Name | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Default | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

Bit 7: International Bit (Si)

Bit 6: Frame Alignment Signal Bit (0)

Bit 5: Frame Alignment Signal Bit (0)

Bit 4: Frame Alignment Signal Bit (1)

Bit 3: Frame Alignment Signal Bit (1)

Bit 2: Frame Alignment Signal Bit (0)

Bit 1: Frame Alignment Signal Bit (1)

Bit 0: Frame Alignment Signal Bit (1)

Register Name: **TR.TNAF**
 Register Description: **Transmit Nonalign Frame Register**
 Register Address: **D1h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|-----|-----|-----|-----|-----|
| Name | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: International Bit (Si)

Bit 6: Frame Nonalignment Signal Bit (1)

Bit 5: Remote Alarm [used to transmit the alarm (A)]

Bit 4: Additional Bit 4 (Sa4)

Bit 3: Additional Bit 5 (Sa5)

Bit 2: Additional Bit 6 (Sa6)

Bit 1: Additional Bit 7 (Sa7)

Bit 0: Additional Bit 8 (Sa8)

Register Name: **TR.TSiAF**
 Register Description: **Transmit Si Bits of the Align Frame**
 Register Address: **D2h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|--------|--------|--------|
| Name | TSiF0 | TSiF2 | TSiF4 | TSiF6 | TSiF8 | TSiF10 | TSiF12 | TSiF14 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Si Bit of Frame 0 (TSiF0)

Bit 6: Si Bit of Frame 2 (TSiF2)

Bit 5: Si Bit of Frame 4 (TSiF4)

Bit 4: Si Bit of Frame 6 (TSiF6)

Bit 3: Si Bit of Frame 8 (TSiF8)

Bit 2: Si Bit of Frame 10 (TSiF10)

Bit 1: Si Bit of Frame 12 (TSiF12)

Bit 0: Si Bit of Frame 14 (TSiF14)

Register Name: **TR.TSiNAF**
 Register Description: **Transmit Si Bits of the Nonalign Frame**
 Register Address: **D3h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|--------|--------|--------|
| Name | TSiF1 | TSiF3 | TSiF5 | TSiF7 | TSiF9 | TSiF11 | TSiF13 | TSiF15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Si Bit of Frame 1 (TSiF1)

Bit 6: Si Bit of Frame 3 (TSiF3)

Bit 5: Si Bit of Frame 5 (TSiF5)

Bit 4: Si Bit of Frame 7 (TSiF7)

Bit 3: Si Bit of Frame 9 (TSiF9)

Bit 2: Si Bit of Frame 11 (TSiF11)

Bit 1: Si Bit of Frame 13 (TSiF13)

Bit 0: Si Bit of Frame 15 (TSiF15)

Register Name: **TR.TRA**
 Register Description: **Transmit Remote Alarm**
 Register Address: **D4h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|--------|--------|--------|
| Name | TRAF1 | TRAF3 | TRAF5 | TRAF7 | TRAF9 | TRAF11 | TRAF13 | TRAF15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Remote Alarm Bit of Frame 1 (TRAF1)

Bit 6: Remote Alarm Bit of Frame 3 (TRAF3)

Bit 5: Remote Alarm Bit of Frame 5 (TRAF5)

Bit 4: Remote Alarm Bit of Frame 7 (TRAF7)

Bit 3: Remote Alarm Bit of Frame 9 (TRAF9)

Bit 2: Remote Alarm Bit of Frame 11 (TRAF11)

Bit 1: Remote Alarm Bit of Frame 13 (TRAF13)

Bit 0: Remote Alarm Bit of Frame 15 (TRAF15)

Register Name: **TR.TSa4**
 Register Description: **Transmit Sa4 Bits**
 Register Address: **D5h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | TSa4F1 | TSa4F3 | TSa4F5 | TSa4F7 | TSa4F9 | TSa4F11 | TSa4F13 | TSa4F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa4 Bit of Frame 1 (TSa4F1)

Bit 6: Sa4 Bit of Frame 3 (TSa4F3)

Bit 5: Sa4 Bit of Frame 5 (TSa4F5)

Bit 4: Sa4 Bit of Frame 7 (TSa4F7)

Bit 3: Sa4 Bit of Frame 9 (TSa4F9)

Bit 2: Sa4 Bit of Frame 11 (TSa4F11)

Bit 1: Sa4 Bit of Frame 13 (TSa4F13)

Bit 0: Sa4 Bit of Frame 15 (TSa4F15)

Register Name: **TR.TSa5**
 Register Description: **Transmitted Sa5 Bits**
 Register Address: **D6h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | TSa5F1 | TSa5F3 | TSa5F5 | TSa5F7 | TSa5F9 | TSa5F11 | TSa5F13 | TSa5F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa5 Bit of Frame 1 (TSa5F1)

Bit 6: Sa5 Bit of Frame 3 (TSa5F3)

Bit 5: Sa5 Bit of Frame 5 (TSa5F5)

Bit 4: Sa5 Bit of Frame 7 (TSa5F7)

Bit 3: Sa5 Bit of Frame 9 (TSa5F9)

Bit 2: Sa5 Bit of Frame 11 (TSa5F11)

Bit 1: Sa5 Bit of Frame 13 (TSa5F13)

Bit 0: Sa5 Bit of Frame 15 (TSa5F15)

Register Name: **TR.TSa6**
 Register Description: **Transmit Sa6 Bits**
 Register Address: **D7h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | TSa6F1 | TSa6F3 | TSa6F5 | TSa6F7 | TSa6F9 | TSa6F11 | TSa6F13 | TSa6F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa6 Bit of Frame 1 (TSa6F1)

Bit 6: Sa6 Bit of Frame 3 (TSa6F3)

Bit 5: Sa6 Bit of Frame 5 (TSa6F5)

Bit 4: Sa6 Bit of Frame 7 (TSa6F7)

Bit 3: Sa6 Bit of Frame 9 (TSa6F9)

Bit 2: Sa6 Bit of Frame 11 (TSa6F11)

Bit 1: Sa6 Bit of Frame 13 (TSa6F13)

Bit 0: Sa6 Bit of Frame 15 (TSa6F15)

Register Name: **TR.TSa7**
 Register Description: **Transmit Sa7 Bits**
 Register Address: **D8h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | TSa7F1 | TSa7F3 | TSa7F5 | TSa7F7 | TSa7F9 | TSa7F11 | TSa7F13 | TSa7F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa7 Bit of Frame 1 (TSa7F1)

Bit 6: Sa7 Bit of Frame 3 (TSa7F3)

Bit 5: Sa7 Bit of Frame 5 (TSa7F5)

Bit 4: Sa7 Bit of Frame 7 (TSa7F7)

Bit 3: Sa7 Bit of Frame 9 (TSa7F9)

Bit 2: Sa7 Bit of Frame 11 (TSa7F11)

Bit 1: Sa7 Bit of Frame 13 (TSa7F13)

Bit 0: Sa7 Bit of Frame 15 (TSa7F15)

Register Name: **TR.TSa8**
 Register Description: **Transmit Sa8 Bits**
 Register Address: **D9h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|---------|---------|---------|
| Name | TSa8F1 | TSa8F3 | TSa8F5 | TSa8F7 | TSa8F9 | TSa8F11 | TSa8F13 | TSa8F15 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa8 Bit of Frame 1 (TSa8F1)

Bit 6: Sa8 Bit of Frame 3 (TSa8F3)

Bit 5: Sa8 Bit of Frame 5 (TSa8F5)

Bit 4: Sa8 Bit of Frame 7 (TSa8F7)

Bit 3: Sa8 Bit of Frame 9 (TSa8F9)

Bit 2: Sa8 Bit of Frame 11 (TSa8F11)

Bit 1: Sa8 Bit of Frame 13 (TSa8F13)

Bit 0: Sa8 Bit of Frame 15 (TSa8F15)

Register Name: **TR.TSACR**
 Register Description: **Transmit Sa Bit Control Register**
 Register Address: **DAh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|----|-----|-----|-----|-----|-----|
| Name | SiAF | SiNAF | RA | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: International Bit in Align Frame Insertion Control Bit (SiAF)

0 = do not insert data from the TR.TSiAF register into the transmit data stream
 1 = insert data from the TR.TSiAF register into the transmit data stream

Bit 6: International Bit in Nonalign Frame Insertion Control Bit (SiNAF)

0 = do not insert data from the TR.TSiNAF register into the transmit data stream
 1 = insert data from the TR.TSiNAF register into the transmit data stream

Bit 5: Remote Alarm Insertion Control Bit (RA)

0 = do not insert data from the TR.TRA register into the transmit data stream
 1 = insert data from the TR.TRA register into the transmit data stream

Bit 4: Additional Bit 4 Insertion Control Bit (Sa4)

0 = do not insert data from the TR.TSa4 register into the transmit data stream
 1 = insert data from the TR.TSa4 register into the transmit data stream

Bit 3: Additional Bit 5 Insertion Control Bit (Sa5)

0 = do not insert data from the TR.TSa5 register into the transmit data stream
 1 = insert data from the TR.TSa5 register into the transmit data stream

Bit 2: Additional Bit 6 Insertion Control Bit (Sa6)

0 = do not insert data from the TR.TSa6 register into the transmit data stream
 1 = insert data from the TR.TSa6 register into the transmit data stream

Bit 1: Additional Bit 7 Insertion Control Bit (Sa7)

0 = do not insert data from the TR.TSa7 register into the transmit data stream
 1 = insert data from the TR.TSa7 register into the transmit data stream

Bit 0: Additional Bit 8 Insertion Control Bit (Sa8)

0 = do not insert data from the TR.TSa8 register into the transmit data stream
 1 = insert data from the TR.TSa8 register into the transmit data stream

Register Name: **TR.BAWC**
 Register Description: **BERT Alternating Word-Count Rate**
 Register Address: **DBh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | ACNT7 | ACNT6 | ACNT5 | ACNT4 | ACNT3 | ACNT2 | ACNT1 | ACNT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Alternating Word-Count Rate Bits 7 to 0 (ACNT7 to ACNT0). ACNT0 is the LSB of the 8-bit alternating word-count rate counter.

Register Name: **TR.BRP1**
 Register Description: **BERT Repetitive Pattern Set Register 1**
 Register Address: **DCh**

| | | | | | | | | |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RPAT7 | RPAT6 | RPAT5 | RPAT4 | RPAT3 | RPAT2 | RPAT1 | RPAT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 7 to 0 (RPAT7 to RPAT0). RPAT0 is the LSB of the 32-bit repetitive pattern set.

Register Name: **TR.BRP2**
 Register Description: **BERT Repetitive Pattern Set Register 2**
 Register Address: **DDh**

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RPAT15 | RPAT14 | RPAT13 | RPAT12 | RPAT11 | RPAT10 | RPAT9 | RPAT8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 15 to 8 (RPAT15 to RPAT8)

Register Name: **TR.BRP3**
 Register Description: **BERT Repetitive Pattern Set Register 3**
 Register Address: **DEh**

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RPAT23 | RPAT22 | RPAT21 | RPAT20 | RPAT19 | RPAT18 | RPAT17 | RPAT16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 23 to 16 (RPAT23 to RPAT16)

Register Name: **TR.BRP4**
 Register Description: **BERT Repetitive Pattern Set Register 4**
 Register Address: **DFh**

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RPAT31 | RPAT30 | RPAT29 | RPAT28 | RPAT27 | RPAT26 | RPAT25 | RPAT24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 31 to 24 (RPAT31 to RPAT24). RPAT31 is the LSB of the 32-bit repetitive pattern set.

Register Name: **TR.BC1**
 Register Description: **BERT Control Register 1**
 Register Address: **E0h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|------|------|-----|-----|-----|----|--------|
| Name | TC | TINV | RINV | PS2 | PS1 | PS0 | LC | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Pattern Load (TC). A low-to-high transition loads the pattern generator with the pattern that is to be generated. This bit should be toggled from low to high whenever the host wishes to load a new pattern. Must be cleared and set again for subsequent loads.

Bit 6: Transmit Invert-Data Enable (TINV)

0 = do not invert the outgoing data stream

1 = invert the outgoing data stream

Bit 5: Receive Invert-Data Enable (RINV)

0 = do not invert the incoming data stream

1 = invert the incoming data stream

Bits 4 to 2: Pattern Select Bits (PS2 to PS0)

| PS2 | PS1 | PS0 | Pattern Definition |
|-----|-----|-----|---|
| 0 | 0 | 0 | Pseudorandom 2E7 - 1 |
| 0 | 0 | 1 | Pseudorandom 2E11 - 1 |
| 0 | 1 | 0 | Pseudorandom 2E15 - 1 |
| 0 | 1 | 1 | Pseudorandom pattern QRSS. A $2^{20} - 1$ pattern with 14 consecutive zero restrictions. |
| 1 | 0 | 0 | Repetitive pattern |
| 1 | 0 | 1 | Alternating word pattern |
| 1 | 1 | 0 | Modified 55 octet (Daly) pattern. The Daly pattern is a repeating 55 octet pattern that is byte-aligned into the active DS0 time slots. The pattern is defined in an ATIS (Alliance for Telecommunications Industry Solutions) Committee T1 Technical Report Number 25 (November 1993). |
| 1 | 1 | 1 | Pseudorandom 2E9 - 1 |

Bit 1: Load Bit and Error Counters (LC). A low-to-high transition latches the current bit and error counts into registers TR.BBC1/TR.BBC2/TR.BBC3/TR.BBC4 and TR.BEC1/TR.BEC2/TR.BEC3 and clears the internal count. This bit should be toggled from low to high whenever the host wishes to begin a new acquisition period. Must be cleared and set again for subsequent loads.

Bit 0: Force Resynchronization (RESYNC). A low-to-high transition forces the receive BERT synchronizer to resynchronize to the incoming data stream. This bit should be toggled from low to high whenever the host wishes to acquire synchronization on a new pattern. Must be cleared and set again for a subsequent resynchronization.

Register Name: **TR.BC2**
 Register Description: **BERT Control Register 2**
 Register Address: **E1h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|-----|------|------|------|------|
| Name | EIB2 | EIB1 | EIB0 | SBE | RPL3 | RPL2 | RPL1 | RPL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 5: Error Insert Bits 2 to 0 (EIB2 to EIB0). Automatically inserts bit errors at the prescribed rate into the generated data pattern. Can be used for verifying error-detection features.

| EIB2 | EIB1 | EIB0 | Error Rate Inserted |
|------|------|------|----------------------------------|
| 0 | 0 | 0 | No errors automatically inserted |
| 0 | 0 | 1 | 10E-1 |
| 0 | 1 | 0 | 10E-2 |
| 0 | 1 | 1 | 10E-3 |
| 1 | 0 | 0 | 10E-4 |
| 1 | 0 | 1 | 10E-5 |
| 1 | 1 | 0 | 10E-6 |
| 1 | 1 | 1 | 10E-7 |

Bit 4: Single Bit-Error Insert (SBE). A low-to-high transition creates a single-bit error. Must be cleared and set again for a subsequent bit error to be inserted.

Bits 3 to 0: Repetitive Pattern Length Bit 3 (RPL3 to RPL0). RPL0 is the LSB and RPL3 is the MSB of a nibble that describes how long the repetitive pattern is. The valid range is 17 (0000) to 32 (1111). These bits are ignored if the receive BERT is programmed for a pseudorandom pattern. To create repetitive patterns fewer than 17 bits in length, the user must set the length to an integer number of the desired length that is less than or equal to 32. For example, to create a 6-bit pattern, the user can set the length to 18 (0001) or to 24 (0111) or to 30 (1101).

| Length (bits) | RPL3 | RPL2 | RPL1 | RPL0 |
|---------------|------|------|------|------|
| 17 | 0 | 0 | 0 | 0 |
| 18 | 0 | 0 | 0 | 1 |
| 19 | 0 | 0 | 1 | 0 |
| 20 | 0 | 0 | 1 | 1 |
| 21 | 0 | 1 | 0 | 0 |
| 22 | 0 | 1 | 0 | 1 |
| 23 | 0 | 1 | 1 | 0 |
| 24 | 0 | 1 | 1 | 1 |
| 25 | 1 | 0 | 0 | 0 |
| 26 | 1 | 0 | 0 | 1 |
| 27 | 1 | 0 | 1 | 0 |
| 28 | 1 | 0 | 1 | 1 |
| 29 | 1 | 1 | 0 | 0 |
| 30 | 1 | 1 | 0 | 1 |
| 31 | 1 | 1 | 1 | 0 |
| 32 | 1 | 1 | 1 | 1 |

Register Name: **TR.BBC1**
 Register Description: **BERT Bit Count Register 1**
 Register Address: **E3h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | BBC7 | BBC6 | BBC5 | BBC4 | BBC3 | BBC2 | BBC1 | BBC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 7 to 0 (BBC7 to BBC0). BBC0 is the LSB of the 32-bit counter.

Register Name: **TR.BBC2**
 Register Description: **BERT Bit Count Register 2**
 Register Address: **E4h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|------|------|
| Name | BBC15 | BBC14 | BBC13 | BBC12 | BBC11 | BBC10 | BBC9 | BBC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 15 to 8 (BBC15 to BBC8)

Register Name: **TR.BBC3**
 Register Description: **BERT Bit Count Register 3**
 Register Address: **E5h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | BBC23 | BBC22 | BBC21 | BBC20 | BBC19 | BBC18 | BBC17 | BBC16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 23 to 16 (BBC23 to BBC16)

Register Name: **TR.BBC4**
 Register Description: **BERT Bit Count Register 4**
 Register Address: **E6h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | BBC31 | BBC30 | BBC29 | BBC28 | BBC27 | BBC26 | BBC25 | BBC24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 31 to 24 (BBC31 to BBC24). BBC31 is the MSB of the 32-bit counter.

Register Name: **TR.BEC1**
 Register Description: **BERT Error-Count Register 1**
 Register Address: **E7h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Counter Bits 7 to 0 (EC7 to EC0). EC0 is the LSB of the 24-bit counter.

Register Name: **TR.BEC2**
 Register Description: **BERT Error-Count Register 2**
 Register Address: **E8h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|-----|-----|
| Name | EC15 | EC14 | EC13 | EC12 | EC11 | EC10 | EC9 | EC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Counter Bits 15 to 8 (EC15 to EC8)

Register Name: **TR.BEC3**
 Register Description: **BERT Error-Count Register 3**
 Register Address: **E9h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | EC23 | EC22 | EC21 | EC20 | EC19 | EC18 | EC17 | EC16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Counter Bits 23 to 16 (EC23 to EC16). EC0 is the MSB of the 24-bit counter.

Register Name: **TR.BIC**
 Register Description: **BERT Interface Control Register**
 Register Address: **EAh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|---|------|------|---|---------|--------|
| Name | — | RFUS | — | TBAT | TFUS | — | BERTDIR | BERTEN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Receive Framed/Unframed Select (RFUS)

- 0 = BERT is not sent data from the F-bit position (framed)
- 1 = BERT is sent data from the F-bit position (unframed)

Bit 4: Transmit Byte-Align Toggle (TBAT). A 0-to-1 transition forces the BERT to byte align its pattern with the transmit formatter. This bit must be transitioned in order to byte align the Daly pattern.

Bit 3: Transmit Framed/Unframed Select (TFUS)

- 0 = BERT does not source data into the F-bit position (framed)
- 1 = BERT does source data into the F-bit position (unframed)

Bit 1: BERT Direction (BERTDIR)

0 = network

BERT transmits toward the network (TTIP and TRING) and receives from the network (RTIP and RRING). The BERT pattern can be looped back to the receiver internally by using the framer loopback function.

1 = system

BERT transmits toward the system backplane (RSERO) and receives from the system backplane (TSERI).

Bit 0: BERT Enable (BERTEN)

0 = BERT disabled

1 = BERT enabled

Register Name: **TR.ERC**
 Register Description: **Error-Rate Control Register**
 Register Address: **EBh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|---|---|----|-----|-----|-----|-----|
| Name | WNOE | — | — | CE | ER3 | ER2 | ER1 | ER0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Write NOE Registers (WNOE). If the host wishes to update to the TR.NOEx registers, this bit must be toggled from a 0 to a 1 after the host has already loaded the prescribed error count into the TR.NOEx registers. The toggling of this bit causes the error count loaded into the TR.NOEx registers to be loaded into the error-insertion circuitry on the next clock cycle. Subsequent updates require that the WNOE bit be set to 0 and then 1 once again.

Bit 4: Constant Errors (CE). When this bit is set high (and the ER0 to ER3 bits are not set to 0000), the error-insertion logic ignores the number-of-error registers (TR.NOE1, TR.NOE2) and generates errors constantly at the selected insertion rate. When CE is set to 0, the TR.NOEx registers determine how many errors are to be inserted.

Bits 3 to 0: Error-Insertion Rate Select Bits (ER3 to ER0)

| ER3 | ER2 | ER1 | ER0 | Error Rate |
|-----|-----|-----|-----|--------------------|
| 0 | 0 | 0 | 0 | No errors inserted |
| 0 | 0 | 0 | 1 | 1 in 16 |
| 0 | 0 | 1 | 0 | 1 in 32 |
| 0 | 0 | 1 | 1 | 1 in 64 |
| 0 | 1 | 0 | 0 | 1 in 128 |
| 0 | 1 | 0 | 1 | 1 in 256 |
| 0 | 1 | 1 | 0 | 1 in 512 |
| 0 | 1 | 1 | 1 | 1 in 1024 |
| 1 | 0 | 0 | 0 | 1 in 2048 |
| 1 | 0 | 0 | 1 | 1 in 4096 |
| 1 | 0 | 1 | 0 | 1 in 8192 |
| 1 | 0 | 1 | 1 | 1 in 16,384 |
| 1 | 1 | 0 | 0 | 1 in 32,768 |
| 1 | 1 | 0 | 1 | 1 in 65,536 |
| 1 | 1 | 1 | 0 | 1 in 131,072 |
| 1 | 1 | 1 | 1 | 1 in 262,144 |

Register Name: **TR.NOE1**
 Register Description: **Number-of-Errors 1**
 Register Address: **ECh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Number-of-Errors Counter Bits 7 to 0 (C7 to C0). Bit C0 is the LSB of the 10-bit counter.

Register Name: **TR.NOE2**
 Register Description: **Number-of-Errors 2**
 Register Address: **EDh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|----|----|
| Name | — | — | — | — | — | — | C9 | C8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 1 and 0: Number-of-Errors Counter Bits 9 and 8 (C9 and C8). Bit C9 is the MSB of the 10-bit counter.

12.7.1 Number-of-Errors Left Register

The host can read the TR.NOELx registers at any time to determine how many errors are left to be inserted.

Register Name: **TR.NOEL1**
 Register Description: **Number-of-Errors Left 1**
 Register Address: **EEh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Number-of-Errors Left Counter Bits 7 to 0 (C7 to C0). Bit C0 is the LSB of the 10-bit counter.

Register Name: **TR.NOEL2**
 Register Description: **Number-of-Errors Left 2**
 Register Address: **EFh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|----|----|
| Name | — | — | — | — | — | — | C9 | C8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 1 and 0: Number-of-Errors Left Counter Bits 9 and 8 (C9 and C8). Bit C9 is the MSB of the 10-bit counter.

13 FUNCTIONAL TIMING

13.1 MII and RMII Interfaces

Each MII Interface Transmit Port has its own TX_CLK and data interface. The data TXD [3:0] operates synchronously with TX_CLK. The LSB is presented first. TX_CLK should be 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation. TX_EN is valid at the same time as the first byte of the preamble. In DTE Mode TX_CLK is input from the external PHY. In DCE Mode, the device provides TX_CLK, derived from an external reference (SYSCLKI).

In Half-Duplex (DTE) Mode, the device supports CRS and COL signals. CRS is active when the PHY detects transmit or receive activity. If there is a collision as indicated by the COL input, the device will replace the data nibbles with jam nibbles. After a “random” time interval, the packet is retransmitted. The MAC will try to send the packet a maximum of 16 times. The jam sequence consists of 55555555h. Note that the COL signal and CRS can be asynchronous to the TX_CLK and are only valid in half duplex mode.

Figure 13-1. MII Transmit Functional Timing

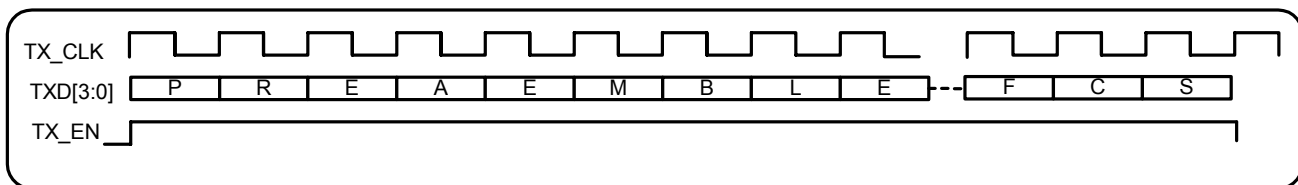
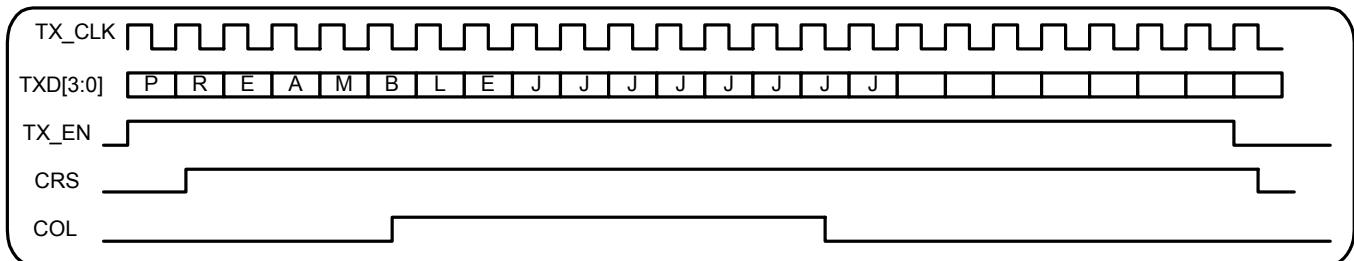
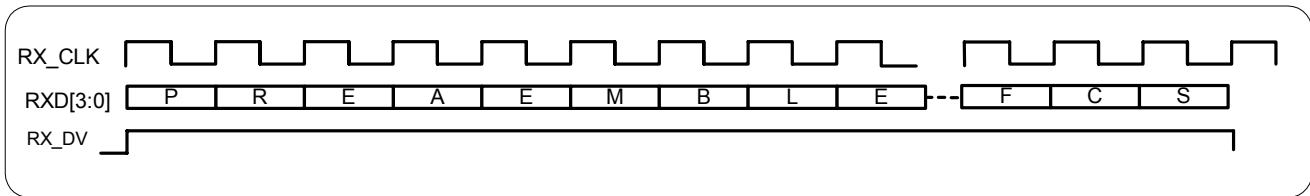


Figure 13-2. MII Transmit Half Duplex with a Collision Functional Timing



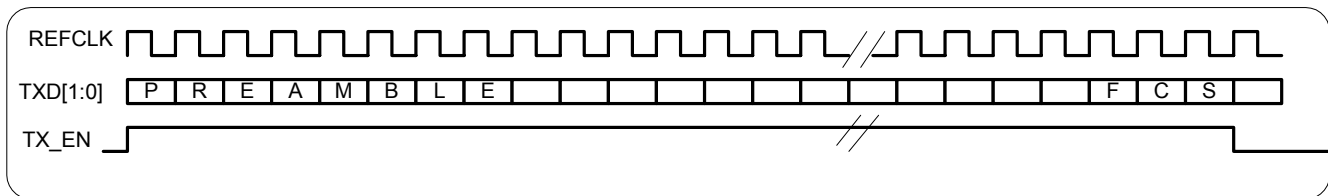
Receive Data (RXD[3:0]) is clocked from the external PHY synchronously with RX_CLK. The RX_CLK signal is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation. RX_DV is asserted by the PHY from the first Nibble of the preamble in 100Mbps operation or first nibble of SFD for 10Mbps operation. The data on RXD[3:0] is not accepted by the MAC if RX_DV is low or RX_ERR is high (in DTE mode). RX_ERR should be tied low when in DCE Mode.

Figure 13-3. MII Receive Functional Timing



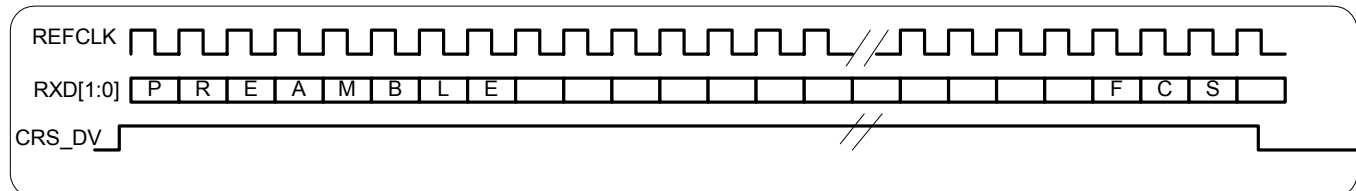
In RMII Mode, TX_EN is high with the first bit of the preamble. The TXD[1:0] is synchronous with the 50MHz REF_CLK. For 10Mbps operation, the data bit outputs are updated every 10 clocks.

Figure 13-4. RMII Transmit Interface Functional Timing



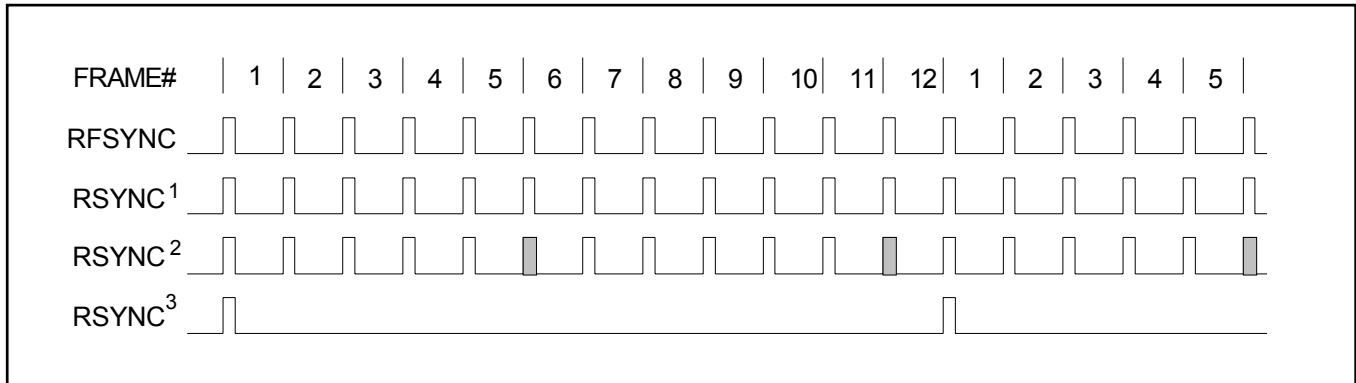
RMII Receive data on RXD[1:0] is expected to be synchronous with the rising edge of the 50MHz REF_CLK. The data is only valid if CRS_DV is high. The external PHY asynchronously drives CRS_DV low during carrier loss.

Figure 13-5. RMII Receive Interface Functional Timing



13.2 T1 Mode

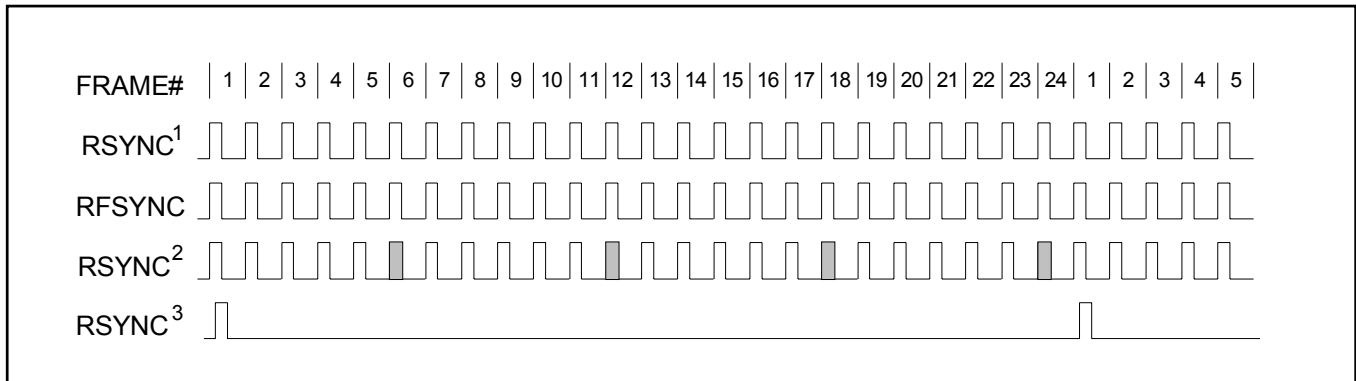
Figure 13-6. Receive Side D4 Timing



NOTES:

- 1) RSYNC in the frame mode (TR.IOCR1.5 = 0) and double-wide frame sync is not enabled (TR.IOCR1.6 = 0).
- 2) RSYNC in the frame mode (TR.IOCR1.5 = 0) and double-wide frame sync is enabled (TR.IOCR1.6 = 1).
- 3) RSYNC in the multiframe mode (TR.IOCR1.5 = 1).

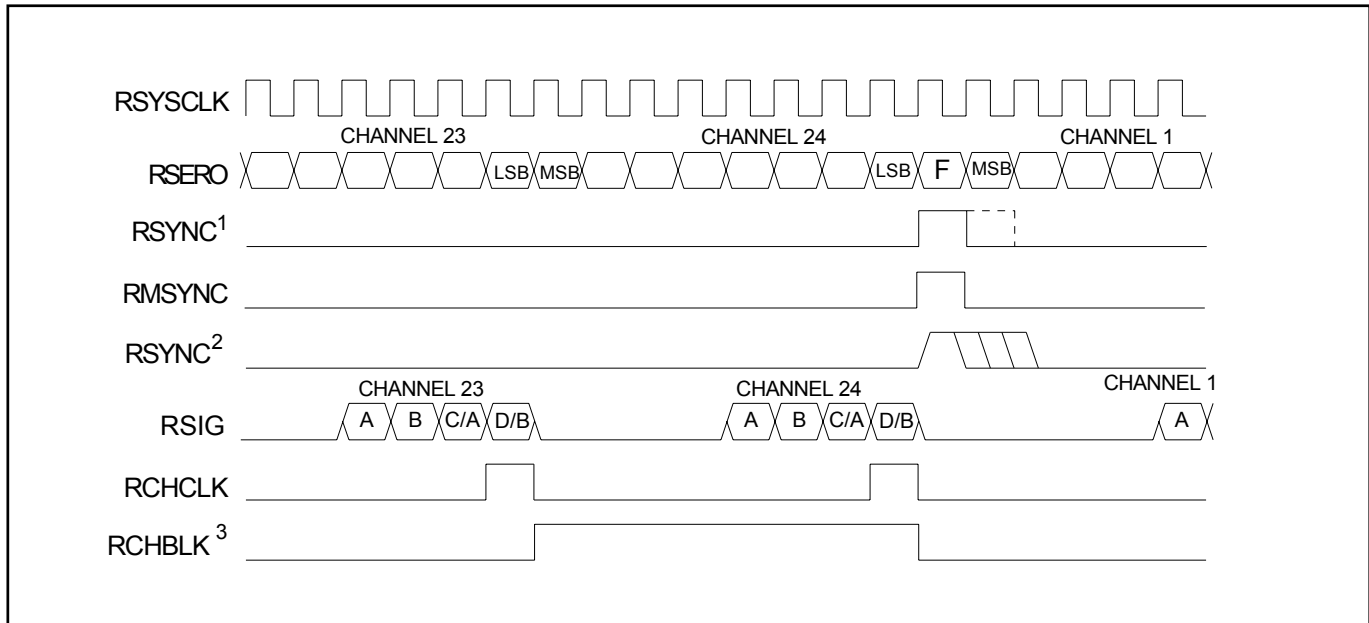
Figure 13-7. Receive Side ESF Timing



NOTES:

- 1) RSYNC in frame mode (TR.IOCR1.4 = 0) and double-wide frame sync is not enabled (TR.IOCR1.6 = 0).
- 2) RSYNC in frame mode (TR.IOCR1.4 = 0) and double-wide frame sync is enabled (TR.IOCR1.6 = 1).
- 3) RSYNC in multiframe mode (TR.IOCR1.4 = 1).

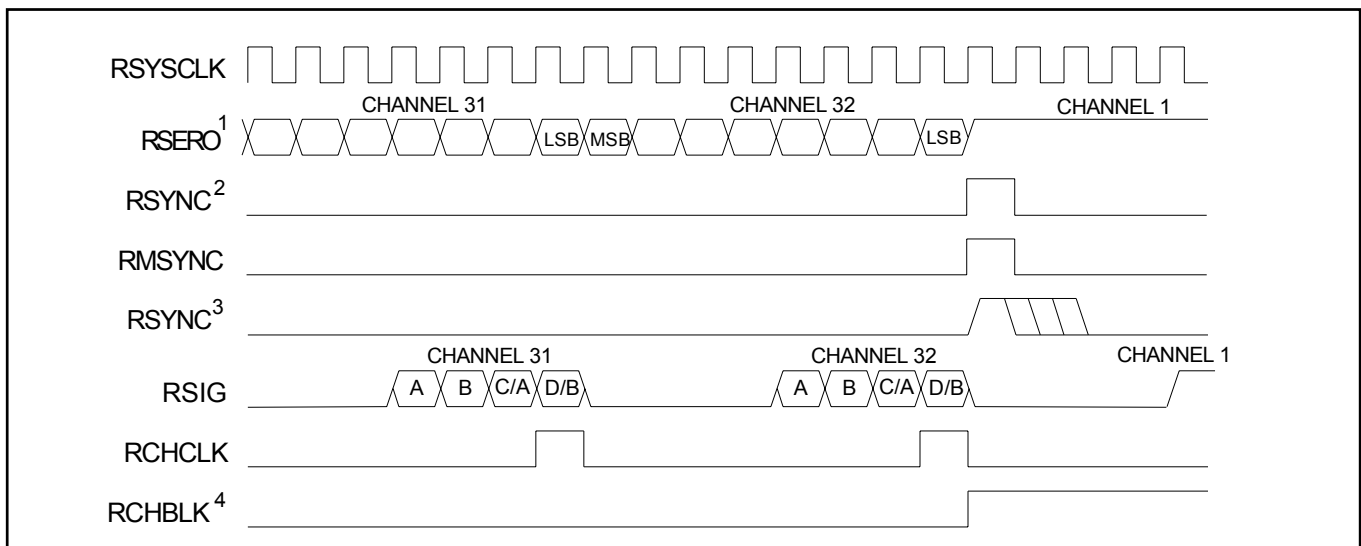
Figure 13-8. Receive Side 1.544MHz Boundary Timing (With Elastic Store Enabled)



NOTES:

- 1) RSYNC is in the output mode (TR.IOCR1.4 = 0).
- 2) RSYNC is in the input mode (TR.IOCR1.4 = 1).
- 3) RCHBLK is programmed to block channel 24.

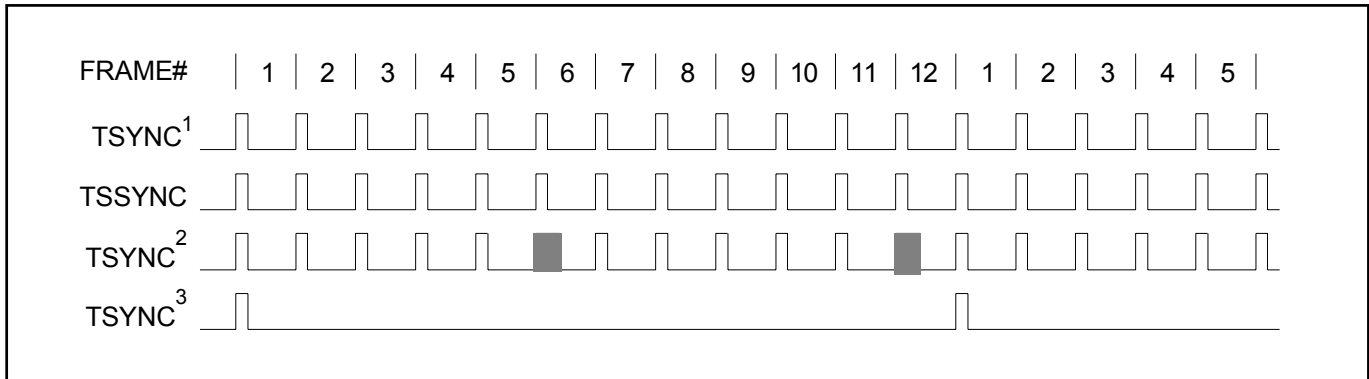
Figure 13-9. Receive Side 2.048MHz Boundary Timing (With Elastic Store Enabled)



NOTES:

- 1) RSERO data in channels 1, 5, 9, 13, 17, 21, 25, and 29 are forced to one.
- 2) RSYNC is in the output mode (TR.IOCR1.4 = 0).
- 3) RSYNC is in the input mode (TR.IOCR1.4 = 1).
- 4) RCHBLK is forced to one in the same channels as RSERO (Note 1).
- 5) The F-bit position is passed through the receive-side elastic store.

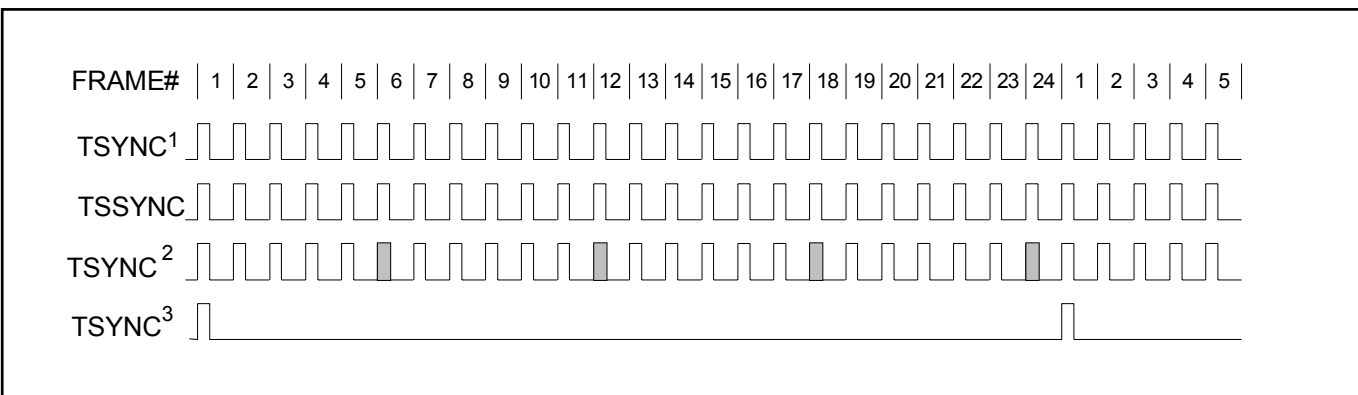
Figure 13-10. Transmit Side D4 Timing



NOTES:

- 1) TSYNC in the frame mode (TR.IOCR1.2 = 0) and double-wide frame sync is not enabled (TR.IOCR1.1 = 0).
- 2) TSYNC in the frame mode (TR.IOCR1.2 = 0) and double-wide frame sync is enabled (TR.IOCR1.1 = 1).
- 3) TSYNC in the multiframe mode (TR.IOCR1.2 = 1).

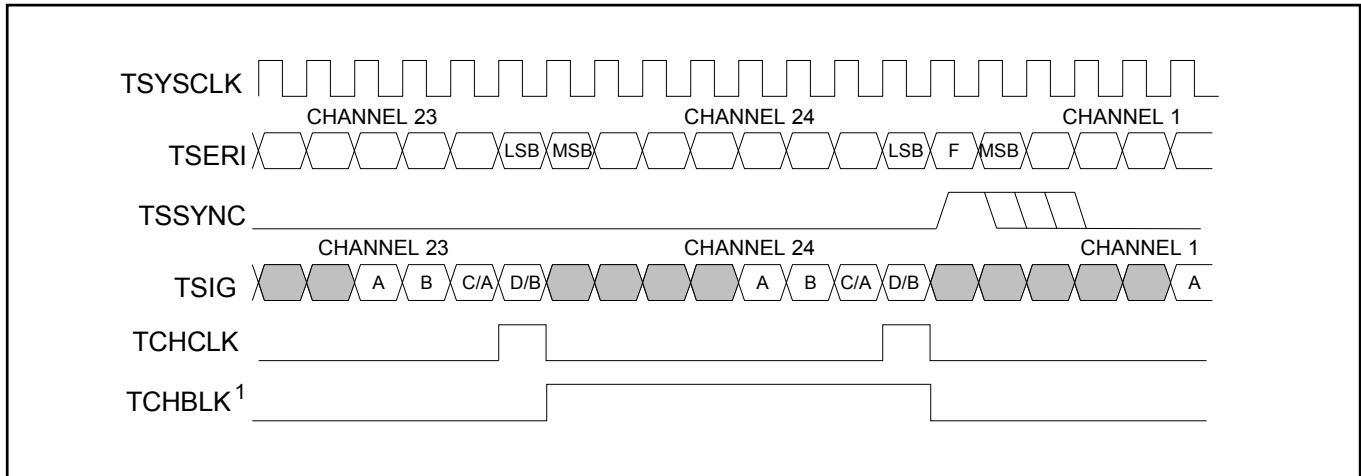
Figure 13-11. Transmit Side ESF Timing



NOTES:

- 1) TSYNC in frame mode (TR.IOCR1.2 = 0) and double-wide frame sync is not enabled (TR.IOCR1.3 = 0).
- 2) TSYNC in frame mode (TR.IOCR1.2 = 0) and double-wide frame sync is enabled (TR.IOCR1.3 = 1).
- 3) TSYNC in multiframe mode (TR.IOCR1.2 = 1).

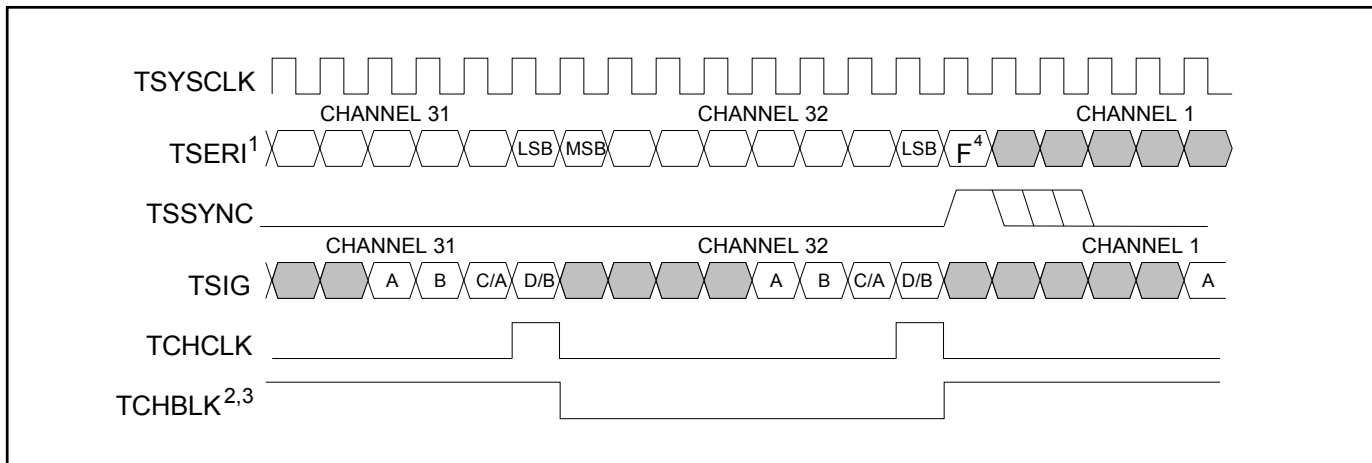
Figure 13-12. Transmit Side 1.544MHz Boundary Timing (With Elastic Store Enabled)



NOTE:

- 1) TCHBLK is programmed to block channel 24 (if the TPCSI bit is set, then the signaling data at TSIG will be ignored during channel 24).

Figure 13-13. Transmit Side 2.048MHz Boundary Timing (With Elastic Store Enabled)

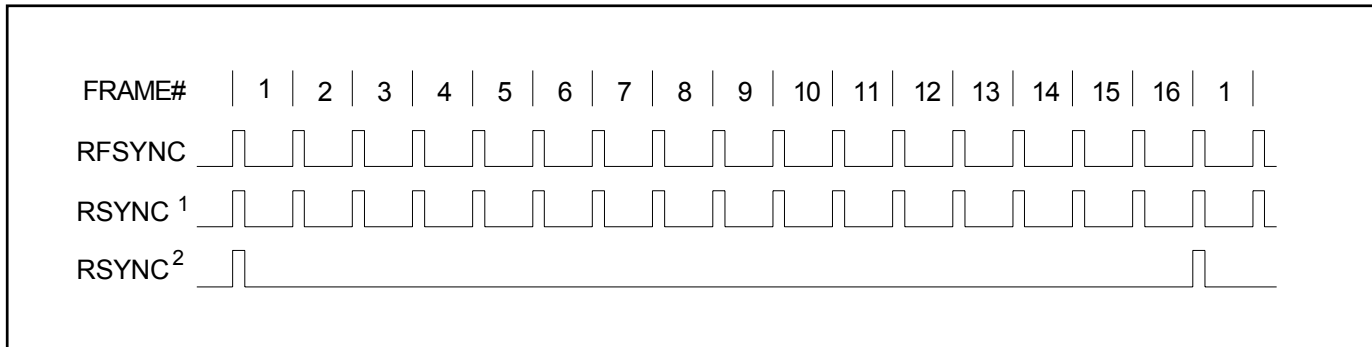


NOTES:

- 1) TSERI data in channels 1, 5, 9, 13, 17, 21, 25, and 29 is ignored.
- 2) TCHBLK is programmed to block channel 31 (if the TPCSI bit is set, then the signaling data at TSIG will be ignored).
- 3) TCHBLK is forced to one in the same channels as TSERI is ignored (Note 1).
- 4) The F-bit position for the T1 frame is sampled and passed through the transmit side elastic store into the MSB bit position of channel 1. (Normally the transmit side formatter overwrites the F-bit position unless the formatter is programmed to pass-through the F-bit position).

13.3 E1 Mode

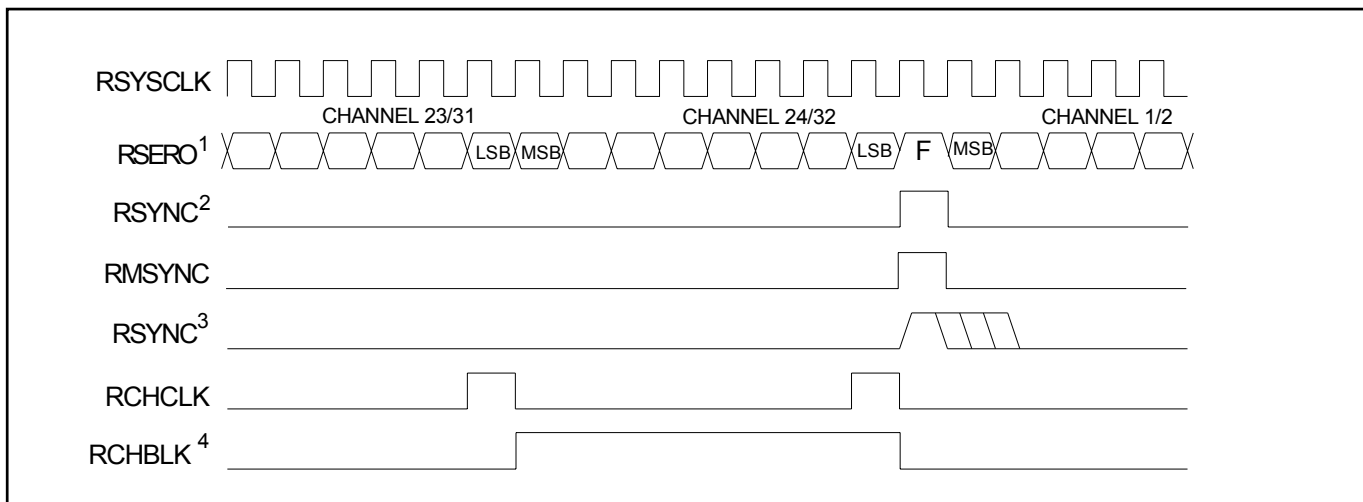
Figure 13-14. Receive Side Timing



NOTES:

- 1) RSYNC in frame mode (TR.IOCR1.5 = 0).
- 2) RSYNC in multiframe mode (TR.IOCR1.5 = 1).
- 3) This diagram assumes the CAS MF begins in the RAF frame.

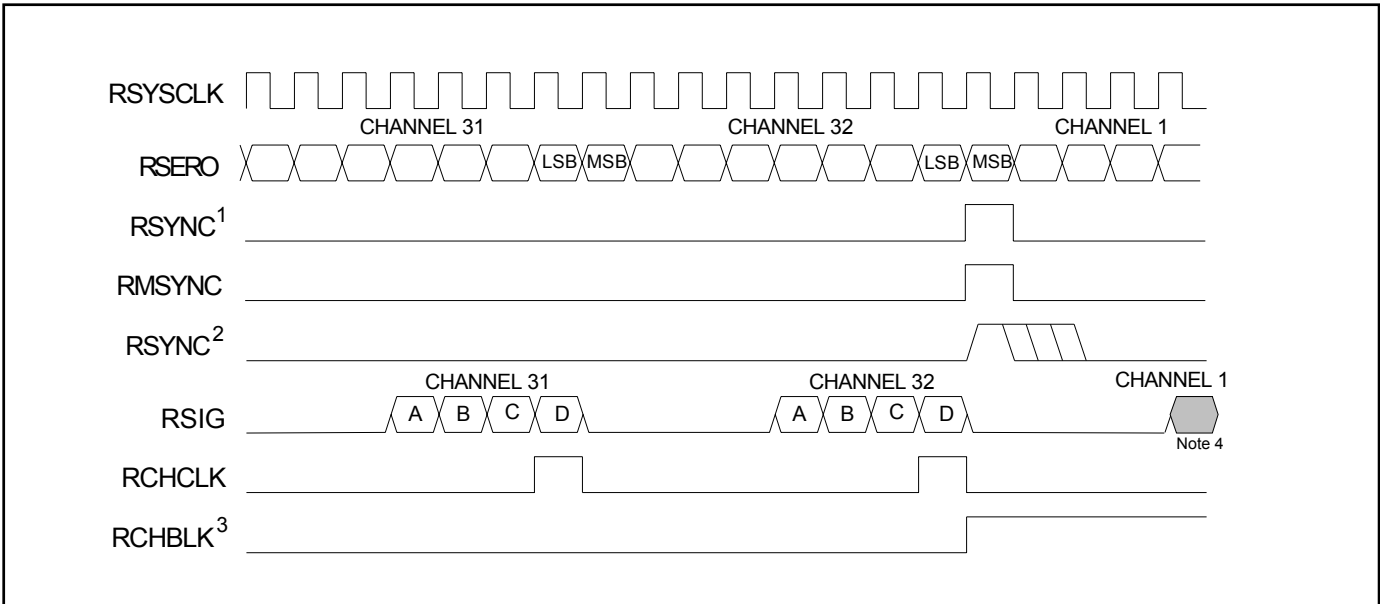
Figure 13-15. Receive Side Boundary Timing, RSYCLK = 1.544MHz (With Elastic Store Enabled)



NOTES:

- 1) Data from the E1 channels 1, 5, 9, 13, 17, 21, 25, and 29 is dropped (channel 2 from the E1 link is mapped to channel 1 of the T1 link, etc.) and the F-bit position is added (forced to one).
- 2) RSYNC in the output mode (TR.IOCR1.4 = 0).
- 3) RSYNC in the input mode (TR.IOCR1.4 = 1).
- 4) RCHBLK is programmed to block channel 24.

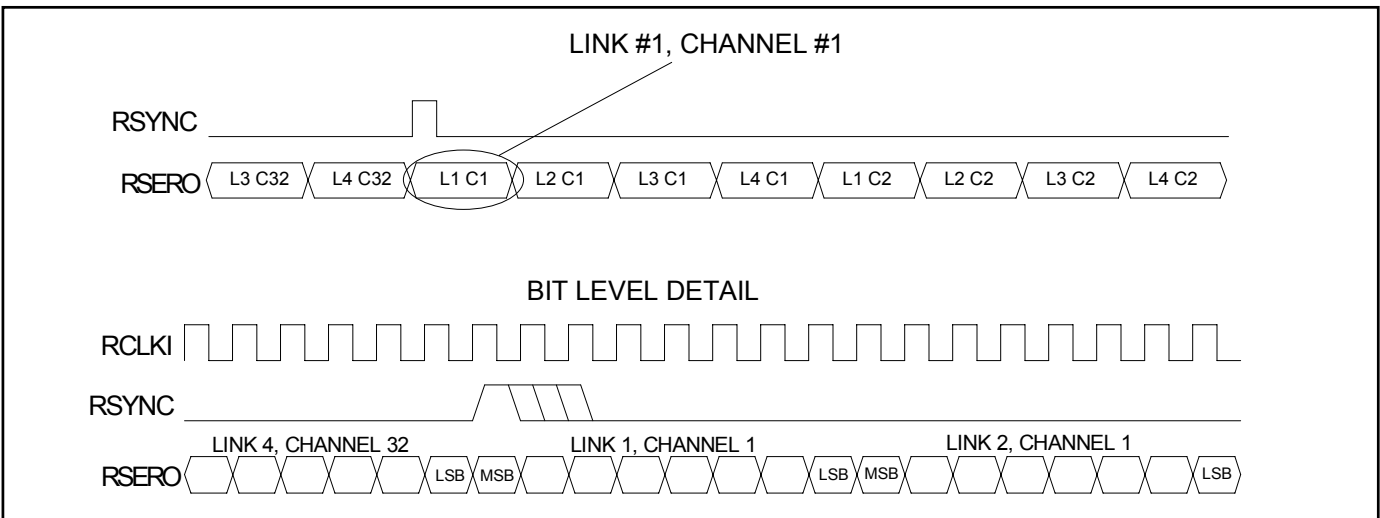
**Figure 13-16. Receive Side Boundary Timing, RSYCLK = 2.048MHz
(With Elastic Store Enabled)**



NOTES:

- 1) RSYNC is in the output mode (TR.IOCR1.4 = 0).
- 2) RSYNC is in the input mode (TR.IOCR1.4 = 1).
- 3) RCHBLK is programmed to block channel 1.
- 4) RSIG normally contains the CAS multiframe-alignment nibble (0000) in channel 1.

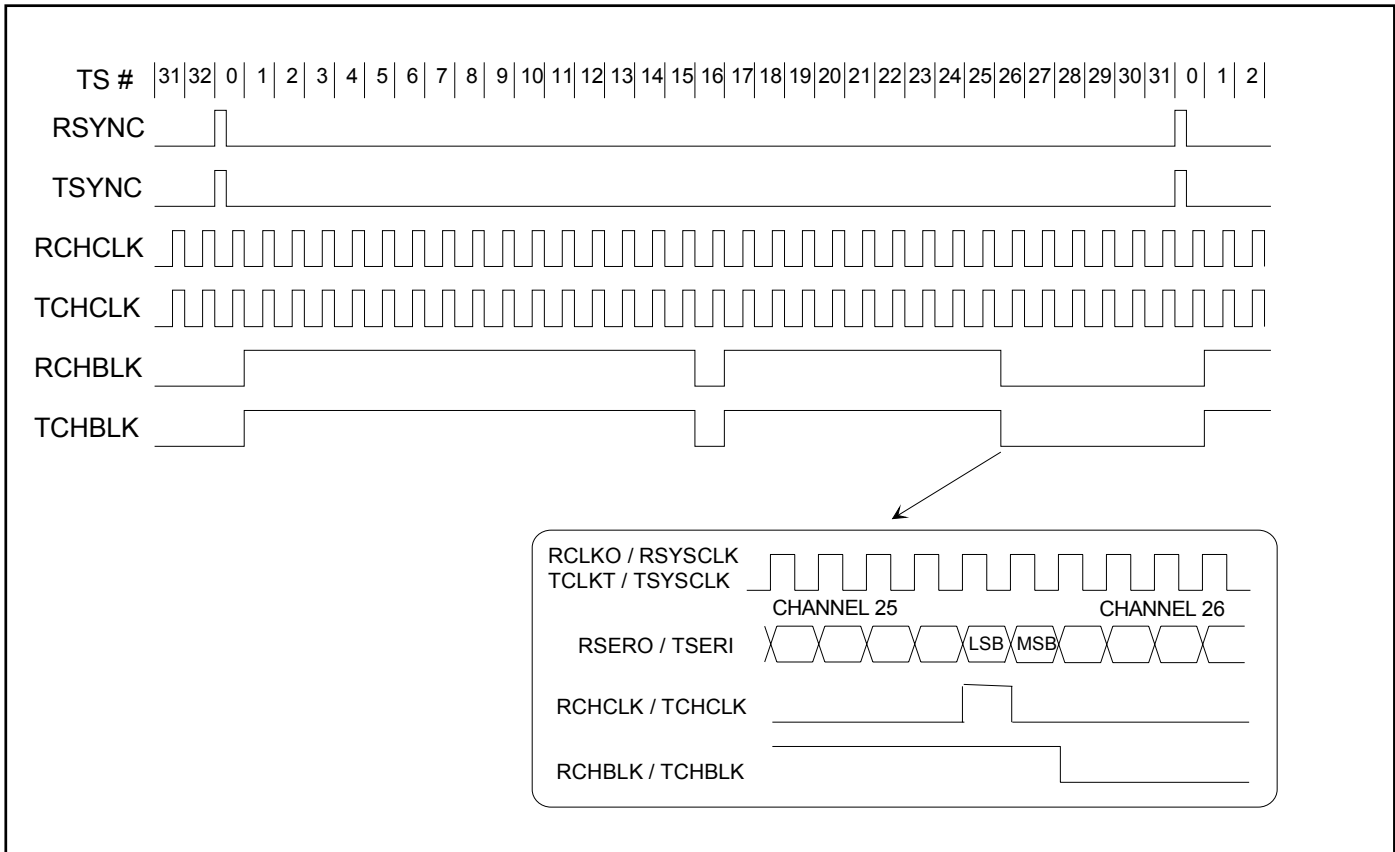
Figure 13-17. Receive IBO Channel Interleave Mode Timing



NOTES:

- 1) 8.192MHz bus configuration.
- 2) Data on unused channels is ignored.

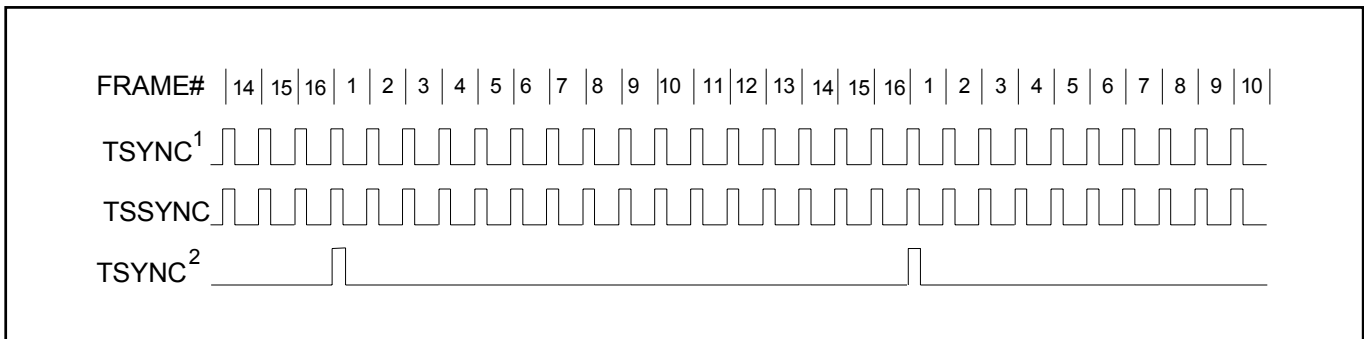
Figure 13-18. G.802 Timing, E1 Mode Only



NOTES:

- 1) RCHBLK or TCHBLK programmed to pulse high during time slots 1 through 15, 17 through 25, and bit 1 of time slot 26.

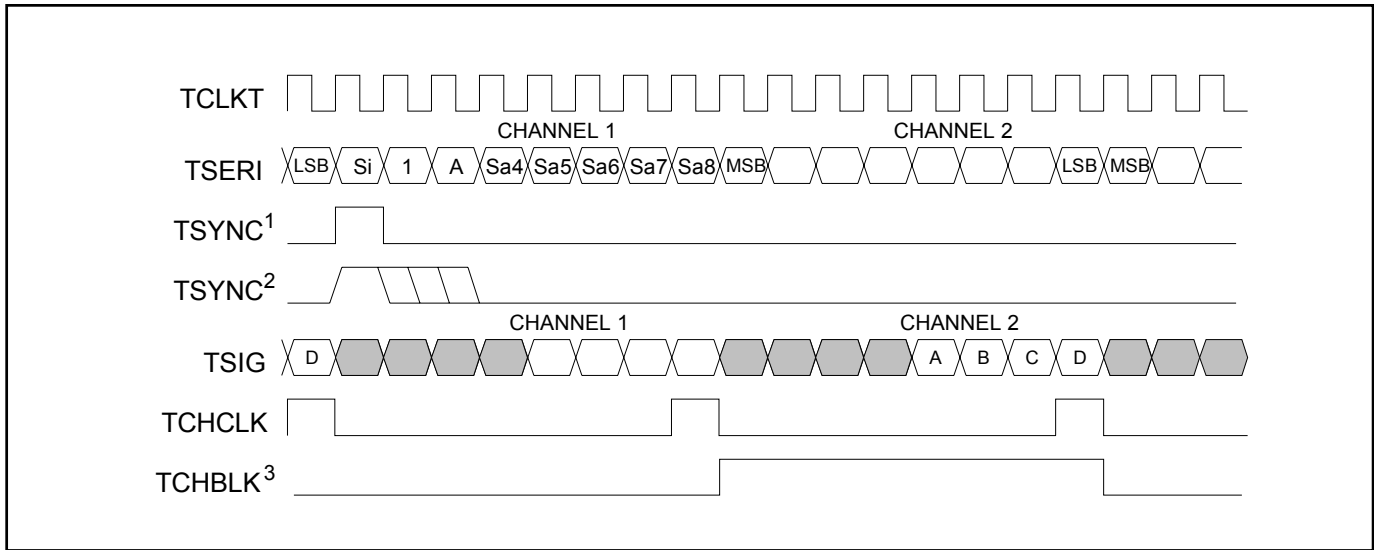
Figure 13-19. Transmit Side Timing



NOTES:

- 1) TSYNC in frame mode (TR.IOCR1.2 = 0).
- 2) TSYNC in multiframe mode (TR.IOCR1.2 = 1).
- 3) This diagram assumes both the CAS MF and the CRC-4 MF begin with the TAF frame.

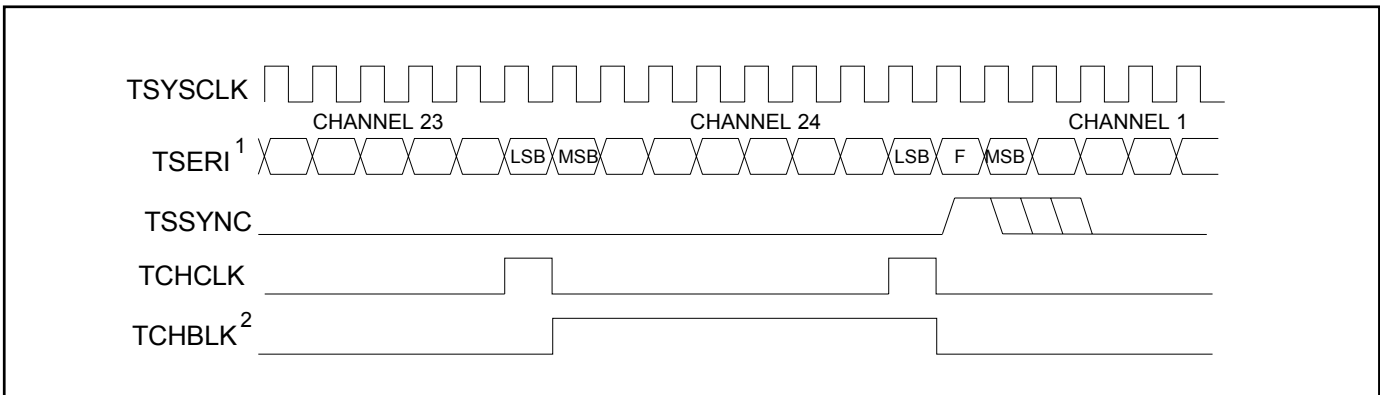
Figure 13-20. Transmit Side Boundary Timing (With Elastic Store Disabled)



NOTES:

- 1) TSYNC is in the output mode (TR.IOCR1.1 = 1.)
- 2) TSYNC is in the input mode (TR.IOCR1.1 = 0).
- 3) TCHBLK is programmed to block channel 2.
- 4) The signaling data at TSIG during channel 1 is normally overwritten in the transmit formatter with the CAS multiframe-alignment nibble (0000).
- 5) Shown is a TNAF frame boundary.

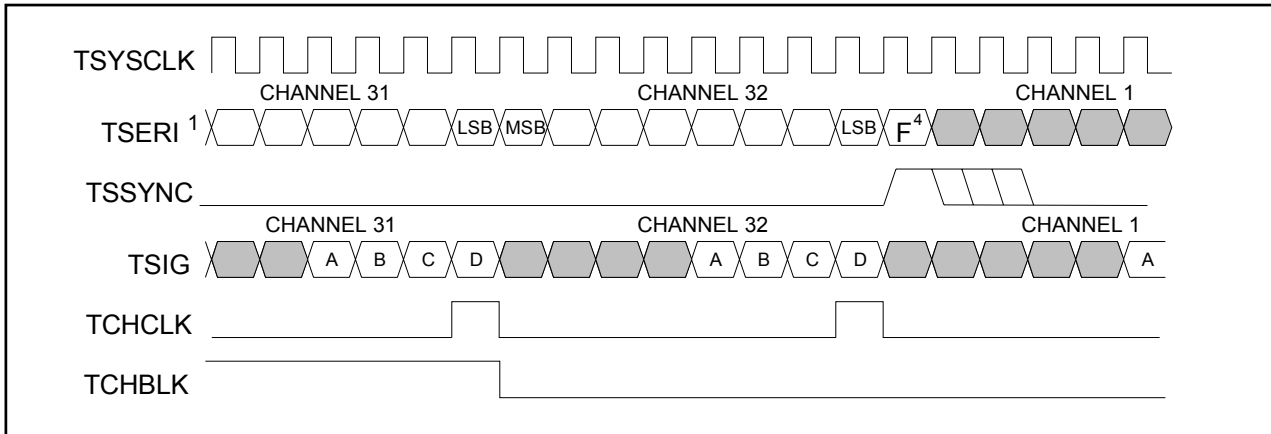
Figure 13-21. Transmit Side Boundary Timing, TSYSCLK = 1.544MHz (With Elastic Store Enabled)



NOTES:

- 1) The F-bit position in the TSERI data is ignored.
- 2) TCHBLK is programmed to block channel 24.

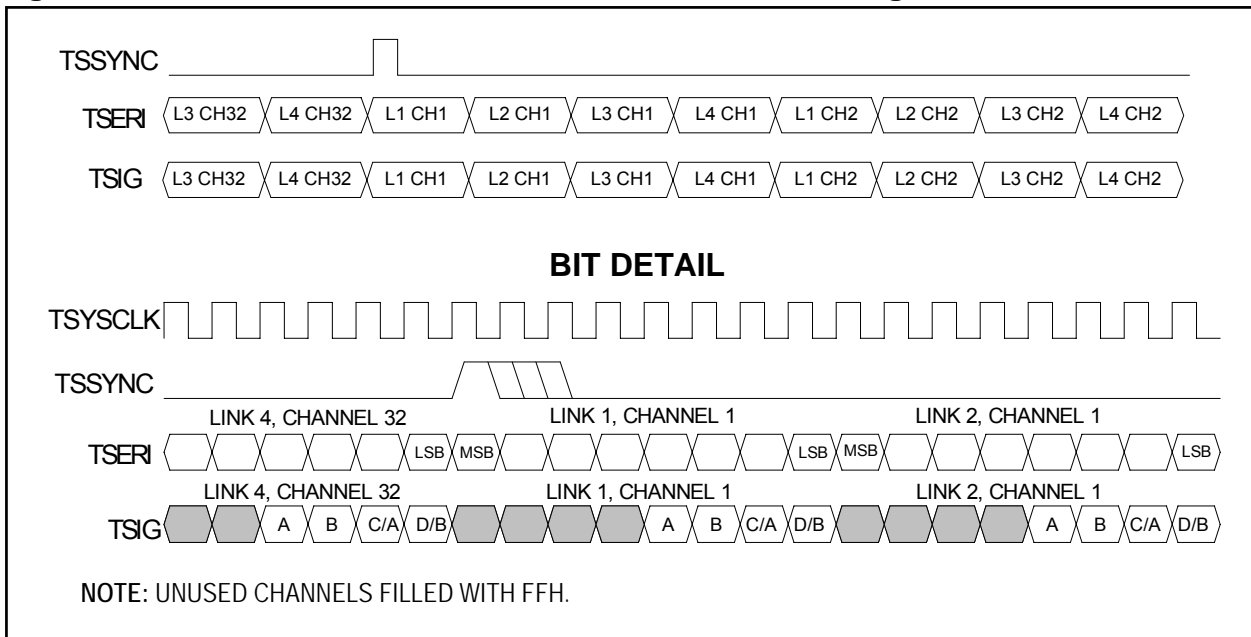
**Figure 13-22. Transmit Side Boundary Timing, TSYCLK = 2.048MHz
(With Elastic Store Enabled)**



NOTE:

- 1) TCHBLK is programmed to block channel 31.

Figure 13-23. Transmit IBO Channel Interleave Mode Timing



14 OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS

| | |
|---|---------------------------------|
| Voltage Range on Any Lead with Respect to V_{SS} (except V_{DD}) | -0.5V to +5.5V |
| Supply Voltage Range ($V_{DD3.3}$) with Respect to V_{SS} | -0.3V to +3.6V |
| Supply Voltage Range ($V_{DD1.8}$) with Respect to V_{SS} | -0.3V to +2.0V |
| Ambient Operating Temperature Range | -40°C to +85°C |
| Junction Operating Temperature Range | 40°C to +125°C |
| Storage Temperature | -55°C to +125°C |
| Soldering Temperature | See IPC/J-STD-020 Specification |

These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability. Ambient Operating Temperature Range is assuming the device is mounted on a JEDEC standard test board in a convection cooled JEDEC test enclosure.

Note: The “typ” values listed below are not production tested.

Table 14-1. Recommended DC Operating Conditions

($V_{DD3.3} = 3.3V \pm 5\%$, $V_{DD1.8} = 1.8V \pm 5\%$, $T_j = -40^\circ\text{C}$ to $+85^\circ\text{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------------|-------------|------------|-------|-------|-------|-------|
| Logic 1 | V_{IH} | | 2.0 | | 3.465 | V |
| Logic 0 | V_{IL} | | -0.3 | | +0.75 | V |
| Supply ($V_{DD3.3}$) $\pm 5\%$ | $V_{DD3.3}$ | | 3.135 | 3.300 | 3.465 | V |
| Supply ($V_{DD1.8}$) $\pm 5\%$ | $V_{DD1.8}$ | | 1.71 | 1.8 | 1.89 | V |

Table 14-2. DC Electrical Characteristics

($V_{DD3.3} = 3.3V \pm 5\%$, $V_{DD1.8} = 1.8V \pm 5\%$, $T_j = -40^\circ\text{C}$ to $+85^\circ\text{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------|-----------------|------|-----|-----|---------------|
| $V_{DD3.3}$ Supply Current at 3.465V | $I_{DD3.3}$ | (Notes 1, 2, 3) | | 600 | | mA |
| $V_{DD1.8}$ Supply Current at 1.89V | $I_{DD1.8}$ | (Notes 1, 2) | | 30 | | mA |
| Lead Capacitance | C_{IO} | (Note 4) | | 7 | | pF |
| Input Leakage | I_{IL} | | -10 | | +10 | μA |
| Input Leakage | I_{ILP} | | -50 | | -10 | μA |
| Output Leakage (when Hi-Z) | I_{LO} | | -10 | | +10 | μA |
| Output Voltage ($I_{OH} = -1.0\text{mA}$) | V_{OH} | All outputs | 2.35 | | | V |
| Output Voltage ($I_{OL} = +1.0\text{mA}$) | V_{OL} | All outputs | | | 0.4 | V |
| Output Voltage ($I_{OH} = -8.0\text{mA}$) | V_{OH} | REF_CLKO | 2.35 | | | V |
| Output Voltage ($I_{OL} = +12.0\text{mA}$) | V_{OL} | TSERO | | | 0.4 | V |

Note 1: Typical power consumption is approximately 2 Watts.

Note 2: All outputs loaded with rated capacitance; all inputs between V_{DD} and V_{SS} ; inputs with pullups connected to V_{DD} .

Note 3: TCLKT = TCLKE = RCLKI = TSYSCLK = RSYSCLK = MCLK = 1.544MHz; outputs open circuited.

Note 4: Value guaranteed by design (GBD).

14.1 Thermal Characteristics

Table 14-3. Thermal Characteristics

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|-----|-------|------|-------|
| Ambient Temperature (Note 1) | -40 | | +85 | °C |
| Junction Temperature | | | +125 | °C |
| Theta-JA (θ_{JA}) in Still Air for 400-Pin 27mm BGA (Notes 2, 3) | | +15.1 | | °C/W |

Table 14-4. Theta-JA vs. Airflow

| AIR FLOW | THETA-JA 400-PIN 27mm BGA | NOTES |
|----------|------------------------------|-------|
| 0m/s | 15.1°C/W | 3 |
| 1m/s | 13.3°C/W | 3 |
| 2.5m/s | 12.3°C/W | 3 |

Note 1: The package is mounted on a four-layer JEDEC standard test board.

Note 2: Theta-JA (θ_{JA}) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board.

Note 3: Value guaranteed by design (GBD).

14.2 MII Interface

Table 14-5. Transmit MII Interface

(Note 1, [Figure 14-1](#))

| PARAMETER | SYMBOL | 10Mbps | | | 100Mbps | | | UNITS |
|----------------------------|--------|--------|-----|-----|---------|-----|-----|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| TX_CLK Period | t1 | | 400 | | | 40 | | ns |
| TX_CLK Low Time | t2 | 140 | | 260 | 14 | | 26 | ns |
| TX_CLK High Time | t3 | 140 | | 260 | 14 | | 26 | ns |
| TX_CLK to TXD, TX_EN Delay | t4 | 0 | | 20 | 0 | | 20 | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Figure 14-1. Transmit MII Interface Timing

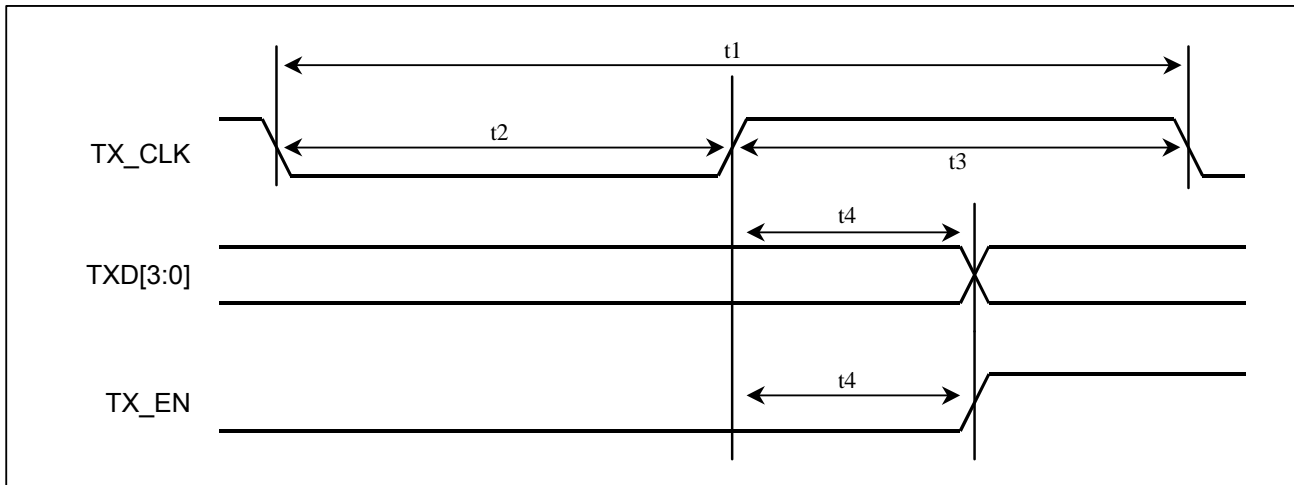
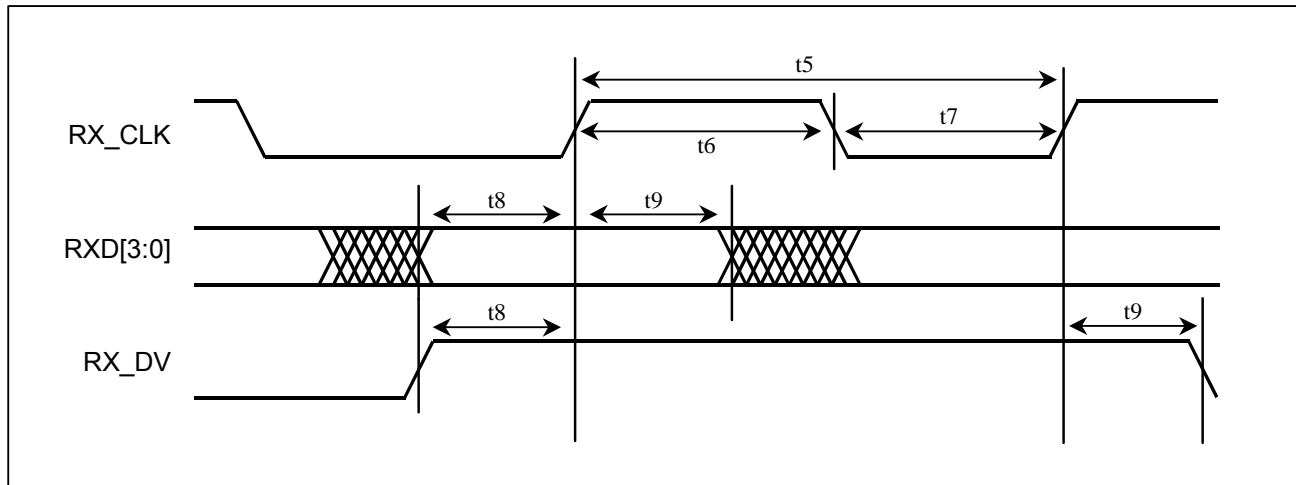


Table 14-6. Receive MII Interface(Note 1, [Figure 14-2](#))

| PARAMETER | SYMBOL | 10Mbps | | | 100Mbps | | | UNITS |
|---------------------------------|--------|--------|-----|-----|---------|-----|-----|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| RX_CLK Period | t5 | | 400 | | | 40 | | ns |
| RX_CLK Low Time | t6 | 140 | | 260 | 14 | | 26 | ns |
| RX_CLK High Time | t7 | 140 | | 260 | 14 | | 26 | ns |
| RXD, RX_DV to RX_CLK Setup Time | t8 | 5 | | | 5 | | | ns |
| RX_CLK to RXD, RX_DV Hold Time | t9 | 5 | | | 5 | | | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Figure 14-2. Receive MII Interface Timing

14.3 RMII Interface

Table 14-7. Transmit RMII Interface

(Note 1, [Figure 14-3](#))

| PARAMETER | SYMBOL | 10Mbps | | | 100Mbps | | | UNITS |
|--------------------------------|--------|--------|-----------------|-----|---------|-----------------|-----|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| REF_CLK Frequency | | | 50MHz ±50ppm | | | 50MHz ±50ppm | | |
| REF_CLK Period | t1 | | 20 | | | 20 | | ns |
| REF_CLK Low Time | t2 | 7 | | 13 | 7 | | 13 | ns |
| REF_CLK High Time | t3 | 7 | | 13 | 7 | | 13 | ns |
| REF_CLK to TXD, TX_EN Delay | t4 | 5 | | 10 | 5 | | 10 | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Figure 14-3. Transmit RMII Interface Timing

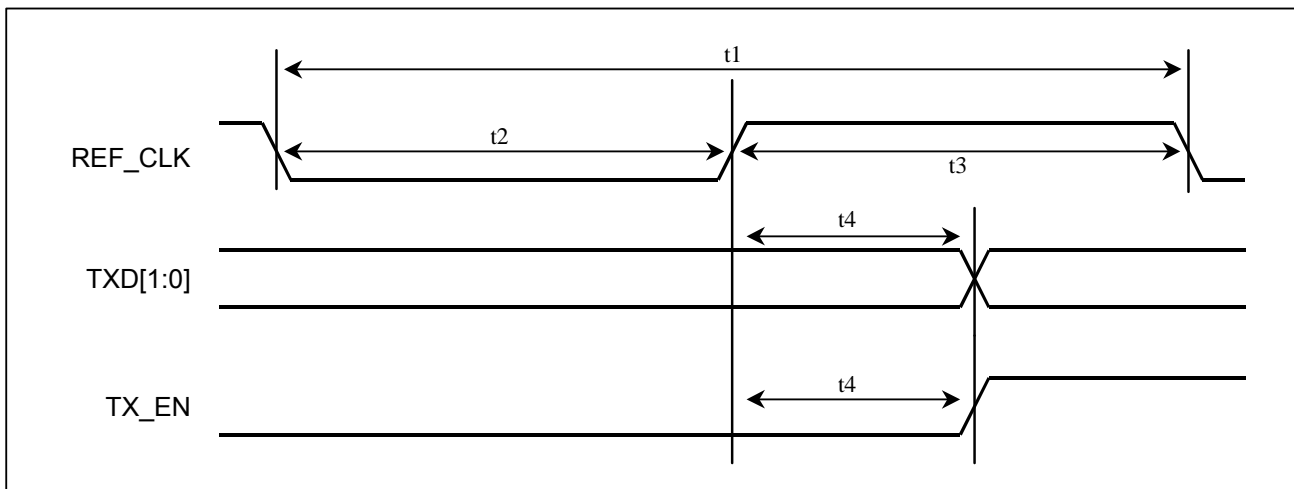


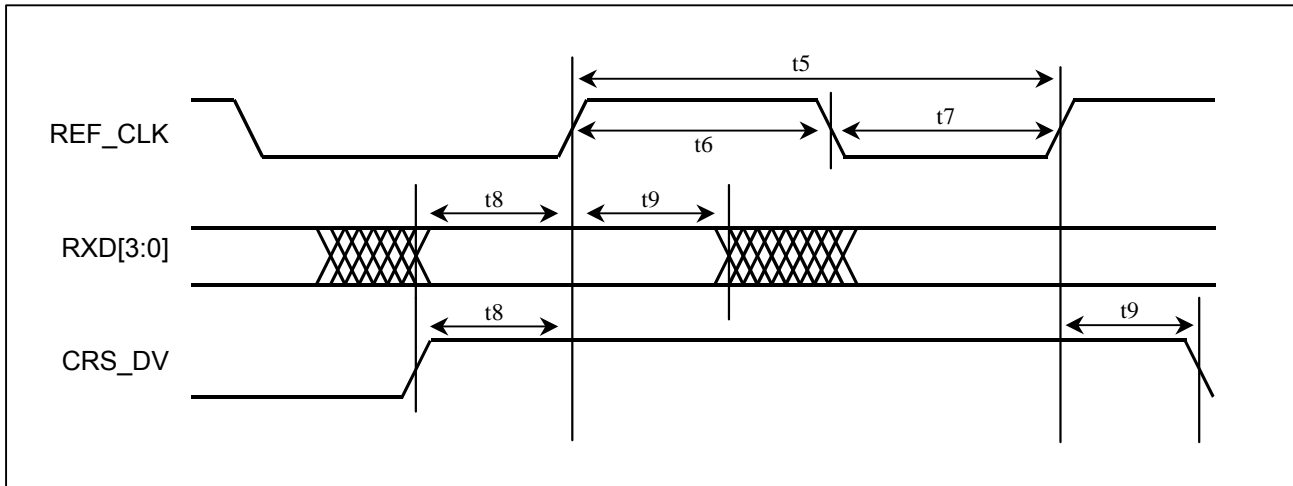
Table 14-8. Receive RMII Interface

(Note 1, [Figure 14-4](#))

| PARAMETER | SYMBOL | 10Mbps | | | 100Mbps | | | UNITS |
|-----------------------------------|--------|--------|-----------------|-----|-----------------|-----|-----|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| REF_CLK Frequency | | | 50MHz ±50ppm | | 50MHz ±50ppm | | MHz | |
| REF_CLK Period | t1 | | 20 | | 20 | | ns | |
| REF_CLK Low Time | t2 | 7 | | 13 | 7 | 13 | ns | |
| REF_CLK High Time | t3 | 7 | | 13 | 7 | 13 | ns | |
| RXD, CRS_DV to REF_CLK Setup Time | t8 | 5 | | | 5 | | ns | |
| REF_CLK to RXD, CRS_DV Hold Time | t9 | 5 | | | 5 | | ns | |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Figure 14-4. Receive RMII Interface Timing



14.4 MDIO Interface

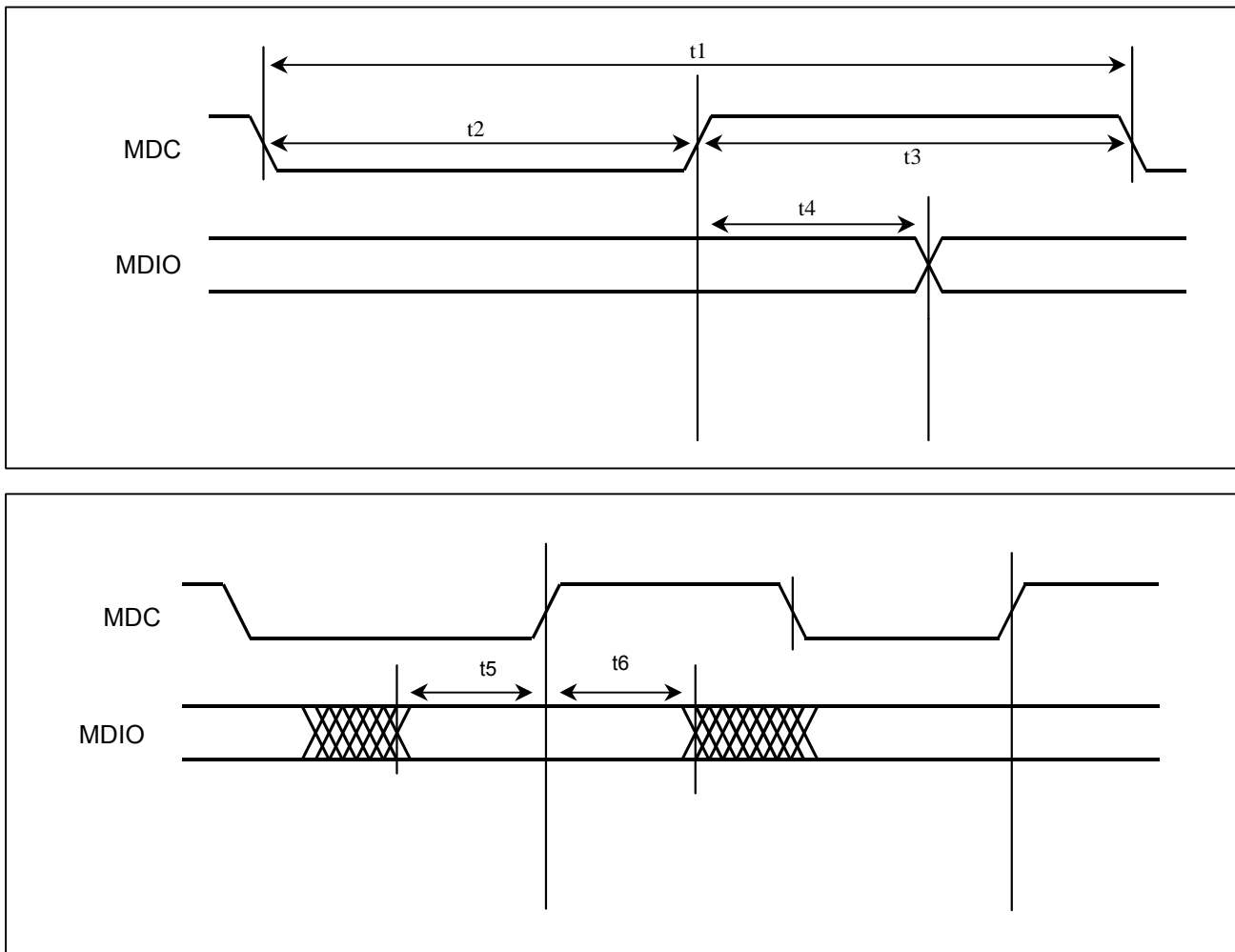
Table 14-9. MDIO Interface

(Note 1, [Figure 14-5](#))

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--------------------------|--------|-----|------|-----|-------|
| MDC Frequency | | | 1.67 | | MHz |
| MDC Period | t1 | 540 | 600 | 660 | ns |
| MDC Low Time | t2 | 270 | 300 | 330 | ns |
| MDC High Time | t3 | 270 | 300 | 330 | ns |
| MDC to MDIO Output Delay | t4 | 20 | | 10 | ns |
| MDIO Setup Time | t5 | 10 | | | ns |
| MDIO Hold Time | t6 | 20 | | | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Figure 14-5. MDIO Interface Timing



14.5 Transmit WAN Interface

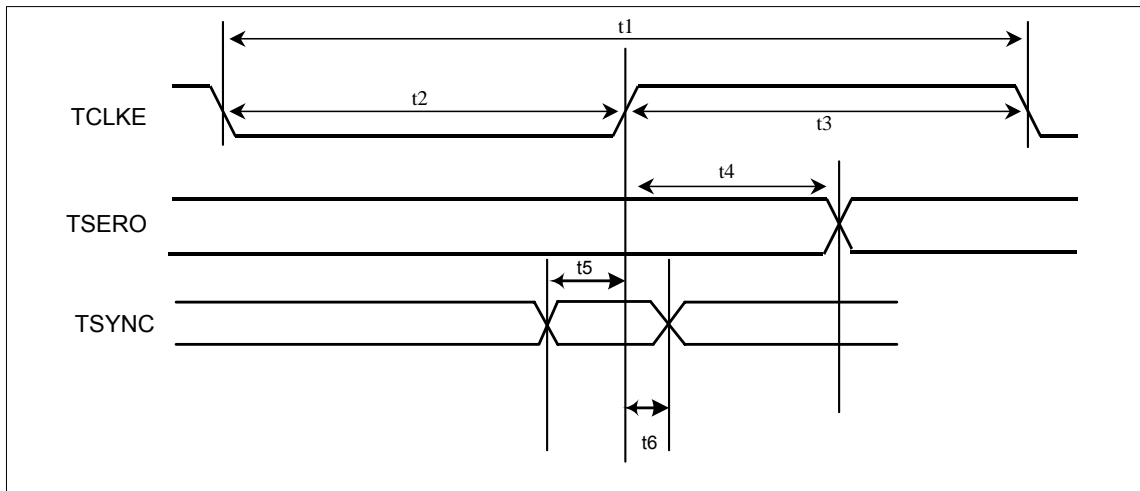
Table 14-10. Transmit WAN Interface

(Note 1, [Figure 14-6](#))

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|-----------------------------|--------|------|-----|-----|-------|
| TCLKE Frequency | | | | 52 | MHz |
| TCLKE Period | t1 | 19.2 | | | ns |
| TCLKE Low Time | t2 | 8 | | | ns |
| TCLKE High Time | t3 | 8 | | | ns |
| TCLKE to TSERO Output Delay | t4 | 3 | | 10 | ns |
| TSYNC Setup Time | t5 | 3.5 | | | ns |
| TSYNC Hold Time | t6 | 7 | | | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Figure 14-6. Transmit WAN Timing



14.6 Receive WAN Interface

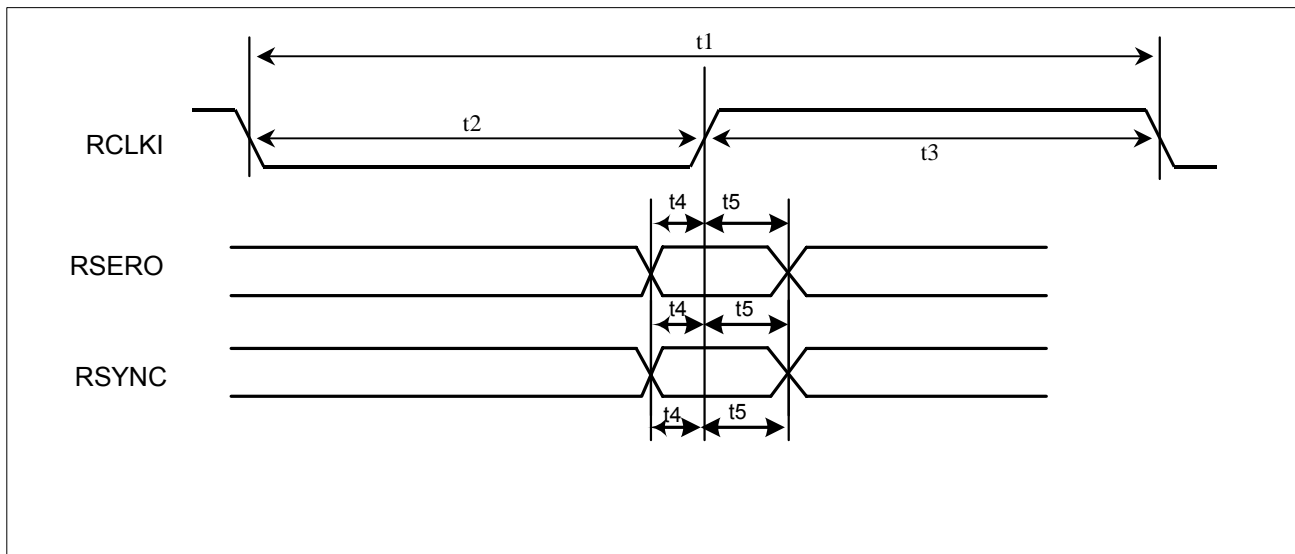
Table 14-11. Receive WAN Interface

(Note 1, [Figure 14-7](#))

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|------------------|--------|------|-----|-----|-------|
| RCLKI Frequency | | | | 52 | MHz |
| RCLKI Period | t1 | 19.2 | | | ns |
| RCLKI Low Time | t2 | 8 | | | ns |
| RCLKI High Time | t3 | 8 | | | ns |
| RSERO Setup time | t4 | 7 | | | ns |
| RSYNC Setup Time | t4 | 7 | | | ns |
| RSERO Hold Time | t5 | 2 | | | ns |
| RSYNC Hold Time | t5 | 2 | | | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Figure 14-7. Receive WAN Timing



14.7 SDRAM Interface

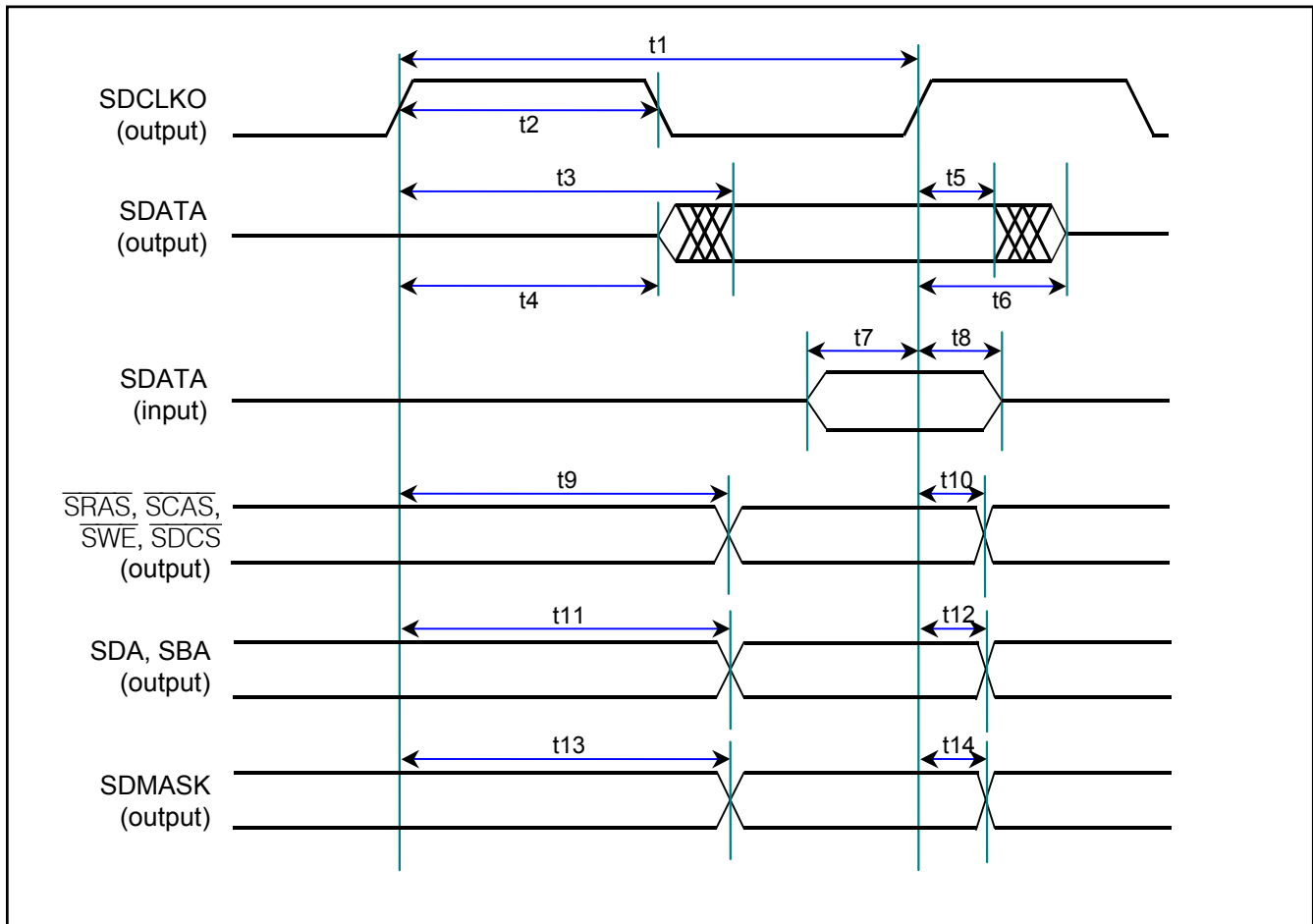
Table 14-12. SDRAM Interface

(Note 1, [Figure 14-8](#))

| PARAMETER | SYMBOL | 100MHz | | | UNITS |
|--|--------|--------|-----|------|-------|
| | | MIN | TYP | MAX | |
| SDCLKO Period | t1 | 9.7 | 10 | 10.3 | ns |
| SDCLKO Duty Cycle | t2 | 4 | | 6 | ns |
| SDCLKO to SDATA Valid Write to SDRAM | t3 | | | 7 | ns |
| SDCLKO to SDATA Drive On Write to SDRAM | t4 | 4 | | | ns |
| SDCLKO to SDATA Invalid Write to SDRAM | t5 | 3 | | | ns |
| SDCLKO to SDATA Drive Off Write to SDRAM | t6 | | | 4 | ns |
| SDATA to SDCLKO Setup Time Read from SDRAM | t7 | 2 | | | ns |
| SDCLKO to SDATA Hold Time Read from SDRAM | t8 | | | 2 | ns |
| SDCLKO to \overline{SRAS} , \overline{SCAS} , \overline{SWE} , \overline{SDCS} Active Read or Write to SDRAM | t9 | | | 5 | ns |
| SDCLKO TO \overline{SRAS} , \overline{SCAS} , \overline{SWE} , \overline{SDCS} Inactive Read or Write to SDRAM | t10 | 2 | | | ns |
| SDCLKO to SDA, SBA Valid Read or Write to SDRAM | t11 | | | 7 | ns |
| SDCLKO to SDA, SBA Invalid Read or Write to SDRAM | t12 | 2 | | | ns |
| SDCLKO to SDMASK Valid Read or Write to SDRAM | t13 | | | 5 | ns |
| SDCLKO TO SDMASK Invalid Read or Write to SDRAM | t14 | 2 | | | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Figure 14-8. SDRAM Interface Timing



14.8 AC Characteristics—Microprocessor Bus

Table 14-13. AC Characteristics—Microprocessor Bus

($V_{DD3.3} = 3.3V \pm 5\%$, $V_{DD1.8} = 1.8V \pm 5\%$, $T_j = -40^\circ\text{C}$ to $+85^\circ\text{C}$.) ([Figure 14-9](#), [Figure 14-10](#), [Figure 14-11](#), and [Figure 14-12](#).)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|--|--------|-----|-----|-----|-------|
| Set-Up Time for A[12:0] Valid to $\overline{\text{CS}}$ / $\overline{\text{CST}}$ Active | t1 | 0 | | | ns |
| Set-Up Time for $\overline{\text{CS}}$ / $\overline{\text{CST}}$ Active to either $\overline{\text{RD}}$, or $\overline{\text{WR}}$ Active | t2 | 0 | | | ns |
| Delay Time from Either $\overline{\text{RD}}$ or $\overline{\text{DS}}$ Active to DATA[7:0] Valid | t3 | | | 75 | ns |
| Hold Time from Either $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Inactive to $\overline{\text{CS}}$ / $\overline{\text{CST}}$ Inactive | t4 | 0 | | | ns |
| Hold Time from $\overline{\text{CS}}$, $\overline{\text{CST}}$, $\overline{\text{RD}}$, or $\overline{\text{DS}}$ Inactive to DATA[7:0] Tri-State | t5 | 5 | | 20 | ns |
| Wait Time from $\overline{\text{RW}}$ Active to Latch Data | t6 | 80 | | | ns |
| Data Set-Up Time to $\overline{\text{DS}}$ Active | t7 | 10 | | | ns |
| Data Hold Time from $\overline{\text{RW}}$ Inactive | t8 | 2 | | | ns |
| Address Hold from $\overline{\text{RW}}$ Inactive | t9 | 0 | | | ns |
| Write Access to Subsequent Write/Read Access Delay Time | t10 | 80 | | | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Figure 14-9. Intel Bus Read Timing (MODEC = 00)

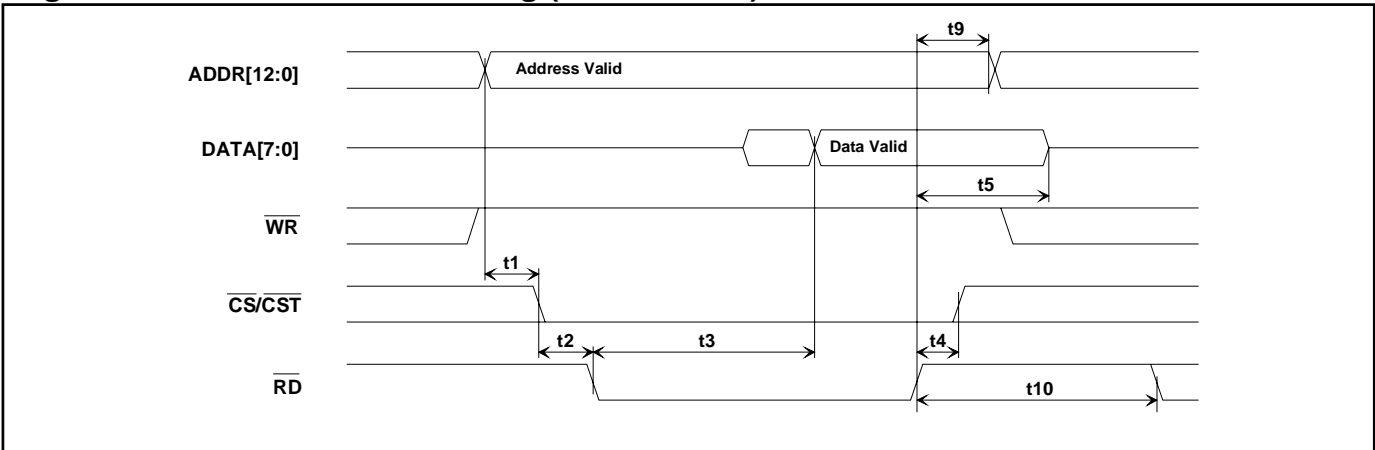


Figure 14-10. Intel Bus Write Timing (MODEC = 00)

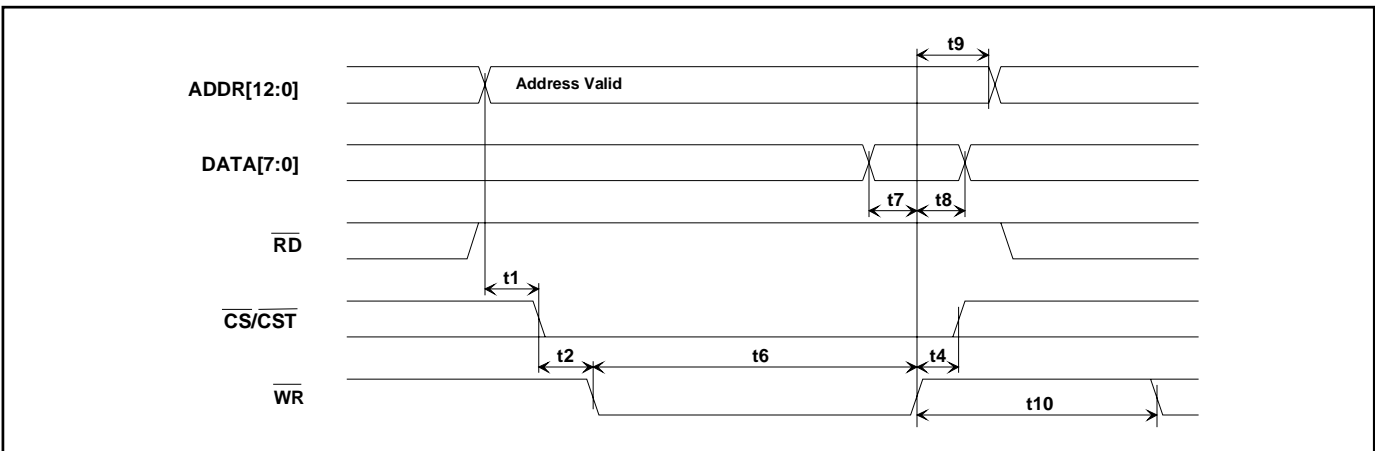


Figure 14-11. Motorola Bus Read Timing (MODEC = 01)

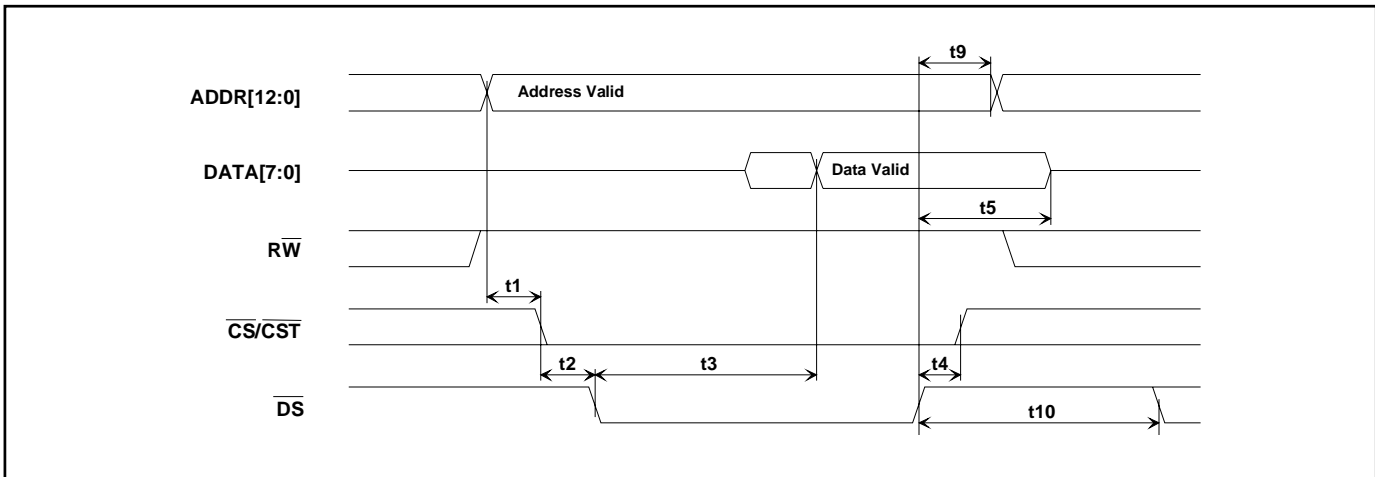
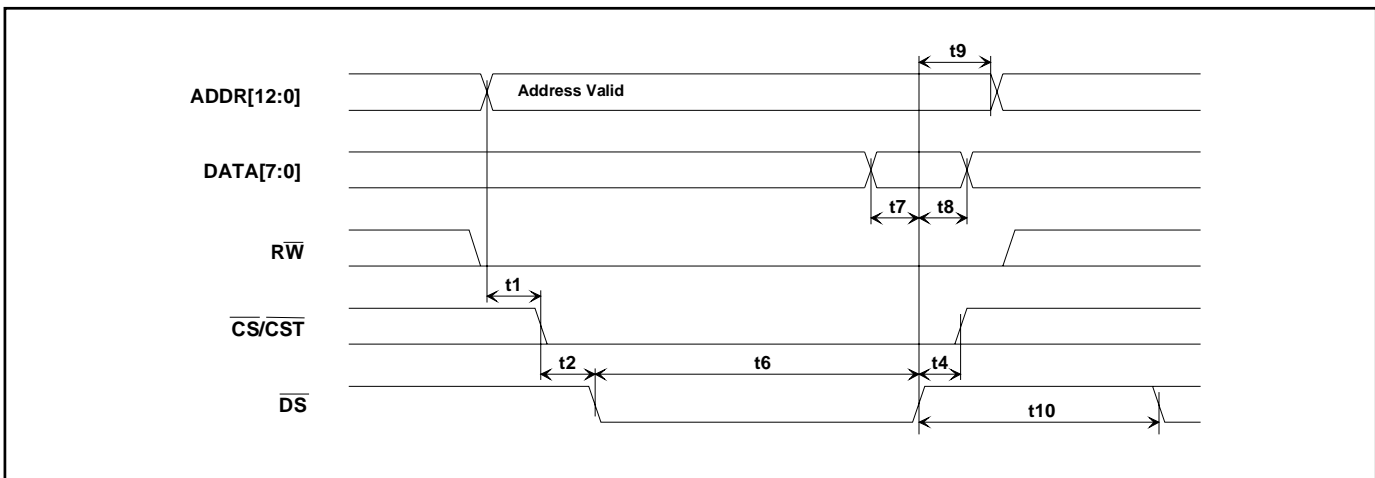


Figure 14-12. Motorola Bus Write Timing (MODEC = 01)



14.9 JTAG Interface Timing

Table 14-14. JTAG Interface

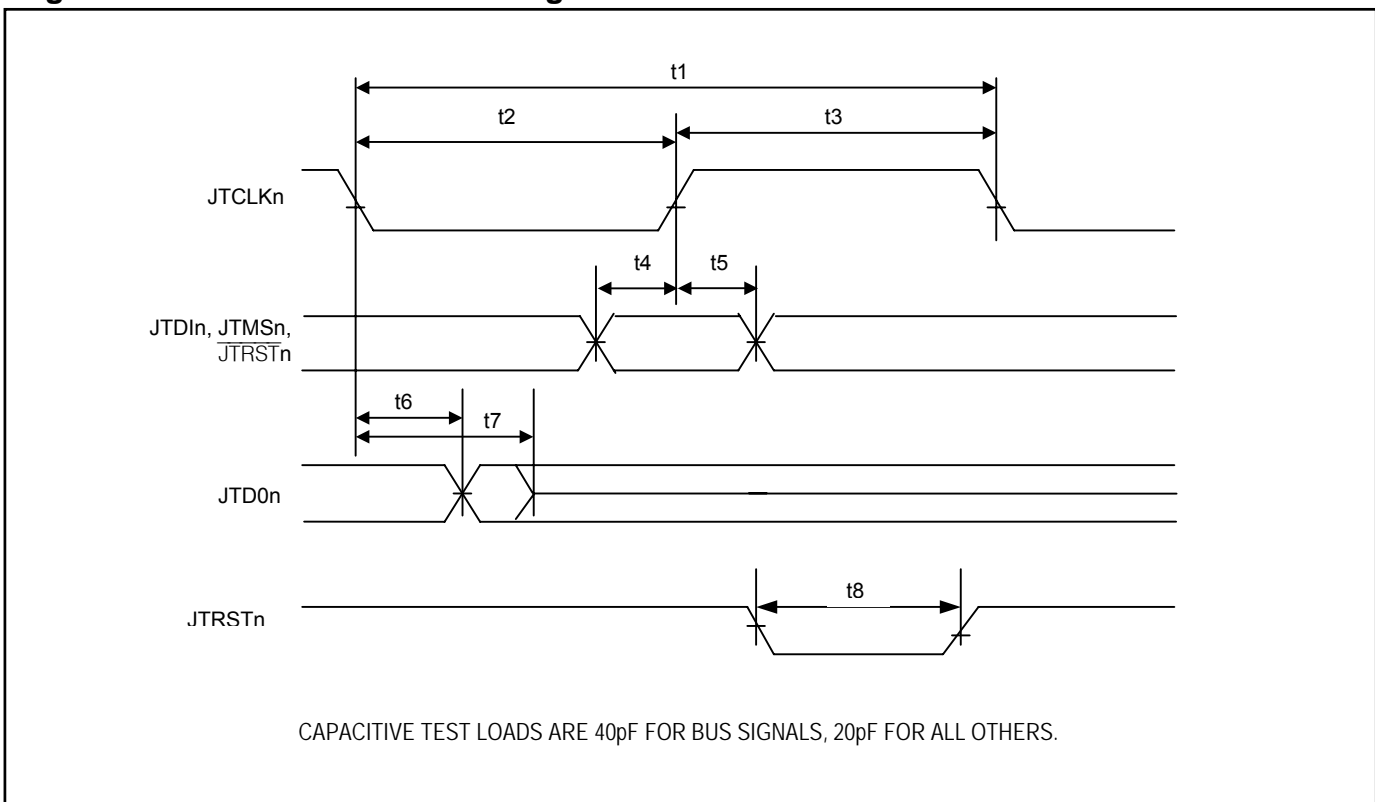
($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.) (Figure 14-13)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------|--------------|-----|------|-----|-------|
| JTCLKn Clock Period | t1 | (Note 1) | | 1000 | | ns |
| JTCLKn Clock High:Low Time | t2:t3 | (Notes 1, 2) | 50 | 500 | | ns |
| JTCLKn to JTDIn, JTMSn Setup Time | t4 | (Note 1) | 2 | | | ns |
| JTCLKn to JTDIn, JTMSn Hold Time | t5 | (Note 1) | 2 | | | ns |
| JTCLKn to JTDOn Delay | t6 | (Note 1) | 2 | | 50 | ns |
| JTCLKn to JTDOn HIZ Delay | t7 | (Note 1) | 2 | | 50 | ns |
| $\overline{\text{JTRSTn}}$ Width Low Time | t8 | (Note 1) | 100 | | | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Note 2: Clock can be stopped high or low.

Figure 14-13. JTAG Interface Timing



14.10 AC Characteristics—Receive Side

Table 14-15. AC Characteristics—Receive Side

($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.) (Note 1) ([Figure 14-14](#) to [Figure 14-18](#))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|------------|-----|--------------|-----|-------|
| RCLKn Period | t_{LP} | | | 488 (E1) | | ns |
| | | | | 648 (T1) | | ns |
| RCLKn Pulse Width | t_{LH} | (Note 2) | 200 | $0.5 t_{LP}$ | | ns |
| | t_{LL} | (Note 2) | 200 | $0.5 t_{LP}$ | | ns |
| RCLKn Pulse Width | t_{LH} | (Note 3) | 150 | $0.5 t_{LP}$ | | ns |
| | t_{LL} | (Note 3) | 150 | $0.5 t_{LP}$ | | ns |
| RCLKI Period | t_{CP} | | | 488 (E1) | | ns |
| | | | | 648 (T1) | | |
| RCLKI Pulse Width | t_{CH} | | 20 | $0.5 t_{CP}$ | | ns |
| | t_{CL} | | 20 | $0.5 t_{CP}$ | | |
| RSYSCLK Period | t_{SP} | (Note 4) | | 648 | | ns |
| | | (Note 5) | | 488 | | ns |
| | | (Note 6) | | 244 | | |
| | | (Note 7) | | 122 | | |
| | | (Note 8) | | 61 | | |
| RSYSCLK Pulse Width | t_{SH} | | 20 | $0.5 t_{SP}$ | | ns |
| | t_{SL} | | 20 | $0.5 t_{SP}$ | | |
| RSYNC Setup to RSYSCLK Falling | t_{SU} | | 20 | | | ns |
| RSYNC Pulse Width | t_{PW} | | 50 | | | ns |
| RPOSI/RNEGI Setup to RCLKI Falling | t_{SU} | | 20 | | | ns |
| RPOSI/RNEGI Hold from RCLKI Falling | t_{HD} | | 20 | | | ns |
| RSYSCLK, RCLKI Rise and Fall Times | t_R, t_F | | | | 22 | ns |
| Delay RCLKn to RPOSO, RNEGO Valid | t_{DD} | | | | 50 | ns |
| Delay RCLKn to RSERO, RDATA, RSIG Valid | t_{D1} | | | | 50 | ns |
| Delay RCLKn to RCHCLK, RSYNC, RCHBLK, RFSYNC | t_{D2} | | | | 50 | ns |
| Delay RSYSCLK to RSERO, RSIG Valid | t_{D3} | | | | 22 | ns |
| Delay RSYSCLK to RCHCLK, CHBLK, RMSYNC, RSYNC | t_{D4} | | | | 22 | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

Note 2: Jitter attenuator enabled in the receive path.

Note 3: Jitter attenuator disabled or enabled in the transmit path.

Note 4: RSYSCLK = 1.544MHz.

Note 5: RSYSCLK = 2.048MHz.

Note 6: RSYSCLK = 4.096MHz.

Note 7: RSYSCLK = 8.192MHz.

Note 8: RSYSCLK = 16.384MHz.

Figure 14-14. Receive Side Timing, Elastic Store Disabled (T1 Mode)

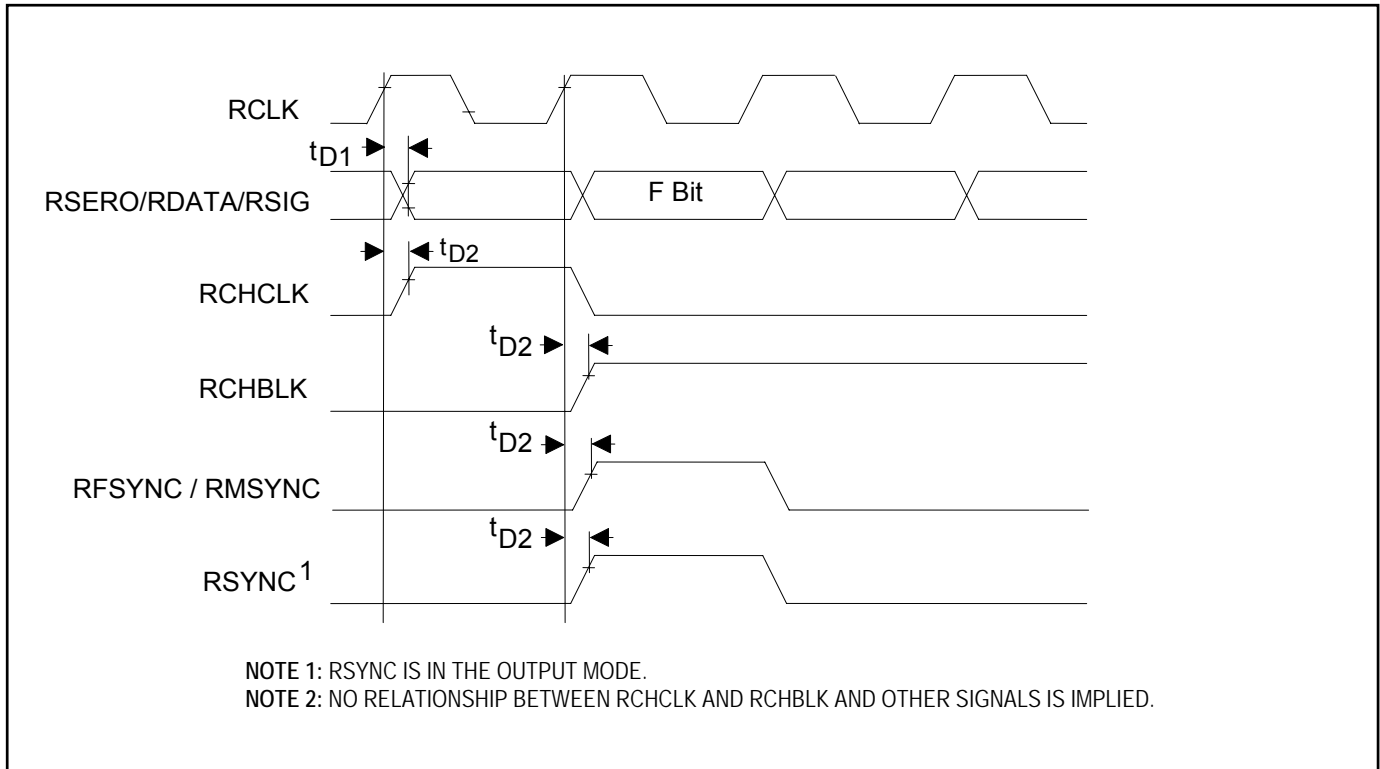


Figure 14-15. Receive Side Timing, Elastic Store Disabled (E1 Mode)

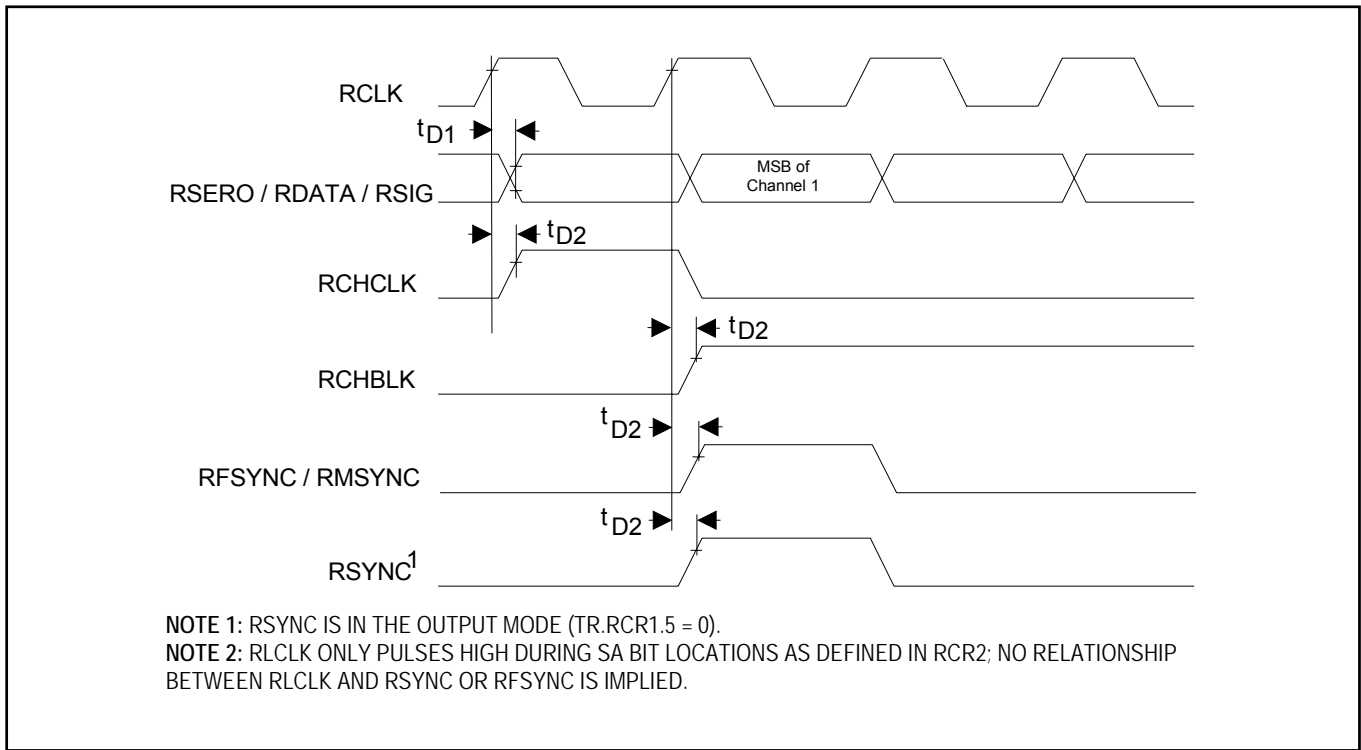
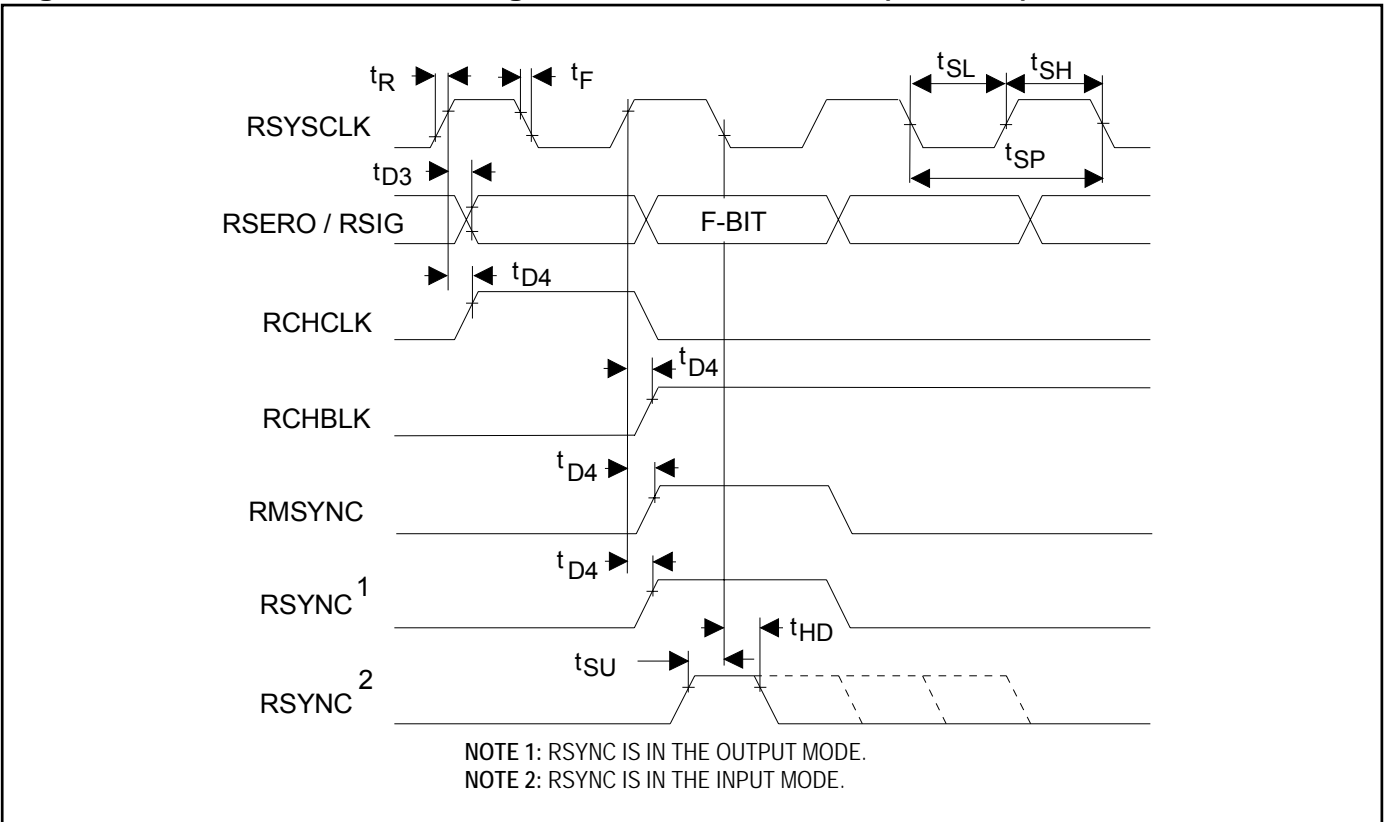


Figure 14-16. Receive Side Timing, Elastic Store Enabled (T1 Mode)



14.11 AC Characteristics—Transmit Side

Table 14-16. AC Characteristics—Transmit Side

($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.) (Note 1) ([Figure 14-19](#) to [Figure 14-21](#))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP (E1) | MAX | UNITS |
|---|------------|------------|-----|--------------|-----|-------|
| TCLKT Period | t_{CP} | | | 488 (E1) | | ns |
| | | | | 648 (T1) | | |
| TCLKT Pulse Width | t_{CH} | | 20 | $0.5 t_{CP}$ | | ns |
| | t_{CL} | | 20 | $0.5 t_{CP}$ | | ns |
| TDCLKI Period | t_{LP} | | | 488 (E1) | | ns |
| | | | | 648 (T1) | | |
| TDCLKI Pulse Width | t_{LH} | | 20 | $0.5 t_{LP}$ | | ns |
| | t_{LL} | | 20 | $0.5 t_{LP}$ | | ns |
| TSYSCLK Period | t_{SP} | (Note 2) | | 648 | | ns |
| | | (Note 3) | | 448 | | ns |
| | | (Note 4) | | 244 | | ns |
| | | (Note 5) | | 122 | | ns |
| | | (Note 6) | | 61 | | ns |
| TSYSCLK Pulse Width | t_{SP} | | 20 | $0.5 t_{SP}$ | | ns |
| | | | 20 | $0.5 t_{SP}$ | | ns |
| TSYNC or TSSYNC Setup to TCLKT or TSYSCLK Falling | t_{SU} | | 20 | | | ns |
| TSYNC or TSSYNC Pulse Width | t_{PW} | | 50 | | | ns |
| TSERI, TSIG, TPOSI, TNEGI Setup to TCLKT, TSYSCLK, TDCLKI Falling | t_{SU} | | 20 | | | ns |
| TSERI, TSIG, Hold from TCLKT or TSYSCLK Falling | t_{HD} | | 20 | | | ns |
| TPOSI, TNEGI Hold from TDCLKI Falling | t_{HD} | | 20 | | | ns |
| TCLKT, TDCLKI, or TSYSCLK Rise and Fall Times | t_R, t_F | | | | 25 | ns |
| Delay TDCLKO to TPOSO, TNEGO Valid | t_{DD} | | | | 50 | ns |
| Delay TCLKT to TCHBLK, TCHCLK, TSYNC | t_{D2} | | | | 50 | ns |
| Delay TSYSCLK to TCHCLK, TCHBLK | t_{D3} | | | | 22 | ns |

Note 1: Timing parameters in this table are guaranteed by design (GBD).

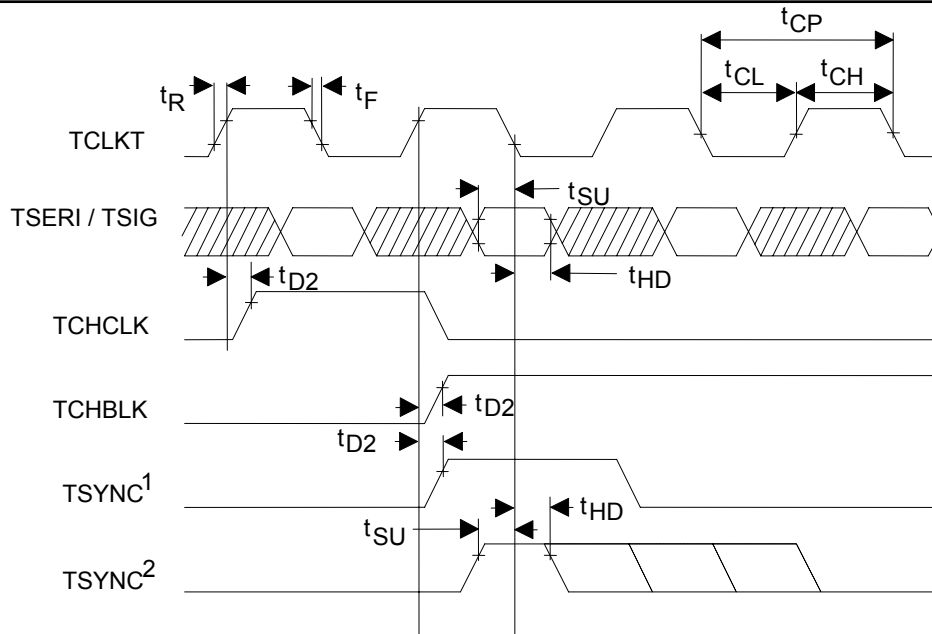
Note 2: TSYSCLK = 1.544MHz.

Note 3: TSYSCLK = 2.048MHz.

Note 4: TSYSCLK = 4.096MHz.

Note 5: TSYSCLK = 8.192MHz.

Note 6: TSYSCLK = 16.384MHz.

Figure 14-19. Transmit Side Timing, Elastic Store Disabled

NOTE 1: TSYNC IS IN THE OUTPUT MODE (TR.TCR2.2 = 1).

NOTE 2: TSYNC IS IN THE INPUT MODE (TR.TCR2.2 = 0).

NOTE 3: TSERI IS SAMPLED ON THE FALLING EDGE OF TCLK WHEN THE TRANSMIT-SIDE ELASTIC STORE IS DISABLED.

NOTE 4: TCHCLK AND TCHBLK ARE SYNCHRONOUS WITH TCLK WHEN THE TRANSMIT-SIDE ELASTIC STORE IS DISABLED.

NOTE 5: NO RELATIONSHIP BETWEEN TCHCLK AND TCHBLK AND THE OTHER SIGNALS IS IMPLIED.

NOTE 6: THIS TIMING DIAGRAM IS INCLUDED FOR SPECIAL APPLICATIONS ONLY. IN MOST APPLICATIONS OF THE DS33R41, THE USER SHOULD REFER TO [Figure 14-20](#).

Figure 14-20. Transmit Side Timing, Elastic Store Enabled

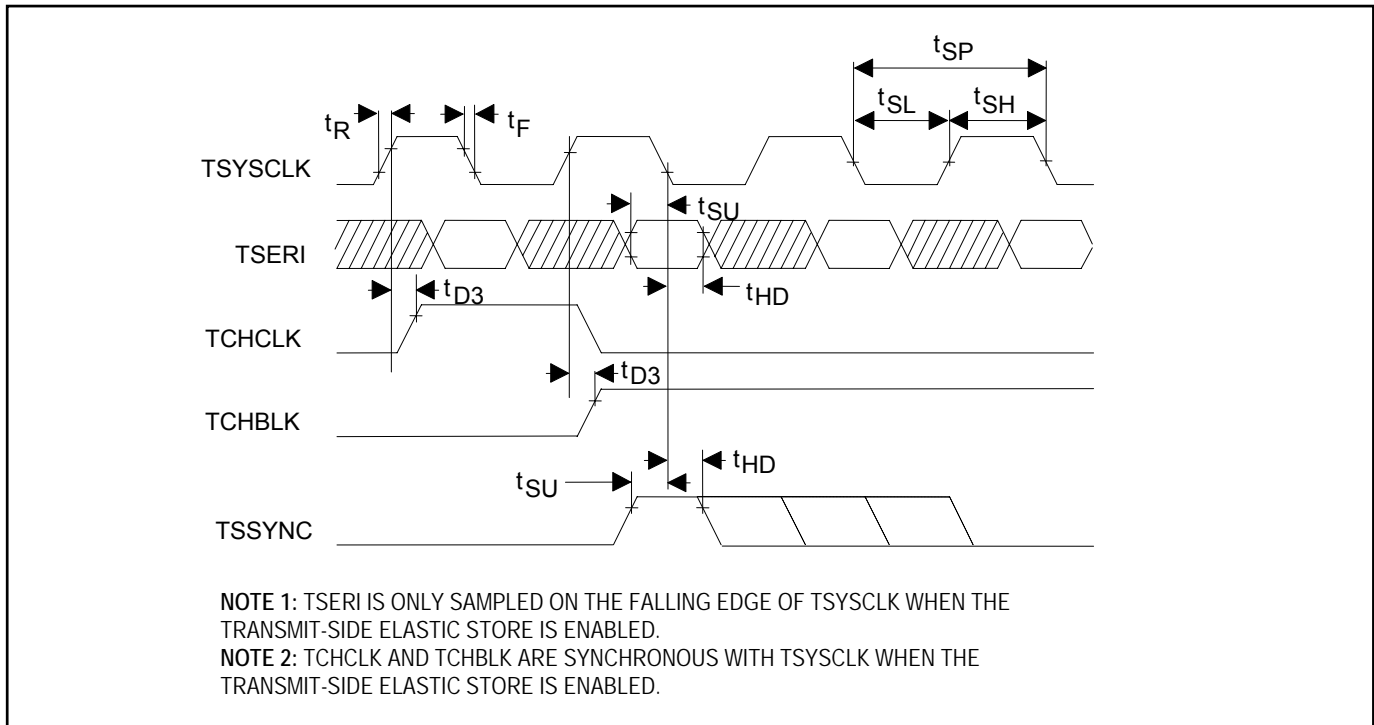
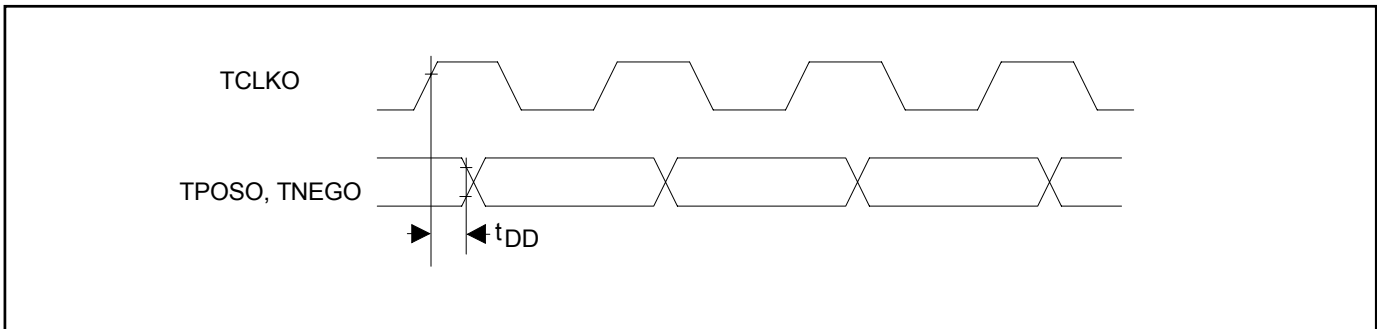


Figure 14-21. Transmit Line Interface Timing



15 JTAG INFORMATION

This device contains dual JTAG controllers and requires special consideration during JTAG test design. For more information on performing JTAG testing using this device, go to www.maxim-ic.com/support.

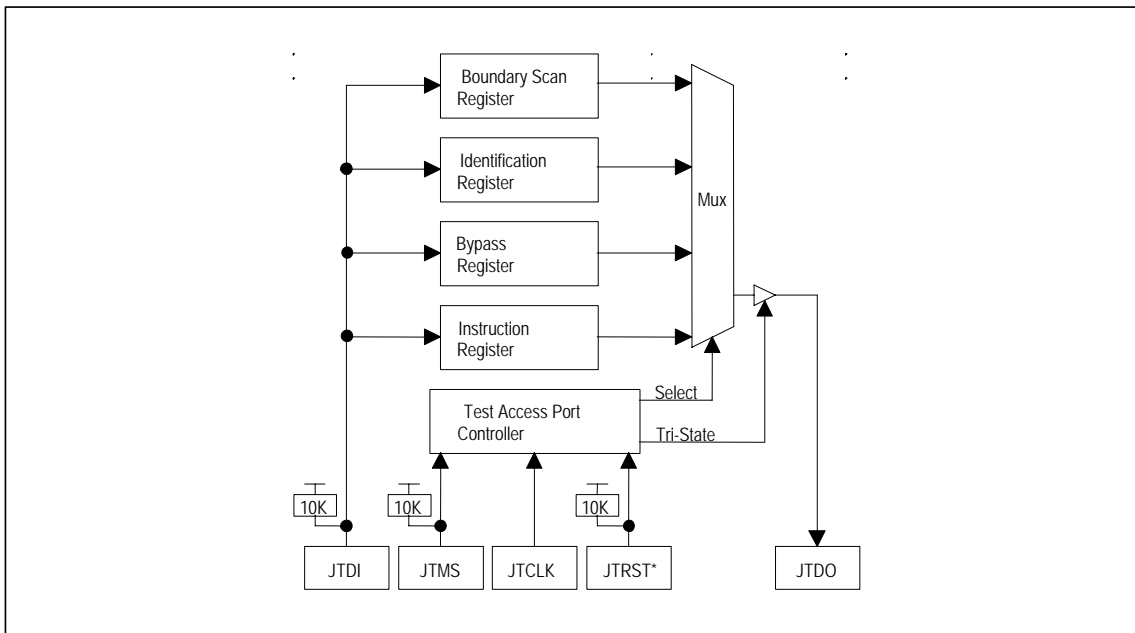
The device supports the standard instruction codes SAMPLE:PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. See [Table 15-1](#). The device contains the following as required by IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

Test Access Port (TAP)
TAP Controller
Instruction Register

Bypass Register
Boundary Scan Register
Device Identification Register

The Test Access Port has the necessary interface pins: $\overline{\text{JTRST}}_n$, JTCLK_n, JTMS_n, JTDI_n, and JTDO_n. See the pin descriptions for details. Refer to IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994 for details about the Boundary Scan Architecture and the Test Access Port.

Figure 15-1. JTAG Functional Block Diagram



15.1 JTAG TAP Controller State Machine Description

This section covers the details on the operation of the Test Access Port (TAP) Controller State Machine. The TAP controller is a finite state machine that responds to the logic level at JTMSn on the rising edge of JTCLKn.

15.2 TAP Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at JTMSn on the rising edge of JTCLKn. See [Figure 15-2](#) for a diagram of the state machine operation.

15.2.1 Test-Logic-Reset

Upon power up, the TAP Controller is in the Test-Logic-Reset state. The Instruction register will contain the IDCODE instruction. All system logic of the device will operate normally.

15.2.2 Run-Test-Idle

The Run-Test-Idle is used between scan operations or during specific tests. The Instruction register and test registers will remain idle.

15.2.3 Select-DR-Scan

All test registers retain their previous state. With JTMSn LOW, a rising edge of JTCLKn moves the controller into the Capture-DR state and will initiate a scan sequence. JTMSn HIGH during a rising edge on JTCLKn moves the controller to the Select-IR-Scan state.

15.2.4 Capture-DR

Data may be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register will remain at its current value. On the rising edge of JTCLKn, the controller will go to the Shift-DR state if JTMSn is LOW or it will go to the Exit1-DR state if JTMSn is HIGH.

15.2.5 Shift-DR

The test data register selected by the current instruction is connected between JTDIn and JTDOn and will shift data one stage towards its serial output on each rising edge of JTCLKn. If a test register selected by the current instruction is not placed in the serial path, it will maintain its previous state.

15.2.6 Exit1-DR

While in this state, a rising edge on JTCLKn will put the controller in the Update-DR state, which terminates the scanning process, if JTMSn is HIGH. A rising edge on JTCLKn with JTMSn LOW will put the controller in the Pause-DR state.

15.2.7 Pause-DR

Shifting of the test registers is halted while in this state. All test registers selected by the current instruction will retain their previous state. The controller will remain in this state while JTMSn is LOW. A rising edge on JTCLKn with JTMSn HIGH will put the controller in the Exit2-DR state.

15.2.8 Exit2-DR

A rising edge on JTCLKn with JTMSn HIGH while in this state will put the controller in the Update-DR state and terminate the scanning process. A rising edge on JTCLKn with JTMSn LOW will enter the Shift-DR state.

15.2.9 Update-DR

A falling edge on JTCLKn while in the Update-DR state will latch the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register.

15.2.10 Select-IR-Scan

All test registers retain their previous state. The instruction register will remain unchanged during this state. With JTMSn LOW, a rising edge on JTCLKn moves the controller into the Capture-IR state and will initiate a scan sequence for the instruction register. JTMSn HIGH during a rising edge on JTCLKn puts the controller back into the Test-Logic-Reset state.

15.2.11 Capture-IR

The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLKn. If JTMSn is HIGH on the rising edge of JTCLKn, the controller will enter the Exit1-IR state. If JTMSn is LOW on the rising edge of JTCLKn, the controller will enter the Shift-IR state.

15.2.12 Shift-IR

In this state, the shift register in the instruction register is connected between JTDIn and JTDOn and shifts data one stage for every rising edge of JTCLKn towards the serial output. The parallel register, as well as all test registers, remains at their previous states. A rising edge on JTCLKn with JTMSn HIGH will move the controller to the Exit1-IR state. A rising edge on JTCLKn with JTMSn LOW will keep the controller in the Shift-IR state while moving data one stage through the instruction shift register.

15.2.13 Exit1-IR

A rising edge on JTCLKn with JTMSn LOW will put the controller in the Pause-IR state. If JTMSn is HIGH on the rising edge of JTCLKn, the controller will enter the Update-IR state and terminate the scanning process.

15.2.14 Pause-IR

Shifting of the instruction shift register is halted temporarily. With JTMSn HIGH, a rising edge on JTCLKn will put the controller in the Exit2-IR state. The controller will remain in the Pause-IR state if JTMSn is LOW during a rising edge on JTCLKn.

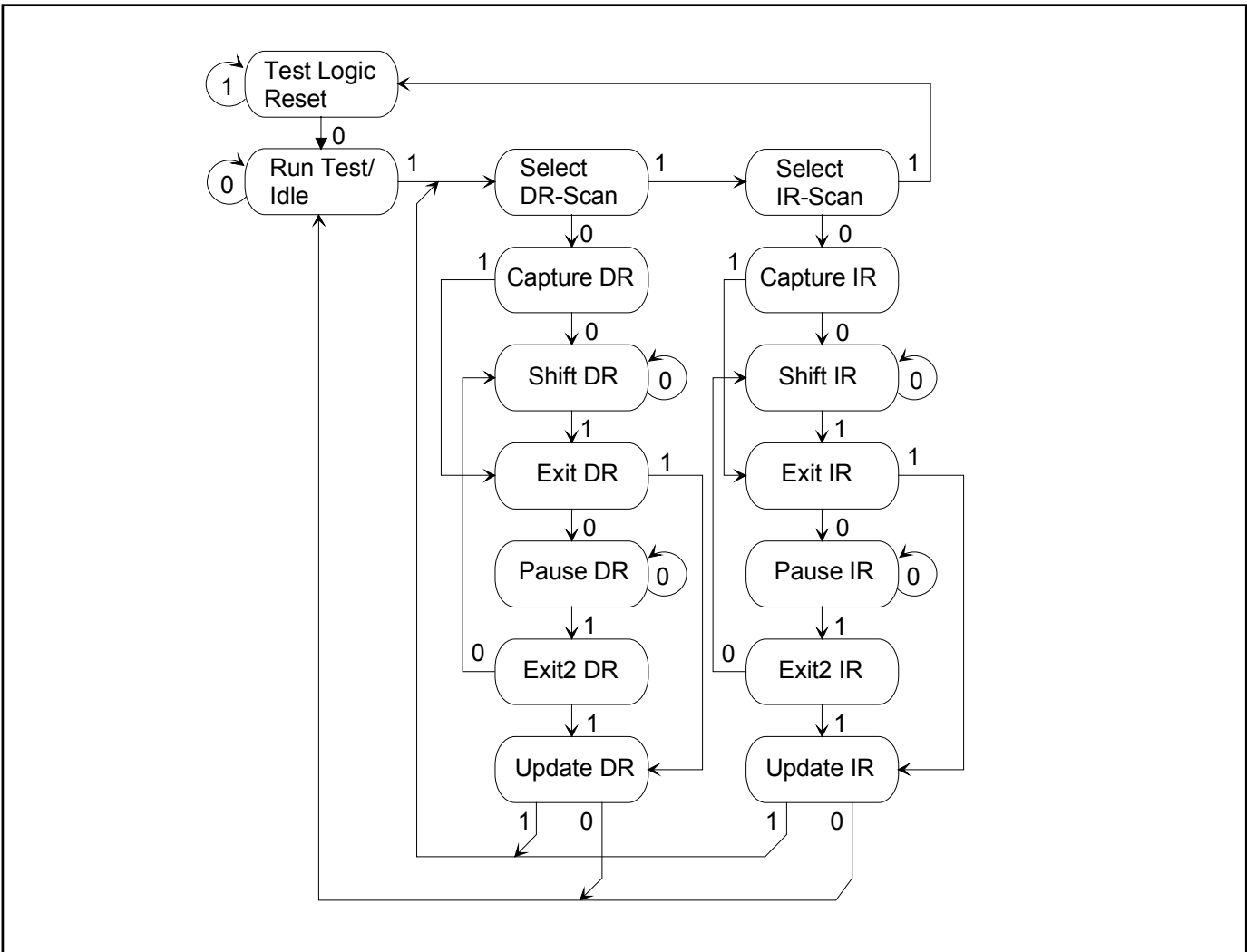
15.2.15 Exit2-IR

A rising edge on JTCLKn with JTMSn LOW will put the controller in the Update-IR state. The controller will loop back to Shift-IR if JTMSn is HIGH during a rising edge of JTCLKn in this state.

15.2.16 Update-IR

The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLKn as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLKn with JTMSn held low will put the controller in the Run-Test-Idle state. With JTMSn HIGH, the controller will enter the Select-DR-Scan state.

Figure 15-2. TAP Controller State Diagram



15.3 Instruction Register

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDIn and JTDO_n. While in the Shift-IR state, a rising edge on JTCLK_n with JTMS_n LOW will shift the data one stage towards the serial output at JTDO_n. A rising edge on JTCLK_n in the Exit1-IR state or the Exit2-IR state with JTMS_n HIGH will move the controller to the Update-IR state. The falling edge of that same JTCLK_n will latch the data in the instruction shift register to the instruction parallel output. Instructions supported by the device and its respective operational binary codes are shown in [Table 15-1](#).

Table 15-1. Instruction Codes for IEEE 1149.1 Architecture

| INSTRUCTION | SELECTED REGISTER | INSTRUCTION CODES |
|----------------|-----------------------|-------------------|
| SAMPLE:PRELOAD | Boundary Scan | 010 |
| BYPASS | Bypass | 111 |
| EXTEST | Boundary Scan | 000 |
| CLAMP | Bypass | 011 |
| HIGHZ | Bypass | 100 |
| IDCODE | Device Identification | 001 |

15.3.1 SAMPLE:PRELOAD

This is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE:PRELOAD also allows the device to shift data into the boundary scan register via JTDIn using the Shift-DR state.

15.3.2 BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDIn connects to JTDO_n through the one-bit bypass test register. This allows data to pass from JTDIn to JTDO_n not affecting the device's normal operation.

15.3.3 EXTEST

This allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins are driven. The boundary scan register is connected between JTDIn and JTDO_n. The Capture-DR will sample all digital inputs into the boundary scan register.

15.3.4 CLAMP

All digital outputs of the device will output data from the boundary scan parallel output while connecting the bypass register between JTDIn and JTDO_n. The outputs will not change during the CLAMP instruction.

15.3.5 HIGHZ

All digital outputs of the device are placed in a high-impedance state. The BYPASS register is connected between JTDIn and JTDO_n.

15.3.6 IDCODE

When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code is loaded into the identification register on the rising edge of JTCLK_n following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO_n. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The ID code will always have a '1' in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version.

15.4 JTAG ID Codes

Table 15-2. ID Code Structure

| DEVICE | REVISION ID[31:28] | DEVICE CODE ID[27:12] | MANUFACTURER'S CODE ID[11:1] | REQUIRED ID[0] |
|-------------------------|-----------------------|--------------------------|---------------------------------|-------------------|
| Ethernet Mapper | 0000 | 0000 0000 0110 0010 | 000 1010 0001 | 1 |
| T1/E1/J1 Transceiver | 0000 | 0000 0000 0010 0010 | 000 1010 0001 | 1 |

15.5 Test Registers

IEEE 1149.1 requires a minimum of two test registers: the bypass register and the boundary scan register. An optional test register has been included with the DS33R41 design. This test register is the identification register and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

15.5.1 Boundary Scan Register

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is n bits in length.

15.5.2 Bypass Register

This is a single one-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions, which provides a short path between JTDIn and JTDO_n.

15.5.3 Identification Register

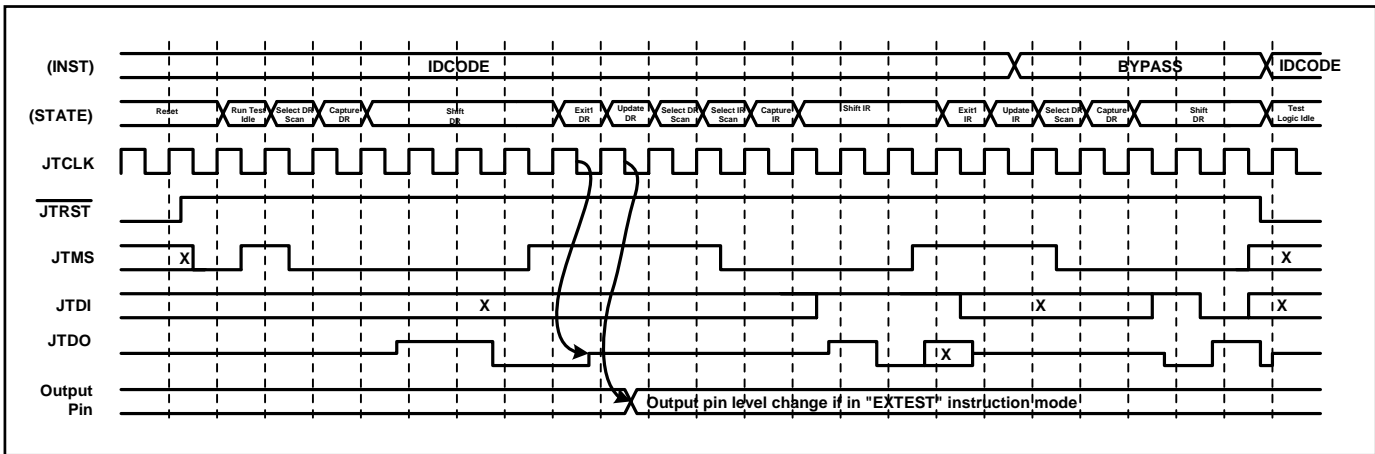
The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

15.6 JTAG Functional Timing

This functional timing for the JTAG circuits shows:

- The JTAG controller starting from reset state.
- Shifting out the first 4 LSB bits of the IDCODE.
- Shifting in the BYPASS instruction (111) while shifting out the mandatory X01 pattern.
- Shifting the TDI pin to the TDO pin through the bypass shift register.
- An asynchronous reset occurs while shifting.

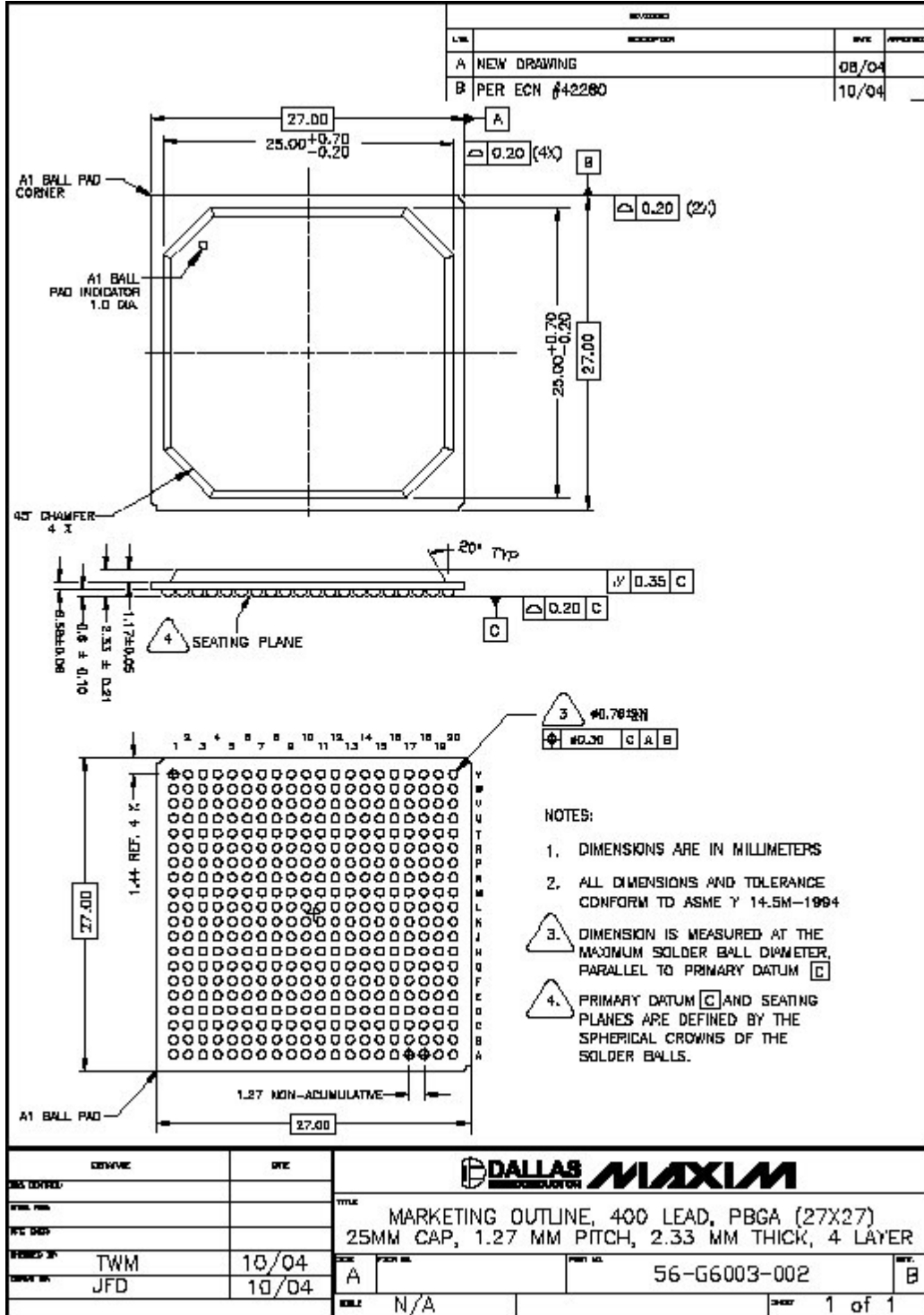
Figure 15-3. JTAG Functional Timing



16 PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)

16.1 400-Ball BGA (27mm x 27mm) (56-G6003-002)



17 DOCUMENT REVISION HISTORY

| REVISION | DESCRIPTION |
|----------|---|
| 102105 | New product release. |
| 011607 | <p>Updates for <i>Table 7-1</i>:</p> <p>(Page 23) Corrected pin description of MDC. (Page 23) Clarified text regarding use of REF_CLK in DCE and RMII modes. (Page 23) Corrected pin description of REF_CLKO. (Page 27) Changed name of RCLKO[1:4] pins to RCLK[1:4] to avoid confusion. (Page 28) Changed name of RDCLKO[1:4] pins to RCLKO[1:4] to avoid confusion. (Page 31) Moved ball names for F12, G10, G11, H3, N8, R6 from V_{SS} to DV_{SS} for proper JTAG grouping.</p> <p>(Page 32) Updates for <i>Figure 7-1</i>:</p> <p>Corrected name for ball D15 to V_{SS} to match pin description. Corrected name for ball G20 to V_{SS} to match pin description. Corrected name for ball H20 to V_{SS} to match pin description. Corrected name for ball J20 to V_{SS} to match pin description. Corrected name for balls B16–B20, C19, D18, D19, D20, F18, F19, and G16 from V_{DD} to V_{DD3.3} to match pin description. Changed name for ball L14 from ZRCLKIO to RCLKI to match pin description. Changed names for ball F12, G10, G11, H3, N8, R6 from V_{SS} to DV_{SS} for proper JTAG grouping.</p> <p>(Page 37, Figure 9-1) Removed reference to 8XCLK. Signal not present in this device. (Page 39) Corrected low-power mode information in Section 9.2. (Page 64) Clarified Section 9.16 on X.86 mode synchronization. (Page 124) Corrected SU.MACCR register map. (Pages 126 and 200) Changed bits 7, 6, and 5 for TR.T1CCR1 from “—” to MCLKS, SIE, and CRC4C; added bit definitions to page 200. (Pages 127, 234) Corrected/changed definition of TR.LBCR.LIUC (bit 4) to Reserved. (Page 135) Clarified the GL.C1QPR register definition. (Page 169) Corrected SU.GCR.H10S bit definition. (Page 174) Corrected the SU.RQLT and SU.RQHT default values to zero. (Page 174) Corrected default value listed in the SU.RMFSRL register definition. (Page 177) Corrected SU.MACCR.PM and SU.MACCR.PAM bit definitions. (Page 204) Corrected default value of TR.IDR register. (Pages 234, 324, 325) Removed references to TDATA (pages 234, 324, 325). Signals not present in this device. (Page 244) Added note to TR.CCR2.0 (BPEN) bit description. (Page 312, Table 14-10) Added TCLKE to TSERO Output Delay Minimum of 3ns; added TCLKE to TSYNC Setup Time Minimum of 3.5ns. (Page 327) Added a note regarding the special considerations required for dual JTAG controllers.</p> |