# AMIS-42665

# High-Speed Low Power CAN Transceiver

ON Semiconductor®

http://onsemi.com

### Description

The AMIS−42665 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

Due to the wide common−mode voltage range of the receiver inputs, the AMIS−42665 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

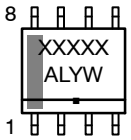
The AMIS−42665 is a new addition to the CAN high−speed transceiver family and offers the following additional features:

### Features

- Wake−up (WU) Over Bus
- Voltage Source via $V_{SPLIT}$ Pin for Stabilizing the Recessive Bus Level (Further EMC Improvement)
- Ideal Passive Behavior when Supply Voltage is Removed
- Extremely Low Current Standby Mode
- Compatible with the ISO 11898 Standard (ISO 11898−2, ISO 11898−5 and SAE J2284)
- High Speed (up to 1 Mbps)
- Ideally Suited for 12 V and 24 V Industrial and Automotive Applications
- Extremely Low Current Standby Mode with Wake−up via the Bus
- Low EME Common−Mode Choke is No Longer Required
- Differential Receiver with Wide Common−Mode Range (±35 V) for High EMS
- Transmit Data (TxD) Dominant Time−out Function
- Thermal Protection
- Bus Pins Protected against Transients in an Automotive Environment
- Power Down Mode in which the Transmitter is Disabled
- Bus and $V_{SPLIT}$ Pins Short Circuit Proof to Supply Voltage and Ground
- Logic Level Inputs Compatible with 3.3 V Devices
- These are Pb−Free Devices

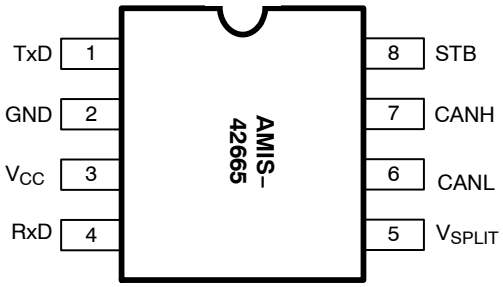
### MARKING DIAGRAM


SOIC−8
CASE 751




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

### PIN ASSIGNMENT




(Top View)

PC20040829.1

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

**Table 1. TECHNICAL CHARACTERISTICS**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | | 4.75 | 5.25 | V |
| $V_{STB}$ | DC Voltage at Pin STB | | −0.3 | $V_{CC}$ | V |
| $V_{TxD}$ | DC Voltage at Pin TxD | | −0.3 | $V_{CC}$ | V |
| $V_{RxD}$ | DC Voltage at Pin RxD | | −0.3 | $V_{CC}$ | V |
| $V_{CANH}$ | DC Voltage at Pin CANH | $0 < V_{CC} < 5.25$ V; No Time Limit | −35 | +35 | V |
| $V_{CANL}$ | DC Voltage at Pin CANL | $0 < V_{CC} < 5.25$ V; No Time Limit | −35 | +35 | V |
| $V_{SPLIT}$ | DC Voltage at Pin $V_{SPLIT}$ | $0 < V_{CC} < 5.25$ V; No Time Limit | −35 | +35 | V |
| $V_{O(dif)(bus\_dom)}$ | Differential Bus Output Voltage in Dominant State | 42.5 Ω < $R_{LT}$ < 60 Ω | 1.5 | 3 | V |
| CM−range | Input Common−Mode Range for Comparator | Guaranteed Differential Receiver Threshold and Leakage Current | −35 | +35 | V |
| $V_{CM-peak}$ | Common−Mode Peak | See Figures 11 and 12 | −500 | 500 | mV |
| $C_{load}$ | Load Capacitance on IC Outputs | | | 10 | pF |
| $t_{pd(rec-dom)}$ | Propagation Delay TxD to RxD | See Figure 7 | 90 | 230 | ns |
| $t_{pd(dom-rec)}$ | Propagation Delay TxD to RxD | See Figure 7 | 90 | 245 | ns |
| $T_J$ | Junction Temperature | | −40 | 150 | °C |

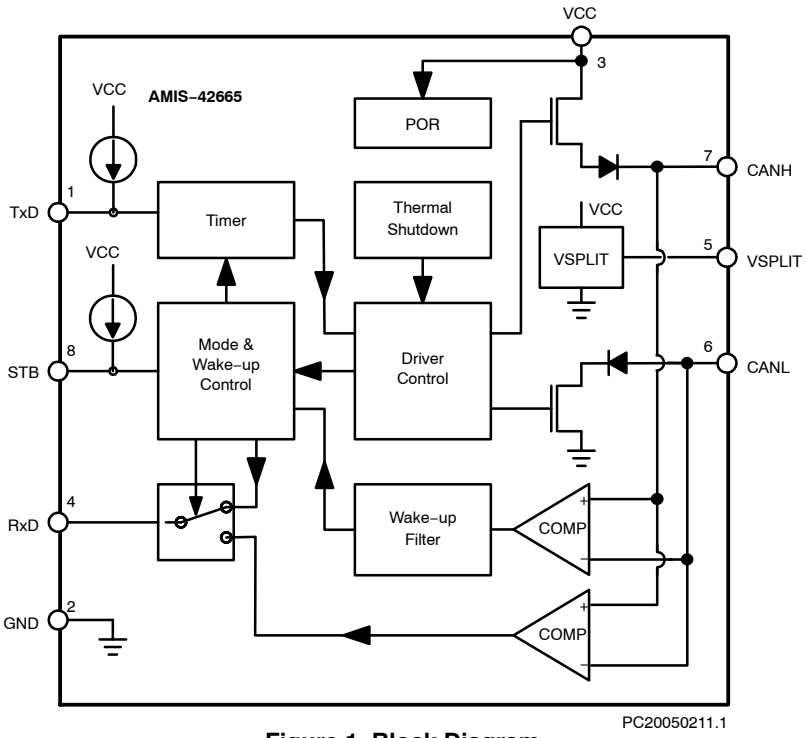



**Figure 1. Block Diagram**

## TYPICAL APPLICATION

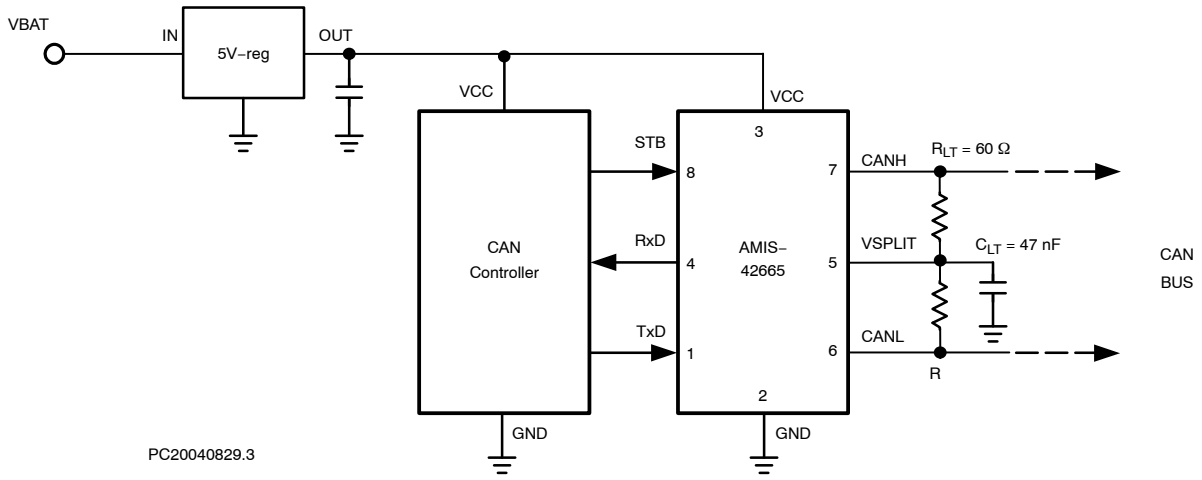



**Figure 2. Application Diagram**

**Table 2. PIN LIST AND DESCRIPTIONS**

| Pin | Name | Description |
|---|---|---|
| 1 | TxD | Transmit Data Input; Low Input → Dominant Driver; Internal Pullup Current |
| 2 | GND | Ground |
| 3 | $V_{CC}$ | Supply Voltage |
| 4 | RxD | Receive Data Output; Dominant transmitter → Low Output |
| 5 | $V_{SPLIT}$ | Common−Mode Stabilization Output |
| 6 | CANL | Low−Level CAN Bus Line (Low in Dominant Mode) |
| 7 | CANH | High−Level CAN Bus Line (High in Dominant Mode) |
| 8 | STB | Standby Mode Control Input |

**Table 3. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | −0.3 | +7 | V |
| $V_{CANH}$ | DC Voltage at Pin CANH | 0 < $V_{CC}$ < 5.25 V; No Time Limit | −50 | +50 | V |
| $V_{CANL}$ | DC Voltage at Pin CANL | 0 < $V_{CC}$ < 5.25 V; No Time Limit | −50 | +50 | V |
| $V_{SPLIT}$ | DC Voltage at Pin $V_{SPLIT}$ | 0 < $V_{CC}$ < 5.25 V; No Time Limit | −50 | +50 | V |
| $V_{TxD}$ | DC Voltage at Pin TxD | | −0.3 | $V_{CC}$ + 0.3 | V |
| $V_{RxD}$ | DC Voltage at Pin RxD | | −0.3 | $V_{CC}$ + 0.3 | V |
| $V_{STB}$ | DC Voltage at Pin STB | | −0.3 | $V_{CC}$ + 0.3 | V |
| $V_{tran(CANH)}$ | Transient Voltage at Pin CANH | Note 1 | −300 | +300 | V |
| $V_{tran(CANL)}$ | Transient voltage at Pin CANL | Note 1 | −300 | +300 | V |
| $V_{tran(VSPLIT)}$ | Transient Voltage at Pin $V_{SPLIT}$ | Note 1 | −300 | +300 | V |
| $V_{esd(CANL/CANH/VSPLIT)}$ | Electrostatic Discharge Voltage at CANH and CANL Pin | Note 2<br>Note 4 | −8<br>−500 | +8<br>+500 | kV<br>V |
| $V_{esd}$ | Electrostatic Discharge Voltage at All Other Pins | Note 2<br>Note 4 | −5<br>−500 | +5<br>+500 | kV<br>V |
| Latch−up | Static Latch−up at all Pins | Note 3 | | 120 | mA |
| $T_{stg}$ | Storage Temperature | | −55 | +150 | °C |
| $T_{amb}$ | Ambient Temperature | | −40 | +125 | °C |
| $T_J$ | Maximum Junction Temperature | | −40 | +170 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Applied transient waveforms in accordance with ISO 7637 part 3, test pulses 1, 2, 3a, and 3b (see Figure 5).
2. Standardized human body model electrostatic discharge (ESD) pulses in accordance to MIL883 method 3015.7.
3. Static latch−up immunity: Static latch−up protection level when tested according to EIA/JESD78.
4. Standardized charged device model ESD pulses when tested according to EOS/ESD DS5.3−1993.

**Table 4. THERMAL CHARACTERISTICS**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{th(vj-a)}$ | Thermal Resistance from Junction−to−Ambient in SOIC−8 Package | In free air | 145 | K/W |
| $R_{th(vj-s)}$ | Thermal Resistance from Junction−to−Substrate of Bare Die | In free air | 45 | K/W |

## FUNCTIONAL DESCRIPTION

AMIS−42665 provides two modes of operation as illustrated in Table 5. These modes are selectable through pin STB.

**Table 5. OPERATING MODES**

| Mode | Pin STB | Pin RXD | |
|---|---|---|---|
| | | Low | High |
| Normal | Low | Bus Dominant | Bus Recessive |
| Standby | High | Wake−up Request Detected | No Wake−up Request Detected |

### Normal Mode

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give extremely low EME.

### Standby Mode

In standby mode both the transmitter and receiver are disabled and a very low−power differential receiver monitors the bus lines for CAN bus activity. The bus lines are terminated to ground and supply current is reduced to a minimum, typically 10 μA. When a wake−up request is

detected by the low−power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of $t_{dbus}$, the RxD pin is driven low by the transceiver to inform the controller of the wake−up request.

### Split Circuit

The $V_{SPLIT}$ Pin is operational only in normal mode. In standby mode this pin is floating. The $V_{SPLIT}$ is connected as shown in Figure 2 and its purpose is to provide a stabilized DC voltage of 0.5 x $V_{CC}$ to the bus avoiding possible steps in the common−mode signal therefore reducing EME. These unwanted steps could be caused by an unpowered node on the network with excessive leakage current from the bus that shifts the recessive voltage from its nominal 0.5 x $V_{CC}$ voltage.

### Wake−up

When a valid wake−up (dominant state longer than $t_{dbus}$) is received during the standby mode the RxD pin is driven low. Wake−up behavior in case of a permanent dominant – due to, for example, a bus short – represents the only difference between the circuit sub−versions listed in the Ordering Information table. It is depicted in Figures 3 and 4. When the standby mode is entered while a dominant is present on the bus, the “unconditioned bus wake−up” versions will signal a bus−wakeup immediately after the state transition (seen as a High−level glitch on RxD). The other version (differing purely by a metal−level modification in the digital part) will signal bus−wakeup only after the initial dominant is released. In this way it’s ensured, that a CAN bus can be put to a low−power mode even if the nodes have a level sensitivity to RxD pin and a permanent dominant is present on the bus.

### Overtemperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 160°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off−state resets when Pin TxD goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

### TxD Dominant Time−out Function

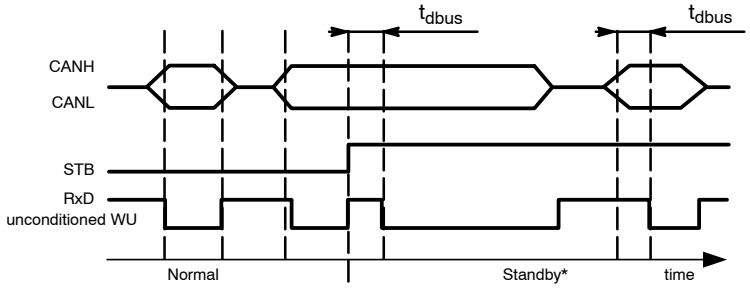
A TxD dominant time−out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if Pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low−level on Pin TxD exceeds the internal timer value $t_{dom(TxD)}$, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on Pin TxD. See Figure 10.

This TxD dominant time−out time ($t_{dom(TxD)}$) defines the minimum possible bit rate to 40 kbps.

### Fail Safe Features

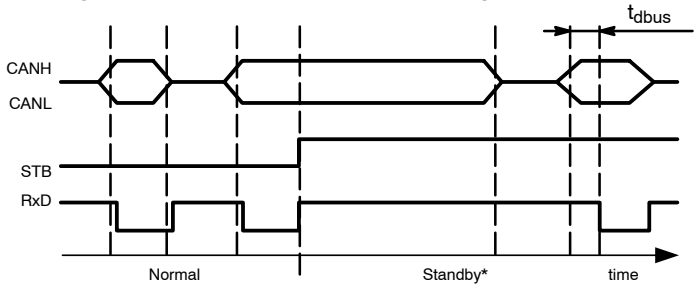
A current−limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 5). Pins TxD and STB are pulled high internally should the input become disconnected. Pins TxD, STB and RxD will be floating, preventing reverse supply should the $V_{CC}$ supply be removed.




*Even if bus dominant signals longer than tdbus are echoed on RxD, the transceiver stays in standby mode until STB is released.

**Figure 3. AMIS42665TJAA1/3 Wake−up Behavior**




*On this derivative, bus dominant signals longer than $t_{dbus}$ are echoed on RxD after the bus passed through a recessive time following the trigtger of STB. The transceiver stays in standby mode until STB is released.

**Figure 4. AMIS42665TJAA6 Wake−up Behavior**

## ELECTRICAL CHARACTERISTICS

**Definitions**

All voltages are referenced to GND (Pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

**CHARACTERISTICS** $V_{CC}$ = 4.75 V to 5.25 V; $T_J$ = −40°C to +150°C; $R_{LT}$ = 60 Ω unless specified otherwise.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY (PIN $V_{CC}$)** | | | | | | |
| $I_{CC}$ | Supply Current | Dominant; $V_{TxD}$ = 0 V<br>Recessive; $V_{TxD}$ = $V_{CC}$ | | 45<br>4 | 65<br>8 | mA |
| $I_{CCS}$ | Supply Current in Standby Mode | $T_{J,max}$ = 100°C | | 10 | 15 | μA |
| **TRANSMITTER DATA INPUT (PIN TxD)** | | | | | | |
| $V_{IH}$ | High−Level Input Voltage | Output Recessive | 2.0 | – | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low−Level Input Voltage | Output Dominant | −0.3 | – | +0.8 | V |
| $I_{IH}$ | High−Level Input Current | $V_{TxD}$ = $V_{CC}$ | −5 | 0 | +5 | μA |
| $I_{IL}$ | Low−Level Input Current | $V_{TxD}$ = 0 V | −75 | −200 | −350 | μA |
| $C_i$ | Input Capacitance | Not Tested | – | 5 | 10 | pF |
| **TRANSMITTER MODE SELECT (PIN STB)** | | | | | | |
| $V_{IH}$ | High−Level Input Voltage | Standby Mode | 2.0 | – | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low−Level Input Voltage | Normal Mode | −0.3 | – | +0.8 | V |
| $I_{IH}$ | High−Level Input Current | $V_{STB}$ = $V_{CC}$ | −5 | 0 | +5 | μA |
| $I_{IL}$ | Low−Level Input Current | $V_{STB}$ = 0 V | −1 | −4 | −10 | μA |
| $C_i$ | Input Capacitance | Not Tested | – | 5 | 10 | pF |
| **RECEIVER DATA OUTPUT (PIN RxD)** | | | | | | |
| $I_{oh}$ | High−Level Output Current | $V_o$ = 0.7 x $V_{CC}$ | −5 | −10 | −15 | mA |
| $I_{ol}$ | Low−Level Output Current | $V_o$ = 0.3 x $V_{CC}$ | 5 | 10 | 15 | mA |
| **BUS LINES (PINS CANH AND CANL)** | | | | | | |
| $V_{o(reces)\ (norm)}$ | Recessive Bus Voltage<br>Normal Mode | $V_{TxD}$ = $V_{CC}$; No Load | 2.0 | 2.5 | 3.0 | V |
| $V_{o(reces)\ (stby)}$ | Recessive Bus Voltage | $V_{TxD}$ = $V_{CC}$; No Load<br>Standby Mode | −100 | 0 | 100 | mV |
| $I_{o(reces)\ (CANH)}$ | Recessive Output Current at Pin CANH | −35 V < $V_{CANH}$ < +35 V;<br>0 V < $V_{CC}$ < 5.25 V | −2.5 | – | +2.5 | mA |
| $I_{o(reces)\ (CANL)}$ | Recessive Output Current at Pin CANL | −35 V < $V_{CANL}$ < +35 V;<br>0 V < $V_{CC}$ < 5.25 V | −2.5 | – | +2.5 | mA |
| $I_{LI(CANH)}$ | Input Leakage Current to Pin CANH | $V_{CC}$ = 0 V;<br>$V_{CANL}$ = $V_{CANH}$ = 5 V | −10 | – | +10 | μA |
| $I_{LI(CANL)}$ | Input Leakage Current to Pin CANL | $V_{CC}$ = 0 V;<br>$V_{CANL}$ = $V_{CANH}$ = 5 V | −10 | – | +10 | μA |
| $V_{o(dom)\ (CANH)}$ | Dominant Output Voltage at Pin CANH | $V_{TxD}$ = 0 V | 3.0 | 3.6 | 4.25 | V |
| $V_{o(dom)\ (CANL)}$ | Dominant Output Voltage at Pin CANL | $V_{TxD}$ = 0 V | 0. 5 | 1.4 | 1.75 | V |
| $V_{o(dif)\ (bus\_dom)}$ | Differential Bus Output Voltage<br>($V_{CANH}$ − $V_{CANL}$) | $V_{TxD}$ = 0 V; Dominant;<br>42.5 Ω < $R_{LT}$ < 60 Ω | 1.5 | 2.25 | 3.0 | V |
| $V_{o(dif)\ (bus\_rec)}$ | Differential Bus Output Voltage<br>($V_{CANH}$ − $V_{CANL}$) | $V_{TxD}$ = $V_{CC}$; Recessive;<br>No Load | −120 | 0 | +50 | mV |
| $I_{o(sc)\ (CANH)}$ | Short Circuit Output Current at Pin CANH | $V_{CANH}$ = 0 V; $V_{TxD}$ = 0 V | −45 | −70 | −120 | mA |

**CHARACTERISTICS** $V_{CC}$ = 4.75 V to 5.25 V; $T_J$ = −40°C to +150°C; $R_{LT}$ = 60 Ω unless specified otherwise.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **BUS LINES (PINS CANH AND CANL)** | | | | | | |
| $I_{o(sc)\ (CANL)}$ | Short Circuit Output Current at Pin CANL | $V_{CANL}$ = 36 V; $V_{TxD}$ = 0 V | 45 | 70 | 120 | mA |
| $V_{i(dif)\ (th)}$ | Differential Receiver Threshold Voltage (see Figure 6) | −5 V < $V_{CANL}$ < +12 V; −5 V < $V_{CANH}$ < +12 V; | 0.5 | 0.7 | 0.9 | V |
| $V_{ihcm(dif)\ (th)}$ | Differential Receiver Threshold Voltage for High Common−Mode (See Figure 6) | −35 V < $V_{CANL}$ < +35 V; −35 V < $V_{CANH}$ < +35 V; | 0.40 | 0.7 | 1.00 | V |
| $V_{i(dif)\ (hys)}$ | Differential Receiver Input Voltage Hysteresis (see Figure 6) | −35 V < $V_{CANL}$ < +35 V; −35 V < $V_{CANH}$ < +35 V; | 50 | 70 | 100 | mV |
| $R_{i(cm)\ (CANH)}$ | Common−Mode Input Resistance at Pin CANH | | 15 | 26 | 37 | kΩ |
| $R_{i(cm)\ (CANL)}$ | Common−Mode Input Resistance at Pin CANL | | 15 | 26 | 37 | kΩ |
| $R_{i(cm)\ (m)}$ | Matching Between Pin CANH and Pin CANL Common Mode Input Resistance | $V_{CANH}$ = $V_{CANL}$ | −3 | 0 | +3 | % |
| $R_{i(dif)}$ | Differential Input Resistance | | 25 | 50 | 75 | kΩ |
| $C_{i(CANH)}$ | Input Capacitance at Pin CANH | $V_{TxD}$ = $V_{CC}$; Not Tested | | 7.5 | 20 | pF |
| $C_{i(CANL)}$ | Input Capacitance at Pin CANL | $V_{TxD}$ = $V_{CC}$; Not Tested | | 7.5 | 20 | pF |
| $C_{i(dif)}$ | Differential Input Capacitance | $V_{TxD}$ = $V_{CC}$; Not Tested | | 3.75 | 10 | pF |
| **COMMON−MODE STABILIZATION (PIN $V_{SPLIT}$)** | | | | | | |
| $V_{SPLIT}$ | Reference Output Voltage at Pin $V_{SPLIT}$ | Normal Mode; −500 μA < $I_{SPLIT}$ < 500 μA | 0.3 x $V_{CC}$ | − | 0.7 x $V_{CC}$ | |
| $I_{SPLIT(i)}$ | $V_{SPLIT}$ Leakage Current | Standby Mode | −5 | | +5 | μA |
| $I_{SPLIT(lim)}$ | $V_{SPLIT}$ Limitation Current | Normal Mode | −3 | | +3 | mA |
| **POWER−ON−RESET (POR)** | | | | | | |
| PORL | POR Level | CANH, CANL in Tri−State Below POR Level | 2.2 | 3.5 | 4.5 | V |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{J(sd)}$ | Shutdown Junction Temperature | | 150 | 160 | 180 | °C |
| **TIMING CHARACTERISTICS** (see Figures 7 and 8) | | | | | | |
| $t_{d(TxD−BUSon)}$ | Delay TXD to Bus Active | $C_l$ = 100 pF Between CANH to CANL | 40 | 85 | 105 | ns |
| $t_{d(TxD−BUSoff)}$ | Delay TXD to Bus Inactive | $C_l$ = 100 pF Between CANH to CANL | 30 | 60 | 105 | ns |
| $t_{d(BUSon−RXD)}$ | Delay Bus Active to RXD | $C_{rxd}$ = 15 pF | 25 | 55 | 105 | ns |
| $t_{d(BUSoff−RXD)}$ | Delay Bus Inactive to RXD | $C_{rxd}$ = 15 pF | 40 | 100 | 105 | ns |
| $t_{pd(rec−dom)}$ | Propagation Delay TXD to RXD from Recessive−to−Dominant | $C_l$ = 100 pF Between CANH to CANL | 90 | | 230 | ns |
| $t_{d(dom−rec)}$ | Propagation Delay TXD to RXD from Dominant−to−Recessive | $C_l$ = 100 pF Between CANH to CANL | 90 | | 245 | ns |
| $t_{d(stb−nm)}$ | Delay Standby Mode to Normal Mode | | 5 | 7.5 | 10 | μs |
| $t_{dbus}$ | Dominant Time for Wake−up via Bus | | 0.75 | 2.5 | 5 | μs |
| $t_{dom(TxD)}$ | TxD Dominant Time for Time Out | $V_{TxD}$ = 0 V | 300 | 650 | 1000 | μs |
| Baudrate | Communication Speed Achievable | | 40k | | 1M | bps |

## MEASUREMENT SETUPS AND DEFINITIONS

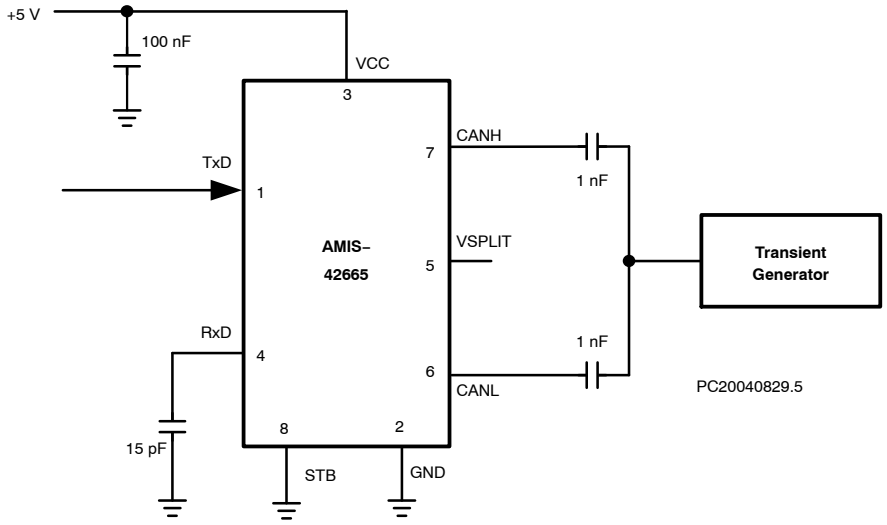



**Figure 5. Test Circuit for Automotive Transients**

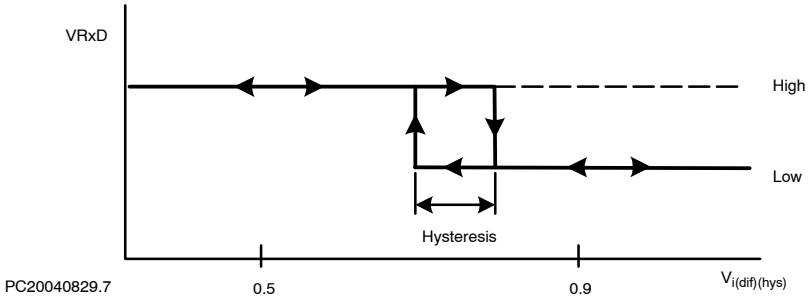



**Figure 6. Hysteresis of the Receiver**

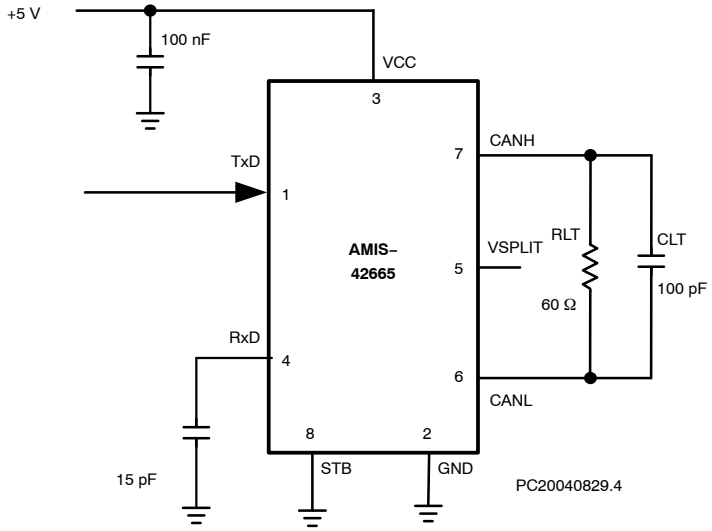



**Figure 7. : Test Circuit for Timing Characteristics**

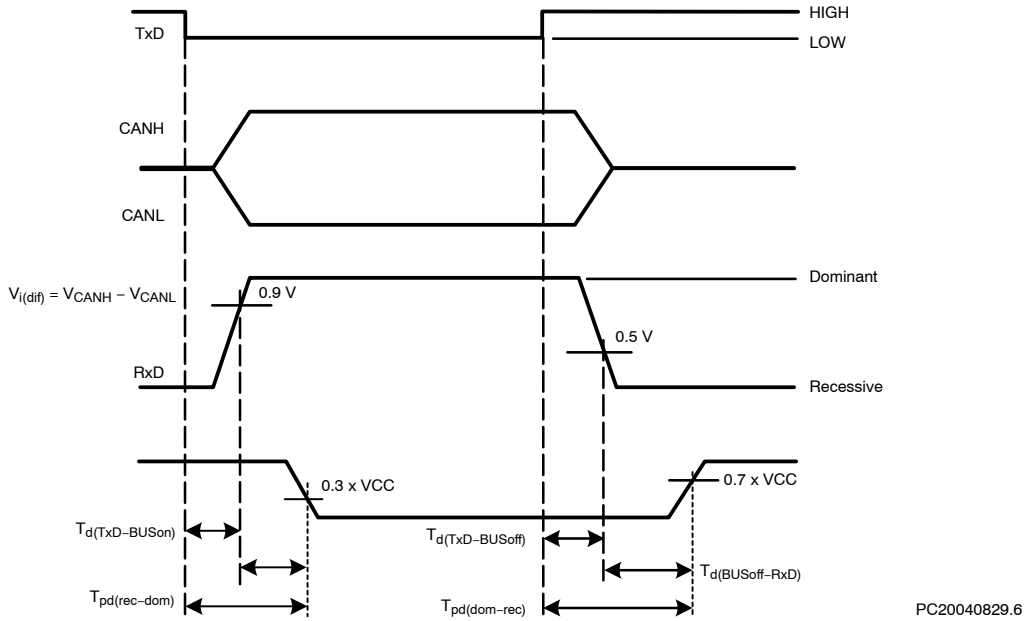



**Figure 8. Timing Diagram for AC Characteristics**

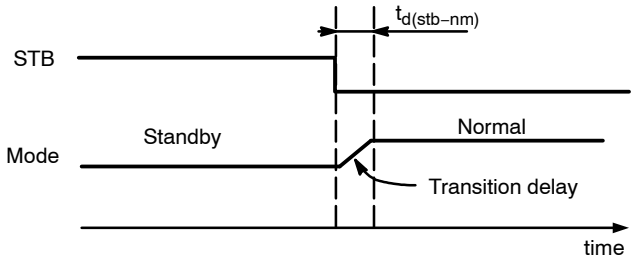



**Figure 9. Transition from Standby to Normal**

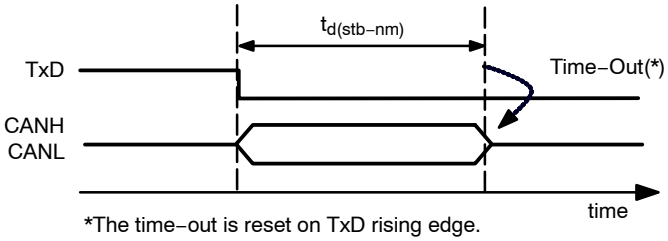



**Figure 10. AMIS−42665 TxD Time−Out Bus Blockage Prevention in Case of Controller Failure**

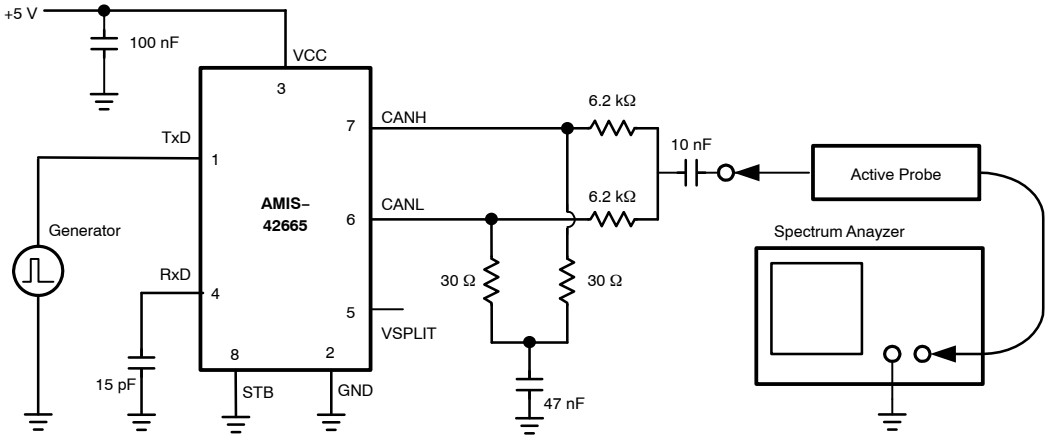



**Figure 11. Basic Test Setup for Electromagnetic Measurement**

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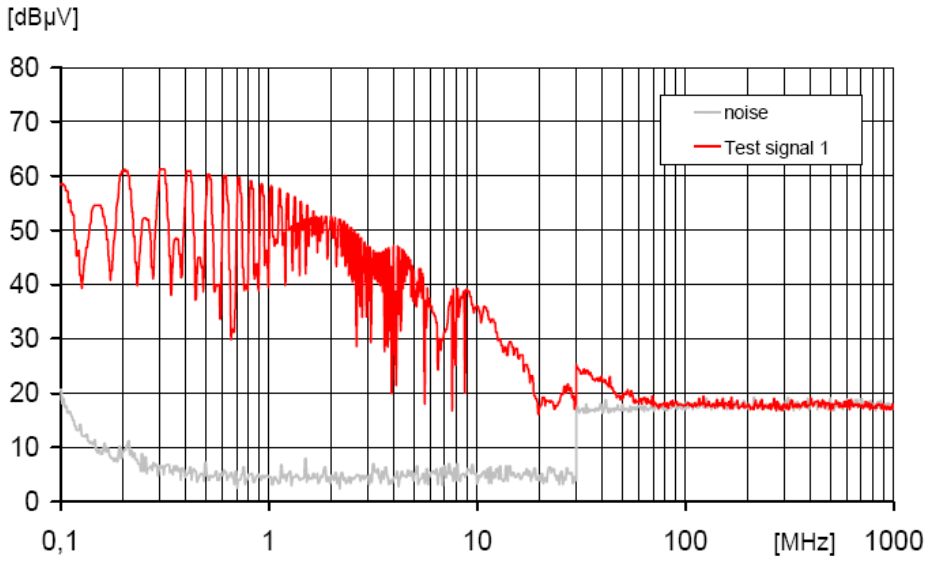



**Figure 12. EME Measurements**

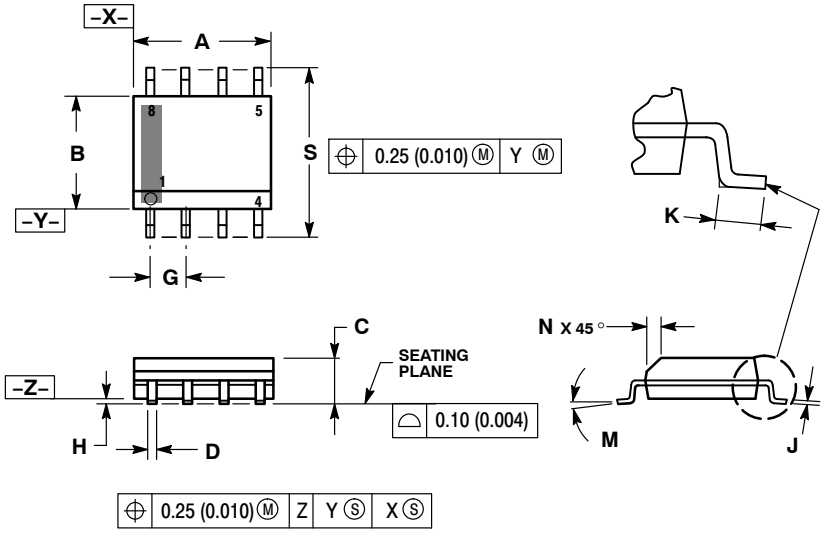
## DEVICE ORDERING INFORMATION

| Part Number | Version | Temperature Range | Package Type | Shipping† |
|---|---|---|---|---|
| AMIS42665TJAA1G | Unconditioned Bus Wake−up | −40°C – 125°C | SOIC−8* (Pb−Free) | 96 Tube / Tray |
| AMIS42665TJAA1RG | | −40°C – 125°C | SOIC−8* (Pb−Free) | 3000 / Tape & Reel |
| AMIS42665TJAA3L | | −40°C – 125°C | SOIC−8** (Pb−Free) | 96 Tube / Tray |
| AMIS42665TJAA3RL | | −40°C – 125°C | SOIC−8** (Pb−Free) | 3000 / Tape & Reel |
| AMIS42665TJAA6G | Bus Wake−up Inactive in Case of Bus Fault | −40°C – 125°C | SOIC−8* (Pb−Free) | 96 Tube / Tray |
| AMIS42665TJAA6RG | | −40°C – 125°C | SOIC−8* (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Matte Sn, JEDEC MS−012
** NiPdAu, JEDEC MS−012

## PACKAGE DIMENSIONS

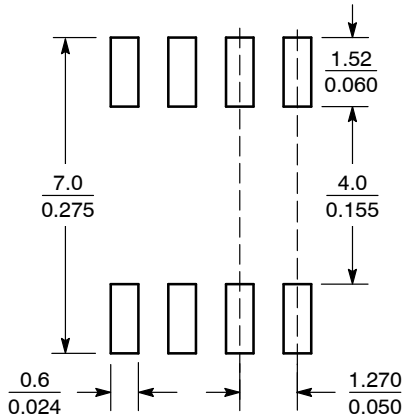
**SOIC−8**
CASE 751−07
ISSUE AJ




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

## SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



## PUBLICATION ORDERING INFORMATION

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