

# VSC8142, 8145, 8147

**VITESSE**

## 2.5G Multi-rate SONET/SDH Transceiver Family



### SPECIFICATIONS:

#### VSC8142

- ▶ Rates: OC-48/12/3, FEC, GbE, Fibre Channel and Other Various Data Rates
- ▶ Power Dissipation: 700mW
- ▶ Selectable Reference Clock Frequency (78MHz or 155MHz)
- ▶ Supply Voltage: 2.5V or Optional 2.5V/3.3V
- ▶ 23mm x 23mm, 208 BGA Package
- ▶ 16-bit LVPECL Parallel Interface
- ▶ Operating Temperature Ranges: -40°C to +85°C Ambient, 0°C to 70°C Ambient

#### VSC8145

- ▶ Rates: OC-48/-12/-3, FEC, GbE, Fibre Channel and Other Various Data Rates
- ▶ Power Dissipation: 800mW
- ▶ Selectable Reference Clock Frequency (155MHz or 622MHz)
- ▶ Supply Voltage: 2.5V
- ▶ 21mm x 21mm, 156 BGA Package
- ▶ 4-bit LVDS Parallel Interface
- ▶ Operating Temperature Ranges: -40°C to +85°C Ambient, 0°C to 70°C Ambient

#### VSC8147

- ▶ Rates: OC-48, FEC
- ▶ Power Dissipation: 800mW
- ▶ Supply Voltage: 2.5V
- ▶ 14mm x 14mm, 100-pin PQFP Package
- ▶ 4-bit LVDS Parallel Interface
- ▶ Operating Temperature Ranges: -40°C to +85°C Ambient, 0°C to 70°C Ambient

### FEATURES:

- ▶ OC-48/-12/-3, FEC, GbE, Fibre Channel and Other Various Data Rates
- ▶ Integrated Clock Recovery and Clock Multiplier Units
- ▶ Wide Ranging PLLs with Bypass Capabilities
- ▶ Low-speed Bit Order Swap (MSB/LSB)
- ▶ On-board FIFO with Auto-reset Function
- ▶ High-speed Clock Output Power-down Option
- ▶ LOS Detect with Auto-lock to Reference Clock
- ▶ Facility, Equipment, and Split Loopback Modes
- ▶ 0.18\_μ CMOS Technology

### APPLICATIONS:

- ▶ SONET/SDH Systems
- ▶ DWDM Systems
- ▶ Optical Crossconnects
- ▶ Optical Test Equipment

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## 2.5G Multi-rate SONET/SDH Transceiver Family

### GENERAL DESCRIPTION:

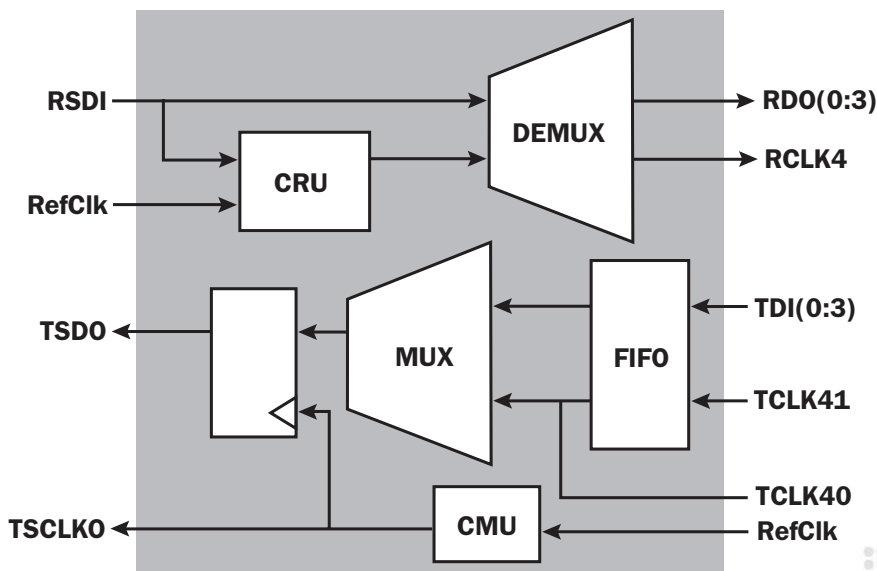


The VSC8142, VSC8145 and VSC8147 are extended multi-rate transceivers with integrated Clock Recovery Unit (CRU) and Clock Multiplier Unit (CMU) for use in SONET/SDH, DWDM, and other optical transport systems. The devices perform all required serialization and deserialization functions for OC-48, OC-12, OC-3, FEC, Gigabit Ethernet, Fibre Channel and FDDI/Fast Ethernet data rates.

The integrated CRU Phase Locked Loop (PLL) recovers the high-speed clock from the input Non-Return to Zero (NRZ) data signal. The integrated CMU PLL multiplies a low-speed reference clock to provide the high-speed serial line clock for internal logic and output retiming. Both CRU and CMU can be bypassed to accommodate rates not supported by the PLLs. The parallel interface incorporates an on-board FIFO with auto-reset to eliminating interfacetiming issues. The devices support serial looptiming as well as Facility, Equipment, and Split loopback modes.

The VSC8142, VSC8145 and VSC8147 exceed the Telecordia and ITU-T standards for jitter generation, tolerance and transfer providing ample design margin. The typical 800mW power dissipation, along with the thermally-enhance packages, eliminates the need for external heatsinks and allow the devices to be used in diverse operating environments. All device are available in commercial and industrial temperature ranges.

### BLOCK DIAGRAM:



For more information on Vitesse products, visit the Vitesse web site at [www.vitesse.com](http://www.vitesse.com) or contact Vitesse Sales at (800) VITESSE or [sales@vitesse.com](mailto:sales@vitesse.com)

### BENEFITS:

- ▶ Full SONET/SDH Jitter Compliance:
  - Low Jitter Generation: less than 5mUI (typical)
  - High Jitter Tolerance: exceeds 2x the SONET mask
- ▶ Wide-ranging PLLs that not only Provide Support for the Standard SONET/SDH Rates, but also for:
  - Fibre Channel, 2xFibre Channel
  - Gigabit Ethernet
  - FEC
  - FDDI
  - Fast Ethernet
- ▶ Integrated CRU and CMU can be Bypassed if an External CDR is Required, (e.g. the All-Rate/Adaptive VSC8123 CDR)
- ▶ The Order of the MSB and LSB on the Low-speed Interfaces can be Reversed, Giving the Designer Increased Flexibility When Laying Out the Board
- ▶ On-board FIFO Auto-Reset Function Eliminates the Need to use an External Logic
- ▶ Loss of Signal Detection on High-speed Data Inputs for Robust Line Monitoring Support
- ▶ Automatic Lock to Reference Clock on LOS Detection Provides Continuous Clocking for Upstream Devices
- ▶ Integrated High-speed and Low-speed Test Capabilities Provide System Diagnostic Support

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