PRELIMINARY

CY2XF23

High-Performance LVDS Oscillator with Frequency Margining - I²C Control

Features

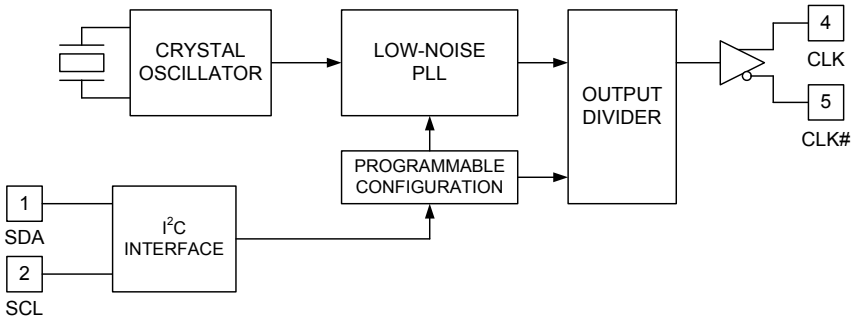
- Low jitter crystal oscillator (XO)
- Less than 1 ps typical root mean square (RMS) phase jitter
- Low-voltage differential signaling (LVDS) output
- Output frequency from 50 MHz to 690 MHz
- Frequency margining through I²C bus
- Factory-configured or field-programmable
- Integrated phase-locked loop (PLL)
- Pb-free package: 5.0 x 3.2 mm leadless chip carrier (LCC)
- Supply voltage: 3.3 V or 2.5 V
- Commercial and industrial temperature ranges

Functional Description

The CY2XF23 is a high-performance and high-frequency XO. It uses a Cypress proprietary low-noise PLL to synthesize the frequency from an integrated crystal. The output frequency can be changed using the I²C bus serial interface, allowing easy frequency margin testing in applications.

The CY2XF23 is available as a factory-configured device or as a field-programmable device. Factory configured devices are configured for general use (see Standard and Application-Specific Factory Configurations) or they can be customer specific.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram – 6-Pin Ceramic LCC

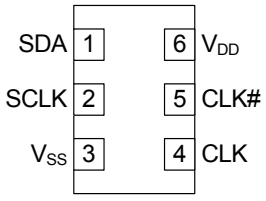


Table 1. Pin Definitions - 6 Pin Ceramic LCC

Pin	Name	I/O Type	Description
1	SDA	I/O	I²C serial data
2	SCLK	CMOS input	I²C serial clock
4, 5	CLK, CLK#	LVDS output	Differential output clock
6	V_{DD}	Power	Supply voltage: 2.5 V or 3.3 V
3	V_{SS}	Power	Ground

Contents

Standard and Application-Specific Factory Configurations

Part Number	Output Frequency	Frequency Word	RMS Phase Jitter (Random)	
			Offset Range	Jitter (Typical)
CY2XF23LXC001T	100.00 MHz (default)	0	637 kHz to 10 MHz	0.52 ps
	95.00 MHz	1	637 kHz to 10 MHz	–
	103.000007 MHz	2	637 kHz to 10 MHz	–
	104.999993 MHz	3	637 kHz to 10 MHz	–
CY2XF23LXI625T	78.125 MHz	0	1.875 MHz to 20 MHz	0.37 ps
	156.25 MHz	1	1.875 MHz to 20 MHz	0.31 ps
	312.50 MHz	2	1.875 MHz to 20 MHz	0.29 ps
	625.00 MHz (default)	3	1.875 MHz to 20 MHz	0.31 ps

Functional Description

The CY2XF23 is a PLL-based high-performance clock generator. It uses an internal crystal oscillator as a reference, and outputs one differential LVDS clock. It has an I^2C bus serial interface[1], which is used to change the output frequency.

The CY2XF23 comes configured for four different frequencies. At power-on, the four configurations are transparently loaded into an internal volatile memory which, in turn, controls the PLL. The user can switch between the four frequencies through the I^2C bus. The user can also configure the CY2XF23 with new output frequencies by shifting new data into the internal memory.

Frequency margining is a common application for this feature. One frequency is used for the standard operating mode of the device, while additional frequencies are available for margin testing, either during product development or in-system manufacturing test.

Note that all configuration changes made using I^2C are temporary and are lost when power is removed from the device. At power-on, the device returns to its original state.

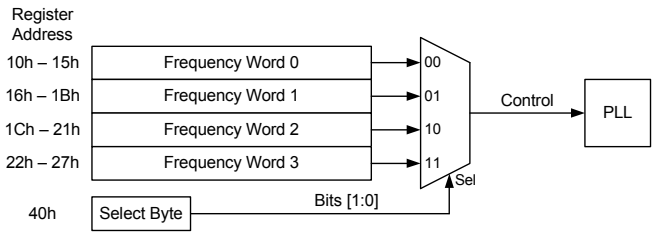
The configuration for a particular frequency is stored in a 6-byte block of memory, known as a word. The CY2XF23 has four such words, labeled ‘Frequency Word 0’ through ‘Frequency Word 3’. An additional register byte contains a 2-bit field, which selects one of the four frequency words. By writing to this select byte, the user can switch back and forth between the four programmed frequencies. The select byte can be configured to select any of the four frequency words at power-on.

When changing the output frequency, the frequency transition is not guaranteed to be smooth. There can be frequency excursions beyond the start frequency and the new frequency. Glitches and runt pulses are possible, and time must be allowed for the PLL to re-lock.

If more than four frequencies are needed, the I^2C bus can be used to change any of the four frequency words. When writing frequency words through I^2C, users should not change the currently selected word. Instead, write one of the three unselected words before changing the select byte to select that new word.

Figure 2 shows how the frequency words are arranged and selected.

Figure 2. Frequency Words



Configuration Software

Cypress provides CyClockWizard™ software that enables users to create data values for shifting into the frequency words. This software is required because the algorithm is too complicated to be described here.

The user specifies the output frequency. The software then calculates the bit stream for up to four frequency words, as outlined by the register addresses for each word seen in Figure 2.

Programming Description

The CY2XF23 is a programmable device. Before being used in an application, it must be programmed with the output frequencies and other variables described in Programming Variables on page 4. Two different device types are available, each with its own programming flow. They are described in the following sections.

Field-Programmable CY2XF23F

Field programmable devices are shipped unprogrammed and must be programmed before being installed on a printed circuit board (PCB). Customers use CyClockWizard™ software to specify the device configuration and generate a joint electron devices engineering council (JEDEC - extension .jed) programming file. Programming of samples and prototype quantities is available using the CyClockWizard software along with a CY3675-CLKMAKER1 CyClockMaker Clock Programmer Kit with a CY3675-LCC6A socket adapter. Cypress’s value added distribution partners also provide programming services. Field programmable devices are designated with an ‘F’ in the part number. They are intended for quick prototyping and inventory reduction. The software and programmer kit hardware can be downloaded from www.cypress.com by clicking the hyperlinks above.

Note
1. The serial interface is I^2C Bus compliant, with the following exceptions: SDA input leakage current, SDA input capacitance, SDA and SCLK are clamped to V_{DD}, setup time, and output hold time.

Factory-Configured CY2XF23

For ready-to-use devices, the CY2XF23 is available with no field programming required. Pre-configured devices (see Standard and Application-Specific Factory Configurations) are available for samples or orders, or a request for a custom configuration can be made. All requests are submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and datasheet with the programmed values. This part number is used for additional sample requests and production orders. The CY2XF23 is one-time programmable (OTP).

Programming Variables

Output Frequencies

The CY2XF23 is programmed with up to four independent output frequencies, which are then selected using the I^2C interface. The device can synthesize frequencies to a resolution of 1 part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

The CY2XF23 has an output frequency range of 50 MHz to 690 MHz, but the range is not continuous. The CY2XF23 cannot generate frequencies in the ranges of 521 MHz to 529 MHz and 596 MHz to 617 MHz.

Industrial versus Commercial Device Performance

Industrial and commercial devices have different internal crystals. They have a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. CyClockWIzard software allows the user to select between and view the expected performance of both options.

Table 2. Device Programming Variables

Variable
Output frequency 0
Output frequency 1
Output frequency 2
Output frequency 3
Temperature range (commercial or industrial)

Memory Map

Five fields can be written via the I^2C bus. Four frequency words define the output frequency. As shown in Table 3, each of these words is a 6-byte field. When writing to a frequency word, all six bytes should be written. They may be written either as individual byte writes, or as a block write. The currently selected frequency word should not be written to. All four words are symmetrical, meaning that a 6-byte value that is valid for one word is also valid for any of the other words, and produces the same frequency.

The fifth field is the select byte, located at byte address 40h. The value written into the two least significant bits determines the active frequency word. The other bits of the byte are reserved and must be written with the values indicated in the table. Users should never write to any address other than the 25 bytes described here.

Table 3. Frequency Words

Frequency Word	Byte Addresses (hex)	Word Select (Select Byte 40h)
0	10h to 15h	00
1	16h to 1Bh	01
2	1Ch to 21h	10
3	22h to 27h	11

Table 4. Register 40h: Select Byte

Bits	Default Value (binary)	Name	Description
7:2	000000	Reserved	Reserved. Always write this value.
1:0	User-defined	Word select	Selects the Frequency Word to determine the output frequency. 00 selects Word 0; 01 selects Word 1; 10 selects Word 2; 11 selects Word 3.

Serial Interface Protocol and Timing

The CY2XF23 uses pins SDA and SCLK for an I^2C bus that operates up to 100 kbits/sec in read or write mode. The CY2XF23 is always a slave on this bus, meaning that it never initiates a bus transaction. The basic write protocol is as follows:

Start Bit; 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; and so on, until STOP Bit. The basic serial format is illustrated in Figure 4 on page 6.

Device Address

The device address is a 7-bit value. The default serial interface address is 69H.

Data Valid

Data is valid when the clock is HIGH, and may only be transitioned when the clock is LOW as illustrated in Figure 5

Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in Figure 6 on page 6.

START Sequence - Start frame is indicated by SDA going LOW when SCLK is HIGH. Every time a start signal is given, the next 8-bit data must be the device address (seven bits) and a R/$\overline{W}$ bit, followed by register address (eight bits) and register data (eight bits).

STOP Sequence - Stop frame is indicated by SDA going HIGH when SCLK is HIGH. A stop frame frees the bus for writing to another part on the same bus or writing to another random register address.

Acknowledge Pulse

During write mode, the CY2XF23 responds with an Acknowledge (ACK) pulse after every eight bits. This is accomplished by pulling the SDA line LOW during the N*9th clock cycle as illustrated in Figure 7 on page 7. (N = the number of bytes transmitted). After the data packet is sent during read mode, the master generates the acknowledge.

Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (SDA = 0/LOW). The next eight bits must contain the data word intended for storage. After the data word is received, the slave responds with another acknowledge bit (SDA = 0/LOW), and the master must end the write sequence with a STOP condition.

Writing Multiple Bytes

To write more than one byte at a time, the master does not end the write sequence with a stop condition. Instead, the master can send multiple contiguous bytes of data to be stored. After each byte, the slave responds with an acknowledge bit, just like after the first byte, and accepts data until the acknowledge bit is responded to by the STOP condition. When receiving multiple bytes, the CY2XF23 internally increments the register address.

Read Operations

Read operations are initiated the same way as write operations except that the R/W bit of the slave address is set to ‘1’ (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The CY2XF23 has an onboard address counter that retains 1 more than the address of the last word access. If the last word written or read was word ‘n’, then a current address read operation would return the value stored in location ‘n+1’. When the CY2XF23 receives the slave address with the R/W bit set to a ‘1’, the CY2XF23 issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition, which causes the CY2XF23 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first the word address must be set. This is accomplished by sending the address to the CY2XF23 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next the master reissues the control byte with the R/W byte set to ‘1’. The CY2XF23 then issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition which causes the CY2XF23 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmission of the first 8-bit data word. This action results in an incrementing of the internal address pointer, and subsequently output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master may serially read the entire contents of the slave device memory. When the internal address pointer points to the FFh register, after the next increment, the pointer will point to the 00h register.

Figure 3. Data Transfer Sequence on the Serial Bus

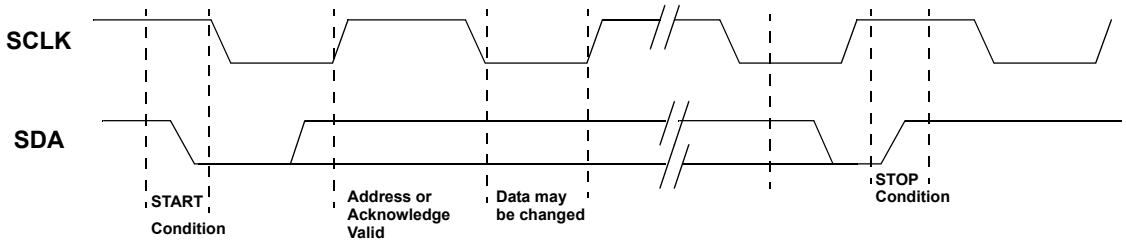


Figure 4. Data Frame Architecture

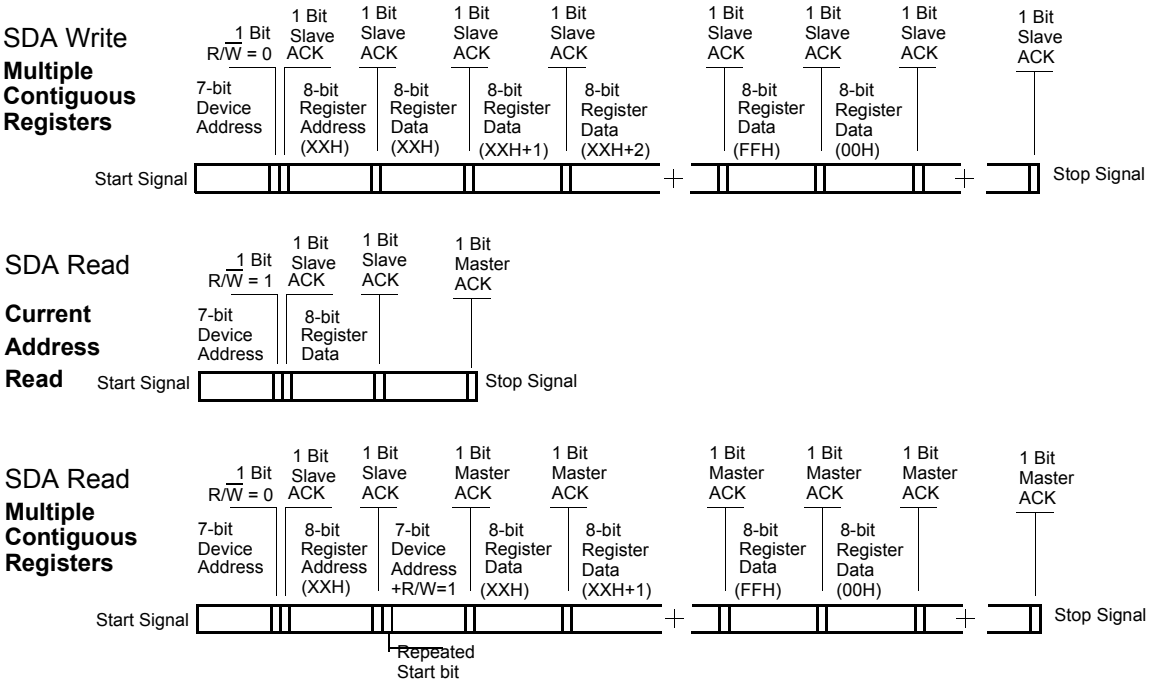


Figure 5. Data Valid and Data Transition Periods

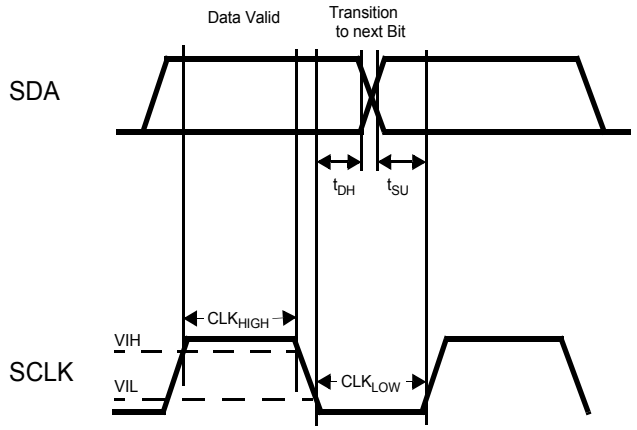


Figure 6. Start and Stop Frame

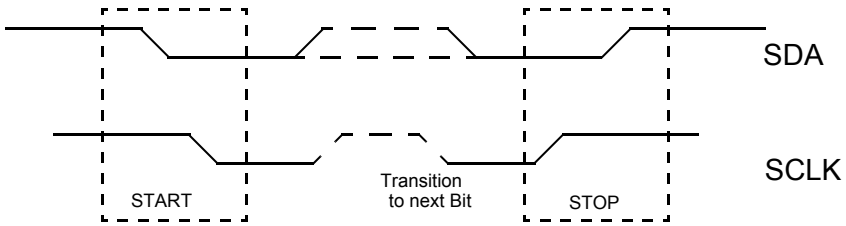
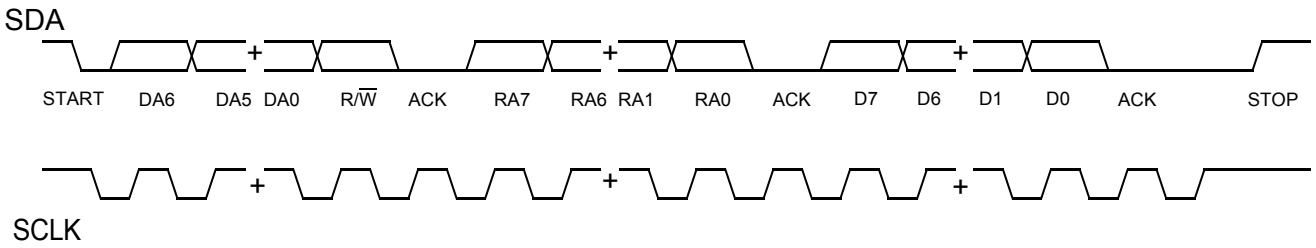


Figure 7. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	4.4	V
V_{IN}[2]	Input voltage, DC	Relative to V_{SS}	–0.5	V_{DD}+0.5	V
T_S	Temperature, storage	Non Operating	–55	135	°C
T_J	Temperature, junction		–40	135	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection human body model (HBM)	JEDEC Std 22-A114-B	2000	–	V
Θ_{JA}[3]	Thermal resistance, junction to ambient	0 m/s airflow	64		°C/W

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	3.3-V supply voltage range	3.135	3.3	3.465	V
	2.5-V supply voltage range	2.375	2.5	2.625	V
T_{PU}	Power-up time for V_{DD} to reach minimum specified voltage (power ramp is monotonic)	0.05	–	500	ms
T_A	Ambient temperature (commercial)	0	–	70	°C
	Ambient temperature (industrial)	–40	–	85	°C

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}[4]	Operating supply current	V_{DD} = 3.465 V, CLK = 150 MHz, output terminated	–	–	120	mA
		V_{DD} = 2.625 V, CLK = 150 MHz, output terminated	–	–	115	mA
V_{OD}	LVDS differential output voltage	V_{DD} = 3.3 V or 2.5 V, defined in Figure 8 as terminated in Figure 13	247	–	454	mV
ΔV_{OD}	Change in V_{OD} between complementary output states	V_{DD} = 3.3 V or 2.5 V, defined in Figure 8 as terminated in Figure 13	–	–	50	mV
V_{OS}	LVDS offset output voltage	V_{DD} = 3.3 V or 2.5 V, defined in Figure 9 as terminated in Figure 13	1.125	–	1.375	V

Notes
2. The voltage on any input or I/O pin cannot exceed the power pin during power up.
3. Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
4. I_{DD} includes ~4 mA of current that is dissipated externally in the output termination resistors.

DC Electrical Characteristics (continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
ΔV_{OS}	Change in V_{OS} between complementary output states	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between CLK and CLK#	–	–	50	mV
V_{OLS}	Output low voltage (SDA)	I_{OL} = 4 mA	–	–	0.1*V_{DD}	V
V_{IH}	Input high voltage		0.7*V_{DD}	–	–	V
V_{IL}	Input low voltage		–	–	0.3*V_{DD}	V
I_{IH0}	Input high current (SDA)	Input = V_{DD}	–	–	115	µA
I_{IH1}	Input high current (SCLK)	Input = V_{DD}	–	–	10	µA
I_{IL0}	Input low current (SDA)	Input = V_{SS}	–50	–	–	µA
I_{IL1}	Input low current (SCLK)	Input = V_{SS}	–20	–	–	µA
C_{IN0}[5]	Input capacitance (SDA)		–	15	–	pF
C_{IN1}[5]	Input capacitance (SCLK)		–	4	–	pF

AC Electrical Characteristics[5]

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{OUT}	Output frequency[6]		50	–	690	MHz
FSC	Frequency stability, commercial devices[7]	V_{DD} = min to max, T_A = 0°C to 70°C	–	–	±35	ppm
FSI	Frequency stability, industrial devices[7]	V_{DD} = min to max, T_A = –40° to 85°C	–	–	±55	ppm
AG	Aging, 10 years		–	–	±15	ppm
T_{DC}	Output duty cycle	F <= 450 MHz, measured at zero crossing	45	50	55	%
		F > 450 MHz, measured at zero crossing	40	50	60	%
T_R, T_F	Output rise and fall time	20% and 80% of full output swing	–	0.35	1.0	ns
T_{LOCK}	Startup time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min.)	–	–	5	ms
T_{LSER}	Relock time	Time for CLK to reach valid frequency from serial bus change to select bits in register 40h, measured from I^2C STOP	–	–	1	ms
$T_{Jitter(\phi)}$	RMS phase jitter (random)	F_{OUT} = 106.25 MHz (12 kHz to 20 MHz)	–	1	–	ps
		Pre-defined factory configurations[8]	See Note 8			ps

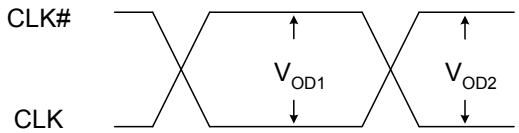
Notes
5. Not 100% tested, guaranteed by design and characterization.
6. This parameter is specified in CyClockWizard software.
7. Frequency stability is the maximum variation in frequency from F_0. It includes initial accuracy, plus variation from temperature and supply voltage.
8. Typical phase noise specs for factory programmed devices are listed in the Standard and Application-Specific Factory Configurations table on page 2.

I²C Bus Timing Specifications[5]

Parameter	Description	Min	Max	Unit
f_{SCLK}	SCLK frequency	–	100	kHz
$t_{HD:STA}$	Start mode time from SDA LOW to SCLK LOW	4	–	µs
t_{LOW}	SCLK LOW period	4.7	–	µs
t_{HIGH}	SCLK HIGH period	4	–	µs
$t_{SU:DAT}$	Input data setup (SDA transition to SCLK rising edge)	1000	–	ns
$t_{HD:DAT}$	Input data hold (SCLK falling edge to SDA transition)	0	–	ns
$t_{HD:DO}$	Output data hold (SCLK falling edge to SDA transition)	200	–	ns
t_{SR}	Rise time of SCLK and SDA	–	300	ns
t_{SF}	Fall time of SCLK and SDA	–	300	ns
$t_{SU:STO}$	Stop mode time from SCLK HIGH to SDA HIGH	4	–	µs
t_{BUF}	Stop mode to start mode	4.7	–	µs

Switching Waveforms

Figure 8. Output Voltage Swing



$$\Delta V_{OD} = V_{OD1} - V_{OD2}$$

Figure 9. Output Offset Voltage

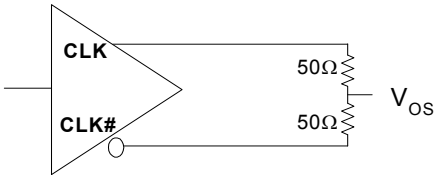
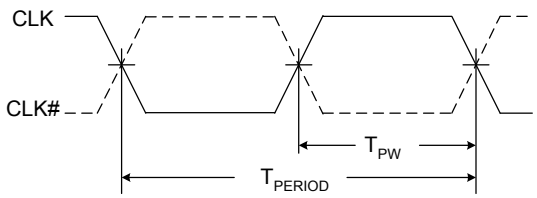


Figure 10. Duty Cycle Timing



$$T_{DC} = \frac{T_{PW}}{T_{PERIOD}}$$

Figure 11. Output Rise and Fall Time

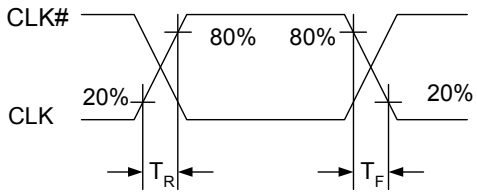
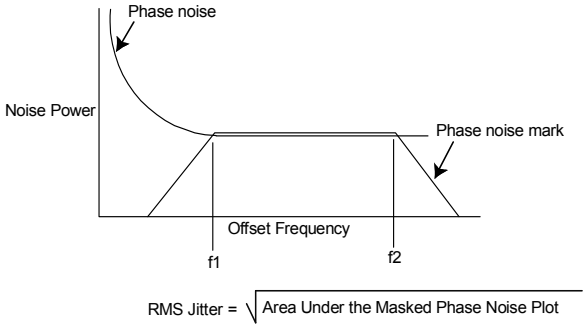
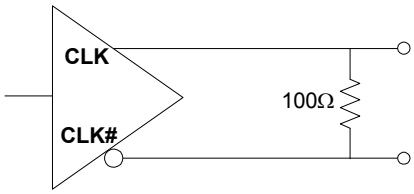


Figure 12. RMS Phase Jitter



Termination Circuits

Figure 13. LVDS Termination



Notes
9. Device configuration details are described in the Standard and Application-Specific Factory Configurations table on page 2.
10. "xxx" indicates factory programmed parts based on customer specific configuration. For more details, contact your local Cypress FAE or Sales Representative.

Ordering Information

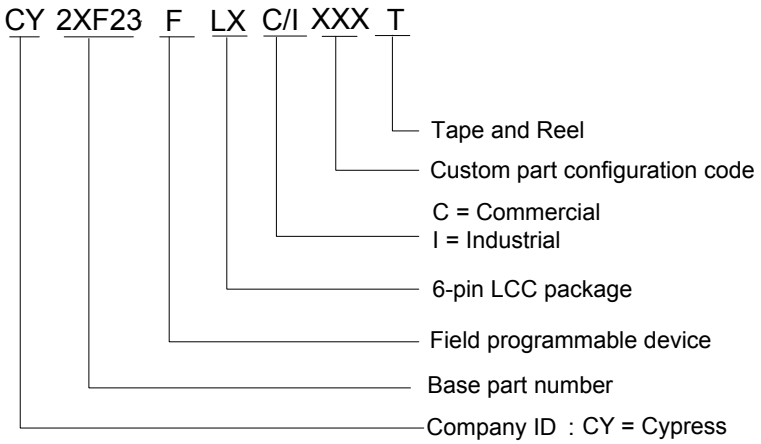
Part Number	Configuration	Package Description	Product Flow
Pb-free			
CY2XF23FLXCT	Field-programmable	6-pin ceramic LCC surface mount device (SMD) - tape and reel	Commercial, 0°C to 70°C
CY2XF23FLXIT	Field-programmable	6-pin ceramic LCC SMD - tape and reel	Industrial, –40°C to 85°C
CY2XF23LXC001T[9]	Factory-configured	6-pin ceramic LCC SMD - tape and reel	Commercial, 0°C to 70°C
CY2XF23LXI625T[9]	Factory-configured	6-pin ceramic LCC SMD - tape and reel	Industrial, –40°C to 85°C

Some product offerings are factory-programmed customer-specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

Possible Configurations

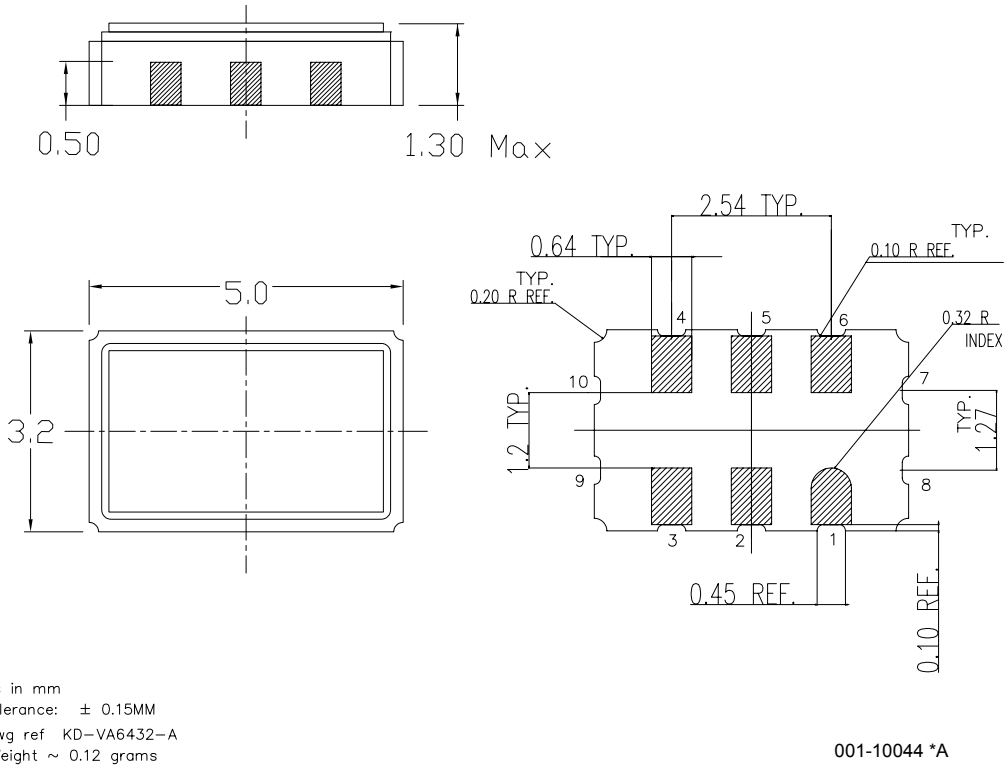
Part Number[10]	Configuration	Package Description	Product Flow
Pb-free			
CY2XF23LXCxxxT	Factory-configured	6-pin ceramic LCC SMD - tape and reel	Commercial, 0°C to 70°C
CY2XF23LXIxxxT	Factory-configured	6-pin ceramic LCC SMD - tape and reel	Industrial, –40°C to 85°C

Ordering Code Definitions



Package Drawings and Dimensions

Figure 14. 6-Pin 3.2x5.0 mm Ceramic LCC LZ06A



Dimensions in mm
General Tolerance: ± 0.15MM
Kyocera dwg ref KD-VA6432-A
Package Weight ~ 0.12 grams

001-10044 *A

Acronyms

Table 5. Acronyms Used in this Document

Acronym	Description
CMOS	complementary metal oxide semiconductor
ESD	electrostatic discharge
FAE	field application engineer
HBM	human body model
JEDEC	joint electron devices engineering council
LCC	leadless chip carrier
LVDS	Low-voltage differential signaling
OE	output enable
PCB	printed circuit board
PLL	phase-locked loop
RMS	root mean square
XO	crystal oscillator

Document History Page

Document Title: CY2XF23 High Performance LVDS Oscillator with Frequency Margining - I2C Control Document Number: 001-53145				
REV.	**ECN NO.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2704379	KVM/PYRS	05/11/2009	New data sheet
*A	2718898	WWZ	06/15/09	Minor ECN to post data sheet to external web
*B	2764787	KVM	09/18/09	Change V_{OD} limits from 250/450 mV to 247/454 mV Add max limit for T_R, T_F: 1.0 ns Change T_{LOCK} max from 10 ms to 5 ms Change T_{LSER} max from 10 ms to 1 ms
*C	2898585	KVM	03/24/2010	Updated Ordering Information Added Possible COnfigurations Updated Package DIagram
*D	2973338	CXQ	07/08/2010	Added Standard and Application-Specific Factory Configurations table on page 2. Added phase jitter specs for pre-defined configurations into the AC Electrical Specifications table (note 8 refers users to the new table on page 2 for typical specs). Added CY2XF23LXI001T and CY2XF23LXI625T devices to the Ordering Information table and added note 9 to reference the configuration descriptions for each new device. Changed all references to CyberClocksOnline software to CyClockWizard. Removed section on phase noise vs jitter SW optimization. Changed description of Word Select feature from default Word 0 to user-defined.

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