LXT9761/62/63/81/82 PHY Transceivers

Specification Update

March 2001

Notice: The LXT9761/81, LXT9762/82, and LXT9763 Multi-Port 10/100 PHY Transceivers may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 249356-002

Contents

Revision History

Date	Version	Page #	Description
March 20, 2001	002	-	Removed pre-production Stepping Errata.
		10	Updated "Markings" table with Manufacturer's Revision Code information.
January 15, 2001	001	-	Converted to Intel format (no technical or material changes).
August 17, 2000	4.4†	11 -16	Added Errata 1, 2, and 3.
May 16, 2000	4.3†	10	Change trace codes for Stepping 6.
March 29, 2000	4.2†	12	Added Errata 4.
† Level One document version number. As of January 15, 2001, this document replaces the Level One document.			

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
LXT9761/9781 — Fast Ethernet 10/100 Multi-Port Transceiver with RMII Datasheet	249048-001
LXT9761/62/63/81/82 Design and Layout Guide Application Note	249014-001
LXT9762/9782 Fast Ethernet 10/100 Multi-Port Transceiver with Serial MII Datasheet	249039-001
LXT9763 Fast Ethernet 10/100 Hex Transceiver with Full MII Datasheet	249110-001
LXD9763 Demo Board - Hex PHY with Standard MII	249350-001
LXD9781 BGA Demo Board with FPGAs for RMII-to-MII Conversion Developer Manual	249044-001
LXD9781 PQFP Demo Board with FPGAs for RMII-to-MII Conversion Developer Manual	249043-001
BGA Demo Board with FPGAs for SMII-to-MII Conversion Developer Manual	249051-001

Nomenclature

Errata are design defects or errors. These may cause the LXT9761/81, LXT9762/82, and LXT9763 Multi-Port 10/100 PHY Transceivers' behaviors to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the LXT9761/81, LXT9762/82, and LXT9763 Multi-Port 10/100 PHY Transceivers product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Specification Clarification applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in stepping indicated. Specification Change or Specification Clarification does not apply to this stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings		Page	Status	ERRATA
	6	7			
1	X		11	Fixed	“100M External Loopback Using Short Cable Length”
2	X		11	Fixed	“10BASE-T Data Inversion”
3	X		11	Fixed	“Power Cycling and JTAG TRST Reset Pin”
4	X		12	Fixed	“Incorrect Display of Activity LED”

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

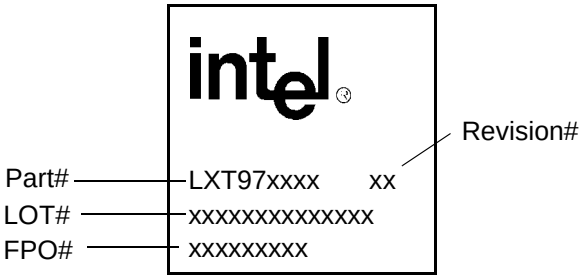
No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

Identification Information

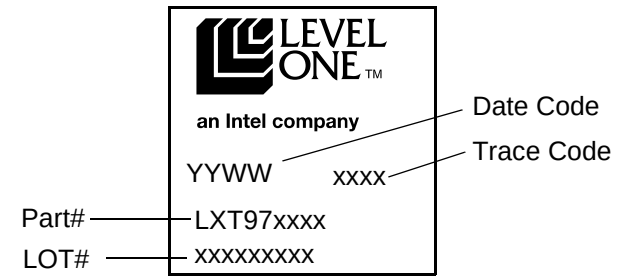
Markings



The silicon stepping in the LXT97xx Data Sheets is referred to as “Manufacturer’s Revision Number.” The silicon stepping number may be read by software from Register 3, bits 3:0 in the LXT97xx transceivers.

Stepping	Revision Number[1]	Trace Codes[2]	Manufacturer’s Revision Number[3]	Notes
6	A9, B2, C3	H*x*9*x*, W*x*K*x*, 4*x*T*x*	0110	
7	A11, C4	H*x*2*x*, 4*x*U*x*	0111	

1. Revision numbers listed on the same line are the same product stepping, but are produced at different fabrication facilities.
2. *x* indicates an insignificant variable.
3. This value is from register bits 3.3:0. Please see the LXT97xx data sheets for more information.



Errata

1. 100M External Loopback Using Short Cable Length

Problem: In applications that require a short external looping plug (looping TPFO to TPFI) with cable lengths typically less than 2 feet, a link problem may occur.

Implication: During external loopback operations that require line-loop length less than 2 feet, the LXT9761/62/63/81/82 input-receiver reference levels may incorrectly slice the twisted-pair signal, causing a loss of link.

Workaround: In applications that require a short cable length or a plug to externally loop the TPFO to the TPFI pins, Register 27, bit 3 should be set to 1.

Normal operation of the transceiver does not require that Register 27.3 be set to 1.

Status: Fixed in silicon Stepping 7.

2. 10BASE-T Data Inversion

Problem: If jitter on the twisted-pair data occurs within a certain time window relative internally to the DPLL Reference Clk and remains constant, inverted RxData can occur.

Implication: When the receive twisted-pair data jitters, the LXT9761/62/63/81/82 devices may pass errored data to the Reconciliation Sublayer. This errored data would be calculated as CRC errors at the MAC and the RXER signal/bit would be active.

Workaround: None.

Status: Fixed in silicon Stepping 7.

3. Power Cycling and JTAG $\overline{\text{TRST}}$ Reset Pin

Problem: Power-on cycling may cause the LXT9761/62/63/81/82 devices to hang in an unknown state due to the improper reset of some internal JTAG control flip-flops.

Implication: Some internal JTAG flip-flops may not be reset properly, which can cause the input and output steering muxes to be selected incorrectly. This incorrect selection may disable any of the digital, MII signal outputs and inputs.

Workaround: Designs not currently using JTAG should tie the $\overline{\text{TRST}}$ pin directly to GND.

Designs using the 5-signal option should tie the $\overline{\text{TRST}}$ pin to GND through a resistor. Suggested value for this resistor is 20 kΩ. A 20 kΩ resistor to GND is strong enough to pull down the internal, weak pull up to a logic 0 for normal operation. This pull down will also allow a JTAG tap controller to operate successfully and overcome the pull-up and pull-down resistors.

Designs using the 4-signal option and not using the $\overline{\text{TRST}}$ pin for reset should use a 20 kΩ pull-down resistor from $\overline{\text{TRST}}$ to GND and control the JTAG $\overline{\text{TRST}}$ pin accordingly.

Status: Fixed in silicon Stepping 7.

4. Incorrect Display of Activity LED

Problem: Under certain traffic conditions the Port Activity LED indicates activity with a slow blinking operation.

This occurs when a port, linked in full-duplex mode with Pulse Stretching enabled, is transmitting and receiving traffic having the same packet size and inter-packet gap (IPG) for an extended period of time.

Normal indication would be for the Activity LED to remain active when transmitting and receiving continuously.

If either packet size or IPG is altered, the Activity LED resumes normal operation.

Implication: The Activity LED indication may not match the traffic rate at the port. Only the Activity LED behavior is affected. Transmit Status and Receive Status LED functionality are not affected.

The Activity LED operation has no impact on data reliability on the port.

Workaround: Possible workarounds include:

- Use Transmit Status or Receive Status instead of Activity as the LED indication.
- Logically ‘OR’ Transmit Status and Receive Status to generate an Activity indicator. This workaround requires external hardware to complete the ‘OR’ function.
- Add external pulse stretching via a PLD while disabling on-chip pulse stretching via Register 20 (20.1 = 0). This workaround requires external hardware and manageability via the MDIO interface. Also, because pulse stretching is global to the device, external logic would need to be added for any LED signal which requires stretching.
- Display both Transmit Status and Receive Status individually.

Status: Fixed in silicon Stepping 7.

Specification Changes

There are no specification changes.

Specification Clarifications

There are no specification clarifications.

Documentation Changes

There are no documentation changes.

Addenda

1. 100BASE-TX Receive Jitter Tolerance

Description: If a receive-link partner operating in 100BASE-TX generates transmitted, low-frequency jitter greater than the IEEE standard, the LXT9761/62/63/81/82 device may produce errors within the Reconciliation Sublayer, which can result in failure to link or to sustain link. The LXT9761/62/63/81/82 devices will be enhanced to allow greater margin to the IEEE standard. The identified change should allow greater design flexibility; however, customers are advised that reliance on such out-of-margin performance is at their own risk.

Status: Implemented in silicon Stepping 7.

2. 10BASE-T Jitter Tolerance

Description: In some 10BASE-T input jitter applications, the LXT9761/62/63/81/82 device margin may be close to the IEEE standard for input jitter tolerance. The LXT9761/62/63/81/82 devices will be enhanced to be optimally centered for 10BASE-T input jitter tolerance. The identified change should allow greater design flexibility; however, customers are advised that reliance on such out-of-margin performance is at their own risk.

Status: Implemented in silicon Stepping 7.