National Semiconductor

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DS91D180/DS91C180

100 MHz M-LVDS Line Driver/Receiver Pair

General Description

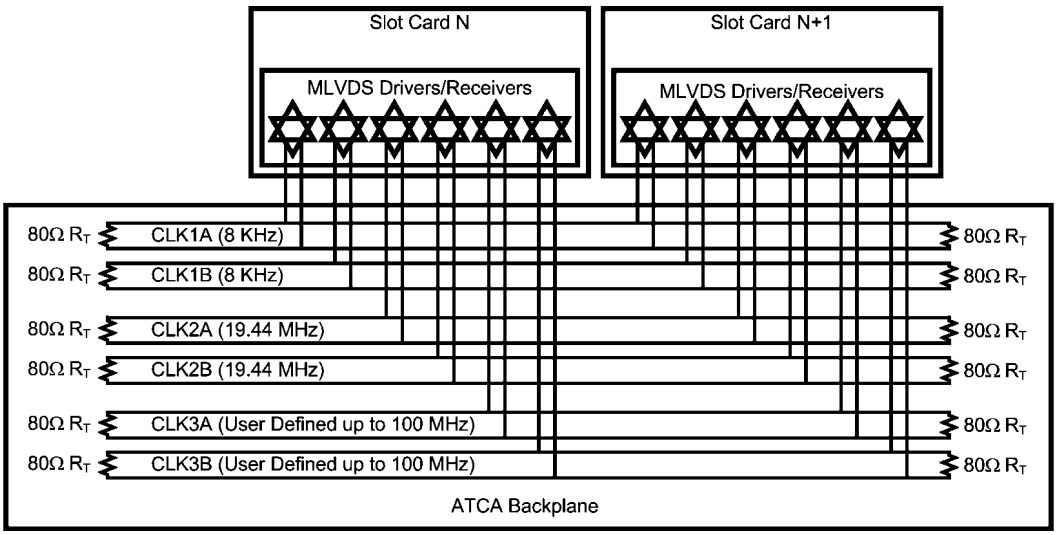
The DS91D180 and DS91C180 are 100 MHz M-LVDS (Multipoint Low Voltage Differential Signaling) line driver/receiver pairs designed for applications that utilize multipoint networks (e.g. clock distribution in ATCA and uTCA based systems). M-LVDS is a new bus interface standard (TIA/EIA-899) optimized for multidrop networks. Controlled edge rates, tight input receiver thresholds and increased drive strength are sone of the key enhancments that make M-LVDS devices an ideal choice for distributing signals via multipoint networks.

The DS91D180/DS91C180 driver input accepts LVTTL/LVCMOS signals and converts them to differential M-LVDS signal levels. The DS91D180/DS91C180 receiver accepts low voltage differential signals (LVDS, B-LVDS, M-LVDS, LV-PECL and CML) and converts them to 3V LVCMOS signals. The DS91D180 device has a M-LVDS type 1 receiver input with no offset.The DS91C180 device has a type 2 receiver input which enable failsafe functionality.

Features

- DC to 100+ MHz / 200+ Mbps low power, low EMI operation
- Optimal for ATCA, uTCA clock distribution networks
- Meets or exceeds TIA/EIA-899 M-LVDS Standard
- Wide Input Common Mode Voltage for Increased Noise Immunity
- DS91D180 has type 1 receiver input
- DS91C180 has type 2 receiver input for fail-safe functionality
- Industrial temperature range
- Space saving SOIC-14 package (JEDEC MS-012)

Typical Application in an ATCA Clock Distribution Network



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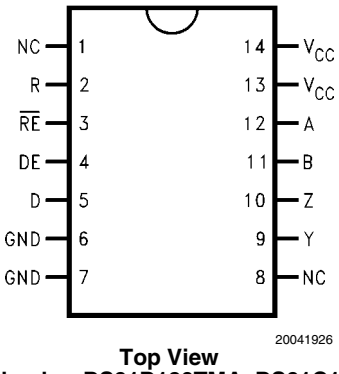
Connection Diagram



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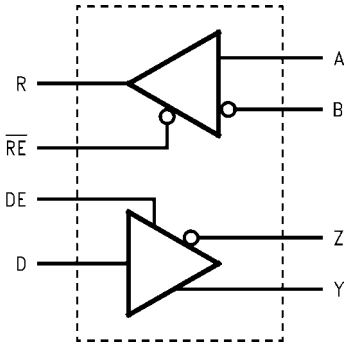
Top View
Order Number DS91D180TMA, DS91C180TMA
See NS Package Number M14A

Logic Diagram



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Ordering Information

Order Number	Receiver Input	Function	Package Type
DS91D180TMA	type 1	Data (0V threshold receiver)	SOIC/M14A
DS91C180TMA	type 2	Control (offset fail-safe receiver)	SOIC/M14A

M-LVDS Receiver Types

The EIA/TIA-899 M-LVDS standard specifies two different types of receiver input stages. A type 1 receiver has a conventional threshold that is centered at the midpoint of the input amplitude, $V_{ID}/2$. A type 2 receiver has a built in offset that is 100mV greater than $V_{ID}/2$. The type 2 receiver offset acts as a failsafe circuit where open or short circuits at the input will always result in the output stage being driven to a low logic state.

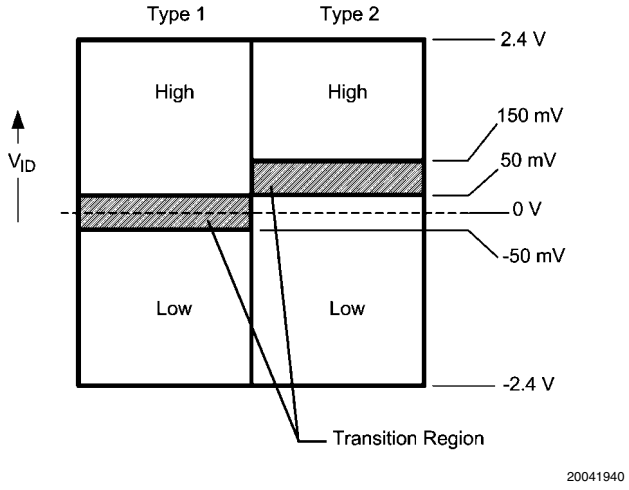

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FIGURE 1. M-LVDS Receiver Input Thresholds

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	−0.3V to +4V
Control Input Voltages	−0.3V to (V_{CC} + 0.3V)
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltages	−1.8V to +4.1V
Receiver Input Voltages	−1.8V to +4.1V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation at +25°C	
SOIC Package	1.1 W
Derate SOIC Package	8.8 mW/°C above +25°C
Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
θ_{JA}	113.7 °C/W
θ_{JC}	36.9 °C/W
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
ESD Ratings:	
(HBM 1.5kΩ, 100pF)	≥ 5 kV
(EIAJ 0Ω, 200pF)	≥ 250 V
(CDM 0Ω, 0pF)	≥ 1000 V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	3.0	3.3	3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	−1.4		+3.8	V
Differential Input Voltage V_{ID}			2.4	V
High Level Input Voltage V_{IH}	2.0		V_{CC}	V
Low Level Input Voltage V_{IL}	0		0.8	V
Operating Free Air Temperature T_A	−40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 2*, *Note 3*, *Note 4*, *Note 8*)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
M-LVDS Driver							
$\lvert V_{YZ}\rvert$	Differential output voltage magnitude	R_L = 50Ω, C_L = 5pF *Figure 2* and *Figure 4*		480		650	mV
ΔV_{YZ}	Change in differential output voltage magnitude between logic states			−50	0	+50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	R_L = 50Ω, C_L = 5pF *Figure 2* and *Figure 3*		0.3	1.8	2.1	V
$\lvert\Delta V_{OS(SS)}\rvert$	Change in steady-state common-mode output voltage between logic states			0		+50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage	($V_{OS(pp)}$ @ 500KHz clock)			143		mV
$V_{Y(OC)}$	Maximum steady-state open-circuit output voltage	*Figure 5*		0		2.4	V
$V_{Z(OC)}$	Maximum steady-state open-circuit output voltage			0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	R_L = 50Ω, C_L = 5pF, C_D = 0.5pF *Figure 7* and *Figure 8* (*Note 9*)				$1.2V_{SS}$	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output			$-0.2V_S$ S			V
I_{IH}	High-level input current (LVTTL inputs)	V_{IH} = 2.0V		-15		15	µA
I_{IL}	Low-level input current (LVTTL inputs)	V_{IL} = 0.8V		-15		15	µA
V_{IKL}	Input Clamp Voltage (LVTTL inputs)	I_{IN} = -18 mA		-1.5			V
I_{OS}	Differential short-circuit output current	*Figure 6*		-43		43	mA
M-LVDS Receiver							
V_{IT+}	Positive-going differential input voltage threshold	See Function Tables	Type 1		20	50	mV
			Type 2		94	150	mV
V_{IT-}	Negative-going differential input voltage threshold	See Function Tables	Type 1	−50	20		mV
			Type 2	50	94		mV
V_{OH}	High-level output voltage	I_{OH} = −8mA		2.4	2.7		V
V_{OL}	Low-level output voltage	I_{OL} = 8mA			0.28	0.4	V
I_{OZ}	TRI-STATE output current	V_O = 0V or 3.6V		−10		10	µA
I_{OSR}	Short circuit Rrceiver output current (LVTTL Output)	V_O = 0V		-90	-48		mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
M-LVDS Bus (Input and Output) Pins						
I_A, I_Y	Receiver input or driver high-impedance output current	$V_{A,Y}$ = 3.8V, $V_{B,Z}$ = 1.2V, DE = GND			32	µA
		$V_{A,Y}$ = 0V or 2.4V, $V_{B,Z}$ = 1.2V, DE = GND	−20		+20	µA
		$V_{A,Y}$ = −1.4V, $V_{B,Z}$ = 1.2V, DE = GND	−32			µA
I_B, I_Z	Receiver input or driver high-impedance output current	$V_{B,Z}$ = 3.8V, $V_{A,Y}$ = 1.2V, DE = GND			32	µA
		$V_{B,Z}$ = 0V or 2.4V, $V_{A,Y}$ = 1.2V, DE = GND	−20		+20	µA
		$V_{B,Z}$ = −1.4V, $V_{A,Y}$ = 1.2V, DE = GND	−32			µA
I_{AB}, I_{YZ}	Receiver input or driver high-impedance output differential current ($I_A - I_B$ or $I_Y - I_Z$)	$V_{A,Y} = V_{B,Z}$, −1.4V ≤ V ≤ 3.8V, DE = GND	−4		+4	µA
$I_{A(OFF)}$, $I_{Y(OFF)}$	Receiver input or driver high-impedance output power-off current	$V_{A,Y}$ = 3.8V, $V_{B,Z}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V			32	µA
		$V_{A,Y}$ = 0V or 2.4V, $V_{B,Z}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V	−20		+20	µA
		$V_{A,Y}$ = −1.4V, $V_{B,Z}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V	−32			µA
$I_{B(OFF)}$, $I_{Z(OFF)}$	Receiver input or driver high-impedance output power-off current	$V_{B,Z}$ = 3.8V, $V_{A,Y}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V			32	µA
		$V_{B,Z}$ = 0V or 2.4V, $V_{A,Y}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V	−20		+20	µA
		$V_{B,Z}$ = −1.4V, $V_{A,Y}$ = 1.2V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V	−32			µA
$I_{AB(OFF)}$, $I_{YZ(OFF)}$	Receiver input or driver high-impedance output power-off differential current ($I_{A(OFF)} - I_{B(OFF)}$ or $I_{Y(OFF)} - I_{Z(OFF)}$)	$V_{A,Y} = V_{B,Z}$, −1.4V ≤ V ≤ 3.8V, DE = 0V, 0V ≤ V_{CC} ≤ 1.5V	−4		+4	µA
C_A, C_B	Receiver input capacitance	V_{CC} = OPEN		5.1		pF
C_Y, C_Z	Driver output capacitance			8.5		pF
C_{AB}	Receiver input differential capacitance			2.5		pF
C_{YZ}	Driver output differential capacitance			5.5		pF
$C_{A/B}$, $C_{Y/Z}$	Receiver input or driver output capacitance balance (C_A/C_B or C_Y/C_Z)			1.0		
SUPPLY CURRENT (V_{CC})						
I_{CCD}	Driver Supply Current	R_L = 50Ω, DE = V_{CC}, $\overline{RE}$ = V_{CC}		17	29.5	mA
I_{CCZ}	TRI-STATE Supply Current	DE = GND, $\overline{RE}$ = V_{CC}		7	9.0	mA
I_{CCR}	Receiver Supply Current	DE = GND, $\overline{RE}$ = GND		14	18.5	mA
I_{CCB}	Supply Current, Driver and Receiver Enabled	DE = V_{CC}, $\overline{RE}$ = GND		20	29.5	mA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (*Note 3*, *Note 8*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AC SPECIFICATION						
t_{PLH}	Differential Propagation Delay Low to High	R_L = 50Ω, C_L = 5 pF,	1.0	3.4	5.5	ns
t_{PHL}	Differential Propagation Delay High to Low	C_D = 0.5 pF	1.0	3.1	5.5	ns
t_{SKD1} ($t_{sk(p)}$)	Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$ (*Note 5*, *Note 9*)	*Figure 7* and *Figure 8*		300	420	ps
t_{SKD3}	Part-to-Part Skew (*Note 6*, *Note 9*)				1.9	ns
t_{TLH} (t_r)	Rise Time (*Note 9*)		1.0	1.8	3.0	ns
t_{THL} (t_f)	Fall Time (*Note 9*)		1.0	1.8	3.0	ns
t_{PZH}	Enable Time (Z to Active High)	R_L = 50Ω, C_L = 5 pF,			8	ns
t_{PZL}	Enable Time (Z to Active Low)	C_D = 0.5 pF			8	ns
t_{PLZ}	Disable Time (Active Low to Z)	*Figure 9* and *Figure 10*			8	ns
t_{PHZ}	Disable Time (Active High to Z)				8	ns
t_{JIT}	Random Jitter, RJ (*Note 9*)	100MHz clock pattern (*Note 7*)		2.5	5.5	psrms
f_{MAX}	Maximum Data Rate		200			Mbps
RECEIVER AC SPECIFICATION						
t_{PLH}	Propagation Delay Low to High	C_L = 15 pF	2.0	4.7	7.5	ns
t_{PHL}	Propagation Delay High to Low	*Figure 11 Figure 12*and *Figure 13*	2.0	5.3	7.5	ns
t_{SKD1} ($t_{sk(p)}$)	Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$ (*Note 5*, *Note 9*)			0.6	1.9	ns
t_{SKD3}	Part-to-Part Skew (*Note 6*, *Note 9*)				1.5	ns
t_{TLH} (t_r)	Rise Time (*Note 9*)		0.5	1.2	3.0	ns
t_{THL} (t_f)	Fall Time (*Note 9*)		0.5	1.2	3.0	ns
t_{PZH}	Enable Time (Z to Active High)	R_L = 500Ω, C_L = 15 pF			10	ns
t_{PZL}	Enable Time (Z to Active Low)	*Figure 14* and *Figure 15*			10	ns
t_{PLZ}	Disable Time (Active Low to Z)				10	ns
t_{PHZ}	Disable Time (Active High to Z)				10	ns
f_{MAX}	Maximum Data Rate		200			Mbps

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 3.3V and T_A = 25°C.

Note 4: The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this datasheet.

Note 5: t_{SKD1}, $\lvert t_{PLHD} - t_{PHLD} \rvert$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 6: t_{SKD3}, Part-to-Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Note 7: Stimulus and fixture jitter has been subtracted.

Note 8: C_L includes fixture capacitance and C_D includes probe capacitance.

Note 9: Not production tested. Guaranteed by a statistical analysis on a sample basis at the time of characterization.

Test Circuits and Waveforms

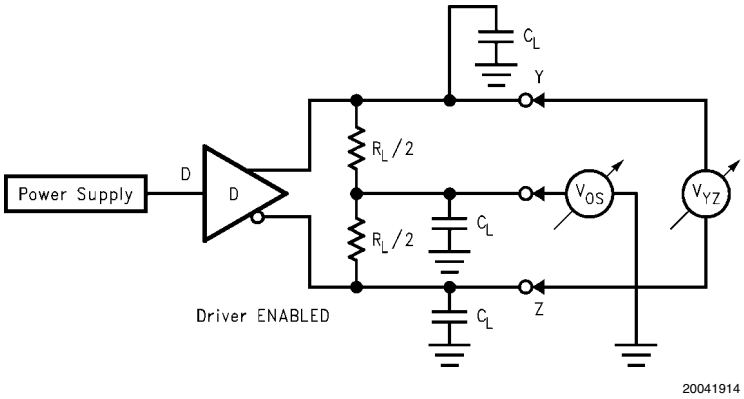


FIGURE 2. Differential Driver Test Circuit

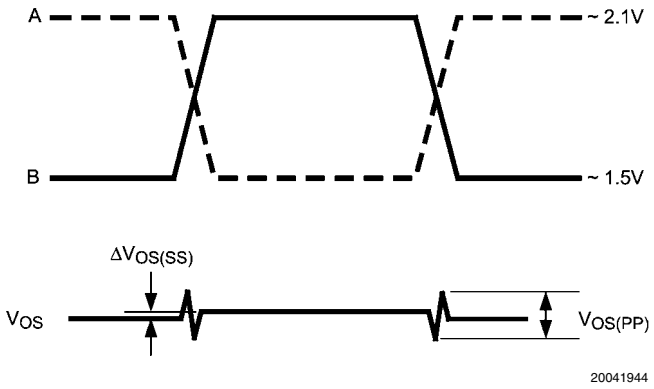


FIGURE 3. Differential Driver Waveforms

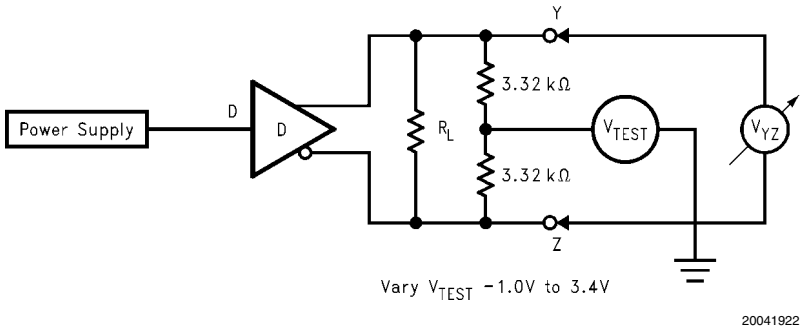


FIGURE 4. Differential Driver Full Load Test Circuit

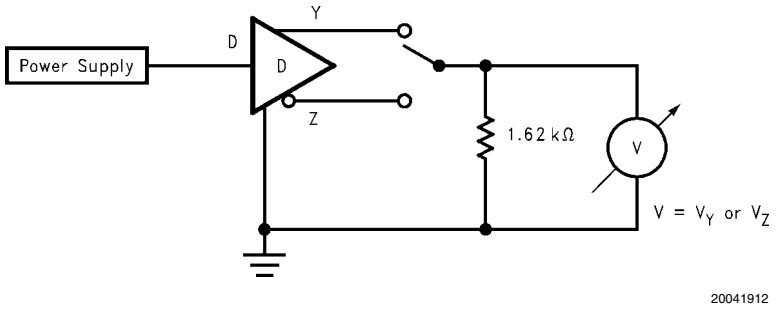


FIGURE 5. Differential Driver DC Open Test Circuit

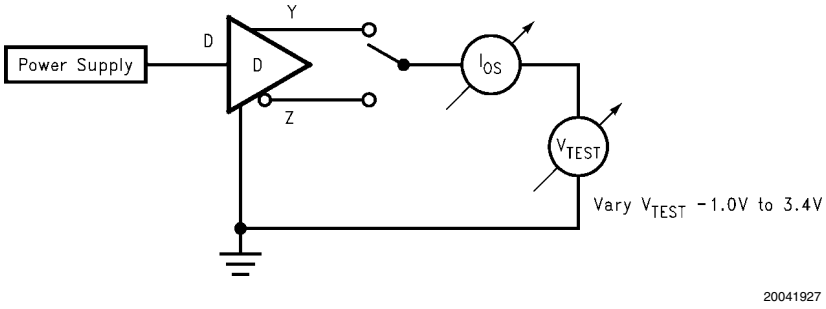


FIGURE 6. Differential Driver Short-Circuit Test Circuit

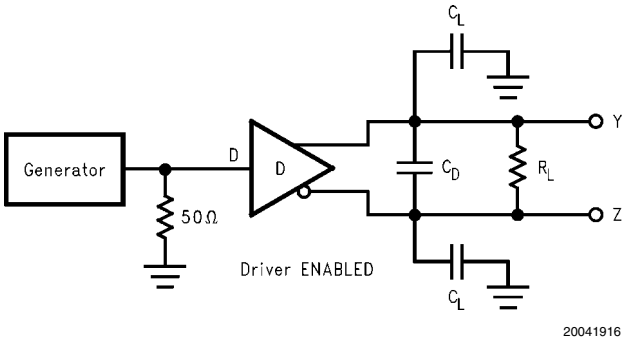


FIGURE 7. Driver Propagation Delay and Transition Time Test Circuit

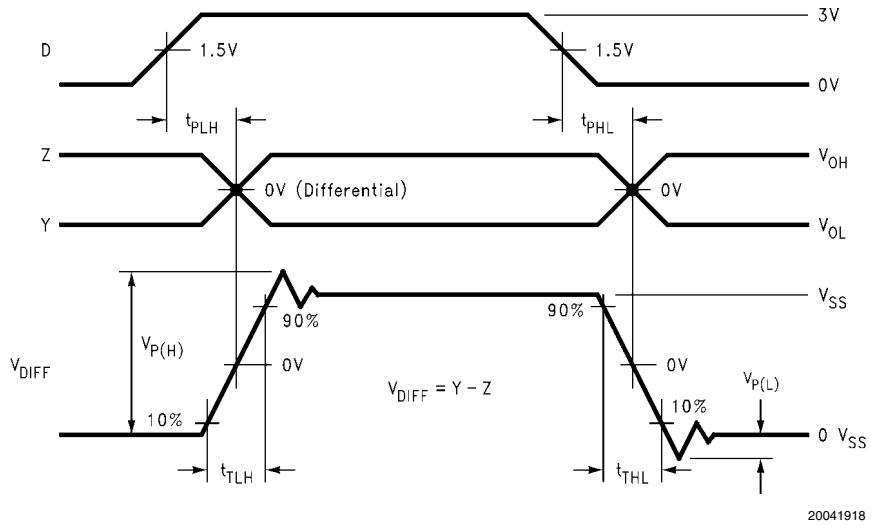


FIGURE 8. Driver Propagation Delays and Transition Time Waveforms

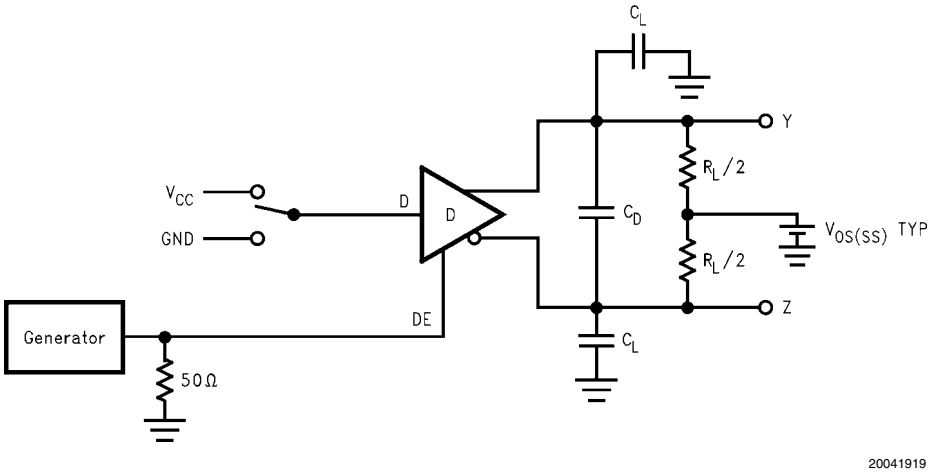


FIGURE 9. Driver TRI-STATE Delay Test Circuit

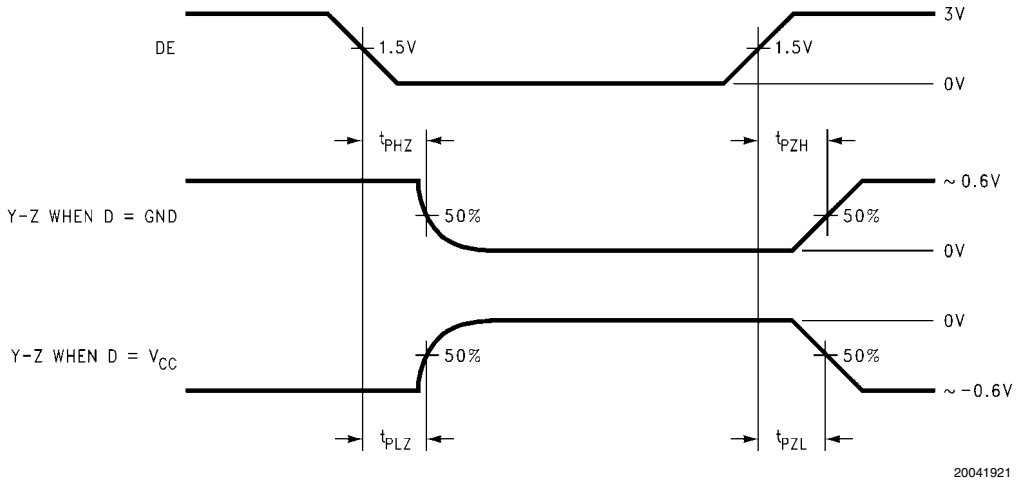


FIGURE 10. Driver TRI-STATE Delay Waveforms

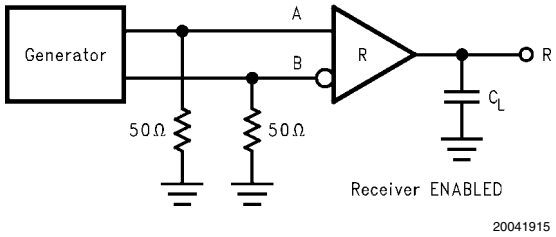


FIGURE 11. Receiver Propagation Delay and Transition Time Test Circuit

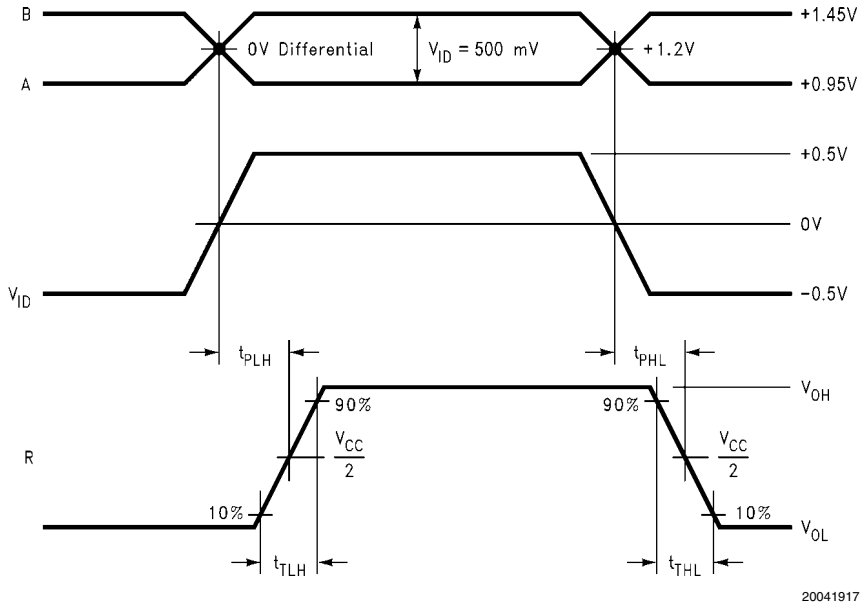


FIGURE 12. Type 1 Receiver Propagation Delay and Transition Time Waveforms

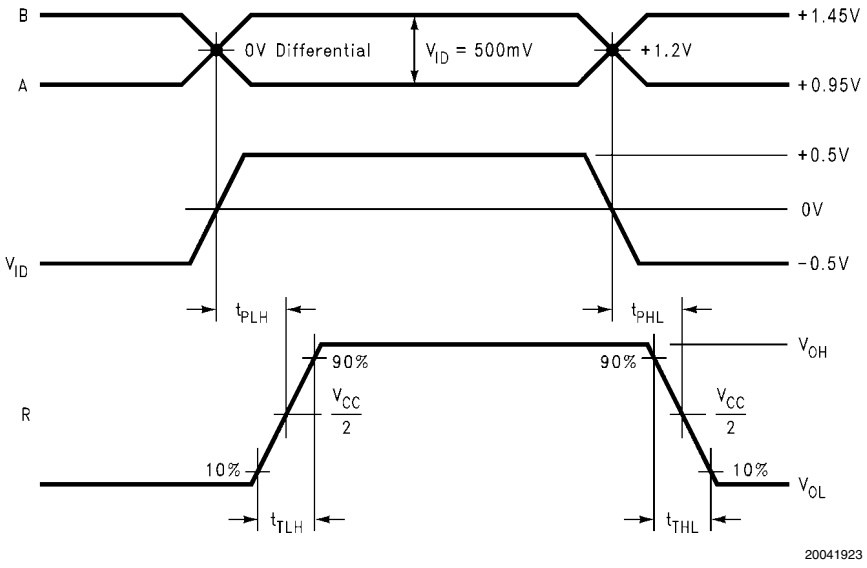


FIGURE 13. Type 2 Receiver Propagation Delay and Transition Time Waveforms

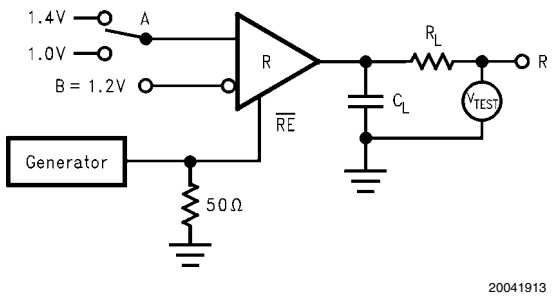


FIGURE 14. Receiver TRI-STATE Delay Test Circuit

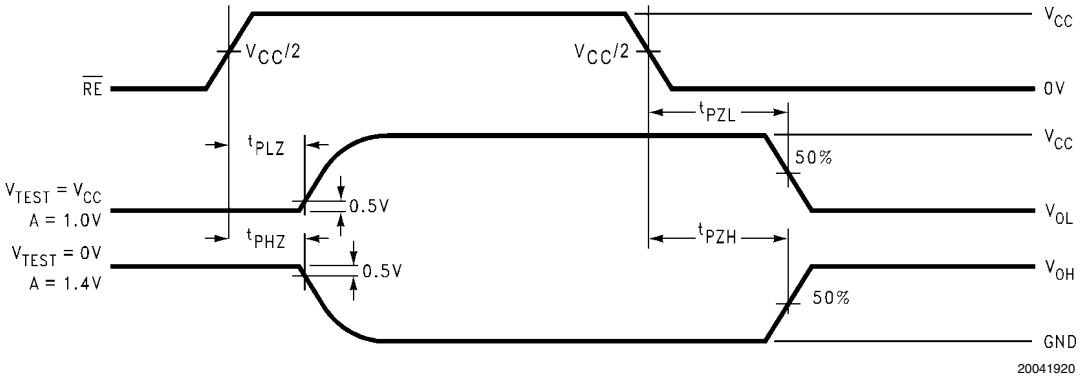


FIGURE 15. Receiver TRI-STATE Delay Waveforms

Function Tables

DS91D180/DS91C180 Transmitting

Inputs		Outputs	
DE	D	Z	Y
2.0V	2.0V	L	H
2.0V	0.8V	H	L
0.8V	X	Z	Z

X — Don't care condition
Z — High impedance state

DS91D180 Receiving

Inputs		Output
$\overline{RE}$	A – B	R
0.8V	≥ +0.05V	H
0.8V	≤ −0.05V	L
0.8V	0V	X
2.0V	X	Z

X — Don't care condition
Z — High impedance state

DS91C180 Receiving

Inputs		Output
$\overline{RE}$	A – B	R
0.8V	≥ +0.15V	H
0.8V	≤ +0.05V	L
0.8V	0V	L
2.0V	X	Z

X — Don't care condition
Z — High impedance state

DS91D180 Receiver Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	−2.400V	1.200V	L
3.800V	3.750V	0.050V	3.775V	H
3.750V	3.800V	−0.050V	3.775V	L
−1.400V	−1.350V	−0.050V	−1.375V	H
−1.350V	−1.400V	0.050V	−1.375V	L

H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE}$ = L)

DS91C180 Receiver Input Threshold Test Voltages

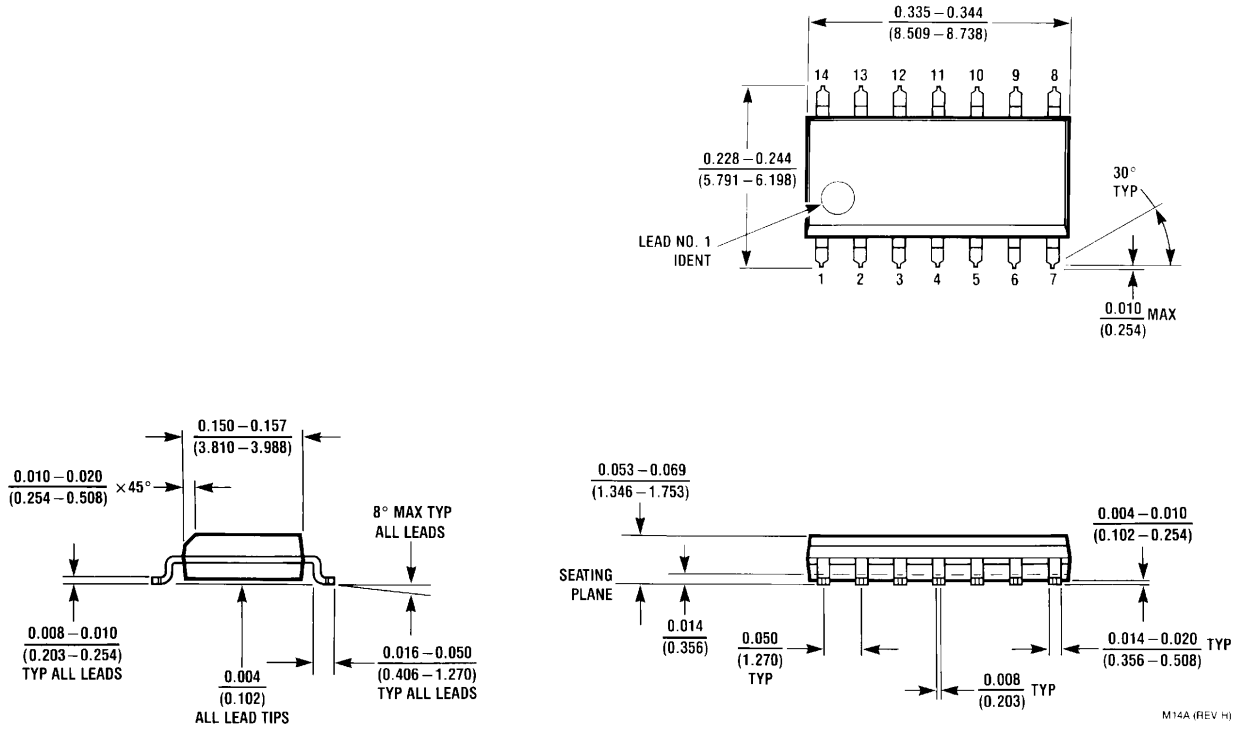
Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	−2.400V	1.200V	L
3.800V	3.650V	0.150V	3.725V	H
3.800V	3.750V	0.050V	3.775V	L
−1.250V	−1.400V	0.150V	−1.325V	H
−1.350V	−1.400V	0.050V	−1.375V	L

H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE}$ = L)

Pin Descriptions

Pin No.	Name	Description
1, 8	NC	No connect.
2	R	Receiver output pin
3	$\overline{RE}$	Receiver enable pin: When $\overline{RE}$ is high, the receiver is disabled. When $\overline{RE}$ is low or open, the receiver is enabled.
4	DE	Driver enable pin: When DE is low, the driver is disabled. When DE is high, the driver is enabled.
5	D	Driver input pin
6, 7	GND	Ground pin
9	Y	Non-inverting driver output pin
10	Z	Inverting driver output pin
11	B	Inverting receiver input pin
12	A	Non-inverting receiver input pin
13, 14	V_{CC}	Power supply pin, +3.3V ± 0.3V

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS91D180TMA, DS91C180TMA
See NS package Number M14A

Notes

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