

## ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E

### FEATURES

- TIA/EIA RS-485/RS-422 compliant
- $\pm 15$  kV ESD protection on RS-485 input/output pins
- Data rates
  - ADM3483E/ADM3488E: 250 kbps
  - ADM3486E: 2.5 Mbps
  - ADM3490E/ADM3491E: 12 Mbps
- Half- and full-duplex options
- Up to 32 nodes on the bus
- Receiver open-circuit, fail-safe design
- Low power shutdown current
  - (ADM3483E/ADM3486E/ADM3491E only)
- Outputs high-Z when disabled or powered off
- Common-mode input range:  $-7$  V to  $+12$  V
- Thermal shutdown and short-circuit protection
- Industry-standard 75176 pinout
- 8-lead and 14-lead narrow SOIC packages

### APPLICATIONS

- Power/energy metering
- Telecommunications
- EMI-sensitive systems
- Industrial control
- Local area networks

### GENERAL DESCRIPTION

The ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E are 3.3 V, low power data transceivers with  $\pm 15$  kV ESD protection suitable for full- and half-duplex communication on multipoint bus transmission lines. They are designed for balanced data transmission, and they comply with TIA/EIA standards RS-485 and RS-422. The ADM3483E/ADM3486E are half-duplex transceivers that share differential lines and have separate enable inputs for the driver and receiver. The full-duplex ADM3488E/ADM3490E/ADM3491E transceivers have dedicated differential line driver outputs and receiver inputs. The ADM3491E also features separate enable inputs for the driver and receiver.

The devices have a  $12\text{ k}\Omega$  receiver input impedance, which allows up to 32 transceivers on a bus. Because only one driver should be enabled at any time, the output of a disabled or powered-down driver is tristated to avoid overloading the bus.

### FUNCTIONAL BLOCK DIAGRAMS

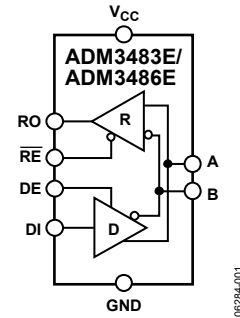


Figure 1.

06284-001

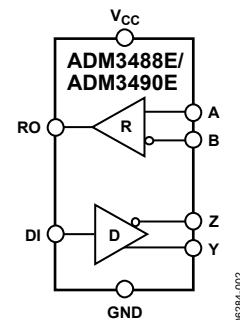


Figure 2.

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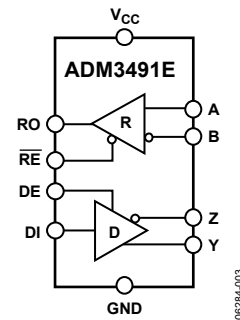


Figure 3.

06284-003

(continued on Page 3)

#### Rev. A

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## REVISION HISTORY

### 10/06—Rev. 0 to Rev. A

Added ADM3483E and ADM3488E .....	Universal
Changes to Figure 1 and Figure 2 .....	1
Inserted Table 3 .....	5
Changes to Figure 4 and Figure 5 .....	8
Inserted Figure 28 and Figure 29 .....	13
Changes to Figure 31 and Figure 32 .....	16
Changes to Figure 34 .....	17
Updated Outline Dimensions .....	18
Changes to Ordering Guide .....	18

### 8/06—Revision 0: Initial Version

# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E

## GENERAL DESCRIPTION

(continued from Page 1)

The driver outputs of the ADM3483E/ADM3486E/ADM3488E are slew rate limited, in order to reduce EMI and data errors caused by reflections from improperly terminated buses. The receiver has a fail-safe feature that ensures a logic high output when the inputs are floating.

Excessive power dissipation caused by bus contention or by output shorting is prevented with a thermal shut-down circuit.

The parts are fully specified over the industrial temperature range and are available in 8-lead and 14-lead narrow SOIC packages.

**Table 1. Selection Table**

Part No.	Guaranteed Data Rate (Mbps)	Supply Voltage (V)	Half/Full Duplex	Slew Rate Limited	Driver/Receiver Enable	±15 kV ESD Protection on Bus Pins	Pin Count
ADM3483E	0.25	3.0 to 3.6	Half	Yes	Yes	Yes	8
ADM3486E	2.5	3.0 to 3.6	Half	Yes	Yes	Yes	8
ADM3488E	0.25	3.0 to 3.6	Full	Yes	No	Yes	8
ADM3490E	12	3.0 to 3.6	Full	No	No	Yes	8
ADM3491E	12	3.0 to 3.6	Full	No	Yes	Yes	14

# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E

## SPECIFICATIONS

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2. ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DRIVER</b>						
Differential Outputs						
Differential Output Voltage	$V_{OD}$	2.0			V	$R_L = 100 \Omega$ (RS-422) (see Figure 7)
		1.5			V	$R_L = 54 \Omega$ (RS-485) (see Figure 7)
		1.5			V	$R_L = 60 \Omega$ (RS-485) (see Figure 8)
$\Delta V_{OD} $ for Complementary Output States <sup>1</sup>	$\Delta V_{OD}$			0.2	V	$R_L = 54 \Omega$ or $100 \Omega$ (see Figure 7)
Common-Mode Output Voltage	$V_{OC}$			3	V	$R_L = 54 \Omega$ or $100 \Omega$ (see Figure 7)
$\Delta V_{OC} $ for Complementary Output States <sup>1</sup>	$\Delta V_{OC}$			0.2	V	$R_L = 54 \Omega$ or $100 \Omega$ (see Figure 7)
Short-Circuit Output Current	$I_{OSD}$	-250			mA	$V_{OUT} = -7 \text{ V}$
				250	mA	$V_{OUT} = 12 \text{ V}$
Output Leakage (Y, Z) (ADM3491E Only)	$I_o$					
Normal Mode				20	$\mu\text{A}$	$DE = 0 \text{ V}$ , $\overline{RE} = 0 \text{ V}$ , $V_{CC} = 0 \text{ V}$ or $3.6 \text{ V}$ , $V_{OUT} = 12 \text{ V}$
		-20			$\mu\text{A}$	$DE = 0 \text{ V}$ , $\overline{RE} = 0 \text{ V}$ , $V_{CC} = 0 \text{ V}$ or $3.6 \text{ V}$ , $V_{OUT} = -7 \text{ V}$
Shutdown Mode				1	$\mu\text{A}$	$DE = 0 \text{ V}$ , $\overline{RE} = V_{CC}$ , $V_{CC} = 0 \text{ V}$ or $3.6 \text{ V}$ , $V_{OUT} = 12 \text{ V}$
		-1			$\mu\text{A}$	$DE = 0 \text{ V}$ , $\overline{RE} = V_{CC}$ , $V_{CC} = 0 \text{ V}$ or $3.6 \text{ V}$ , $V_{OUT} = -7 \text{ V}$
Logic Inputs						
Input High Voltage	$V_{IH}$	2.0			V	$DE, DI, \overline{RE}$
Input Low Voltage	$V_{IL}$			0.8	V	$DE, DI, \overline{RE}$
Logic Input Current	$I_{IN1}$			$\pm 2$	$\mu\text{A}$	$DE, DI, \overline{RE}$
<b>RECEIVER</b>						
Differential Inputs						
Differential Input Threshold Voltage	$V_{TH}$	-0.2		0.2	V	$-7 \text{ V} < V_{CM} < +12 \text{ V}$
Input Hysteresis	$\Delta V_{TH}$		50		mV	$V_{CM} = 0 \text{ V}$
Input Resistance (A, B)	$R_{IN}$	12			k $\Omega$	$-7 \text{ V} < V_{CM} < +12 \text{ V}$
Input Current (A, B)	$I_{IN2}$			1.0	mA	$DE = 0 \text{ V}$ , $V_{CC} = 0 \text{ V}$ or $3.6 \text{ V}$ , $V_{IN} = 12 \text{ V}$
		-0.8			mA	$DE = 0 \text{ V}$ , $V_{CC} = 0 \text{ V}$ or $3.6 \text{ V}$ , $V_{IN} = -7 \text{ V}$
RO Logic Output						
Output High Voltage	$V_{OH}$	$V_{CC} - 0.4$			V	$I_{OUT} = -1.5 \text{ mA}$ , $V_{ID} = 200 \text{ mV}$ (see Figure 9)
Output Low Voltage	$V_{OL}$			0.4	V	$I_{OUT} = 2.5 \text{ mA}$ , $V_{ID} = 200 \text{ mV}$ (see Figure 9)
Short-Circuit Output Current	$I_{OSR}$	$\pm 8$		$\pm 60$	mA	$0 \text{ V} < V_{RO} < V_{CC}$
Tristate Output Leakage Current	$I_{OZR}$			$\pm 1$	$\mu\text{A}$	$V_{CC} = 3.6 \text{ V}$ , $0 \text{ V} < V_{OUT} < V_{CC}$
<b>POWER SUPPLY</b>						
Voltage Range	$V_{CC}$	3.0		3.6	V	
Supply Current	$I_{CC}$		1.1	2.2	mA	No load, $DI = 0 \text{ V}$ or $V_{CC}$ , $DE = V_{CC}$ , $\overline{RE} = 0 \text{ V}$ or $V_{CC}$
			0.95	1.9	mA	No load, $DI = 0 \text{ V}$ or $V_{CC}$ , $DE = 0 \text{ V}$ , $\overline{RE} = 0 \text{ V}$
Shutdown Current	$I_{SHDN}$		0.002	1	$\mu\text{A}$	$DE = 0 \text{ V}$ , $\overline{RE} = V_{CC}$ , $DI = 0 \text{ V}$ or $V_{CC}$
<b>ESD PROTECTION</b>						
A, B, Y, Z Pins			$\pm 15$		kV	Human body model
All Pins Except A, B, Y, Z Pins			$\pm 4$		kV	Human body model

<sup>1</sup>  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in  $V_{OD}$  and  $V_{OC}$ , respectively, when DI input changes state.

# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E

## DRIVER TIMING SPECIFICATIONS

$V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**Table 3. ADM3483E/ADM3488E**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM DATA RATE		250			kbps	
DIFFERENTIAL OUTPUT DELAY	$t_{DD}$	600	900	1400	ns	$R_L = 60\ \Omega$ (see Figure 10)
DIFFERENTIAL OUTPUT TRANSITION TIME	$t_{TD}$	400	740	1200	ns	$R_L = 60\ \Omega$ (see Figure 10)
PROPAGATION DELAY						
From Low to High Level	$t_{PLH}$	700	930	1500	ns	$R_L = 27\ \Omega$ (see Figure 11)
From High to Low Level	$t_{PHL}$	700	930	1500	ns	$R_L = 27\ \Omega$ (see Figure 11)
$ t_{PLH} - t_{PHL} $ PROPAGATION DELAY SKEW <sup>1</sup>	$t_{PDS}$		$\pm 50$		ns	$R_L = 27\ \Omega$ (see Figure 11)
ENABLE/DISABLE TIMING (ADM3483E ONLY)						
Enable Time to Low Level	$t_{PZL}$		900	1300	ns	$R_L = 110\ \Omega$ (see Figure 13)
Enable Time to High Level	$t_{PZH}$		600	800	ns	$R_L = 110\ \Omega$ (see Figure 12)
Disable Time from Low Level	$t_{PLZ}$		50	80	ns	$R_L = 110\ \Omega$ (see Figure 13)
Disable Time from High Level	$t_{PHZ}$		50	80	ns	$R_L = 110\ \Omega$ (see Figure 12)
Enable Time from Shutdown to Low Level	$t_{PSL}$		1.9	2.7	$\mu\text{s}$	$R_L = 110\ \Omega$ (see Figure 13)
Enable Time from Shutdown to High Level	$t_{PSH}$		2.2	3.0	$\mu\text{s}$	$R_L = 110\ \Omega$ (see Figure 12)

<sup>1</sup> Measured on  $|t_{PLH}(Y) - t_{PHL}(Y)|$  and  $|t_{PLH}(Z) - t_{PHL}(Z)|$ .

$V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**Table 4. ADM3486E**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM DATA RATE		2.5			Mbps	
DIFFERENTIAL OUTPUT DELAY	$t_{DD}$	20	42	70	ns	$R_L = 60\ \Omega$ (see Figure 10)
DIFFERENTIAL OUTPUT TRANSITION TIME	$t_{TD}$	15	28	60	ns	$R_L = 60\ \Omega$ (see Figure 10)
PROPAGATION DELAY						
From Low to High Level	$t_{PLH}$	20	42	75	ns	$R_L = 27\ \Omega$ (see Figure 11)
From High to Low Level	$t_{PHL}$	20	42	75	ns	$R_L = 27\ \Omega$ (see Figure 11)
$ t_{PLH} - t_{PHL} $ PROPAGATION DELAY SKEW <sup>1</sup>	$t_{PDS}$		-6	$\pm 12$	ns	$R_L = 27\ \Omega$ (see Figure 11)
ENABLE/DISABLE TIMING						
Enable Time to Low Level	$t_{PZL}$		52	100	ns	$R_L = 110\ \Omega$ (see Figure 13)
Enable Time to High Level	$t_{PZH}$		52	100	ns	$R_L = 110\ \Omega$ (see Figure 12)
Disable Time from Low Level	$t_{PLZ}$		40	80	ns	$R_L = 110\ \Omega$ (see Figure 13)
Disable Time from High Level	$t_{PHZ}$		40	80	ns	$R_L = 110\ \Omega$ (see Figure 12)
Enable Time from Shutdown to Low Level	$t_{PSL}$		700	1000	ns	$R_L = 110\ \Omega$ (see Figure 13)
Enable Time from Shutdown to High Level	$t_{PSH}$		700	1000	ns	$R_L = 110\ \Omega$ (see Figure 12)

<sup>1</sup> Measured on  $|t_{PLH}(Y) - t_{PHL}(Y)|$  and  $|t_{PLH}(Z) - t_{PHL}(Z)|$ .

# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E

$V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**Table 5. ADM3490E/ADM3491E**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM DATA RATE		12	15		Mbps	
DIFFERENTIAL OUTPUT DELAY	$t_{DD}$	1	22	35	ns	$R_L = 60\ \Omega$ (see Figure 10)
DIFFERENTIAL OUTPUT TRANSITION TIME	$t_{TD}$	3	11	25	ns	$R_L = 60\ \Omega$ (see Figure 10)
PROPAGATION DELAY						
From Low to High Level	$t_{PLH}$	7	23	35	ns	$R_L = 27\ \Omega$ (see Figure 11)
From High to Low Level	$t_{PHL}$	7	23	35	ns	$R_L = 27\ \Omega$ (see Figure 11)
$ t_{PLH} - t_{PHL} $ PROPAGATION DELAY SKEW <sup>1</sup>	$t_{PDS}$		-1.4	$\pm 8$	ns	$R_L = 27\ \Omega$ (see Figure 11)
ENABLE/DISABLE TIMING (ADM3491E ONLY)						
Enable Time to Low Level	$t_{PZL}$		42	90	ns	$R_L = 110\ \Omega$ (see Figure 13)
Enable Time to High Level	$t_{PZH}$		42	90	ns	$R_L = 110\ \Omega$ (see Figure 12)
Disable Time from Low Level	$t_{PLZ}$		35	80	ns	$R_L = 110\ \Omega$ (see Figure 13)
Disable Time from High Level	$t_{PHZ}$		35	80	ns	$R_L = 110\ \Omega$ (see Figure 12)
Enable Time from Shutdown to Low Level	$t_{PSL}$		650	900	ns	$R_L = 110\ \Omega$ (see Figure 13)
Enable Time from Shutdown to High Level	$t_{PSH}$		650	900	ns	$R_L = 110\ \Omega$ (see Figure 12)

<sup>1</sup> Measured on  $|t_{PLH}(Y) - t_{PHL}(Y)|$  and  $|t_{PLH}(Z) - t_{PHL}(Z)|$ .

## RECEIVER TIMING SPECIFICATIONS

$V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**Table 6. ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
PROPAGATION DELAY						
From Low to High Level	$t_{RPLH}$					
ADM3486E/ADM3490E/ADM3491E		25	62	90	ns	$V_{ID} = 0\text{ V to }3.0\text{ V}$ , $C_L = 15\text{ pF}$ (see Figure 14)
ADM3483E/ADM3488E		25	75	120	ns	$V_{ID} = 0\text{ V to }3.0\text{ V}$ , $C_L = 15\text{ pF}$ (see Figure 14)
From High to Low Level	$t_{RPHL}$					
ADM3486E/ADM3490E/ADM3491E		25	62	90	ns	$V_{ID} = 0\text{ V to }3.0\text{ V}$ , $C_L = 15\text{ pF}$ (see Figure 14)
ADM3483E/ADM3488E		25	75	120	ns	$V_{ID} = 0\text{ V to }3.0\text{ V}$ , $C_L = 15\text{ pF}$ (see Figure 14)
$ t_{RPLH} - t_{RPHL} $ PROPAGATION DELAY SKEW	$t_{RPDS}$					
ADM3486E/ADM3490E/ADM3491E			+6	$\pm 10$	ns	$V_{ID} = 0\text{ V to }3.0\text{ V}$ , $C_L = 15\text{ pF}$ (see Figure 14)
ADM3483E/ADM3488E			+12	$\pm 20$	ns	$V_{ID} = 0\text{ V to }3.0\text{ V}$ , $C_L = 15\text{ pF}$ (see Figure 14)
ENABLE/DISABLE TIMING (ADM3483E/ADM3486E/ADM3491E ONLY)						
Enable Time to Low Level	$t_{RPZL}$		25	50	ns	$C_L = 15\text{ pF}$ (see Figure 15)
Enable Time to High Level	$t_{RPZH}$		25	50	ns	$C_L = 15\text{ pF}$ (see Figure 15)
Disable Time from Low Level	$t_{RPLZ}$		25	45	ns	$C_L = 15\text{ pF}$ (see Figure 15)
Disable Time from High Level	$t_{RPHZ}$		25	45	ns	$C_L = 15\text{ pF}$ (see Figure 15)
Enable Time from Shutdown to Low Level	$t_{RPSL}$		720	1400	ns	$C_L = 15\text{ pF}$ (see Figure 15)
Enable Time from Shutdown to High Level	$t_{RPSH}$		720	1400	ns	$C_L = 15\text{ pF}$ (see Figure 15)
Time to Shutdown <sup>1</sup>	$t_{SHDN}$	80	190	300	ns	

<sup>1</sup> The transceivers are put into shutdown mode by bringing the  $\overline{RE}$  high and the DE low. If the inputs are in this state for less than 80 ns, the parts are guaranteed not to enter shutdown. If the parts are in this state for 300 ns or more, the parts are guaranteed to enter shutdown.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 7.

Parameter	Rating
$V_{CC}$ to GND	-0.3 V to +6 V
Digital Input/Output Voltage (DE, $\overline{RE}$ , DI)	-0.3 V to +6 V
Receiver Output Voltage (RO)	-0.3 V to ( $V_{CC} + 0.3$ V)
Driver Output (A, B, Y, Z)/Receiver Input (A, B) Voltage	-8 V to +13 V
Driver Output Current	$\pm 250$ mA
Operating Temperature Range	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
$\theta_{JA}$ Thermal Impedance	
8-Lead SOIC_N	158°C/W
14-Lead SOIC_N	120°C/W
Lead Temperature, Soldering (20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

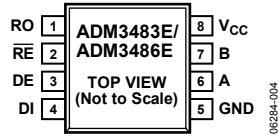


Figure 4. ADM3483E/ADM3486E Pin Configuration

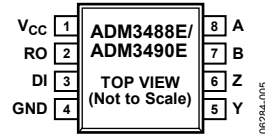
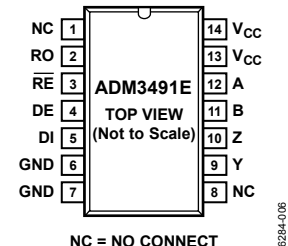


Figure 5. ADM3488E/ADM3490E Pin Configuration



NC = NO CONNECT

Figure 6. ADM3491E Pin Configuration

Table 8. Pin Function Descriptions

ADM3483E/ ADM3486E Pin No.	ADM3488E/ ADM3490E Pin No.	ADM3491E Pin No.	Mnemonic	Description
1	2	2	RO	Receiver Output. If $A > B$ by 200 mV, RO is high; if $A < B$ by 200 mV, RO is low.
2	N/A	3	$\overline{RE}$	Receiver Output Enable. A low level enables the receiver output. A high level places it in a high impedance state. If $\overline{RE}$ is high and DE is low, the device enters a low power shutdown mode.
3	N/A	4	DE	Driver Output Enable. A high level enables the driver differential A and B outputs. A low level places it in a high impedance state. If $\overline{RE}$ is high and DE is low, the device enters a low power shutdown mode.
4	3	5	DI	Driver Input. With a half-duplex part when the driver is enabled, a logic low on DI forces A low and B high; a logic high on DI forces A high and B low. With a full-duplex part when the driver is enabled, a logic low on DI forces Y low and Z high; a logic high on DI forces Y high and Z low.
5	4	6, 7	GND	Ground.
N/A	5	9	Y	Noninverting Driver Output.
6	N/A	N/A	A	Noninverting Receiver Input A and Noninverting Driver Output A.
N/A	8	12	A	Noninverting Receiver Input A.
N/A	6	10	Z	Inverting Driver Output.
7	N/A	N/A	B	Inverting Receiver Input B and Inverting Driver Output B.
N/A	7	11	B	Inverting Receiver Input B.
8	1	13, 14	V <sub>CC</sub>	Power Supply, 3.3 V $\pm$ 0.3 V. Bypass V <sub>CC</sub> to GND with a 0.1 $\mu$ F capacitor.
N/A	N/A	1, 8	NC	No Connect. Not internally connected. Can be connected to GND.



TEST CIRCUITS AND SWITCHING CHARACTERISTICS

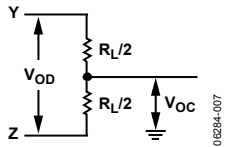


Figure 7. Driver Differential Output Voltage and Common-Mode Output Voltage

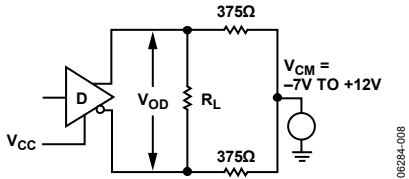


Figure 8. Driver Differential Output Voltage with Varying Common-Mode Voltage

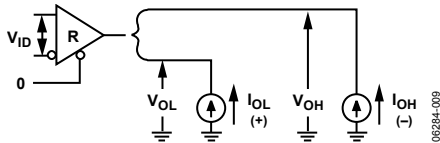


Figure 9. Receiver Output Voltage High and Output Voltage Low

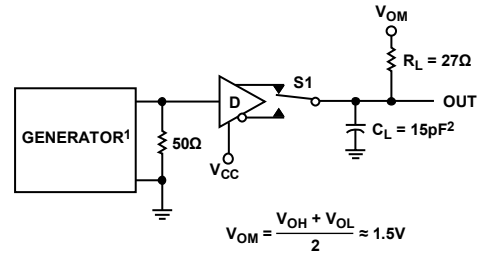


Figure 10. Driver Differential Output Delay and Transition Times

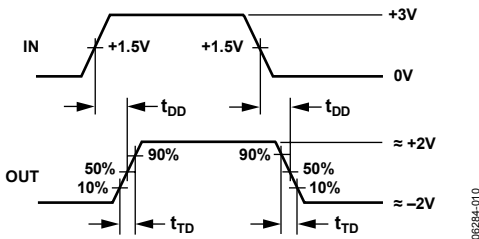


Figure 11. Driver Propagation Delays

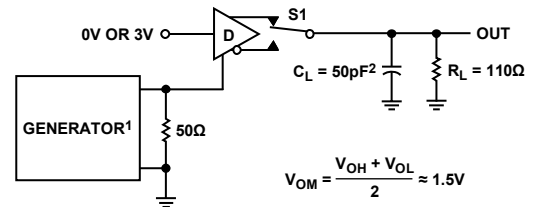


Figure 12. Driver Enable and Disable Times ( $t_{PZH}$ ,  $t_{PSH}$ ,  $t_{PHZ}$ )

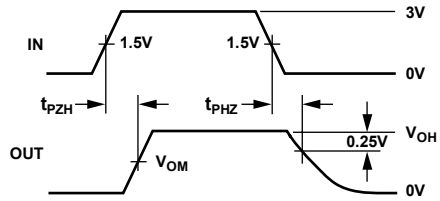
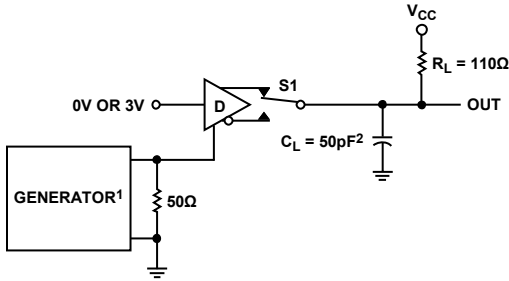


Figure 13. Driver Enable and Disable Times ( $t_{PZH}$ ,  $t_{PSH}$ ,  $t_{PHZ}$ )

# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_r \leq 6.0\text{ns}$ ,  $Z_0 = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

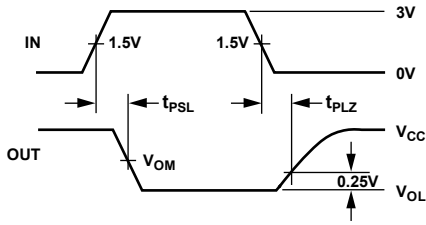
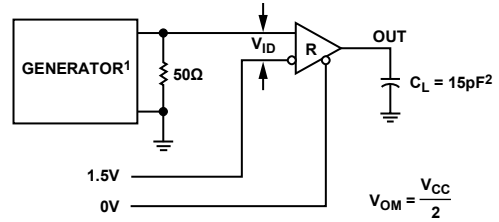


Figure 13. Driver Enable and Disable Times ( $t_{PZL}$ ,  $t_{PSL}$ ,  $t_{PLZ}$ )



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_r \leq 6.0\text{ns}$ ,  $Z_0 = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

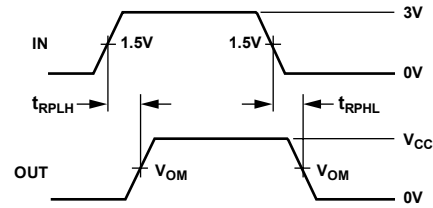
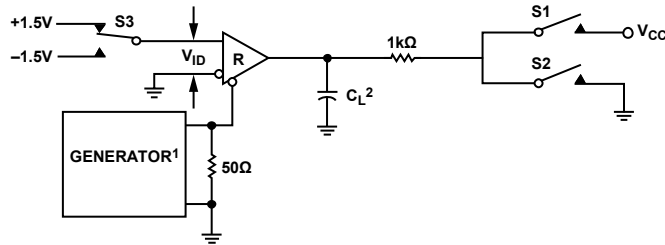


Figure 14. Receiver Propagation Delays



<sup>1</sup>PPR = 250kHz, 50% DUTY CYCLE,  $t_r \leq 6.0\text{ns}$ ,  $Z_0 = 50\Omega$ .  
<sup>2</sup> $C_L$  INCLUDES PROBE AND STRAY CAPACITANCE.

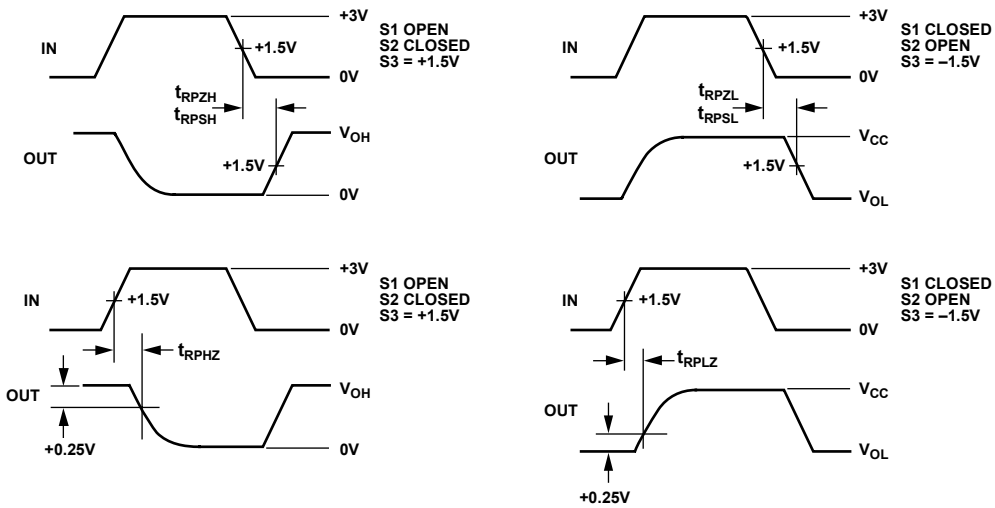


Figure 15. Receiver Enable and Disable Times

## TYPICAL PERFORMANCE CHARACTERISTICS

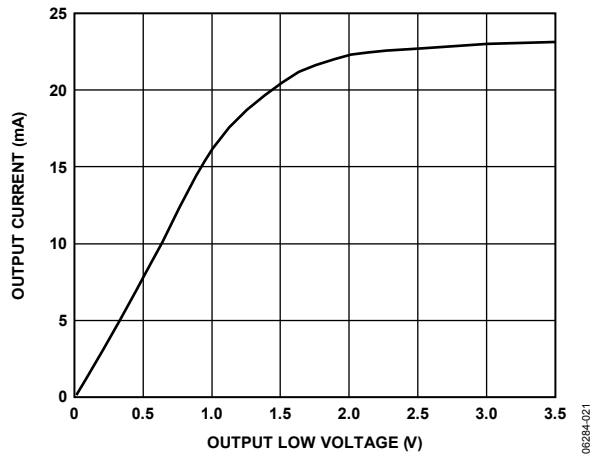


Figure 16. Output Current vs. Receiver Output Low Voltage

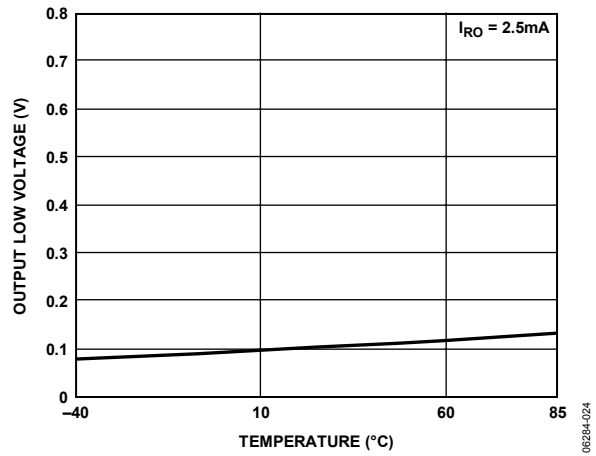


Figure 19. Receiver Output Low Voltage vs. Temperature

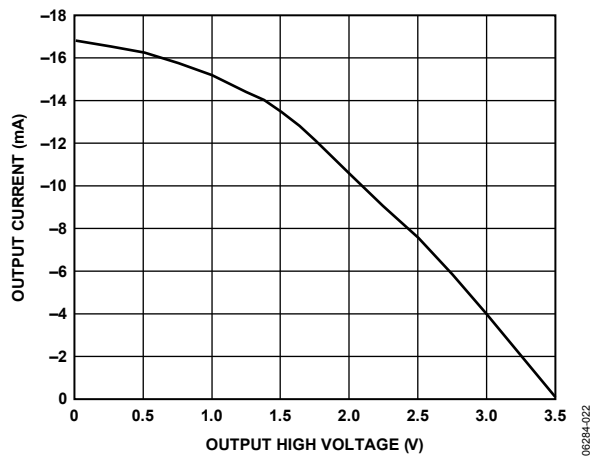


Figure 17. Output Current vs. Receiver Output High Voltage

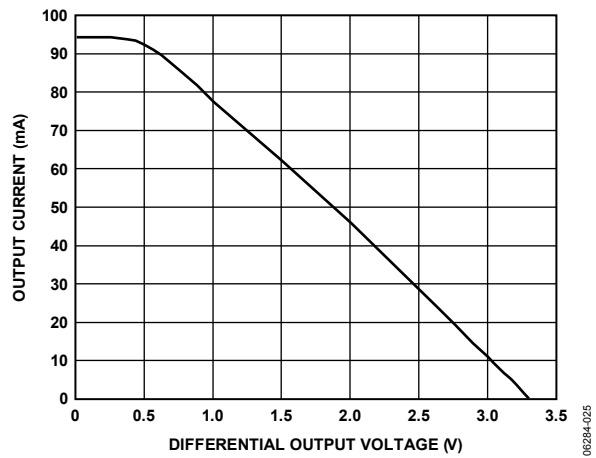


Figure 20. Driver Output Current vs. Differential Output Voltage

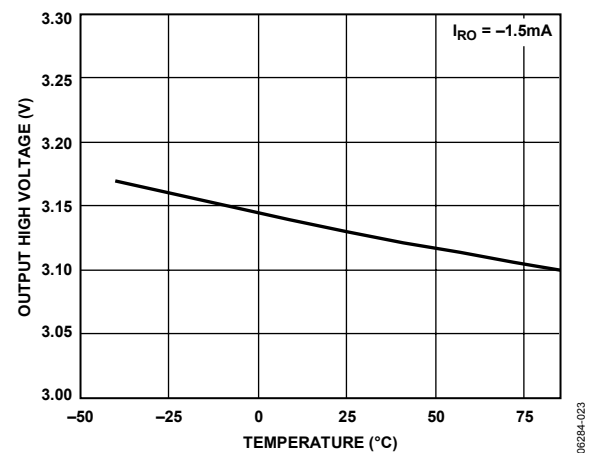


Figure 18. Receiver Output High Voltage vs. Temperature

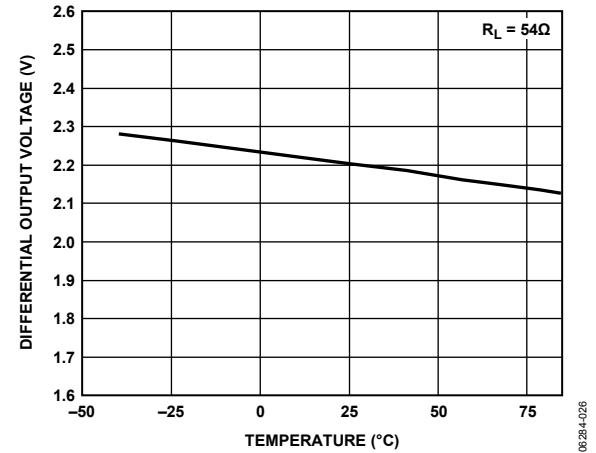


Figure 21. Driver Differential Output Voltage vs. Temperature

# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E

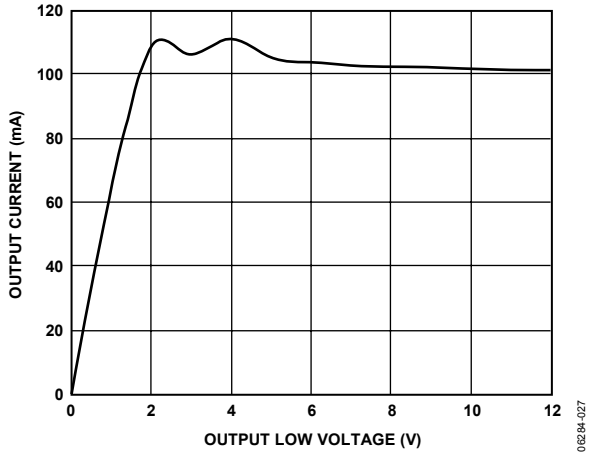


Figure 22. Output Current vs. Driver Output Low Voltage

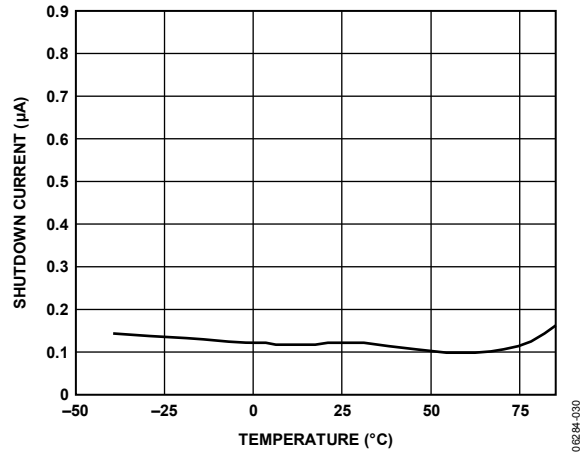


Figure 25. Shutdown Current vs. Temperature

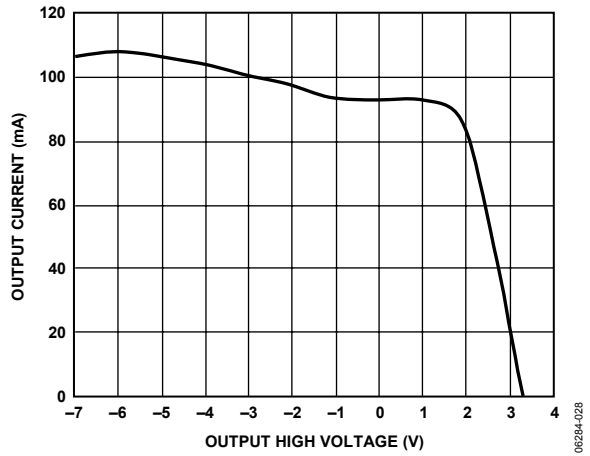


Figure 23. Output Current vs. Driver Output High Voltage

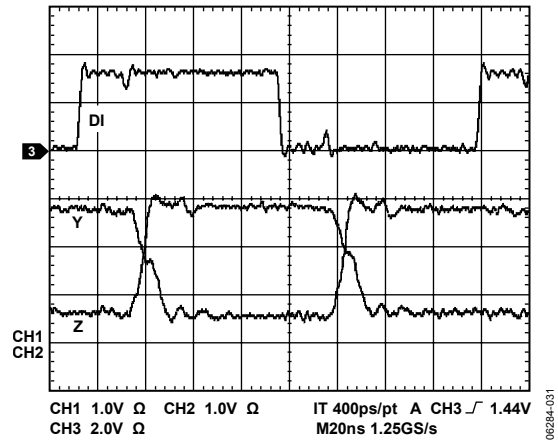


Figure 26. ADM3490E/ADM3491E Driver Propagation Delay

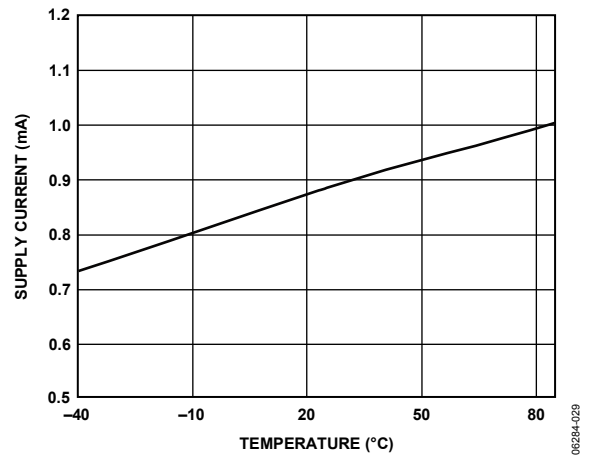


Figure 24. Supply Current vs. Temperature

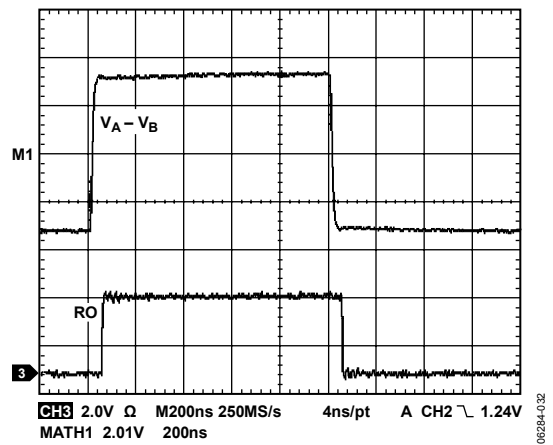


Figure 27. ADM3490E/ADM3491E Receiver Propagation Delay, Driven by External RS-485 Device

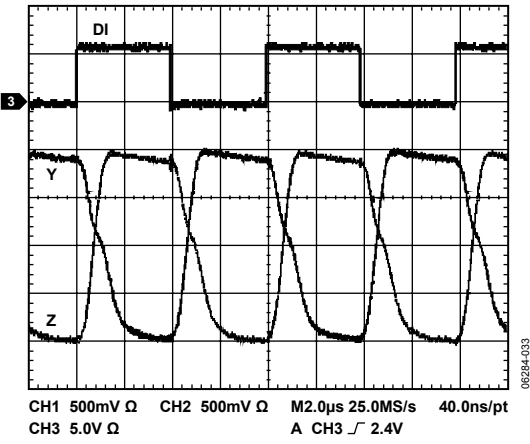


Figure 28. ADM3483E/ADM3488E Driver Propagation Delay

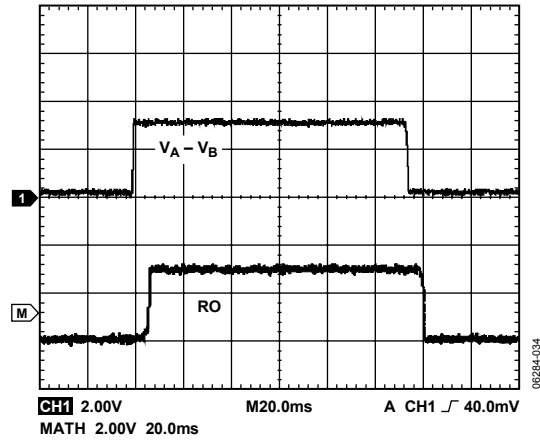


Figure 29. ADM3483E/ADM3488E Receiver Propagation Delay

# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E

## CIRCUIT DESCRIPTION

The ADM34xxE are low power transceivers for RS-485 and RS-422 communications. The ADM3483E/ADM3488E operate at data rates up to 250 kbps. The ADM3486E operates at data rates up to 2.5 Mbps, and the ADM3490E/ADM3491E transmit at up to 12 Mbps. The ADM3488E/ADM3490E/ADM3491E are full-duplex transceivers, and the ADM3483E/ADM3486E are half duplex. Driver enable (DE) and receiver enable ( $\overline{\text{RE}}$ ) pins are included on the ADM3483E/ADM3486E/ADM3491E. When disabled, the driver and receiver outputs are high impedance.

### DEVICES WITH RECEIVER/DRIVER ENABLE—ADM3483E/ADM3486E/ADM3491E

Table 9. Transmitting Truth Table

Transmitting Inputs			Transmitting Outputs		Mode
$\overline{\text{RE}}$	DE	DI	A <sup>1</sup> , Y <sup>2</sup>	B <sup>1</sup> , Z <sup>2</sup>	
X <sup>3</sup>	1	1	1	0	Normal
X <sup>3</sup>	1	0	0	1	Normal
0	0	X <sup>3</sup>	High-Z <sup>4</sup>	High-Z <sup>4</sup>	Normal
1	0	X <sup>3</sup>	High-Z <sup>4</sup>	High-Z <sup>4</sup>	Shutdown

<sup>1</sup> ADM3483E and ADM3486E only.

<sup>2</sup> ADM3491E only.

<sup>3</sup> X = don't care.

<sup>4</sup> High-Z = high impedance.

Table 10. Receiving Truth Table

Receiving Inputs				Receiving Output	Mode
$\overline{\text{RE}}$	DE <sup>1</sup>	DE <sup>2</sup>	A – B	RO	
0	0	X <sup>3</sup>	$\geq +0.2\text{V}$	1	Normal
0	0	X <sup>3</sup>	$\leq -0.2\text{V}$	0	Normal
0	0	X <sup>3</sup>	Inputs open	1	Normal
1	0	X <sup>3</sup>	X <sup>3</sup>	High-Z <sup>4</sup>	Shutdown

<sup>1</sup> ADM3483E and ADM3486E only.

<sup>2</sup> ADM3491E only.

<sup>3</sup> X = don't care.

<sup>4</sup> High-Z = high impedance.

### DEVICES WITHOUT RECEIVER/DRIVER ENABLE—ADM3488E/ADM3490E

Table 11. Transmitting Truth Table

Transmitting Input	Transmitting Outputs	
DI	Z	Y
1	0	1
0	1	0

Table 12. Receiving Truth Table

Receiving Input A – B	Receiving Output RO
$\geq +0.2\text{V}$	1
$\leq -0.2\text{V}$	0
Inputs open	1

### LOW POWER SHUTDOWN MODE—ADM3483E/ADM3486E/ADM3491E

The ADM3483E/ADM3486E/ADM3491E are put into a low power shutdown mode by bringing both  $\overline{\text{RE}}$  high and DE low. The devices do not shut down unless both the driver and the receiver are disabled (high impedance). In shutdown mode, the devices typically draw less than 1  $\mu\text{A}$  of supply current. For these devices, the  $t_{\text{PSH}}$  and the  $t_{\text{PSL}}$  enable times assume the part was in the low power shutdown mode; the  $t_{\text{PZH}}$  and the  $t_{\text{PZL}}$  enable times assume the receiver or the driver was disabled, but the part was not shut down.

### DRIVER OUTPUT PROTECTION

The ADM34xxE family implements two ways to prevent excessive output current and power dissipation caused by faults or by bus contention. A current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see the Typical Performance Characteristics section). In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively.

### PROPAGATION DELAY

Figure 11, Figure 14, Figure 26, and Figure 27 show the typical propagation delays. Skew time is simply the difference between the low-to-high and the high-to-low propagation delays. Small driver/receiver skew times help maintain a symmetrical mark-space ratio (50% duty cycle).

The receiver skew time,  $|t_{\text{PRHL}} - t_{\text{PHL}}|$ , is under 10 ns (20 ns for the ADM3483E/ADM3488E). The driver skew time is 8 ns for the ADM3490E/ADM3491E, 12 ns for the ADM3486E, and typically under 50 ns for the ADM3483E/ADM3488E.

### LINE LENGTH VS. DATA RATE

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, Figure 34 illustrates an example of a line repeater.

## ±15 kV ESD PROTECTION

Two coupling methods are used for ESD testing: contact discharge and air-gap discharge. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage but does not make direct contact with the test unit. With air-gap discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, therefore the term air-gap discharge. This method is influenced by humidity, temperature, barometric pressure, distance, and rate of closure of the discharge gun. The contact discharge method, while less realistic, is more repeatable and is gaining acceptance and preference over the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time, coupled with high voltages, can cause failures in unprotected semiconductors. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device can suffer from parametric degradation that can result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

Input/output lines are particularly vulnerable to ESD damage. Simply touching or connecting an input/output cable can result in a static discharge that can damage or completely destroy the interface product connected to the input/output port. It is extremely important, therefore, to have high levels of ESD protection on the input/output lines.

The ESD discharge can induce latch-up in the device under test, so it is important that ESD testing on the input/output pins be carried out while device power is applied. This type of testing is more representative of a real-world input/output discharge, which occurs when the equipment is operating normally.

The transmitter outputs and receiver inputs of the ADM34xxE family are characterized for protection to a ±15 kV limit using the human body model.

### HUMAN BODY MODEL

Figure 30 shows the human body model and the current waveform it generates when discharged into a low impedance. This model consists of a 100 pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5 kΩ resistor.

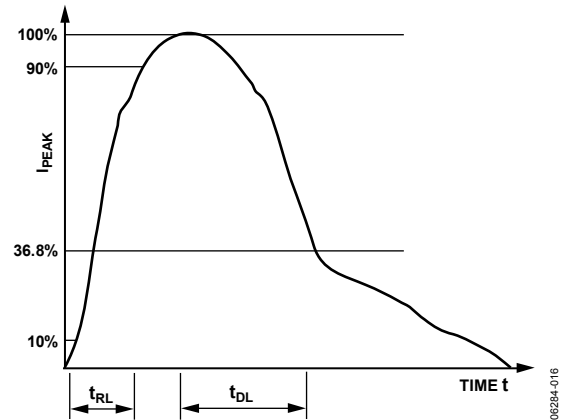
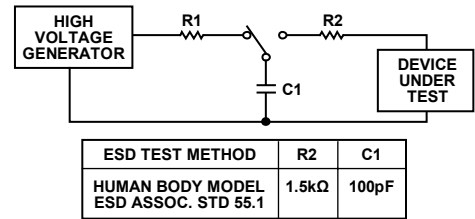
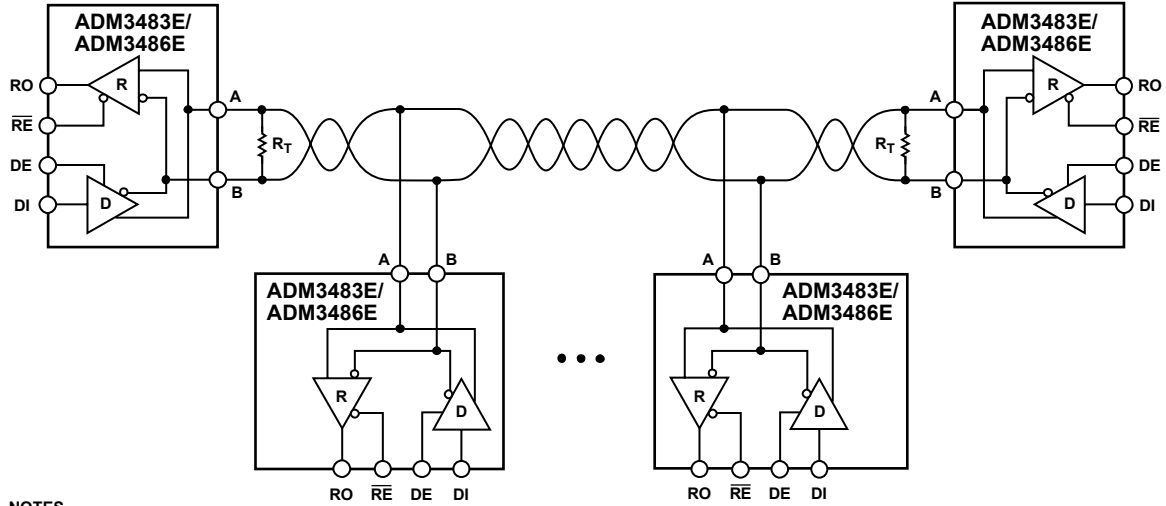


Figure 30. Human Body Model and Current Waveform

### TYPICAL APPLICATIONS

The ADM3483E/ADM3486E/ADM3491E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. The ADM3488E/ADM3490E full-duplex transceiver is designed to be used in a daisy-chain network topology or in a point-to-point application (see Figure 32). The ADM3483E/ADM3486E are half-duplex RS-485 transceivers that can be used in a multidrop bus configuration, as shown in Figure 31. The ADM3488E/ADM3490E/ADM3491E can also be used as a line repeater, for use with cable lengths longer than 4000 feet, as shown in Figure 34. To minimize reflections, the line must be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E



- NOTES**
1. MAXIMUM NUMBER OF TRANSCEIVERS ON BUS: 32.
  2.  $R_T$  IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 31. ADM3483E/ADM3486E Typical Half-Duplex RS-485 Network

06284-017

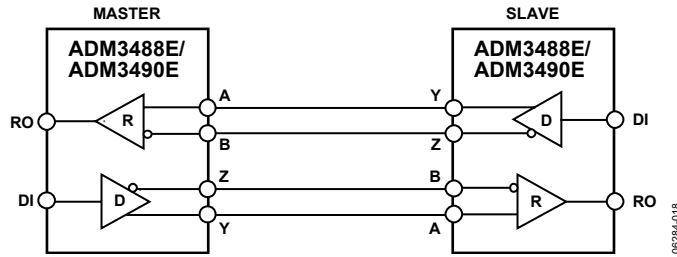
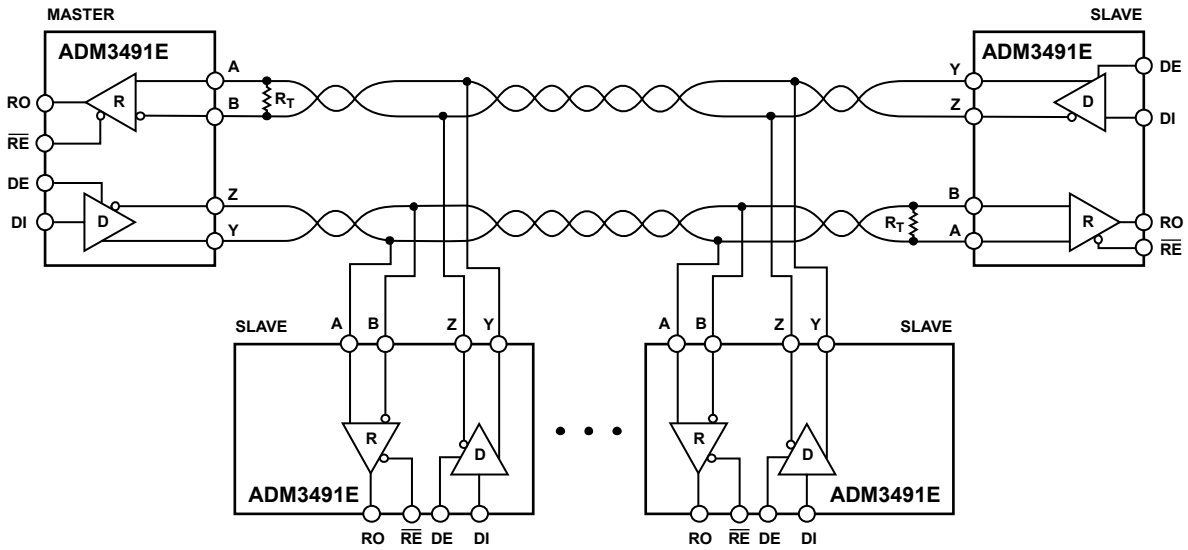


Figure 32. ADM3488E/ADM3490E Full-Duplex Point-to-Point Applications

06284-018



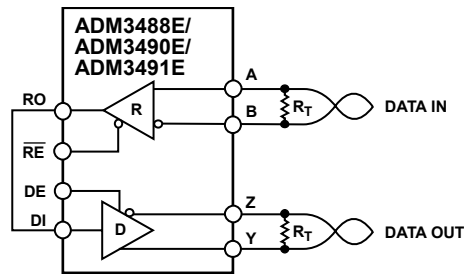
# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E



- NOTES**
1. MAXIMUM NUMBER OF NODES: 32.
  2.  $R_T$  IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 33. ADM3491E Full-Duplex RS-485 Network

06284-019



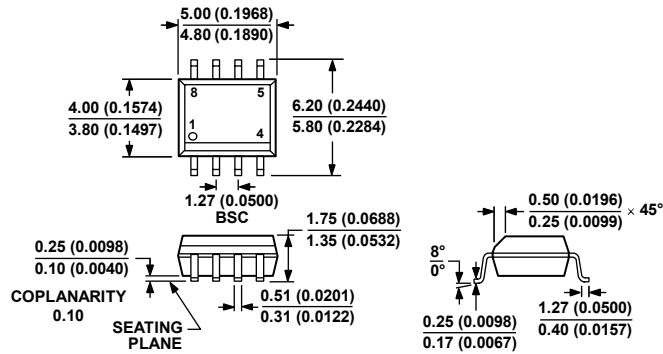
- NOTES**
1.  $R_T$  IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.
  2. RE AND DE PINS ON ADM3491E ONLY.

Figure 34. Line Repeater for ADM3488E/ADM3490E/ADM3491E

06284-020

# ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E

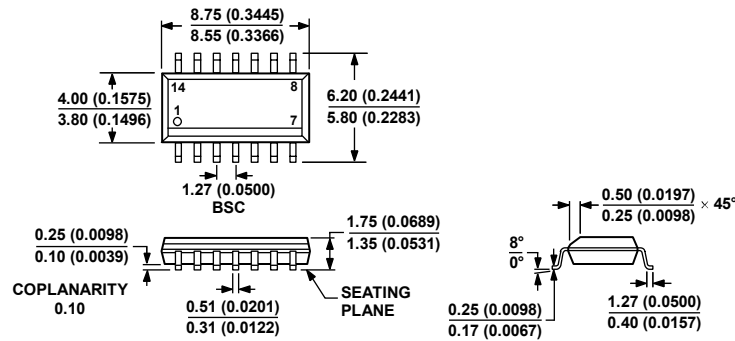
## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 35. 8-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
(R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 36. 14-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
(R-14)

Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADM3483EARZ <sup>1</sup>	-40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
ADM3483EARZ-REEL7 <sup>1</sup>	-40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	1,000
ADM3486EARZ <sup>1</sup>	-40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
ADM3486EARZ-REEL7 <sup>1</sup>	-40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	1,000
ADM3488EARZ <sup>1</sup>	-40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
ADM3488EARZ-REEL7 <sup>1</sup>	-40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	1,000
ADM3490EARZ <sup>1</sup>	-40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	
ADM3490EARZ-REEL7 <sup>1</sup>	-40°C to +85°C	8-Lead Standard Small Outline Package (SOIC_N)	R-8	1,000
ADM3491EARZ <sup>1</sup>	-40°C to +85°C	14-Lead Standard Small Outline Package (SOIC_N)	R-14	
ADM3491EARZ-REEL7 <sup>1</sup>	-40°C to +85°C	14-Lead Standard Small Outline Package (SOIC_N)	R-14	1,000

<sup>1</sup> Z = Pb-free part.

**NOTES**

**ADM3483E/ADM3486E/ADM3488E/ADM3490E/ADM3491E**

## **NOTES**