$\mathcal{N}ational\ Semiconductor$

May 1989

DP8409A Multi-Mode Dynamic RAM Controller/Driver

General Description

Dynamic memory system designs, which formerly required several support chips to drive the memory array, can now be implemented with a single IC . . . the DP8409A Multi-Mode Dynamic RAM Controller/Driver. The DP8409A is capable of driving all 16k and 64k Dynamic RAMs (DRAMs) as well as 256k DRAMs. Since the DP8409A is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, the major performance disadvantage of multiple-chip memory drive and control.

The DP8409A's 8 modes of operation offer a wide selection of DRAM control capabilities. Memory access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The DP8409A is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. All output drivers are capable of driving 500 pF loads with propagation delays of 25 ns. The DP8409A timing parameters are specified driving the typical load capacitance of 88 DRAMs, including trace capacitance.

The DP8409A has 3 mode-control pins: M2, M1, and M0, where M2 is in general $\overline{REFRESH}$. These 3 pins select 8 modes of operation. Inputs B1 and B0 in the memory access modes (M2 = 1), are select inputs which select one of four $\overline{RAS}$ outputs. During normal access, the 9 address outputs can be selected from the Row Address Latch or the Column Address Latch. During refresh, the 9-bit on-chip refresh counter is enabled onto the address bus and in this mode all $\overline{RAS}$ outputs are selected, while $\overline{CAS}$ is inhibited.
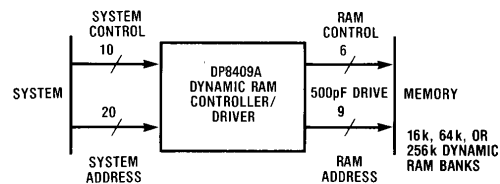
The DP8409A can drive up to 4 banks of DRAMs, with each bank comprised of 16k's, 64k's, or 256k's. Control signal outputs $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are provided with the same drive capability. Each $\overline{RAS}$ output drives one bank of DRAMs so that the four $\overline{RAS}$ outputs are used to select the banks, while $\overline{CAS}$, $\overline{WE}$, and the multiplexed addresses can be connected to all of the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the data outputs in TRI-STATE®. Only the bank with its associated $\overline{RAS}$ low will be written to or read from.

Operational Features

■ All DRAM drive functions on one chip—minimizes skew on outputs, maximizes AC peformance

■ On-chip capacitive-load drives (specified to drive up to 88 DRAMs)

■ Drives directly all 16k, 64k, and 256k DRAMs

■ Capable of addressing 64k, 256k, or 1M words

■ Propagation delays of 25 ns typical at 500 pF load

■ $\overline{CAS}$ goes low automatically after column addresses are valid if desired

■ Auto Access mode provides $\overline{RAS}$, row to column select, then $\overline{CAS}$ automatically and fast

■ $\overline{WE}$ follows $\overline{WIN}$ unconditionally—offering READ, WRITE or READ-MODIFY-WRITE cycles

■ On-chip 9-bit refresh counter with selectable End-of-Count (127, 255 or 511)

■ End-of-Count indicated by RF I/O pin going low at 127, 255 or 511

■ Low input on RF I/O resets 9-bit refresh counter

■ $\overline{CAS}$ inhibited during refresh cycle

■ Fall-through latches on address inputs controlled by ADS

■ TRI-STATE outputs allow multi-controller addressing of memory

■ Control output signals go high-impedance logic "1" when disabled for memory sharing

■ Power-up: counter reset, control signals high, address outputs TRI-STATE, and End-of-Count set to 127

Mode Features

■ 8 modes of operation: 3 access, 3 refresh, and 2 set-up

■ 2 externally controlled modes: 1 access and 1 refresh (Modes 0, 4)

■ 2 auto-access modes $\overline{RAS} \rightarrow R/\overline{C} \rightarrow \overline{CAS}$ automatic, with t_{RAH} = 20 or 30 ns minimum (Modes 5, 6)

■ Auto-access mode allows Hidden Refreshing (Mode 5)

■ Forced Refresh requested on RF I/O if no Hidden Refresh (Mode 5)

■ Forced Refresh performed after system acknowledge of request (Mode 1)

■ Automatic Burst Refresh mode stops at End-of-Count of 127, 255, or 511 (Mode 2)

■ 2 All-$\overline{RAS}$ Acces modes externally or automatically controlled for memory initialization (Modes 3a, 3b)

■ Automatic All-$\overline{RAS}$ mode with external 8-bit counter frees system for other set-up routines (Mode 3a)

■ End-of-Count value of Refresh Counter set by B1 and B0 (Mode 7)

```
        SYSTEM                      RAM
        CONTROL                   CONTROL
          10                         6
                 ┌──────────────┐
                 │   DP8409A    │
                 │ DYNAMIC RAM  │ 500pF DRIVE   MEMORY
SYSTEM           │ CONTROLLER/  │      9
          20     │   DRIVER     │            16k, 64k, OR
                 └──────────────┘            256k DYNAMIC
        SYSTEM                      RAM       RAM BANKS
        ADDRESS                   ADDRESS
```

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PAL® is a registered trademark of and used under license with Monolithic Memories Inc.

RRD-B30M105/Printed in U. S. A.

Block and Connection Diagrams
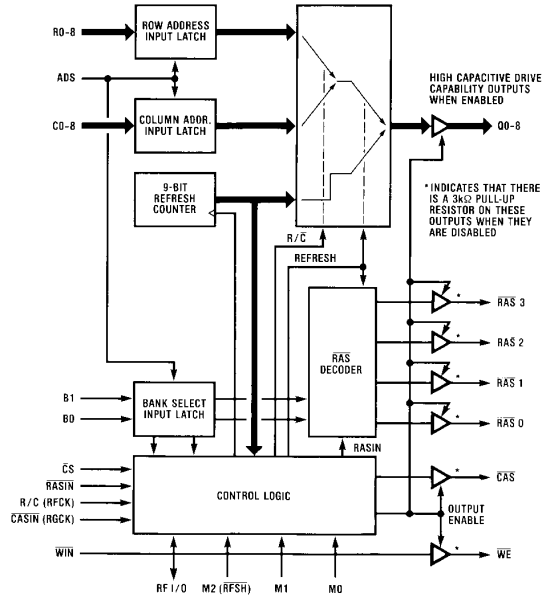
TL/F/8409–2

**Order Number DP8409AD, DP8409AN,
DP8409AN-3 or DP8409AV-2
See NS Package Number D48A, N48A or V68A**

68 Pin PCC

TL/F/8409–3

Dual-In-Line Package

Top View

TL/F/8409–5

Pin Definitions

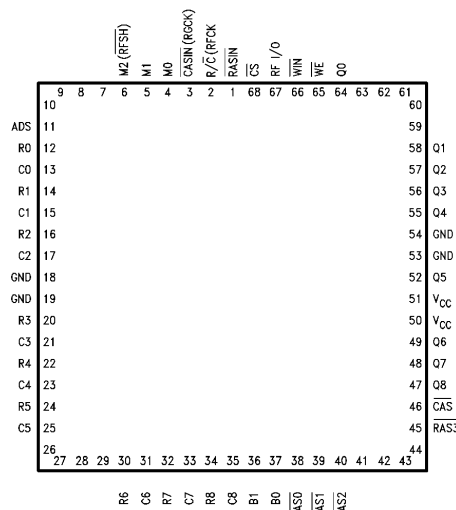V_{CC}, GND, GND—V_{CC} = 5V ±5%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution would be a 1 μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected as close as possible to pins 36 and 38 to reduce lead inductance. See figure below.
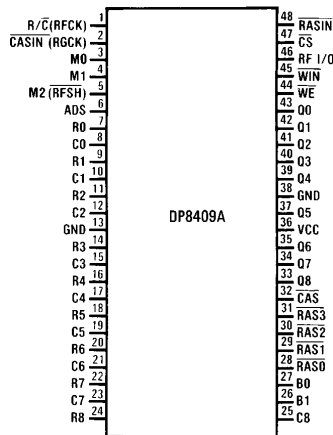

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*Capacitor values should be chosen depending on the particular application.

R0–R8: Row Address Inputs.

C0–C8: Column Address Inputs.

Q0–Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.*

$\overline{RASIN}$: Row Address Strobe Input—Enables selected $\overline{RAS}_n$ output when M2 ($\overline{RFSH}$) is high, or all $\overline{RAS}_n$ outputs when $\overline{RFSH}$ is low.

R/$\overline{C}$ (RFCK)—In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/Column Select Input: selects either the row or column address input latch onto the output bus.

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Pin Definitions (Continued)

TABLE I. DP8409A Mode Select Options

Mode	($\overline{\text{RFSH}}$) M2	M1	M0	Mode of Operation	Conditions
0	0	0	0	Externally Controlled Refresh	RF I/O = $\overline{\text{EOC}}$
1	0	0	1	Auto Refresh—Forced	RF I/O = Refresh Request ($\overline{\text{RFRQ}}$)
2	0	1	0	Internal Auto Burst Refresh	RF I/O = $\overline{\text{EOC}}$
3a	0	1	1	All $\overline{\text{RAS}}$ Auto Write	RF I/O = $\overline{\text{EOC}}$; All $\overline{\text{RAS}}$ Active
3b	0	1	1	Externally Controlled All $\overline{\text{RAS}}$ Access	All $\overline{\text{RAS}}$ Active
4	1	0	0	Externally Controlled Access	Active $\overline{\text{RAS}}$ Defined by Table II
5	1	0	1	Auto Access, Slow t_{RAH}, Hidden Refresh	Active $\overline{\text{RAS}}$ Defined by Table II
6	1	1	0	Auto Access, Fast t_{RAH}	Active $\overline{\text{RAS}}$ Defined by Table II
7	1	1	1	Set End of Count	See Table III for Mode 7

$\overline{\text{CASIN}}$ (RGCK)—In Auto-Refresh Mode, Auto Burst Mode, and All-$\overline{\text{RAS}}$ Auto-Write Mode, this pin is the $\overline{\text{RAS}}$ Generator Clock input. In all other modes it is $\overline{\text{CASIN}}$ (Column Address Strobe Input), which inhibits $\overline{\text{CAS}}$ output when high in Modes 4 and 3b. In Mode 6 it can be used to prolong $\overline{\text{CAS}}$ output.

ADS: Address (Latch) Strobe Input—Row Address, Column Address, and Bank Select Latches are fall-through with ADS high; Latches on high-to-low transition.

$\overline{\text{CS}}$: **Chip Select Input**—The TRI-STATE mode will Address Outputs and puts the control signal into a high-impedance logic ''1'' state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.

M0, M1, M2: Mode Control Inputs—These 3 control pins determine the 8 major modes of operation of the DP8409A as depicted in Table I.

RF I/O—The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low in Modes 0 and 2 when the End-of-Count output is at 127, 255, or 511 (see Table III). In Auto-Refresh Mode it is the Refresh Request output.

$\overline{\text{WIN}}$: **Write Enable Input.**

$\overline{\text{WE}}$: **Write Enable Output**—Buffered output from $\overline{\text{WIN}}$.*

$\overline{\text{CAS}}$: **Column Address Strobe Output**—In Modes 3a, 5, and 6, $\overline{\text{CAS}}$ transitions low following valid column address. In Modes 3b and 4, it goes low after R/$\overline{\text{C}}$ goes low, or follows $\overline{\text{CASIN}}$ going low if R/$\overline{\text{C}}$ is already low. $\overline{\text{CAS}}$ is high duing refresh.*

$\overline{\text{RAS}}$ 0–3: **Row Address Strobe Outputs**—Selects a memory bank decoded from B1 and B0 (see Table II), if $\overline{\text{RFSH}}$ is high. If $\overline{\text{RFSH}}$ is low, all banks are selected.*

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{\text{RAS}}$ outputs when $\overline{\text{RASIN}}$ goes low. Also used to define End-of-Count in Mode 7 (Table III).

Conditions for All Modes

INPUT ADDRESSING

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be per-

manently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{\text{RASIN}}$ and R/$\overline{\text{C}}$ are initially high. When the address inputs are enabled into the address latches, the row addresses appear on the Q outputs. The address strobe also inputs the bank-select address, (B0 and B1). If $\overline{\text{CS}}$ is low, all outputs are enabled. When $\overline{\text{CS}}$ is transitioned high, the address outputs go TRI-STATE and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other DP8409As for multi-addressing. All outputs go active about 50 ns after the chip is selected again. If $\overline{\text{CS}}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

DRIVE CAPABILITY

The DP8409A has timing parameters that are specified with up to 600 pF loads. In a typical memory system this is equivalent to about 88, 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of *Figure 10*. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

Because of distributed trace capacitance and inductance and DRAM input capacitance, current spikes can be created, causing overshoots and undershoots at the DRAM inputs that can change the contents of the DRAMs or even destroy them. To remove these spikes, a damping resistor (low inductance, carbon) can be inserted between the DP8409A driver outputs and the DRAMs, as close as possible to the DP8409A. The values of the damping resistors may differ between the different control outputs; $\overline{\text{RAS}}$s, $\overline{\text{CAS}}$, Q's, and $\overline{\text{WE}}$. The damping resistors should be determined by the first prototypes (not wire-wrapped due to the larger distributed capacitance and inductance). The best values for the damping resistors are the critical values giving a critically damped transition on the control outputs. Typical values for the damping resistors will be between 15Ω and 100Ω, the lower the loading the higher the value. (For more information, see AN-305 ''Precautions to Take When Driving Memories.'')

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Conditions for All Modes (Continued)

DP8409A DRIVING ANY 16k OR 64k DRAMs

The DP8409A can drive any 16k or 64k DRAMs. All 16k DRAMs are basically the same configuration, including the newer 5V-only version. Hence, in most applications, different manufacturers' DRAMs are interchangeable (for the same supply-rail chips), and the DP8409A can drive all 16k DRAMs (see *Figure 1a*).

There are three basic configurations for the 5V-only 64k DRAMs: a 128-row by 512-column array with an on-RAM refresh counter, a 128-row by 512-column array with no on-RAM refresh counter, and a 256-row by 256-column array

with no on-RAM refresh counter. The DP8409A can drive all three configurations, and at the same time allows them all to be interchangeable (as shown in *Figures 1b* and *1c*), providing maximum flexibility in the choice of DRAMs. Since the 9-bit on-chip refresh counter can be used as a 7-bit refresh counter for the 128-row configuration, or as an 8-bit refresh counter for the 256-row configuration, the on-RAM refresh counter (if present) is never used. As long as 128 rows are refreshed every 2 ms (i.e. 256 rows in 4 ms) all DRAM types are correctly refreshed.
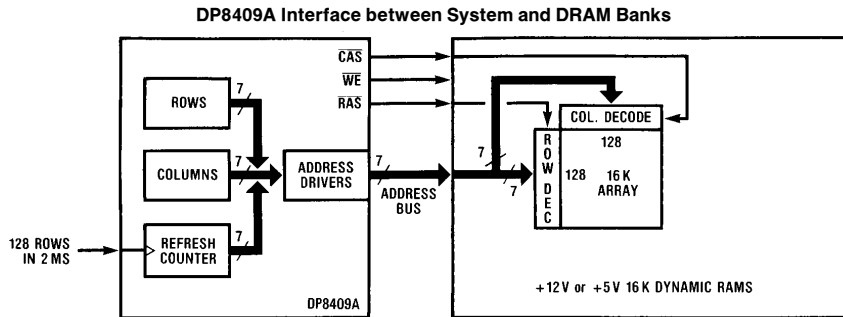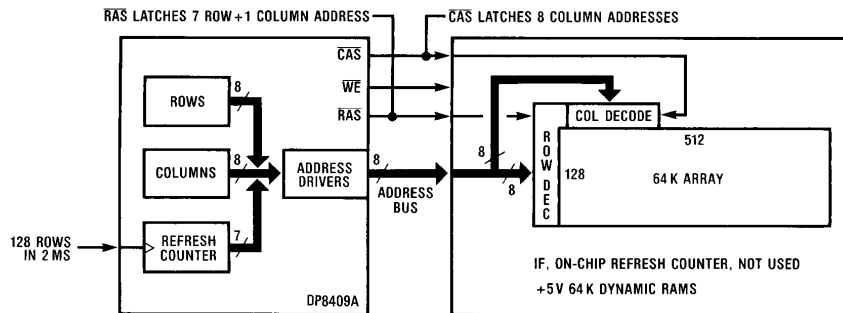
DP8409A Interface between System and DRAM Banks

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FIGURE 1a. DP8409A with any 16k DRAMs

ONLY LS 7 BITS OF REFRESH COUNTER USED FOR THE 7 ROW ADDRESSES.
MSB NOT USED BUT CAN TOGGLE

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FIGURE 1b. DP8409A with 128 Row x 512 Column 64k DRAM
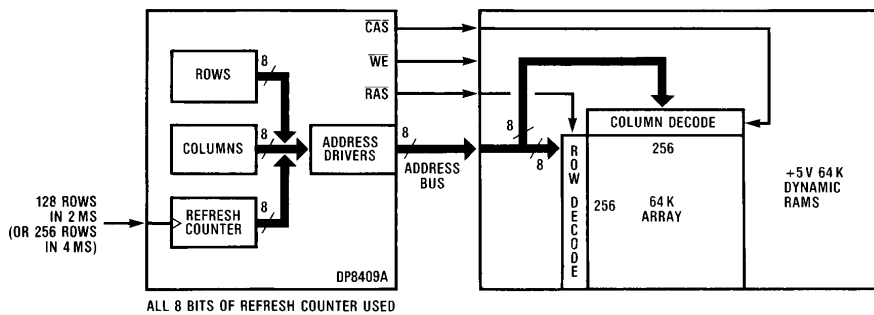

ALL 8 BITS OF REFRESH COUNTER USED

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FIGURE 1c. DP8409A with 256 x 256 Column 64k DRAM

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Conditions for All Modes (Continued)

When the DP8409A is in a refresh mode, the RF I/O pin indicates that the on-chip refresh counter has reached its end-of-count. This end-of-count is selectable as 127, 255 or 512 to accommodate 16k, 64k or 256k DRAMs. Although the end-of-count may be chosen to be any of these, the counter always counts to 511 before rolling over to zero.

READ, WRITE, AND READ-MODIFY-WRITE CYCLES

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

POWER-UP INITIALIZE

When V_{CC} is first applied to the DP8409A, an initialize pulse clears the refresh counter, the internal control flip-flops, and set the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3V, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to TRI-STATE. As V_{CC} increases above 2.3V, control of these outputs is granted to the system.

DP8409A Functional Mode Descriptions

Note: All delay parameters stated in text refer to the DP8409A. Substitute the respective delay numbers for the DP8409-2 or DP8409-3 when using these devices.

MODE 0—EXTERNALLY CONTROLLED REFRESH

Figure 2 is the Externally Controlled Refresh Timing. In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled. When $\overline{RAS}$ occurs, the enabled row in the DRAM is refreshed. If the Externally Controlled Refresh mode, all $\overline{RAS}$ outputs are enabled following $\overline{RASIN}$, and $\overline{CAS}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{RASIN}$ or $\overline{RFSH}$ goes low-to-high after a refresh. RF I/O goes low when the count is 127, 255, or 511, as set by End-of-Count (see Table III), with $\overline{RASIN}$ and $\overline{RFSH}$ low. To reset the counter to all zeros, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and RFSH must be skewed transitioning low such that the refresh address is valid on the address outputs of the controller before the $\overline{RAS}$ outputs go low. The amount of time that RFSH should go low before $\overline{RASIN}$ does depends on the capacitive loading of the address and $\overline{RAS}$ lines. For the load specified in the switching characteristics of this data sheet, 10 ns is sufficient. Refer to *Figure 2*.

To perform externally controlled burst refresh, $\overline{RASIN}$ is toggled while RFSH is held low. The refresh counter increments with $\overline{RASIN}$ going low to high, so that the DRAM rows are refreshed in succession by $\overline{RASIN}$ going high to low.
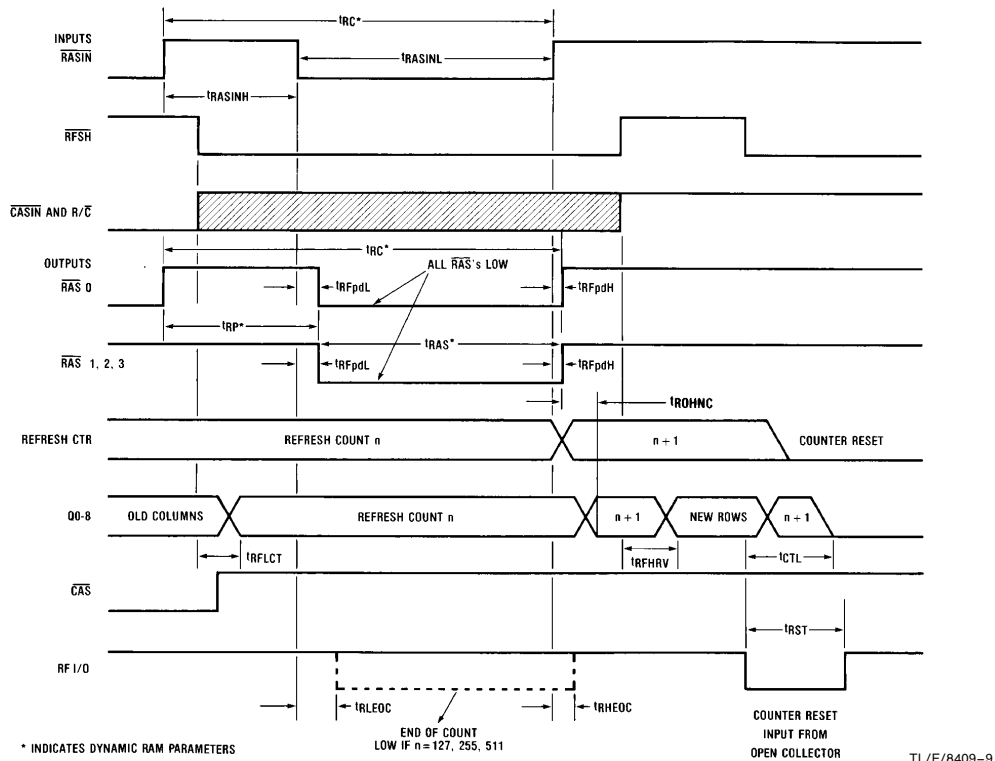

FIGURE 2. External Control Refresh Cycle (Mode 0)

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DP8409A Functional Mode Descriptions (Continued)

MODE 1—AUTOMATIC FORCED REFRESH

In Mode 1, the R/$\overline{C}$ (RFCK) pin becomes RFCK (refresh cycle clock), instead of R/$\overline{C}$, and $\overline{CAS}$ remains high. If RFCK is kept permanently high, then whenever M2 ($\overline{RFSH}$) goes low, an externally controlled refresh will occur and all $\overline{RAS}$ outputs will follow $\overline{RASIN}$, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but when set low externally through an open-collector driver, the refresh counter resets as normal. This externally controlled method may be preferred when operating in the Automatic Access mode (Mode 5), where hidden or forced refreshing is undesirable, but refreshing is still necessary.

If RFCK is an input clock signal, one (and only one) refresh cycle must take place every RFCK cycle. Refer to *Figure 9*. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O ($\overline{Refresh Request}$) goes low immediately after RFCK goes low, indicating to the system that a forced refresh is requested. The system must allow a forced refresh to take place while RFCK is low (refer to *Figure 3*). The $\overline{Refresh Request}$ signal on RF I/O may be connected to a $\overline{Hold}$ or $\overline{Bus Request}$ input to the system. The system acknowledges the $\overline{Hold}$ or $\overline{Bus Request}$ when ready, and outputs Hold Acknowledge or $\overline{Bus Request Acknowledge}$. If this is connected to the M2 ($\overline{RFSH}$) pin, a forced-refresh cycle will be initiated by the DP8409A, and $\overline{RAS}$ will be internally generated on all four $\overline{RAS}$ outputs, to strobe the refresh counter contents on the address outputs into all the DRAMs. An external $\overline{RAS}$ Generator Clock (RGCK) is required for this function. It is fed to the $\overline{CASIN}$ (RGCK) pin, and may be up to 10 MHz. Whenever M2 goes low (inducing a forced refresh), $\overline{RAS}$ remains high for one to two periods of RGCK, depending on when M2 goes low relative to the high-to-low triggering edge of RGCK; $\overline{RAS}$ then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to $\overline{RAS}$ going low, M2 should go low t$_{RFSRG}$ before the next falling edge of RGCK. The $\overline{Refresh Request}$ on RF I/O is terminated as $\overline{RAS}$ begins, so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh $\overline{RAS}$ will have ended, and normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh $\overline{RAS}$ end in less than 2 periods of RGCK from the time $\overline{RAS}$ went low, then M2 may be high earlier than t$_{RQHRF}$ after RGCK goes low and $\overline{RAS}$ will go high t$_{RFRH}$ after M2, if $\overline{CS}$ is low. If $\overline{CS}$ is high, the $\overline{RAS}$ will go high after 25 ns after M2 goes high.

To allow the forced refresh, the system will have been inactive for about 4 periods of RGCK, which can be as fast as 400 ns every RFCK cycle. To guarantee a refresh of 128 rows every 2 ms, a period of up to 16 μs is required for RFCK. In other words, the system may be down for as little as 400 ns every 16 μs, or 2.5% of the time. Although this is not excessive, it may be preferable to perform a Hidden Refresh each RFCK cycle, which is allowed while still in the Auto-Access mode, (Mode 5).
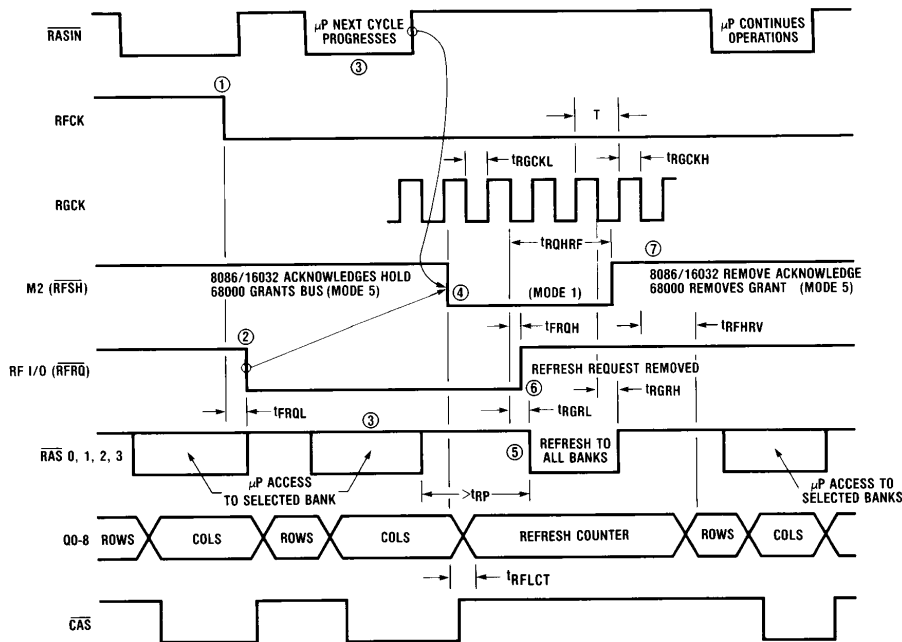

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FIGURE 3. DP8409A Performing a Forced Refresh (Mode 5 → 1 → 5) with Various Microprocessors

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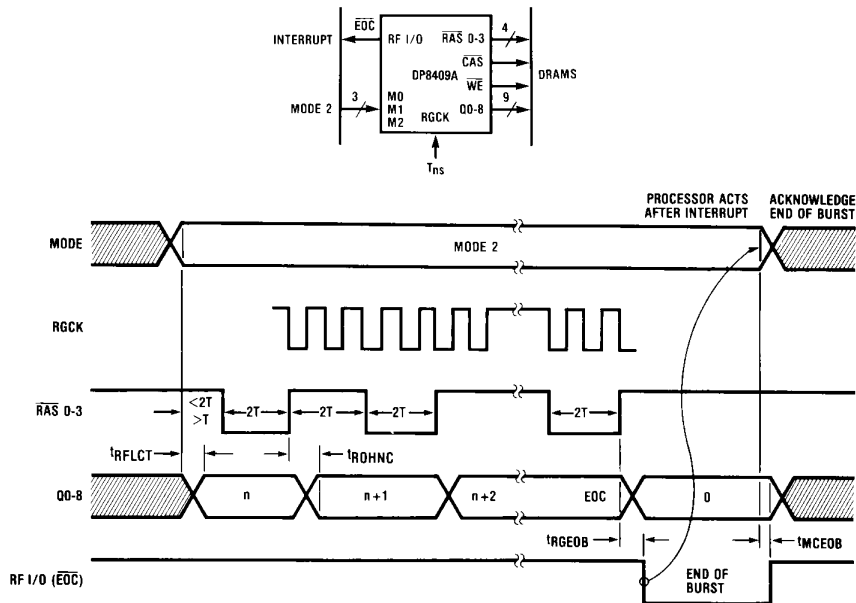## DP8409A Functional Mode Descriptions (Continued)

FIGURE 4. Auto-Burst Mode, Mode 2

TL/F/8409–11

MODE 2—AUTOMATIC BURST REFRESH

This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2 ms (see *Figure 4*). When the DP8409A enters this mode, $\overline{CASIN}$ (RGCK) becomes the $\overline{RAS}$ Generator Clock (RGCK), and $\overline{RASIN}$ is disabled. $\overline{CAS}$ remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last $\overline{RAS}$ has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to indicate the End-of-Burst conditions.

The signal on all four $\overline{RAS}$ outputs is just a divide-by-four of RGCK; in other words, if RGCK has a 100 ns period, $\overline{RAS}$ is high and low for 200 ns each cycle. The refresh counter increments at the end of each $\overline{RAS}$, starting from the count it contained when the mode was entered. If this was zero, then for a RGCK with a 100 ns period with End-of-Count set to 127, RF I/O will go low after 128×0.4 μs, or 51.2 μs. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins.

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the DP8409A (set to Mode 2), causing it to perform a complete burst refresh. When end-of-burst occurs (after 26 μs), power can then be removed from the DP8409A for 2 ms, consuming an average power of 1.3% of normal operating power. No control signal glitches occur when switching power to the DP8409A.

MODE 3a—ALL-$\overline{RAS}$ AUTOMATIC WRITE

Mode 3a is useful at system initialization, when the memory is being cleared (i.e., with all-zeros in the data field and the

corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All $\overline{RAS}$ outputs are activated, as in refresh, and so are $\overline{CAS}$ and $\overline{WE}$. To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations.

To select this mode, B1 and B0 must have previously been set to 00, 01, or 10 in Mode 7, depending on the DRAM size. For example, for 16k DRAMs, B1 and B0 are 00. For 64k DRAMs, B1 and B0 are 01, so that for the configuration of *Figure 1b*, the 8 refresh counter bits are strobed by $\overline{RAS}$ into the 7 row addresses and the ninth column address. After this Automatic-Write process, B1 and B0 must be set again in Mode 7 to 00 to set End-of-Count to 127. For the configuration of *Figure 1c*, B1 and B0 set to 01 will work for Automatic-Write and End-of-Count equals 255.

In this mode, R/$\overline{C}$ is disabled, $\overline{WE}$ is permanently enabled low, and $\overline{CASIN}$ (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127, 255, or 511 (as set by End-of-Count in Mode 7), and the $\overline{RAS}$ outputs are active.

Referring to *Figure 5a*, an external 8-bit counter (for 64k DRAMs) with TRI-STATE outputs is required and must be connected to the column address inputs. It is enabled only during this mode, and is clocked from RF I/O. The DP8409A refresh counter is used to address the rows, and the column address is supplied by the external counter. Every row for each column address is written to in all four banks. At the End-of-Count RF I/O goes low, which clocks the external counter.

Therefore, for each column address, the refresh counter first outputs row-0 to the address bus and all four $\overline{RAS}$ outputs strobe this row address into the DRAMs (see *Figure 5b*). A minimum of 30 ns after $\overline{RAS}$ goes low (t_{RAH} = 30 ns), the refresh counter is disabled and the column ad-

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DP8409A Functional Mode Descriptions (Continued)

dress input latch is enabled onto the address bus. About 14 ns after the column address is valid, $\overline{CAS}$ goes low, (t_{ASC} = +14 ns), strobing the column address into the DRAMs. When $\overline{RAS}$ and $\overline{CAS}$ go high the refresh counter increments to the next row and the cycle repeats. Since $\overline{WE}$ is kept low in this mode, the data at DI (input data) of the DRAMs is written into each row of the latched column. During each cycle $\overline{RAS}$ is high for two periods of RGCK and low for two periods, giving a total write-cycle time of 400 ns minimum, which is adequate for most 16k and 64k DRAMs. On the last row of a column, RF I/O increments the external counter to the next column address.

At the end of the last column address, an interrupt is generated from the external counter to let the system know that initialization has been completed. During the entire initialization time, the system can be performing other initialization functions. This approach to memory initialization is both automatic and fast. For instance, if four banks of 64k DRAMs are used, and RGCK is 100 ns, a write cycle to the same location in all four banks takes 400 ns, so the total time taken in initializing the 64k DRAMs is 65k $\times$ 400 ns or 26 ms. When the system receives the interrupt, the external counter must be permanently disabled. ADS and $\overline{CS}$ are interfaced by the system, and the DP8409A mode is changed. The interrupt must then be disabled.
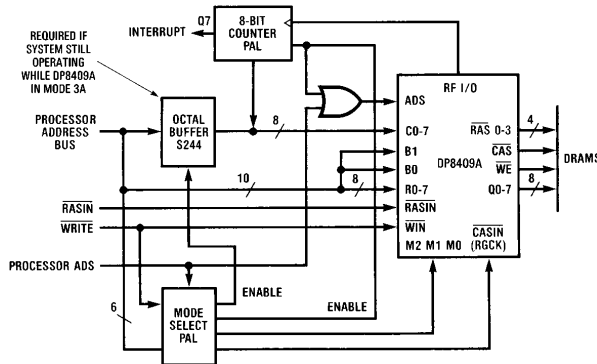
TL/F/8409–12

FIGURE 5a. DP8409A Extra Circuitry Required for All-$\overline{RAS}$ Auto Write Mode, Mode 3a
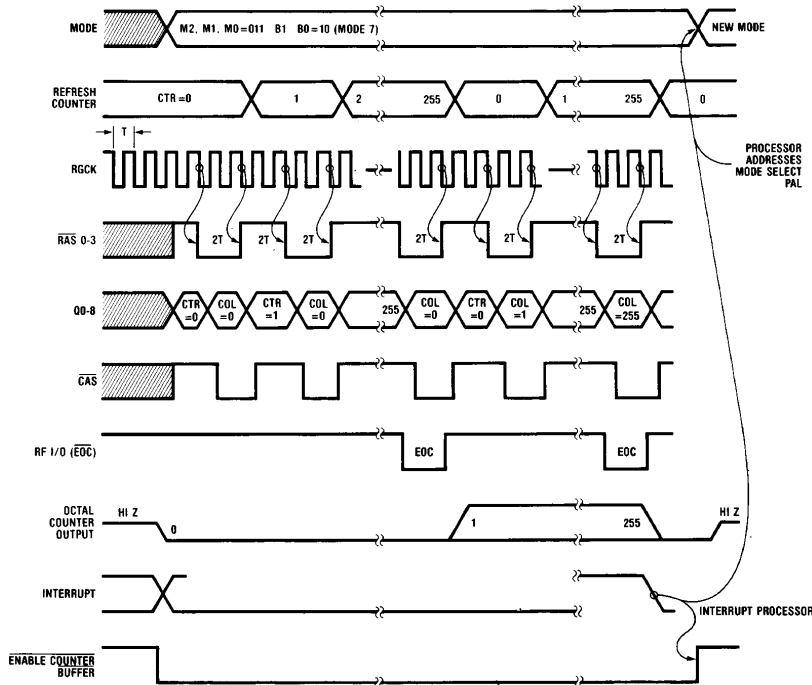
TL/F/8409–13

FIGURE 5b. DP8409A All-$\overline{RAS}$ Auto Write Mode, Mode 3a, Timing Waveform

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DP8409A Functional Mode Descriptions (Continued)

MODE 3b—EXTERNALLY CONTROLLED ALL-$\overline{RAS}$ WRITE

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialization, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the DP8409A for the next write cycle. This method is slower than Mode 3a since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialization, and is not free for other initialization operations. However, initialization sequence timing is under system control, which may provide some system advantage.

MODE 4—EXTERNALLY CONTROLLED ACCESS

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in *Figure 6*.

Output Address Selection

Refer to *Figure 7a*. With M2 ($\overline{RFSH}$) and R/$\overline{C}$ high, the row address latch contents are transferred to the multiplexed address bus output Q0–Q8, provided $\overline{CS}$ is set low. The column address latch contents are output after R/$\overline{C}$ goes low. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0–Q8. This selects one of the $\overline{RAS}$ outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 ns later column addresses appear on the Q outputs.

*Resistors required depends on DRAM load.

DRAMs MAYBE 16K, 64K OR 256K

FOR 4 BANKS, CAN DRIVE 16 DATA BITS +6 CHECK BITS FOR ECC

FOR 2 BANKS, CAN DRIVE 32 DATA BITS +7 CHECK BITS FOR ECC

FOR 1 BANK, CAN DRIVE 64 DATA BITS +8 CHECK BITS FOR ECC

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FIGURE 6. Typical Application of DP8409A Using External Control Access and Refresh in Modes 0 and 4

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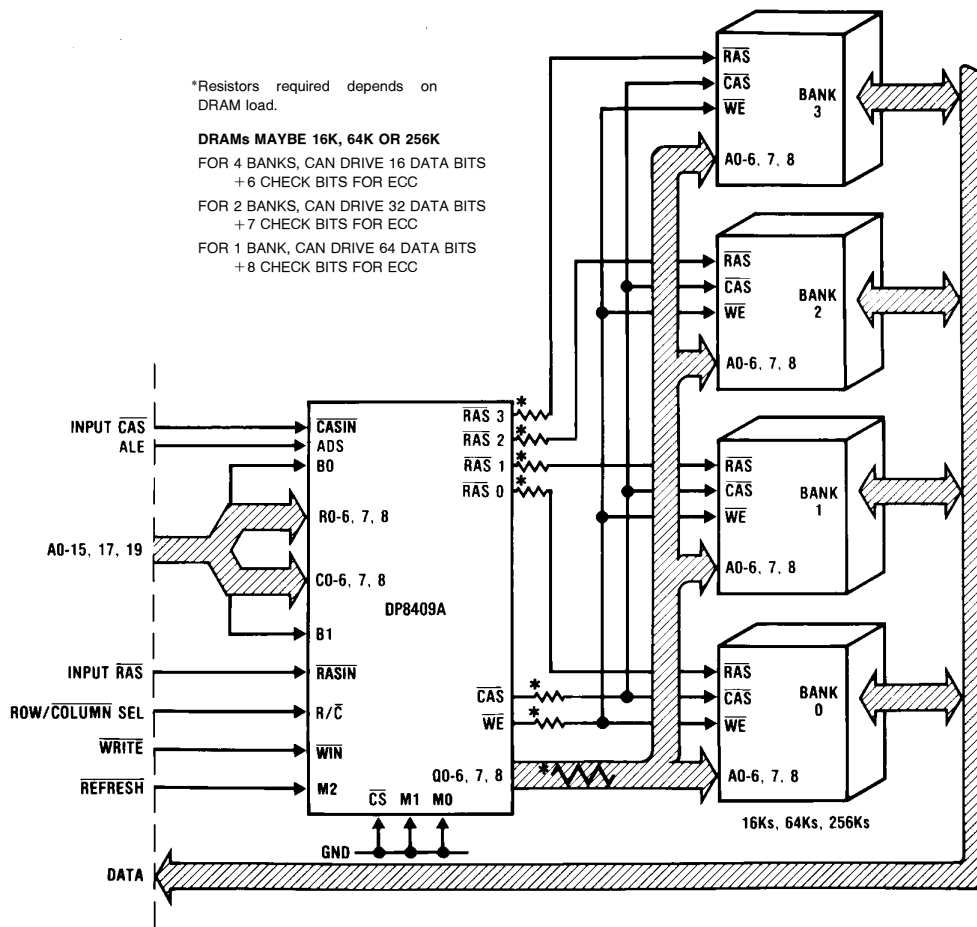
DP8409A Functional Mode Descriptions (Continued)
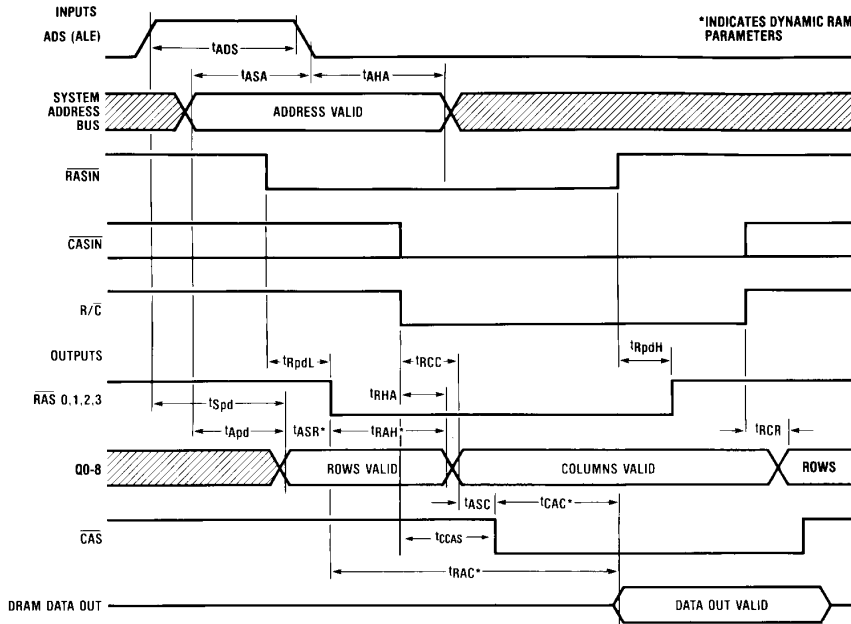
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FIGURE 7a. Read Cycle Timing (Mode 4)

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FIGURE 7b. Write Cycle Timing (Mode 4)

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DP8409A Functional Mode Descriptions (Continued)

Automatic CAS Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/$\overline{C}$. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see *Figure 7b*). If $\overline{CASIN}$ is low when R/$\overline{C}$ goes low, $\over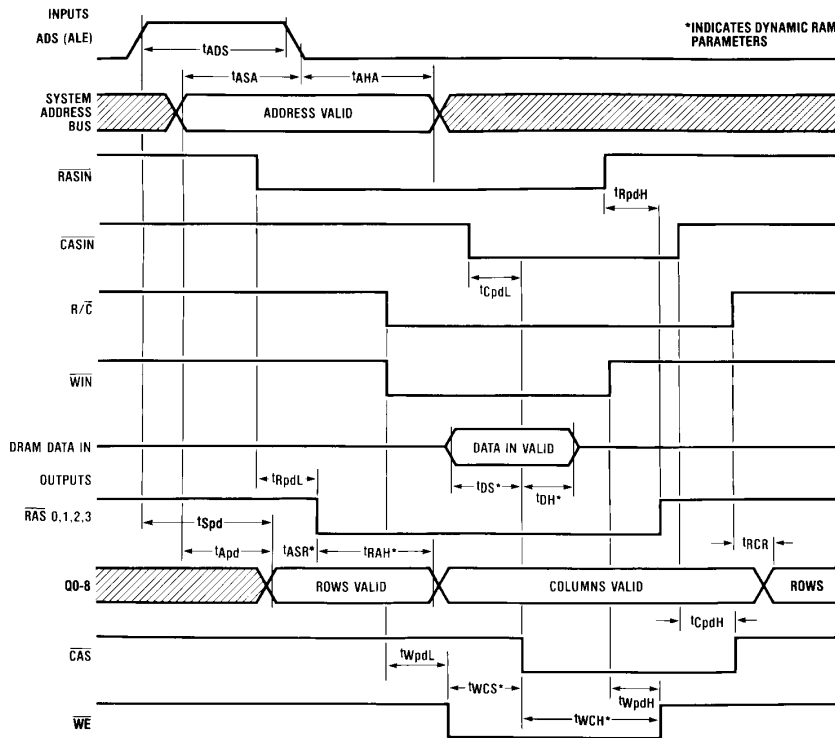line{CAS}$ will be automatically generated, following the row to column transition by about 20 ns (see *Figure 7a*). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or -10 ns. In other words, a t_{ASC} greater than 0 ns is safe.

Fast Memory Access

AC parameters t_{DIF1}, t_{DIF2} may be used to determine the minimum delays required between $\overline{RASIN}$, R/$\overline{C}$, and $\overline{CASIN}$ (see Application Brief 9; "Fastest DRAM Access Mode").

MODE 5—AUTOMATIC ACCESS WITH HIDDEN REFRESH

The Auto Access with Hidden Refresh mode has two advantages over the Externally Controlled Access mode, due to the fact that all outputs except $\overline{WE}$ are initiated from $\overline{RASIN}$. First, inputs R/$\overline{C}$ and $\overline{CASIN}$ are unnecessary and can be used for other functions (see Refreshing, below). Secondly, because the output control signals are derived internally from one input signal ($\overline{RASIN}$), timing-skew problems are reduced, thereby reducing memory access time substantially or allowing use of slower DRAMs. The automatic access features of Mode 5 (and Mode 6) of the DP8409A make DRAM accessing appear essentially "static".

Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multi-plexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{CAS}$ occurs. This is all performed automatically by the DP8409A in this mode.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the DP8409A. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The DP8409A in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see *Figure 8a*).

Next, the row address is disabled after t_{RAH} (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typcial figures are for heavy capacitive loading, of approximately 88 DRAMs.

This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.
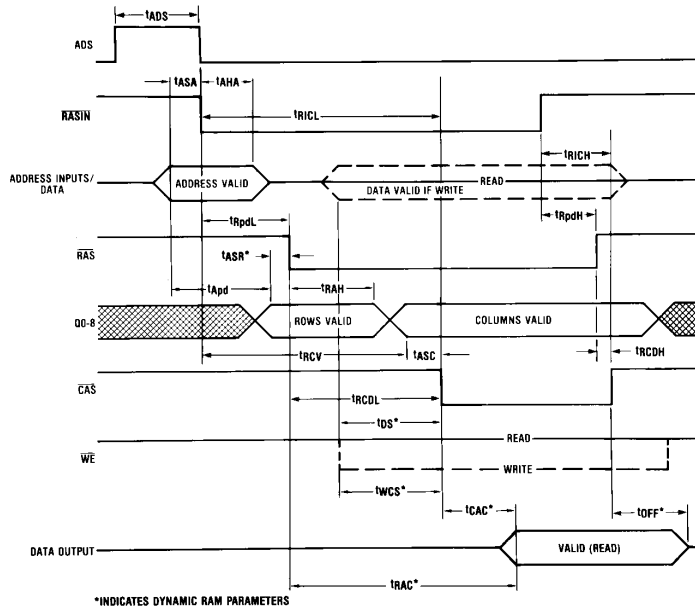
Refreshing

Because R/$\overline{C}$ and $\overline{CASIN}$ are not used in this mode, R/$\overline{C}$ becomes RFCK (refresh clock) and $\overline{CASIN}$ becomes RGCK ($\overline{RAS}$ generator clock). With these two signals it is possible to peform refreshing without extra ICs, and without holding up the processor.

One refresh cycle must occur during each refresh clock period and then the refresh address must be incremented to the next refresh cycle. As long as 128 rows are refreshed every 2 ms (one row every 16 μs), all 16k and 64k DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than 16 μs. RFCK going high sets an internal refresh-request flip-flop. First the DP8409A will attempt to perform a hidden refresh so that the system throughput will not be affected. If, during the time RFCK is high, $\overline{CS}$ on the DP8409A goes high and $\overline{RASIN}$ occurs, a hidden refresh will occur. In this case, $\overline{RASIN}$ should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the DP8409A will perform a refresh. The refresh counter is enabled to the address outputs whenever $\overline{CS}$ goes high with RFCK high, and all $\overline{RAS}$ outputs follow $\overline{RASIN}$. If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flip-flop is reset so no further refresh can occur until the next RFCK period starts with the positive-going edge of RFCK. Refer to *Figure 9*.

To determine the probability of a Hidden Refresh occurring, assume each system cycle takes 400 ns and RFCK is high for 8 μs, then the system has 20 chances to not select the DP8409A. If during this time a hidden refresh did not occur, then the DP8409A forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After RFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 ($\overline{RFSH}$) low does the DP8409A initiate a forced refresh (which is performed automatically). Refer to Mode 1, and *Figure 3*. The internal refresh request flip-flop is then reset.

Figure 9 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and $\overline{CS}$ again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic "1") and the address outputs go TRI-STATE until $\overline{CS}$ again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50-percent; in fact, the low-time should be designed to be a minimum. This is determined by the worst-case time (required by the system) to respond to the DP8409A's forced-refresh request.

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DP8409A Functional Mode Descriptions (Continued)

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FIGURE 8a. Modes 5, 6 Timing (CASIN High in Mode 6)
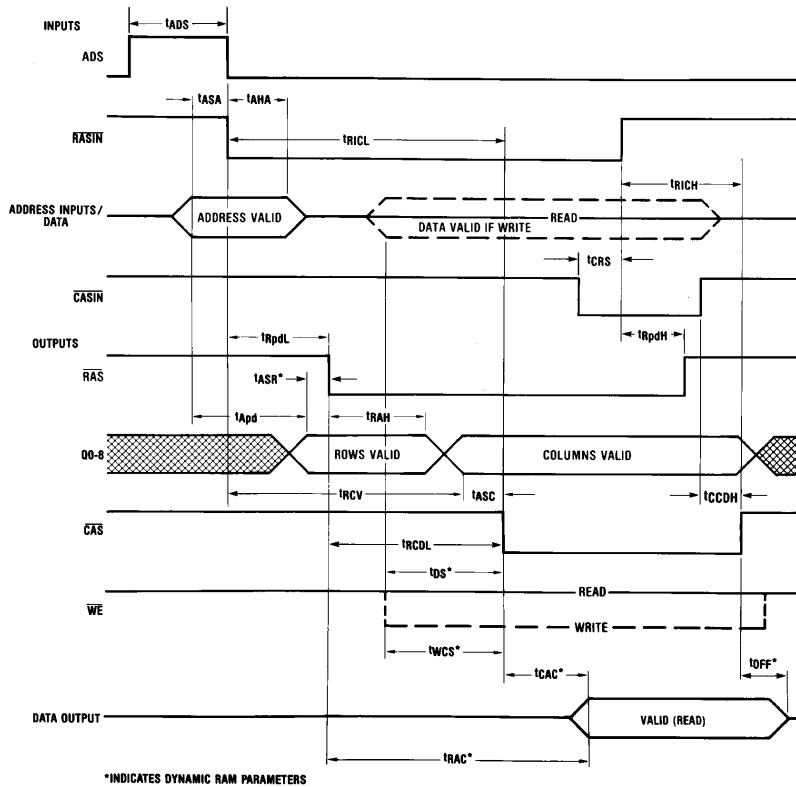
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FIGURE 8b. Mode 6 Timing, Extended CAS

DP8409A Functional Mode Descriptions (Continued)
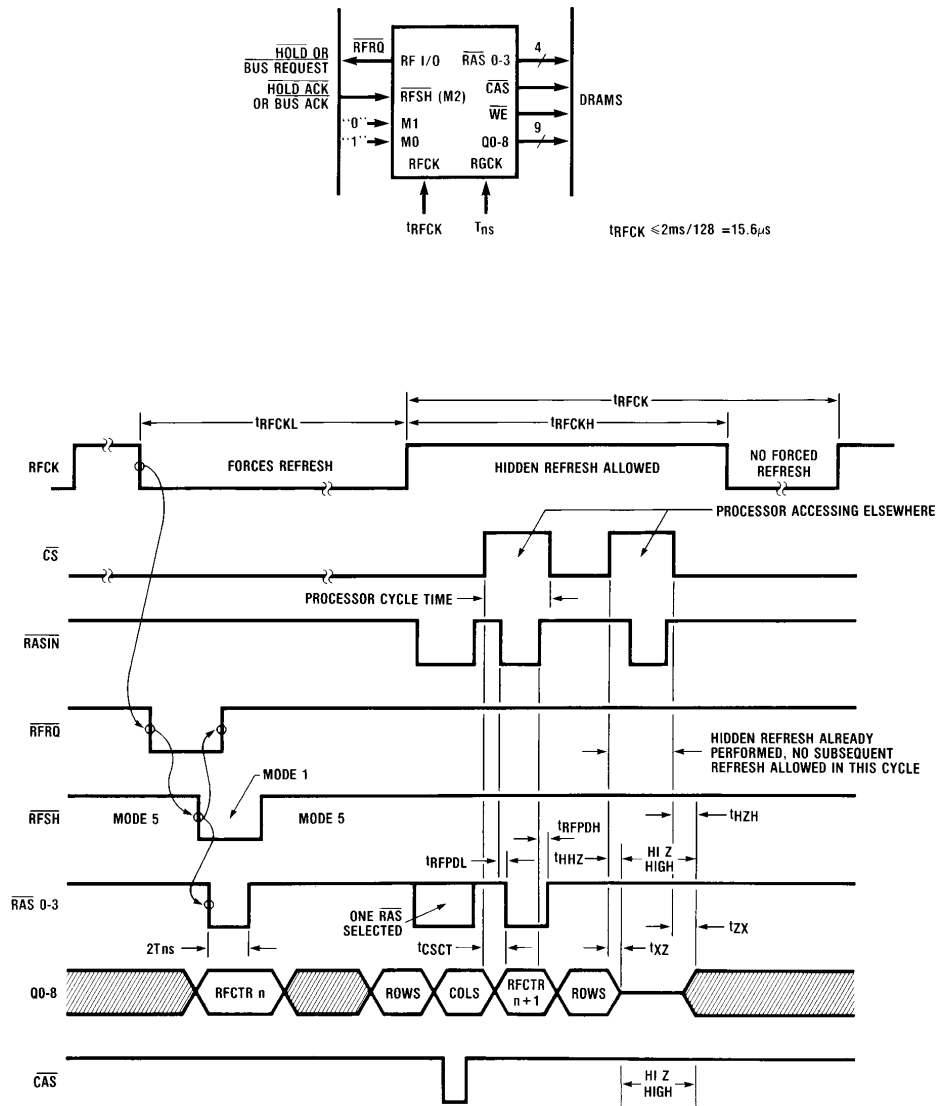
FIGURE 9. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing

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DP8409A Functional Mode Descriptions (Continued)

TABLE II. Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Note that $\overline{RASIN}$ going low earlier than t_{CSRL} after $\overline{CS}$ goes low may result in the DP8409A interpreting the $\overline{RASIN}$ as a hidden refresh $\overline{RASIN}$ if no hidden refresh has occurred in the current RFCK cycle. In this case, all $\overline{RAS}$ outputs would go low for a short time. Thus, it is suggested that when using Mode 5, $\overline{RASIN}$ should be held high until t_{CSRL} after $\overline{CS}$ goes low if a refresh is not intended. Similarly, $\overline{CS}$ should be held low for a minimum of t_{CSRL} after $\overline{RASIN}$ returns high when ending the access in Mode 5.

MODE 6—FAST AUTOMATIC ACCESS

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20 ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10 ns to 15 ns) in applications requiring fast access times; $\overline{RASIN}$ to $\overline{CAS}$ is typically 105 ns.

In this mode, the R/$\overline{C}$ (RFCK) pin is not used, but $\overline{CASIN}$ (RGCK) is used as $\overline{CASIN}$ to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to *Figure 8b*. This is de-

sirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by $\overline{CASIN}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{CASIN}$ subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, $\overline{CASIN}$ should be set high in Mode 6.

There is no internal refresh-request flip-flop in this mode, so any refreshing required must be done by entering Mode 0 or Mode 2.

MODE 7—SET END-OF-COUNT

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table III). With B1 and B0 the same $\overline{EOC}$ is 127; with B1 = 0 and B0 = 1, $\overline{EOC}$ is 255; and with B1 = 1 and B0 = 0, $\overline{EOC}$ is 511. This selected value of $\overline{EOC}$ will be used until the next Mode 7 selection. At power-up the $\overline{EOC}$ is automatically set to 127 (B1 and B0 set to 11).

TABLE III. Mode 7

Bank Select (Strobed by ADS)		End of Count Selected
B1	B0	
0	0	127
0	1	255
1	0	511
1	1	127
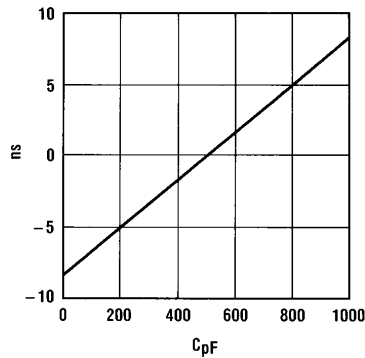
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FIGURE 10. Change in Propagation Delay vs. Loading Capacitance Relative to a 500 pF Load

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Storage Temperature Range	$-65°C$ to $+150°C$
Input Voltage	5.5V
Output Current	150 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Maximum Power Dissipation* at 25°C

Cavity Package	3542 mW
Molded Package	2833 mW

*Derate cavity package 23.6 mW/°C above 25°C; derate molded package 22.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.75	5.25	V
T_A Ambient Temperature	0	$+70$	°C

Electrical Characteristics $V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ (unless otherwise noted) (Notes 2, 6)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_C	Input Clamp Voltage	$V_{CC} = $ Min, $I_C = -12$ mA		-0.8	-1.2	V
I_{IH1}	Input High Current for ADS, R/$\overline{C}$ Only	$V_{IN} = 2.5V$		2.0	100	μA
I_{IH2}	Input High Current for All Other Inputs*	$V_{IN} = 2.5V$		1.0	50	μA
I_I RSI	Output Load Current for RF I/O	$V_{IN} = 0.5V$, Output High		-1.5	-2.5	mA
I_I CTL	Output Load Current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	$V_{IN} = 0.5V$, Chip Deselect		-1.5	-2.5	mA
I_{IL1}	Input Low Current for ADS, R/$\overline{C}$ Only	$V_{IN} = 0.5V$		-0.1	-1.0	mA
I_{IL2}	Input Low Current for All Other Inputs*	$V_{IN} = 0.5V$		-0.05	-0.5	mA
V_{IL}	Input Low Threshold				0.8	V
V_{IH}	Input High Threshold		2.0			V
V_{OL1}	Output Low Voltage*	$I_{OL} = 20$ mA		0.3	0.5	V
V_{OL2}	Output Low Voltage for RF I/O	$I_{OL} = 10$ mA		0.3	0.5	V
V_{OH1}	Output High Voltage*	$I_{OH} = -1$ mA	2.4	3.5		V
V_{OH2}	Output High Voltage for RF I/O	$I_{OH} = -100 \mu$A	2.4	3.5		V
I_{1D}	Output High Drive Current*	$V_{OUT} = 0.8V$ (Note 3)		-200		mA
I_{0D}	Output Low Drive Current*	$V_{OUT} = 2.7V$ (Note 3)		200		mA
I_{OZ}	TRI-STATE Output Current (Address Outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, $\overline{CS} = 2.0V$, Mode 4	-50	1.0	50	μA
I_{CC}	Supply Current	$V_{CC} = $ Max		250	325	mA

*Except RF I/O Output.

Switching Characteristics: DP8409A/DP8409A-3

$V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, $C_L = 500$ pF; $\overline{RAS0}$–$\overline{RAS3}$, $C_L = 150$ pF; $\overline{WE}$, $C_L = 500$ pF; $\overline{CAS}$, $C_L = 600$ pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	8409			8409A-3			Units
			Min	Typ	Max	Min	Typ	Max	
ACCESS									
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*	95	125	160	95	125	185	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*	80	105	140	80	105	160	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*	40	48	60	40	48	70	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*	50	63	80	50	63	95	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*		98	125		98	145	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*		78	105		78	120	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 8a*		40	65		40	65	ns

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Switching Characteristics: DP8409A/DP8409A-3 (Continued)

$V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, $C_L = 500$ pF; $\overline{RAS0}$–$\overline{RAS3}$, $C_L = 150$ pF; $\overline{WE}$, $C_L = 500$ pF; $\overline{CAS}$, $C_L = 600$ pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	DP8409A			DP8409A-3			Units
			Min	Typ	Max	Min	Typ	Max	
ACCESS (Continued)									
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 8b	40	54	70	40	54	80	ns
t_{RAH}	Row Address Hold Time (Mode 5)	Figure 8a	30			30			ns
t_{RAH}	Row Address Hold Time (Mode 6)	Figures 8a, 8b	20			20			ns
t_{ASC}	Column Address Setup Time (Mode 5)	Figure 8a	8			8			ns
t_{ASC}	Column Address Setup Time (Mode 6)	Figures 8a, 8b	6			6			ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	Figure 8a		90	120		90	140	ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	Figures 8a, 8b		75	105		75	120	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 7a, 7b, 8a, 8b	20	27	35	20	27	40	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 7a, 7b, 8a, 8b	15	23	32	15	23	37	ns
t_{APDL}	Address Input to Output Low Delay	Figures 7a, 7b, 8a, 8b		25	40		25	46	ns
t_{APDH}	Address Input to Output High Delay	Figures 7a, 7b, 8a, 8b		25	40		25	46	ns
t_{SPDL}	Address Strobe to Address Output Low	Figures 7a, 7b		40	60		40	70	ns
t_{SPDH}	Address Strobe to Address Output High	Figures 7a, 7b		40	60		40	70	ns
t_{ASA}	Address Set-Up Time to ADS	Figures 7a, 7b, 8a, 8b	15			15			ns
t_{AHA}	Address Hold Time from ADS	Figures 7a, 7b, 8a, 8b	15			15			ns
t_{ADS}	Address Strobe Pulse Width	Figures 7a, 7b, 8a, 8b	30			30			ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 7b	15	25	30	15	25	35	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 7b	15	30	60	15	30	70	ns
t_{CRS}	$\overline{CASIN}$ Set-Up Time to $\overline{RASIN}$ High (Mode 6)	Figure 8b	35			35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ Low in Mode 4)	Figure 7b	32	41	68	32	41	77	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ Low in Mode 4)	Figure 7b	25	39	50	25	39	60	ns
t_{RCC}	Column Select to Column Address Valid	Figure 7a		40	58		40	67	ns
t_{RCR}	Row Select to Row Address Valid	Figures 7a, 7b		40	58		40	67	ns
t_{RHA}	Row Address Held from Column Select	Figure 7a	10			10			ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low (Mode 4 Auto $\overline{CAS}$)	Figure 7a		65	90				ns
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$)	See Mode 4 Descrip.			13			18	ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$)	See Mode 4 Descrip.			13			18	ns
REFRESH									
t_{RC}	Refresh Cycle Period	Figure 2	100			100			ns
$t_{RASINL, H}$	Pulse Width of $\overline{RASIN}$ during Refresh	Figure 2	50			50			ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figures 2, 9	35	50	70	35	50	80	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figures 2, 9	30	40	55	30	40	65	ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = X, Figures 2, 3, 4		47	60		47	70	ns

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Switching Characteristics: DP8409A/DP8409A-3 (Continued)

$V_{CC} = 5.0V \pm 5\%$, $0°C \le T_A \le 70°C$ (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, $C_L = 500$ pF; $\overline{RAS0}$–$\overline{RAS3}$, $C_L = 150$ pF; $\overline{WE}$, $C_L = 500$ pF; $\overline{CAS}$, $C_L = 600$ pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	DP8409A			DP8409A-3			Units
			Min	Typ	Max	Min	Typ	Max	
REFRESH (Continued)									
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	*Figures 2, 3*		45	60		45	70	ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	*Figures 2, 4*		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	$C_L = 50$ pF, *Figure 2*			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	$C_L = 50$ pF, *Figure 2*			80			80	ns
t_{RGEOB}	RGCK Low to End-of-Burst Low	$C_L = 50$ pF, *Figure 4*			95			95	ns
t_{MCEOB}	Mode Change to End-of-Burst High	$C_L = 50$ pF, *Figure 4*			75			75	ns
t_{RST}	Counter Reset Pulse Width	*Figure 2*	70			70			ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	*Figure 2*			100			100	ns
$t_{RFCKL, H}$	Minimum Pulse Width of RFCK	*Figure 9*	100			100			ns
T	Period of $\overline{RAS}$ Generator Clock	*Figure 3*	100			100			ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	*Figure 3*	35			40			ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	*Figure 3*	35			40			ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ Low	$C_L = 50$ pF, *Figure 3*		20	30		20	30	ns
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	$C_L = 50$ pF, *Figure 3*		50	75		50	75	ns
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	*Figure 3*	50	65	95	50	65	95	ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	*Figure 3*	40	60	85	40	60	85	ns
t_{RQHRF}	$\overline{RFSH}$ Hold Time from $\overline{RFSH}$ $\overline{RQST}$ (RF I/O)	*Figure 3*	2T			2T			ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (ending forced RFSH)	See Mode 1 Descrip.	55	80	110	55	80	125	ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-Up to RGCK Low (Mode 1)	See Mode 1 Descrip.	35			40			ns
t_{CSCT}	$\overline{CS}$ High to RFSH Counter Valid	*Figure 9*		55	70		55	75	ns
t_{CSRL}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low	See Mode 5 Descrip.	30			30			ns
TRI-STATE									
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	*Figures 9, 12,* R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	$C_L = 15$ pF, *Figures 9, 12,* R2 = 1k, S1 Open		20	40		20	40	ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	*Figures 9, 12,* R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	$C_L = 15$ pF, *Figures 9, 12,* R1 = 1k, S2 Open		25	50		25	50	ns
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	*Figures 9, 12,* R2 = 750Ω, S1 Open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	$C_L = 15$ pF, *Figures 9, 12,* R2 = 750Ω, S1 Open		40	75		40	75	ns

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Switching Characteristics: DP8409A/DP8409A-3 (Continued)

$V_{CC} = 5.0V \pm 5\%$, 0°C $\leq T_A \leq$ 70°C (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	DP8409A			DP8409A-3			Units
			Min	Typ	Max	Min	Typ	Max	
TRI-STATE (Continued)									
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	*Figure 12,* S1, S2 Open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	C_L = 15 pF, *Figure 12,* R2 = 750Ω, S1 Open		50	80		50	80	ns

Switching Characteristics: DP8409A-2

$V_{CC} = 5.0V \pm 5\%$, 0°C $\leq T_A \leq$ 70°C (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, C_L = 500 pF; $\overline{RAS0}$–$\overline{RAS3}$, C_L = 150 pF; $\overline{WE}$, C_L = 500 pF; $\overline{CAS}$, C_L = 600 pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	8409A-2			Units
			Min	Typ	Max	
ACCESS						
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*	75	100	130	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*	65	90	115	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*	40	48	60	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*	50	63	80	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*		75	100	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figures 8a, 8b*		65	85	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	*Figure 8a*		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 8a*		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	*Figure 8b*	40	54	70	ns
t_{RAH}	Row Address Hold Time (Mode 5) (Note 7)	*Figure 8a*	20			ns
t_{RAH}	Row Address Hold Time (Mode 6) (Note 7)	*Figures 8a, 8b*	12			ns
t_{ASC}	Column Address Set-Up Time (Mode 5)	*Figure 8a*	3			ns
t_{ASC}	Column Address Set-Up Time (Mode 6)	*Figures 8a, 8b*	3			ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	*Figure 8a*		80	105	ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	*Figures 8a, 8b*		70	90	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	*Figures 7a, 7b, 8a, 8b*	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	*Figures 7a, 7b, 8a, 8b*	15	23	32	ns
t_{APDL}	Address Input to Output Low Delay	*Figures 7a, 7b, 8a, 8b*		25	40	ns
t_{APDH}	Address Input to Output High Delay	*Figures 7a, 7b, 8a, 8b*		25	40	ns
t_{SPDL}	Address Strobe to Address Output Low	*Figures 7a, 7b*		40	60	ns
t_{SPDH}	Address Strobe to Address Output High	*Figures 7a, 7b*		40	60	ns
t_{ASA}	Address Set-Up Time to ADS	*Figures 7a, 7b, 8a, 8b*	15			ns
t_{AHA}	Address Hold Time from ADS	*Figures 7a, 7b, 8a, 8b*	15			ns
t_{ADS}	Address Strobe Pulse Width	*Figures 7a, 7b, 8a, 8b*	30			ns

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Switching Characteristics: DP8409A-2 (Continued)

$V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, $C_L = 500$ pF; $\overline{RAS0}$–$\overline{RAS3}$, $C_L = 150$ pF; $\overline{WE}$, $C_L = 500$ pF; $\overline{CAS}$, $C_L = 600$ pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	8409A-2			Units
			Min	Typ	Max	
ACCESS (Continued)						
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 7b*	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	*Figure 7b*	15	30	60	ns
t_{CRS}	$\overline{CASIN}$ Set-Up Time to $\overline{RASIN}$ High (Mode 6)	*Figure 8b*	35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ Low in Mode 4)	*Figure 7b*	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ Low in Mode 4)	*Figure 7b*	25	39	50	ns
t_{RCC}	Column Select to Column Address Valid	*Figure 7a*		40	58	ns
t_{RCR}	Row Select to Row Address Valid	*Figures 7a, 7b*		40	58	ns
t_{RHA}	Row Address Held from Column Select	*Figure 7a*	10			ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low (Mode 4 Auto $\overline{CAS}$)	*Figure 7a*		55	75	ns
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$)	See Mode 4 Descript.			13	ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$)	See Mode 4 Descript.			13	ns
REFRESH						
t_{RC}	Refresh Cycle Period	*Figure 2*	100			ns
$t_{RASINL, H}$	Pulse Width of $\overline{RASIN}$ during Refresh	*Figure 2*	50			ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	*Figures 2, 9*	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	*Figures 2, 9*	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS} = X$, *Figures 2, 3, 4*		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	*Figures 2, 3*		45	60	ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	*Figures 2, 4*		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	$C_L = 50$ pF, *Figure 2*			80	ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	$C_L = 50$ pF, *Figure 2*			80	ns
t_{RGEOB}	RGCK Low to End-of-Burst Low	$C_L = 50$ pF, *Figure 4*			95	ns
t_{MCEOB}	Mode Change to End-of-Burst High	$C_L = 50$ pF, *Figure 4*			75	ns
t_{RST}	Counter Reset Pulse Width	*Figure 2*	70			ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	*Figure 2*			100	ns
$t_{RFCKL, H}$	Minimum Pulse Width of RFCK	*Figure 9*	100			ns
T	Period of $\overline{RAS}$ Generator Clock	*Figure 3*	100			ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	*Figure 3*	35			ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	*Figure 3*	35			ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ Low	$C_L = 50$ pF, *Figure 3*		20	30	ns

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Switching Characteristics: DP8409A-2 (Continued)

$V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ (unless otherwise noted) (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q8, $C_L = 500$ pF; $\overline{RAS0}$–$\overline{RAS3}$, $C_L = 150$ pF; $\overline{WE}$, $C_L = 500$ pF; $\overline{CAS}$, $C_L = 600$ pF, (unless otherwise noted). See *Figure 11* for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7 kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Parameter	Conditions	8409A-2 Min	8409A-2 Typ	8409A-2 Max	Units
REFRESH (Continued)						
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	$C_L = 50$ pF, *Figure 3*		50	75	ns
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	*Figure 3*	50	65	95	ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	*Figure 3*	40	60	85	ns
t_{RQHRF}	$\overline{RFSH}$ Hold Time from $\overline{RFSH}$ $\overline{RQST}$ (RF I/O)	*Figure 3*	2T			ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (Ending Forced RFSH)	See Mode 1 Descrip.	55	80	110	ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-Up to RGCK Low (Mode 1)	See Mode 1 Descrip.	35			ns
t_{CSCT}	$\overline{CS}$ High to RFSH Counter Valid	*Figure 9*		55	70	ns
t_{CSRL}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low	See Mode 5 Descrip.	30			ns
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	*Figures 9, 12*, R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	$C_L = 15$ pF, *Figures 9, 12*, R2 = 1k, S1 Open		20	40	ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	*Figures 9, 12*, R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	$C_L = 15$ pF, *Figures 9, 12*, R1 = 1k, S2 Open		25	50	ns
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	*Figures 9, 12*, R2 = 750Ω, S1 Open		50	80	ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	$C_L = 15$ pF, *Figures 9, 12*, R2 = 750Ω, S1 Open		40	75	ns
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	*Figure 12*, S1, S2 Open		45	75	ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	$C_L = 15$ pF, *Figure 12*, R2 = 750Ω, S1 Open		50	80	ns

Input Capacitance $T_A = 25°C$ (Notes 2, 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance ADS, R/$\overline{C}$			8		pF
C_{IN}	Input Capacitance All Other Inputs			5		pF

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing these parameters. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F = 2.5$ ns, f = 2.5 MHz, $t_{PW} = 200$ ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

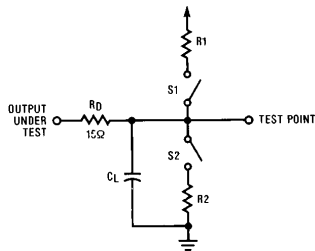**Note 5:** The load capacitance on RF I/O should not exceed 50 pF.

Note 6: Applies to all DP8409A versions unless otherwise specified.

Note 7: The DP8409A-2 device can only be used with memory devices that meet the t_{RAH} specification indicated.
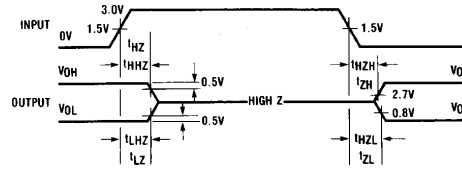
20

Applications

If external control is preferred, the DP8409A may be used in Mode 0 or 4, as in *Figure 6*.

If basic auto access and refresh are required, then in cases where the user requires the minimum of external complexity, Modes 1 and 5 are ideal, as shown in *Figure 13a*. The DP843X2 is used to provide proper arbitration between memory access and refresh. This chip supplies all the necessary control signals to the processor as well as the DP8409A. Furthermore, two separate $\overline{CAS}$ outputs are also included for systems using byte-writing. The refresh clock RFCK may be divided down from either RGCK using an IC counter such as the DM74LS393 or better still, the DP84300 Programmable Refresh Timer. The DP84300 can provide RFCK periods ranging from 15.4 μs to 15.6 μs based on the input clock of 2 to 10 MHz. *Figure 13b* shows the general timing diagram for interfacing the DP8409A to different microprocessors using the interface controller DP843X2.
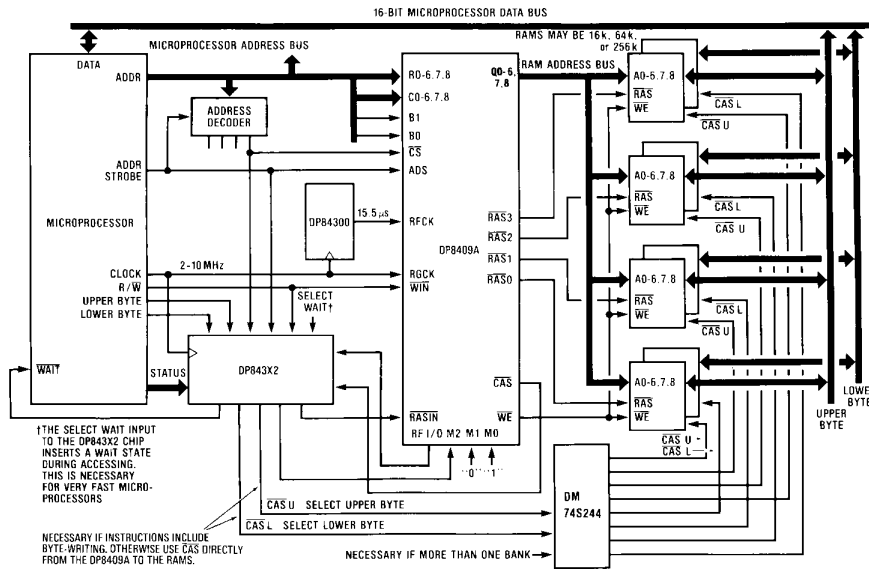
If the system is complex, requiring automatic access and refresh, burst refresh, and all-banks auto-write, then more circuitry is required to select the mode. This may be accomplished by utilizing a PAL®. The PAL has two functions. One as an address comparator, so that when the desired port address occurs (programmed in the PAL), the comparator gates the data into a latch, where it is connected to the mode pins of the DP8409A. Hence the mode of the DP8409A can be changed as desired with one PAL chip merely by addressing the PAL location, and then outputting data to the mode-control pins. In this manner, all the automatic modes may be selected, assigning R/C as RFCK always, and $\overline{CASIN}$ as RGCK always. The output from $\overline{RF\ I/O}$ may be used as End-of-Count to an interrupt, or $\overline{Refresh\ Request}$ to $\overline{HOLD}$ or $\overline{BUS\ REQUEST}$. A complex system may use Modes 5 and 1 for automatic access and refresh, Modes 3a and 7 for system initialization, and Mode 2 (auto-burst refresh) before and after DMA.

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FIGURE 11. Output Load Circuit

TL/F/8409–22

FIGURE 12. Waveform

TL/F/8409–23

FIGURE 13a. Connecting the DP8409A Between the 16-Bit Microprocessor and Memory
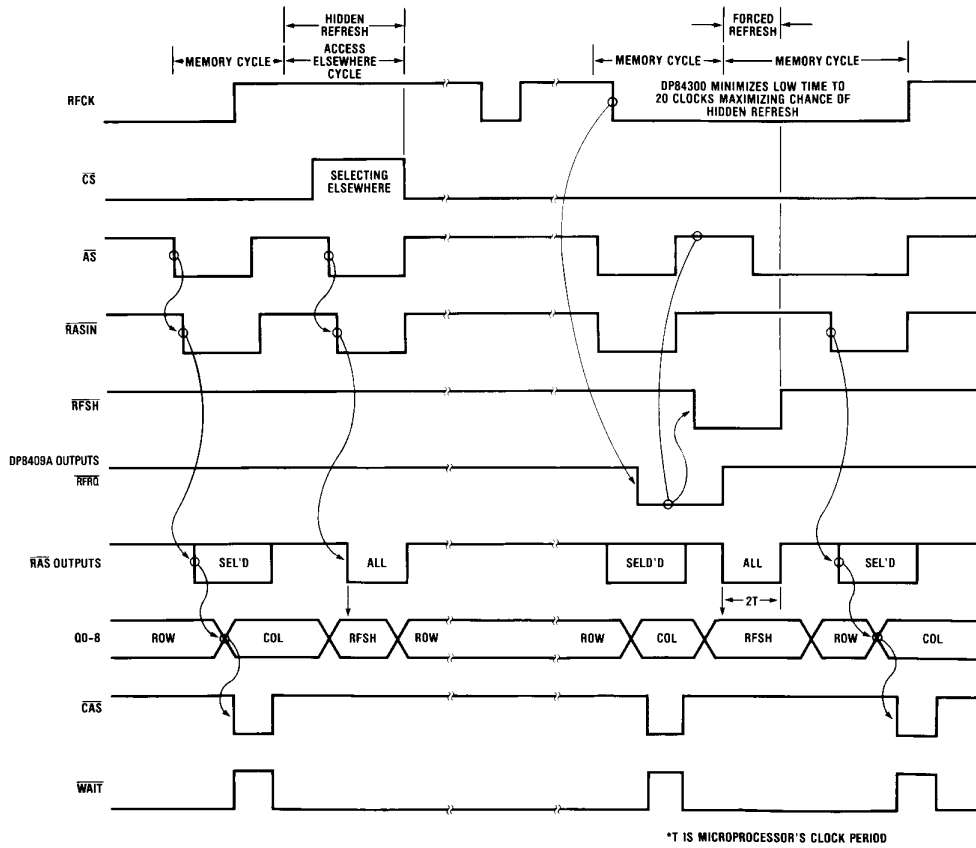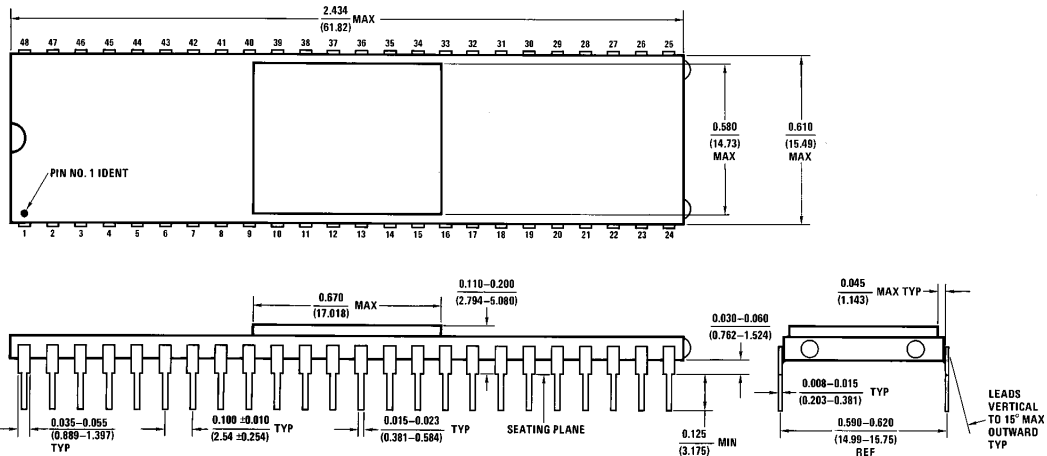
21

Applications (Continued)
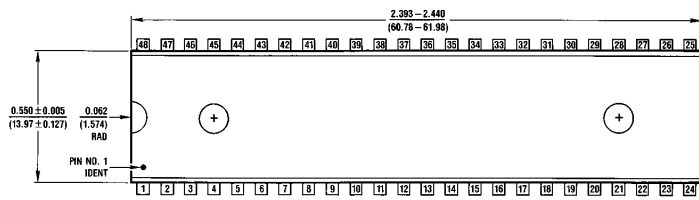

TL/F/8409-24

FIGURE 13b. DP8409A Auto Refresh

Physical Dimensions inches (millimeters)

48-Lead Dual-In-Line Package (D)
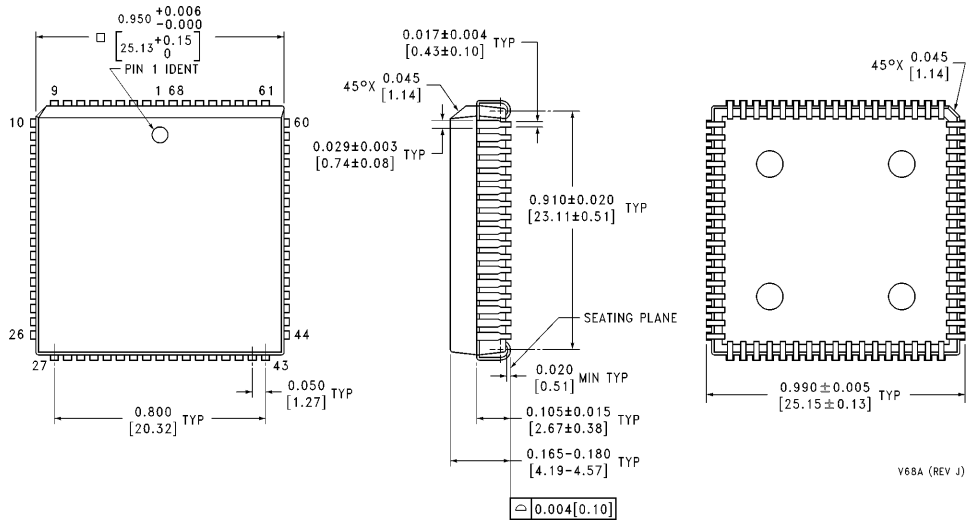**Order Number DP8409AD, DP8409AD-2 or DP8409AD-3**
NS Package Number D48A

48-Lead Molded Dual-In-Line Package (N)
Order Number DP8409AN, DP8409AN-2 or DP8409AN-3
NS Package Number N48A

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Physical Dimensions inches (millimeters) (Continued)

0.950 +0.006 −0.000

[25.13 +0.15 0]

PIN 1 IDENT

9   1 68   61

10   60

26   44

27   43

0.050 [1.27] TYP

0.800 [20.32] TYP

0.017±0.004 [0.43±0.10] TYP

45°X 0.045 [1.14]

0.029±0.003 [0.74±0.08] TYP

0.910±0.020 [23.11±0.51] TYP

SEATING PLANE

0.020 [0.51] MIN TYP

0.105±0.015 [2.67±0.38] TYP

0.165−0.180 [4.19−4.57] TYP

0.004[0.10]

45°X 0.045 [1.14]

0.990±0.005 [25.15±0.13] TYP

V68A (REV J)

Plastic Chip Carrier (V)
Order Number DP8409AV or DP8409AV-2
NS Package Number V68A

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.