TDA19978A

Quad HDMI 1.3a receiver interface with equalizer (HDTV up to 1080p, up to UXGA for PC's format)

Rev. 03 — 11 May 2010 Product data sheet

1. General description

The TDA19978A is a four inputs HDMI 1.3a compliant receiver with embedded EDID memory.

The TDA19978A embeds an auto adaptive equalizer to improve the signal quality and to allow the use of a large range of cables (up to 25 m, laboratory tested, contact NXP Semiconductors for more details).

The HDCP keys set is stored in a non-volatile embedded memory for maximal security. Software drivers are delivered with the IC to ease configuration and use.

The TDA19978A supports:

- TV resolutions from 480i (1440 × 480i at 60 Hz) and 576i (1440 × 576i at 50 Hz) to HDTV (up to 1920 × 1080p at 50/60 Hz)
- WUXGA (1920 × 1200p at 60 Hz) reduced blanking format
- PC resolutions from VGA (640 × 480p at 60 Hz) to UXGA (1600 × 1200p at 60 Hz)
- Deep Color mode 10-bit and 12-bit (up to 205 MHz TMDS clock)
- IEC 60958/IEC 61937, One Bit Audio (SACD), DST (compressed DSD) and HBR stream
- Gamut boundary description

The TDA19978A includes:

- An improved audio clock generation (an external reference clock is used)
- An improved system for an accurate recognition of PC and TV formats
- The generation of a 128/256/512 × f_s system clock allowing the use of simple audio DACs without integrated PLL, such as UDA1334BTS

Embedded oscillator (an external crystal can be used).

The TDA19978A converts a HDMI stream with or without HDCP into RGB or YCbCr digital signal.

The YCbCr digital output signal can be 4:4:4 or 4:2:2 semi-planar format following the ITU-R BT.601 standard or 4:2:2 ITU-R BT.656 format.

The TDA19978A can adjust the timing of the video port ($t_{su(o)}$ and $t_{h(o)}$).

All settings are controllable via the I^2C-bus.

2. Features and benefits

- Compliant with HDMI 1.3a, DVI 1.0, CEA-861-D and HDCP 1.2 standards
- Quad independent HDMI inputs, up to 205 MHz (HDMI frequency)
- Embedded auto adaptive equalizer on HDMI links
- Embedded volatile EDID memory (253 shared bytes and three bytes dedicated per HDMI input) for zero, one, two, three or four HDMI inputs
- Support color depth processing (8-bit, 10-bit or 12-bit per color)
- Receive color Gamut Metadata Packet with interrupt on each update and readable on I^2C-bus
- Up to four S/PDIF or I^2S-bus outputs (eight channels) with a sampling rate up to 192 kHz with IEC 60958/IEC 61937 stream
- Support HBR audio stream up to 768 kHz with four demultiplexed S/PDIF or I^2S-bus outputs
- Support HBR streams (e.g. DTS-HD master audio and Dolby TrueHD up to eight channels thanks to HBR packet for stream with a frame rate up to 768 kHz)
- Support DSD and DST audio stream up to six DSD channels output for SACD (support DST Audio Packet)
- Channel status decoder supporting multi-channels reception
- Improved audio clock generation using an external reference clock.
- Included system/master clock output (128/256/512 $\times$ f_s) allowing to use the UDA1334BTS
- HDMI interface support all HDTV formats (up to 1920 $\times$ 1080p at 50/60 Hz) and up to UXGA (1600 $\times$ 1200p at 60 Hz) for PC's formats (WUXGA (1920 $\times$ 1200p at 60 Hz) reduced blanking supported)
- Embedded oscillator (an external crystal can be used)
- Frame and field detection for interlaced video signal
- Sync timing measurements for format recognition
- Improved system for measurements of blanking and video active area which allows an accurate recognition of PC and TV formats
- HDCP with repeater capability
- Embedded non-volatile memory to store HDCP keys
- Programmable color space conversion of RGB or YCbCr input signal into YCbCr or RGB
- Output format RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2 semi-planar following the ITU-R BT.601 standard or YCbCr 4:2:2 ITU-R BT.656
- 8-bit, 10-bit or 12-bit output formats (up to 10-bit only in 4:4:4 format) selectable via the I^2C-bus
- Adjustable timing of video port ($t_{su(o)}$ and $t_{h(o)}$) via the I^2C-bus
- Integrated downsampling-by-two with selectable filters on Cb and Cr channels for 4:2:2 mode
- Internal video and audio pattern generator
- Controllable via the I^2C-bus; 5 V tolerant and bit rate up to 400 kbit/s
- DDC inputs 5 V tolerant and bit rate up to 400 kbit/s
- LV-TTL outputs
- Power-down mode

- CMOS process
- 1.8 V and 3.3 V power supplies
- Lead-free HLQFP144 package

3. Applications

- HDTV
- YCbCr or RGB high-speed video digitizer
- Projector, plasma and LCD TV
- Rear projection TV
- High-end TV
- Home theater amplifier
- DVD recorder
- AVR and HDMI splitter

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital inputs: pins RXxC+, RXxC− (x = A, B, C, D)						
$f_{clk(max)}$	maximum clock frequency		205	-	-	MHz
Clock timing output: pins VCLK, ACLK and SYSCLK						
$f_{clk(max)}$	maximum clock frequency	pin VCLK	165	-	-	MHz
		pin ACLK	25	-	-	MHz
		pin SYSCLK	50	-	-	MHz
Supplies						
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)		3.135	3.3	3.465	V
$V_{DDH(1V8)}$	HDMI supply voltage (1.8 V)		1.71	1.8	1.89	V
$V_{DDI(3V3)}$	input supply voltage (3.3 V)		3.135	3.3	3.465	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		1.71	1.8	1.89	V
$V_{DDO(3V3)}$	output supply voltage (3.3 V)		3.135	3.3	3.465	V
P	power dissipation	active mode [1]				
		720p at 60 Hz	-	0.75	-	W
		1080p at 60 Hz	-	1.13	-	W
		1080p at 60 Hz; Deep Color mode	-	1.63	-	W
P_{cons}	power consumption	Power-down mode				
		pin PD = HIGH	-	1	-	mW
		I^2C-bus; EDID and HDCP memory power-up	-	4	-	mW
		I^2C-bus; EDID; activity detection and HDCP memory power-up	-	150	-	mW

[1] With 30 % of activity on video port output.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA19978AHV	HLQFP144	plastic thermal enhanced low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm; exposed die pad	SOT612-3

6. Block diagram

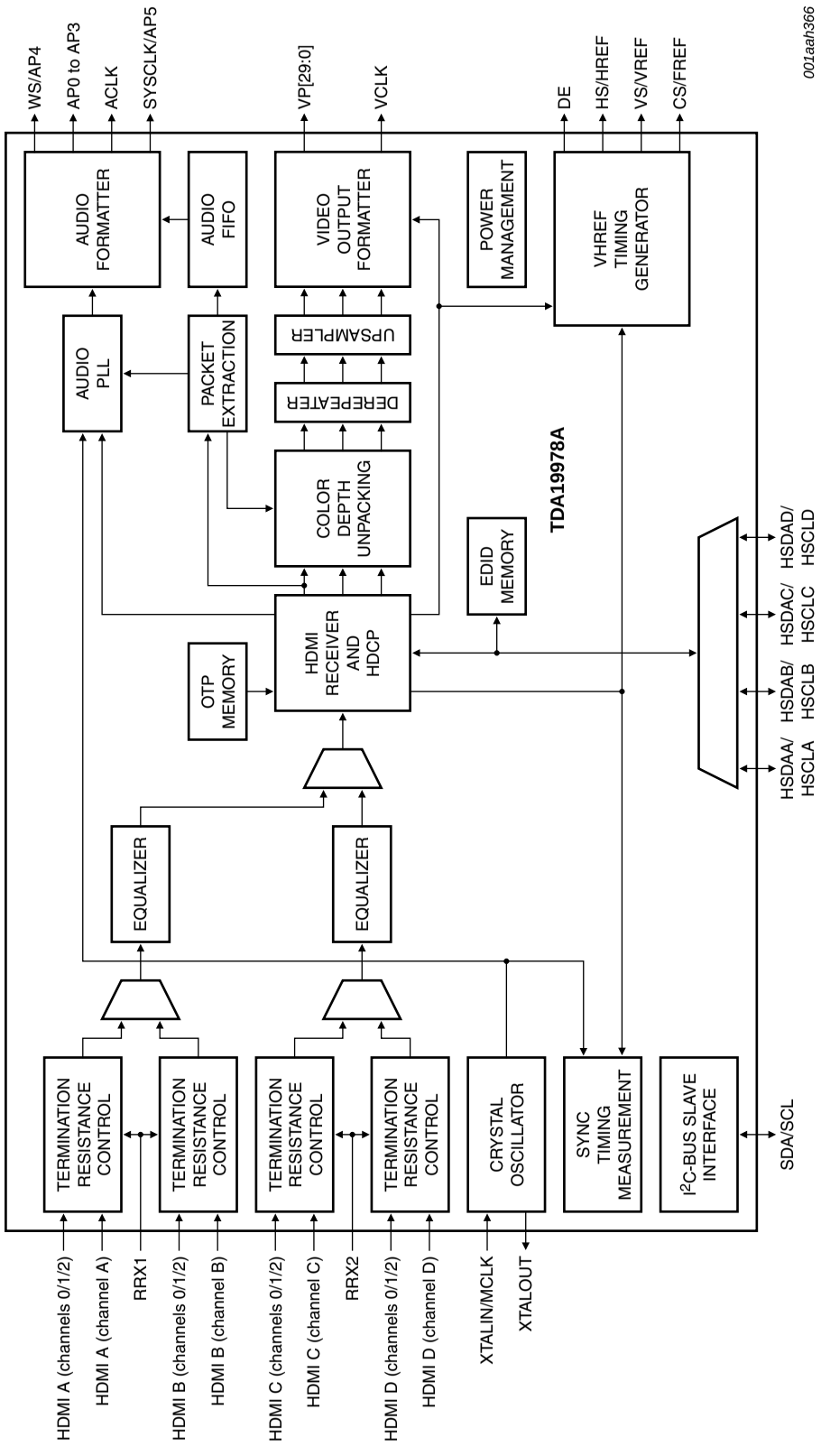

Fig 1. Block diagram

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDx(3V3)}$	supply voltage on all 3.3 V pins		−0.5	+4.6	V
$V_{DDx(1V8)}$	supply voltage on all 1.8 V pins		−0.5	+2.5	V
ΔV_{DD}	supply voltage difference		−0.5	+0.5	V
I_O	output current		-	35	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		-	125	°C
V_{ESD}	electrostatic discharge voltage	HBM	−2000	+2000	V

8. Abbreviations

Table 4. Abbreviations

Acronym	Description
ACR	Audio Clock Regeneration
AVR	Audio Video Receiver
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DDC-bus	Display Data Channel bus
DSD	Direct Stream Digital
DST	Direct Stream Transfer
DTS-HD	Digital Theater Systems HD
DVD	Digital Versatile Disc
DVI	Digital Video Interface
EDID	Extended Display Identification Data
HBM	Human Body Model
HBR	High-Bitrate
HD	High-Definition
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition TeleVision
LV-TTL	Low Voltage Transistor-Transistor Logic
OBA	One Bit Audio
OTP	One Time Programmable
PLL	Phase-Locked Loop
RGB	Red Green Blue
SACD	Super Audio CD
SVGA	Super Video Graphics Array
SXGA	Super eXtended Graphics Array

Table 4. Abbreviations *...continued*

Acronym	Description
S/PDIF	Sony/Philips Digital Interface Format
TMDS	Transition Minimized Differential Signaling
UXGA	Ultra eXtended Graphics Array
VGA	Video Graphics Array
WUXGA	Wide Ultra eXtended Graphics Array
XGA	eXtended Graphics Array
YCbCr	Y = Luminance, Cb = Chroma blue, Cr = Chroma red
YUV	Y = Luminance, UV= Chroma

9. Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA19978A_SDS_3	20100511	Product data sheet	-	TDA19978A_SDS_1[1]
Modifications:	• Section 1 “General description”: updated the Deep Color mode in 12-bit • Section 2 “Features and benefits”: replaced 225 MHz by 205 MHz • Table 1 “Quick reference data”: updated			
TDA19978A_SDS_1	20080528	Objective data sheet	-	-

[1] Revision 2 is not available.

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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12. Contents

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