AN-142

Wake-on-LAN and Wake-Up Event of Power Management in the KSZ8841-PMQL

Introduction

The KSZ8841-PMQL supports Wake-on-LAN (WoL) and Wake-Up power management event functions. These features enable the system to return to a normal operating state when a WoL or a wake event occurs. This application note describes the Wake-on-LAN and Wake-up Event of the Power Management operation on the KSZ8841-PMQL.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Term Definitions

- Power Management: A specification that defines power-saving states of devices and systems. A spec-compliant device implements registers to control and report status for its Power Management function.
- Wake Event: An event that causes a device in Power Management mode to signal the system.
- PME Enable (PME_Enable): Bit 8 of the Power Management Control and Status Register CPMC. Setting this bit to 1 allows the device to assert the PMEN pin when it detects a wake event.
- Wake-on-LAN Mode: A device is in Wake-on-LAN (WoL) mode if it is programmed to enable the receipt of Wake-Up Frame or Magic Packet™ frame other than the fully operational state and is allowed to signal a wake event to the system by Ethernet frame.
- PMEN (pin14): This pin is similar in function to a system interrupt (INTRN pin). When asserted, it signals the system that a wake event has occurred.
- PME Status (PME_Status) -bit 15 of CPMC: When 1, indicates the device detected a wake event. If PME Enable is also set to 1, then the device will assert PMEN whenever the device meets a wake-up condition. Software can writes a 1 to this bit to clear it.
- Magic Packet: A specific packet of information sent to remotely wake up a sleeping or powered off PC on a network, it is handled by the LAN controller.

Wake-on-LAN

There are two parts involved to support Wake-on-LAN. The first part is the Wake-Up Frame detection and the second part is Magic Packet frame detection.

Wake-Up Frame Detection

The Wake-Up Frame detection can be enabled by the following procedure:

- Set the Wake-Up Frame bit [0-3] in the Wake-Up Frame Control and Status Register WFCR. Place the KSZ8841-PMQL into the Wake-Up Frame detection mode. In this mode, normal data receiving is disabled, and detection logic within the MAC examines receive data for the pre-programmed Wake-Up Frame patterns is enabled.
- Before putting the MAC into the Wake-Up Frame detection state, the host must provide the detection logic with a list of sample frames and their corresponding byte masks. This information is written into the Wake-Up Frame 0-3 Byte Mask Registers (offset 0x0220-0x025A). These are set of registers for Wake-Up Frame detection.
- The MAC supports four programmable Wake-Up Frames that can support many different receive packet patterns. If the Wake-Up Frame bit [0-3] in WFCR register is enabled, the Wake-Up Frame function receives all frames addressed to the MAC. It then checks each incoming frame against the enabled Wake-Up Frame mask register and recognizes the frame as a remote Wake-Up Frame to see if it matches the value of the Wake-Up Frame CRC Register to be pre-programmed based on the mask bytes of the Wake-Up Frame Mask Registers.
- In order to determine which bytes of the frames should be checked by the CRC module, the MAC uses a programmable byte mask for each of the Wake-Up Frames.
- The byte mask is a 64-bit field that corresponds to the first 64Bytes of a Wake-Up Frame. The KSZ8841-PMQL supports up to 4 Wake-Up Frames by setting WFCR register bit [3-0].
- When the PME Enable bit and WFCR register bit [3-0] are set, incoming frames are filtered based on the settings in Wake-Up Frame 0-3 CRC Register and Wake-Up Frame 0-3 Byte Mask Register. In other words, a frame must pass filters in order to be received. This is a desirable feature in WoL mode since it prevents the non-wake frames from filling the receive FIFO. However, it is not desirable in normal operating mode, since it will not allow non-wake frames from being received. Therefore, the driver should ensure that the PME Enable bit is set to 0 and WFCR register bit [3-0] are reset for normal operation. In Wake-Up Frame mode, the host software also needs to set Wake-Up Frame 0-3 CRC Register and Wake-Up Frame 0-3 Byte Mask Register first. In Table 1, shows the Wake-Up Frame register's structure.

Magic Packet is a trademark of Advanced Mirco Devices, Inc.

CRC and Byte Mask Registers for Wake-Up Frame 0	
bit31 bit16	bit15 bit 0
Wake-Up Frame 0 CRC 1 Register (0x0222) WF0CRC1	Wake-Up Frame 0 CRC 0 Register (0x0220) WF0CRC0
bit31 bit16	bit15 bit 0
Wake-Up Frame 0 Byte Mask 1 Register (0x0226) WF0BM1	Wake-Up Frame 0 Byte Mask 0 Register (0x0224) WF0BM0
bit63 bit48	bit47 bit32
Wake-Up Frame 0 Byte Mask 3 Register (0x022A) WF0BM3	Wake-Up Frame 0 Byte Mask 2 Register (0x0228) WF0BM2
CRC and Byte Mask Registers for Wake-Up Frame 1	
31 16	15 0
Wake-Up Frame 1 CRC 1 Register (0x0232) WF1CRC1	Wake-Up Frame 1 CRC 0 Register (0x0230) WF1CRC0
31 16	15 0
Wake-Up Frame 1 Byte Mask 1 Register (0x0236) WF1BM1	Wake-Up Frame 1 Byte Mask 0 Register (0x0234) WF1BM0
63 48	47 32
Wake-Up Frame 1 Byte Mask 3 Register (0x032A) WF1BM3	Wake-Up Frame 1 Byte Mask 2 Register (0x0238) WF1BM2
CRC and Byte Mask Registers for Wake-Up Frame 2	
31 16	15 0
Wake-Up Frame 2 CRC 1 Register (0x0242) WF2CRC1	Wake-Up Frame 2 Byte Mask 0 Register (0x0244) WF2BM0
31 16	15 0
Wake-Up Frame 2 Byte Mask 1 Register (0x0246) WF2BM1	Wake-Up Frame 2 Byte Mask 0 Register (0x0244) WF2BM0
63 48	47 32
Wake-Up Frame 2 Byte Mask 3 Register (0x042A) WF2BM3	Wake-Up Frame 2 Byte Mask 2 Register (0x0248) WF2BM2
CRC and Byte Mask Registers for Wake-Up Frame 3	
31 16	15 0
Wake-Up Frame 3 CRC 1 Register (0x0242) WF3CRC1	Wake-Up Frame 3 CRC 0 Register (0x0240) WF3CRC0
31 16	15 0
Wake-Up Frame 3 Byte Mask 1 Register (0x0246) WF3BM1	Wake-Up Frame 3 Byte Mask 0 Register (0x0244) WF3BM0
63 48	47 32
Wake-Up Frame 3 Byte Mask 3 Register (0x042A) WF3BM3	Wake-Up Frame 3 Byte Mask 2 Register (0x0248) WF3BM2

Table 1. Wake-Up Frame Register Structure

How to Set Wake-Up Frame

The KSZ8841-PMQL supports up to four Wake-Up Frames. Each Wake-Up Frame can be defined by the user. Initially, the user needs to know the Wake-Up Frame pattern that they are planning to use. The user can mask or select first 64bytes of the Wake-Up Frame by Wake-Up Frame Mask Register. Each bit of the mask register corresponds to each byte of the Wake-Up Frame. For example, bit 0 of the Wake-Up Frame 0 Mask 0 Register corresponds to the first byte of Wake-Up Frame, bit 1 of the Wake-Up Frame 0 Mask 0 Register corresponds to the second byte of the Wake-Up Frame and similarly, bit 63 of the Wake-Up Frame 3 Mask 3 Register corresponds to the 64th byte of the Wake-Up Frame (see Table 1 for all bits of the Wake-Up Frame 0-3 Mask Register). When the mask register bits are set to 1, the device will perform cyclic redundancy codes and calculate all the selected bytes for cyclic redundancy codes based upon the Ethernet CRC-32 standard. After the device finishes the CRC calculations for a Wake-Up Frame, the result of the CRC calculation is compared against the value of the 32-bit Wake-Up Frame 0-3 CRC 0-1 registers. If the calculation value is same as the value of the corresponding Wake-Up Frame 0-3 CRC 0-1 registers, then the incoming frame is treated as the Wake-Up Frame and the PMEN pin is asserted for remote control function. The user also needs to calculate the values of the Wake-Up Frame in advance based on the known Wake-Up Frame pattern and then write the calculated CRC value to the Wake-Up Frame 0-3 CRC 0-1 registers.

The following steps are required to place the KSZ8841-PMQL into Wake-Up Frame mode:

1. Set PME_Enable bit 8 in CPMC register.
2. Setup Wake-up Frame 0-3 Enable bit [0-3] in WFCR register to select how many wake-up frame will be supported for the Wake-Up Frame mode.
3. Setup 64bit Wake-Up Frame 0-3 Mask 0-3 registers based on the Wake-Up Frame pattern, set to '1' means the byte to be selected, set to '0' means the byte to be masked.
4. The user can define the Wake-Up Frame pattern by them. For the Wake-Up Frame to be detected, the user needs to calculate all selected bytes of the Wake-Up Frame in advance for cyclic redundancy codes by Ethernet CRC-32 standard and write the 32-bit CRC calculation result to the 32-bit Wake-Up Frame 0-3 CRC 0-1 registers for the device identification the Wake-Up Frame. The user can select the first 64 Bytes of a Wake-Up Frame at most.
5. User also can find a software with source code from our software documents provided in the hardware.c \ether_CRC ( ) and then run the software program to calculate CRC result.

In the Wake-Up Frame mode, the device will calculate incoming frames based on the selected bytes of the Wake-Up Frame 0-3 Mask 0-3 Register. If the frame has the same result with one of the 32-bit Wake-Up Frame 0-3 CRC 0-1 registers, then the frame is treated as a remote Wake-Up Frame and the PMEN pin is asserted for the remote control purpose.

Involved Control Registers and bits are shown in Table 2.

Register	Bit	Name	Description	Default
CPMC	8	PME_Enable	If this bit is set, the KSZ8841 can assert the PME_N pin. Otherwise, assertion of the PME_N pin is disabled. This bit is cleared on power-up reset only and is not modified by either hardware or software reset.	0
WFCR	3	WF3E	Wake up Frame 3 Enable When set, it enables the wake up frame 3 pattern detection. When reset, the wake up frame pattern detection is disabled.	0
	2	WF2E	Wake up Frame 2 Enable When set, it enables the wake up frame 2 pattern detection. When reset, the wake up frame pattern detection is disabled.	0
	1	WF1E	Wake up Frame 1 Enable When set, it enables the wake up frame 1 pattern detection. When reset, the wake up frame pattern detection is disabled.	0
	0	WF0E	Wake up Frame 0 Enable When set, it enables the wake up frame 0 pattern detection. When reset, the wake up frame pattern detection is disabled.	0

Table 2. Control Registers and Bits for Magic Packet Frame

The system can bring the device out of the Wake-Up Frame mode by resetting MPRXE bit [3-0] in WFCR register.

Magic Packet Frame Detection

Setting the Magic Packet RX Enable bit 7 (MPRXE) in the Wake Frame Control Register WFCR, places the KSZ8841PMQL in the Magic Packet detection mode. In this mode, normal data reception is disabled and detection logic within the MAC examines receiving data for a Magic Packet.

Once the KSZ8841PMQL has been put into Magic Packet Enable mode, the device will disable normal network activity and will no longer generate any transmits. The device will monitor all incoming frames to determine if any of them is a Magic Packet frame.

A Magic Packet must also meet the basic addressing requirements such as Source Address (SA), Destination Address (DA), which may be the receiving station's MAC address, or a multicast or broadcast address, and CRC.

The Magic Packet has a specific sequence consisting of 16 duplications of the MAC address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined by 6 bytes of FFh. The device will also accept a broadcast frame, as long as the 16 duplications of the MAC address match the address of the machine to be awakened.

If the MAC address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the LAN controller will be scanning for the data sequence (assuming an Ethernet frame):

DESTINATION SOURCE MISC: FF FF FF FF FF FF

11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66

MISC CRC

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the frame's destination.

If the LAN controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ8841-PMQL detects this sort of the data sequence, then it can assert the PMEN pin to wake up the system by the Magic Packet.

How to Set Magic Packet Frame

The following steps are required to place the KSZ8841PMQL into WoL Magic Packet mode:

1. Set PME_Enable bit 8 in CPMC register.
2. Set Magic Packet RX Enable bit [7] in WFCR Wake-Up Frame Control Register to enable the Magic Packet pattern detection.

Involved Control Registers and bits are shown in Table 3.

Register	Bit	Name	Description	Default
CPMC	8	PME_Enable	If this bit is set, the KSZ8841 can assert the PME_N pin. Otherwise, assertion of the PME_N pin is disabled. This bit is cleared on power-up reset only and is not modified by either hardware or software reset.	0
WFCR	7	MPRXE	Magic Packet RX Enable When set, it enables the Magic Packet pattern detection. When reset, the Magic Packet pattern detection is disabled.	0

Table 3. Control Registers and Bits for Magic Packet Frame

The system can bring the device out of the wake-up Magic Packet mode by setting MPRXE bit [7] = 0 in WFCR register.

Wake-up Event of Power Management

Wake Events

If the device detects a wake event while in WoL mode, it will assert the PMEN pin low to signal to the system that a wake event has occurred.

The KSZ8841-PMQL supports the wake-up events of power management states specified by PCI power management specifications D0, D1, D2 and D3 hot states. Those states are described as follows.

D0 State

The D0 state is the normal operational state of the device

D1 State

The D1 state is the least power-saving Power Management state and may not be used by the operating system. The system will only respond to PCI configuration transactions and therefore will not transmit data. The device can initiate the assertion of the PMEN pin (assuming the PME Enable bit is set to 1) in D1 state. Upon returning to the D0 state, the system must re-enable I/O and memory space and turn on bus master capability.

D2 State

The D2 state has the same features as the D1 state, and the system may turn off the PCI clock, further reducing power. Like the D1 state, the D2 state might not be used by the operating system.

D3hot State

The D3hot state is often known as the Standby state. Similar to the D2 and D1 states, the system in D3hot state will respond to PCI configuration transactions as long as the PCI clock is running.

When the system exits the D3hot state, all PCI configuration registers except for the PME Enable and PME Status bits are reset to their default values. This means the operating system must reinitialize the system's PCI configuration registers.

How to Configure and Apply the Wake-up Event of Power Management

The following steps are required to support the KSZ8841-PMQL into wake-up in power management mode:

1. Program the ConfigParam field in the EEPROM. Set PME_D2 bit 12, PME_D1 bit 11, D2_ SUP bit 10 and D2_ SUP bit 9, these values of bits will be loaded to PMCR and CCID registers (those registers are read only) when power up or reset KSZ8841-PMQL device.
2. Enable PME_Enable bit 8 in Power Management Control and Status Register CPMC.
3. CPU can control and write the Power Management Control and Status Register CPMC bit [1-0] to set current power states of system. If the power states are D1, D2 and D3 (hot), then the PMEN pin will be asserted for wake-up event of power management for the different power states.

All Involved Control Registers and bits are shown in Table 4.

Register	Bit	Name	Description	Default
PMCR	14	PME Support D3 (hot)	This bit is 1 only, it is indicating that the KSZ8841-PMQL can assert PME event (PMEN pin 14) in D3 (hot) power state.	1
	13	PME Support D2	If this bit is set, the KSZ8841-PMQL asserts PME event (PMEN pin 14) when the KSZ8841 is in D2 power state and PME_EN (see bit8 in PMCS register) is set. Otherwise, the KSZ8841-PMQL does not assert PME event (PMEN pin 14) when the KSZ8841-PMQL is in D2 power state. The value of this bit is loaded from the PME_D2 bit in the EEPROM 0x6 word.	0
	12	PME Support D1	If this bit is set, the KSZ8841-PMQL asserts PME event (PMEN pin 14) when the KSZ8841-PMQL is in D1 power state and PME_EN (see bit8 in PMCS register) is set. Otherwise, the KSZ8841PMQL does not assert PME event (PMEN pin 14) when the KSZ8841PMQL is in D1 power state. The value of this bit loaded from the PME_D1 bit in the EEPROM 0x6 word.	0
	10	D2 Support	If this bit is set, it indicates that the KSZ8841-PMQL support D2 power state. The value of this bit is loaded from the D2_SUP bit in the EEPROM 0x6 word. (This bit is 0 only if without EEPROM).	0

	9	D1 Support	If this bit is set, it indicates that the KSZ8841-PMQL support D1 power state. The value of this bit loaded from the D1_SUP bit in the EEPROM 0x6 word. (This bit is 0 only if without EEPROM).	0
CPMC	8	PME_Enable	If this bit is set, the KSZ8841-PMQL can assert the PME_N pin. Otherwise, assertion of the PME_N pin is disabled. This bit is cleared on power-up reset only and is not modified by either hardware or software reset.	0
	1-10	Power State	This field is used to set the current power state of the system and to assert a power management event. The definitions of the field values are: 0: D0 1: D1 2: D2 3: D3 (hot) This field gets a value of 0 after power up and reset.	0

Table 4. Control Registers and Bits for Wake-Up Event of Power Management

The system can bring the device out of the wake-up event mode of power management as described below:

1. Disable PME_Enable in CPMC register.
2. To set Power State bits [1-0] to D0 state in CPMC register.

Conclusion

Since the KSZ8841-PMQL Ethernet controller supports the functions for Wake-on-LAN and Wake Event of the power management, the user can use any kind of Magic Packet frame or Wake-Up Frames to apply for remote control and wake-up by Ethernet network and Ethernet packet. With applications in industrial and consumer domain, the KSZ8841-PMQL Ethernet controller provides these methods to meet these kinds of control demand.

Using the Wake-Up event feature of the power management, the users can control their system at different power states for the power management purpose.

The features of Wake-Up Frame, Magic Packet frame and wake-up event of power management enables Micrel's Ethernet single-port controller to be used for industrial control, saving energy in products such as remote management applications.

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