Errata: CS8900A - Silicon revisions: D, F, & H

Reference CS8900A Data Sheet revision DS271F3 dated September 2004.

ESD Performance Testing Methodology

The CS8900A revisions D, F, & H ESD performance is tested using both the Cirrus Logic method and the Jedec method.

The results of the ESD qualification are:

- Cirrus Logic method machine model passes 200 volts and fails 400 volts.
- Cirrus Logic method human body model passes 2K volts and fails 4K volts.

JEDEC specification JESD22-A115A machine model meets class A.

JEDEC specification JESD22-A114C human body model meets class 0.