

32,768 Hz silicon oscillator**Features**

- Fixed frequency 32,768 Hz
- $\pm 1.0\%$ (0 to 70 °C), $\pm 1.2\%$ (–30 to 85 °C) frequency accuracy over all conditions
- 1.65 to 1.95 V, 2.7 to 3.6 V operation
- Low operating current, ultra low standby current
- Push-pull, CMOS compatible frequency (square wave) output
- Chip enable input, active high, internal 150 k Ω pull-down
- Fast and stable startup
- No external components required
- Temperature range: –30 to +85 °C
- Package: SC70-5L
- RoHS compliant

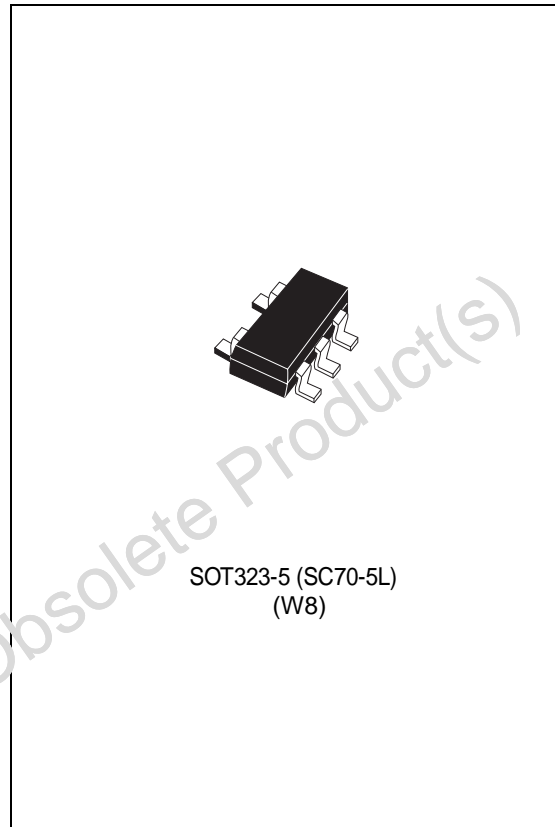
Applications

- Low-speed microprocessor clock
- Display drivers
- Any application with multiple inputs sharing a common clock source

Description

The STCL132K silicon oscillator devices are reliable, easy to use, 5-pin low-cost silicon oscillators developed primarily for microprocessor clock applications, display drivers or other system applications where tighter clock accuracy is not critical. Compared to crystal oscillators, silicon oscillators offer the advantages of faster startup, smaller size and improved immunity to shock, vibration and EMI.

The STCL132K silicon oscillator devices are equipped with chip enable input, offering an easy way to stop microprocessor clocking during a power saving mode while at the same time significantly reducing the oscillator current consumption.



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1 Pin descriptions

Figure 1. SC70-5L pin connections

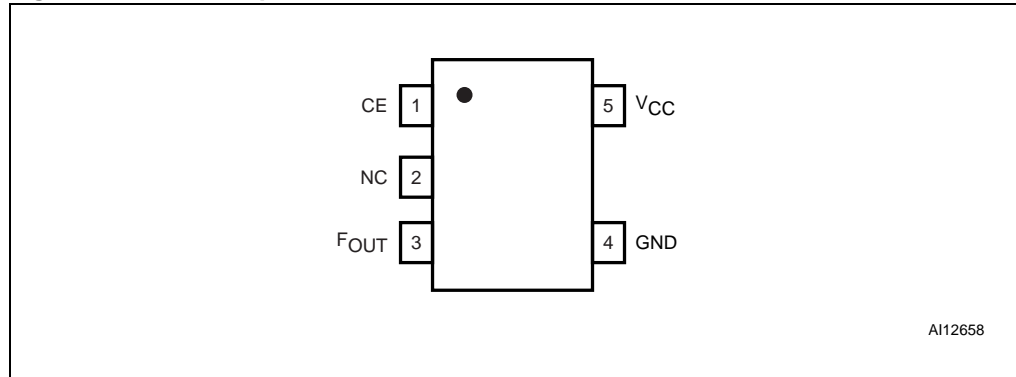
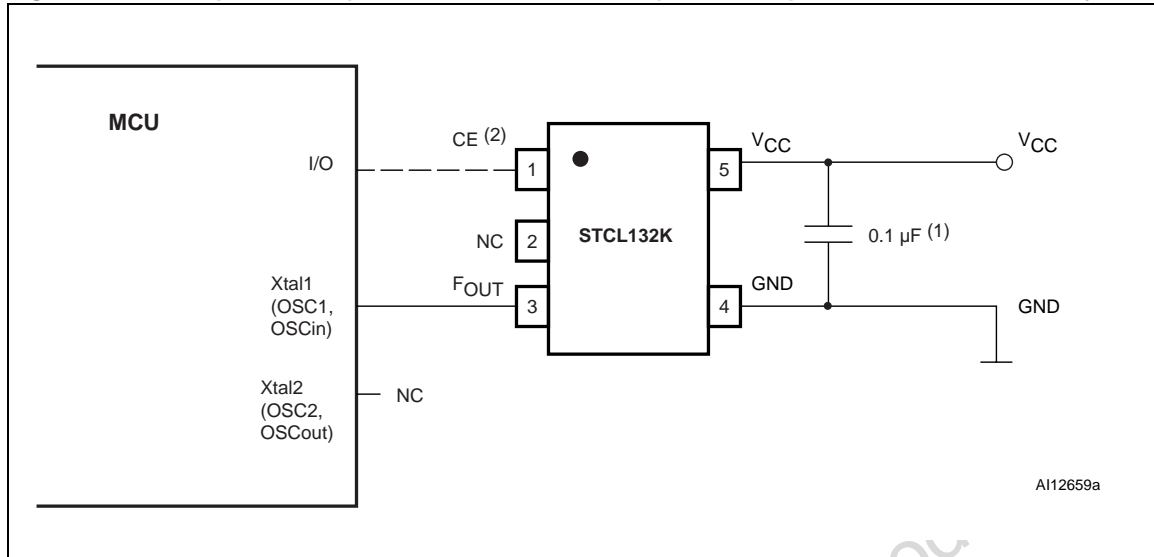


Table 1. Signal names

Symbol	Description
V_{CC}	Positive supply voltage pin
F_{OUT}	Frequency (square wave) output, CMOS compatible, push-pull
CE	Chip Enable input, CMOS level, active high, internal 150 k Ω pull-down resistor
GND	Ground
NC	No Connect

2 Typical application circuit

Figure 2. Microprocessor (MCU, microcontroller unit) clock – replacement of a 32 KHz crystal



1. For reliable operation and to further improve immunity to harsh environment, the minimum 0.1 µF decoupling capacitor is recommended to be placed as close as possible to the V_{CC} and GND pins of the oscillator device. The whole oscillator block should then be placed near the microprocessor clock input.
2. Internal 150 kΩ pull-down resistor is implemented on the CE input. If the chip enable feature is not used, in active mode connect the CE pin to V_{CC}. In applications utilizing standby mode and where the CE pin is connected to the controlling I/O port of the clocked microprocessor, for successful startup of the microprocessor at power-on, initial logic high level needs to be secured on the CE pin to ensure clocking occurs during the power-on reset until the microprocessor program starts and the controlling I/O port takes over the CE control.

3 Operation

Use of the STCL132K silicon oscillator device is very simple. Once power is applied to V_{CC} pin, a CMOS-compatible square wave output signal is provided on the F_{OUT} output pin (in active mode the Chip Enable (CE) input pin must be at a logic high level).

3.1 Chip enable

This feature allows the user to stop the clock and significantly reduce the current consumption when the application is put into power saving mode.

When used to clock the microprocessor in place of a crystal, the need for chip enable input stems from a difference in the way microprocessors normally disable their clock. In the case of a crystal or ceramic resonator, when going into power saving mode, the processor simply opens the internal Xtal inverter feedback which results in stopping the crystal oscillations; however in the case of the silicon oscillators this would not work and the oscillator would continue to run. So in order to use this feature, one of the microprocessor's output pins must be configured to control the silicon oscillator's Chip Enable (CE) input, see typical application circuit diagram in [Figure 2](#).

3.2 Transition to disable

At the moment when the Chip Enable (CE) input goes low, the oscillator's output F_{OUT} will immediately go low; then during the disable period the output remains low.

Note: For advanced microprocessor applications, other disable modes can be made available as a product option (F_{OUT} completes the last clock period, and then remains low or provides 32 additional cycles before going low to allow the processor to complete the pipelined instructions, etc.). Also, a product option with output in a high-impedance state to allow the system to alternate between several oscillators connected in parallel can be made available. Contact local ST sales office for availability.

3.3 Fast startup and stable wakeup from disable

The total startup time until oscillations internally stabilize and remain within specifications is typically 90 μ s, i.e. shorter than duration of the first three periods of the generated output signal, see [Section 5: DC and AC parameters](#). This means that 90 μ s after power-on or wakeup from disable a first valid period of the output signal occurs on the F_{OUT} pin and is within the specified frequency and duty cycle range (in the meantime the output remains low). This is in comparison to typically milliseconds for crystal oscillators.

4 Maximum rating

Stressing the device above the rating listed in [Table 2: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off)	-55 to 150	°C
$T_{SLD}^{(1)}$	Lead solder temperature for 10 seconds	260	°C
V_I	Input voltage	-0.3 to $V_{CC} + 0.3$	V
V_{CC}	Supply voltage	-0.3 to 4.6	V
ESD - MM	Machine Model JESD22-A115-A level A ⁽²⁾	100	V
ESD - HBM	Human Body Model JESD22-A114-B level 2 ⁽²⁾	2	kV
ESD - CDM	Charged Device Model ⁽²⁾	1	kV

1. Reflow at peak temperature of 260 °C (total thermal budget not to exceed 245 °C for more than 30 seconds).

2. For all external pins.

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic [Table 4](#) are derived from tests performed under the measurement conditions listed in the [Table 3](#). Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. DC and AC measurement conditions⁽¹⁾

Parameter	STCL132KRxxx	STCL132KWxxx
V _{CC} supply voltage	1.65 to 1.95 V	2.7 to 3.6 V
Ambient operating temperature	0 to 70 °C, -30 to +85 °C	0 to 70 °C, -30 to +85 °C
Load capacitance (C _L)	12 pF	12 pF

1. Unless otherwise specified.

Table 4. DC and AC parameters

Symbol	Description	Test condition	Min	Typ	Max	Unit
V _{CC}	Operating voltage	STCL132KRxxx	1.65		1.95	V
		STCL132KWxxx	2.7		3.6	V
I _{CC}	Operating current	V _{CC} = 1.65 to 1.95 V, (STCL132KRxxx) output unloaded		60	85	μA
		V _{CC} = 2.7 to 3.6 V, (STCL132KWxxx) output unloaded		85	105	μA
I _{CC2}	Standby current	CE = GND			1	μA
V _{OL}	Output voltage low	I _{OL} = 2 mA			0.2 V _{CC}	V
V _{OH}	Output voltage high	I _{OH} = -2 mA	V _{CC} - 0.2 V			V
V _{IL}	Input low voltage (CE)				0.35 V _{CC}	V
V _{IH}	Input high voltage (CE)		0.65 V _{CC}			V
R _{PD}	Internal pull-down resistor			150		kΩ
	Frequency accuracy ⁽¹⁾	V _{CC} = 1.65 to 1.95 V, -30 to +85 °C (STCL132KRxxx)	-1.2		+1.2	%
		V _{CC} = 1.65 to 1.95 V, 0 to +70 °C (STCL132KRxxx)	-1.0		+1.0	%
		V _{CC} = 2.7 to 3.6 V, -30 to +85 °C (STCL132KWxxx)	-1.2		+1.2	%
		V _{CC} = 2.7 to 3.6 V, 0 to +70 °C (STCL132KWxxx)	-1.0		+1.0	%
	Frequency temperature coefficient		-150		+180	ppm/°C
	Jitter	Cycle-to-cycle, over 20 s		150		ns _{p-p}
	Duty cycle	Taken at half of the signal amplitude	45	50	55	%
t _{START}	Startup time	From the point when V _{CC} reached min operating voltage or CE went high until valid output signal occurs on the F _{OUT} pin (in the meantime output remains low)		90	120	μs
t _R , t _F	Rise/fall time	C _L = 12 pF; 10 to 90 % of the amplitude		10		ns
C _L	Load capacitance			12		pF

1. Typical frequency shift due to aging is ±0.2%. Aging stresses include one solder reflow (260 °C peak) and 1000 hrs V_{CC} biased, 125 °C op-life.

6 Typical operating characteristics and scope plots

Figure 3. Frequency vs. temperature (STCL132KRxxx)

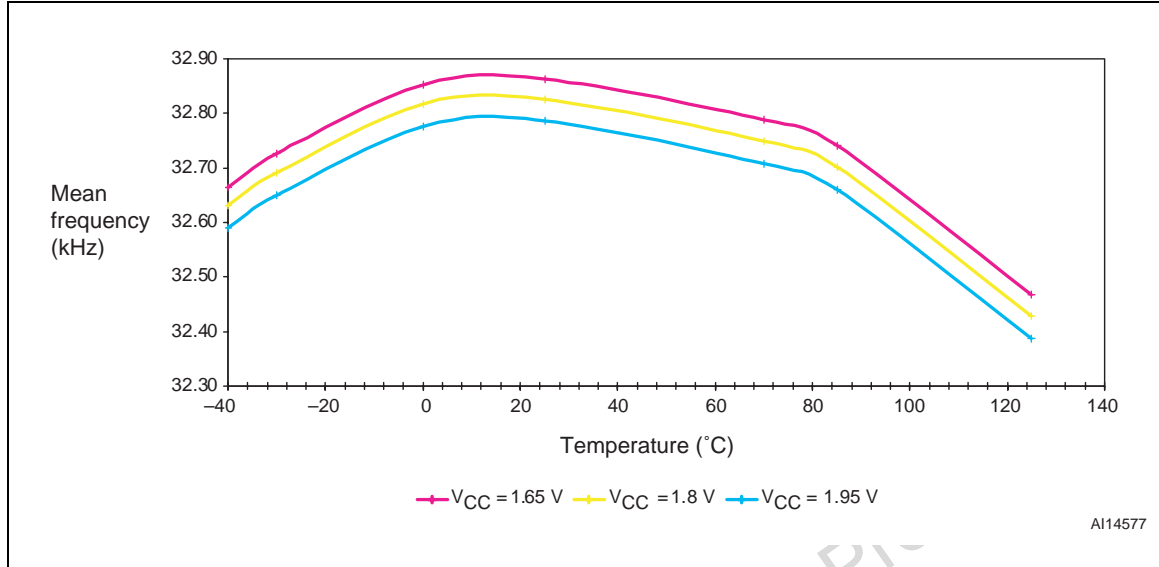


Figure 4. Duty cycle vs. temperature (STCL132KRxxx)

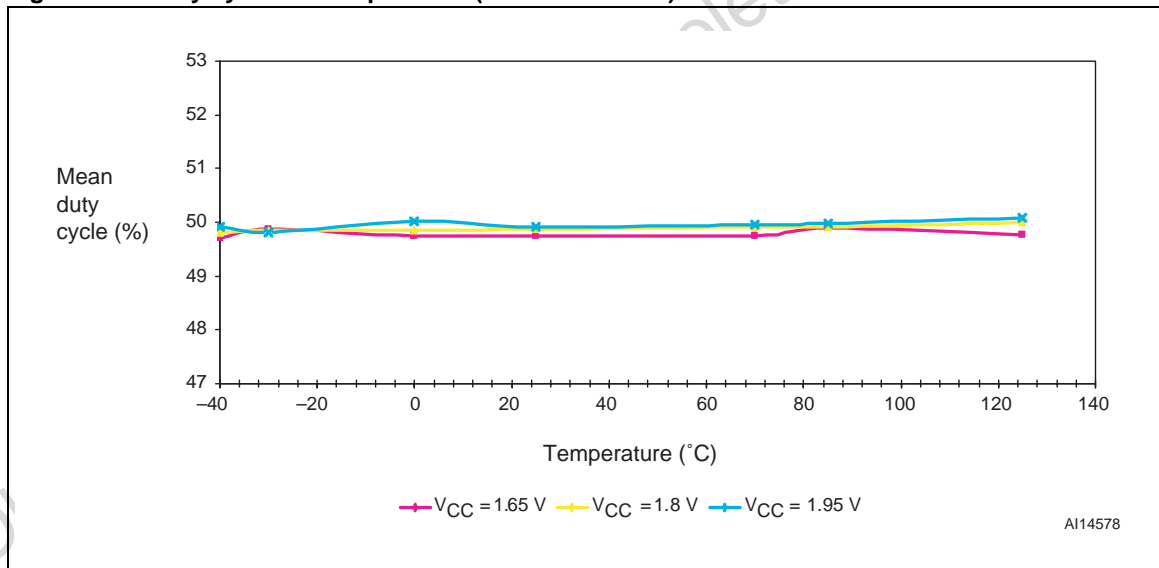


Figure 5. Active supply current vs. temperature (STCL132KRxxx)

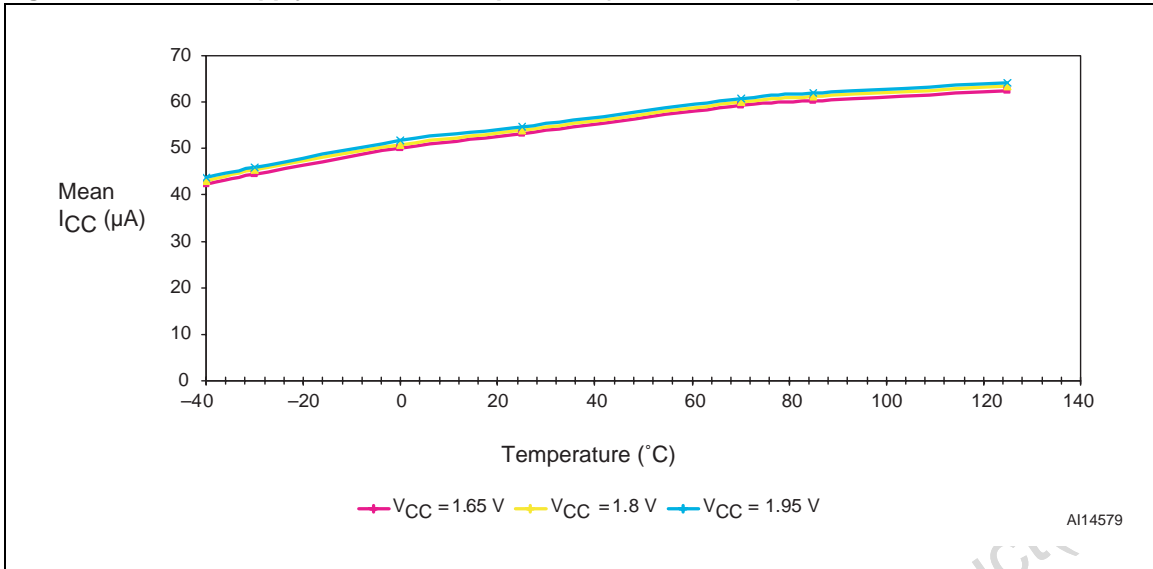


Figure 6. Standby supply current vs. temperature (STCL132KRxxx)

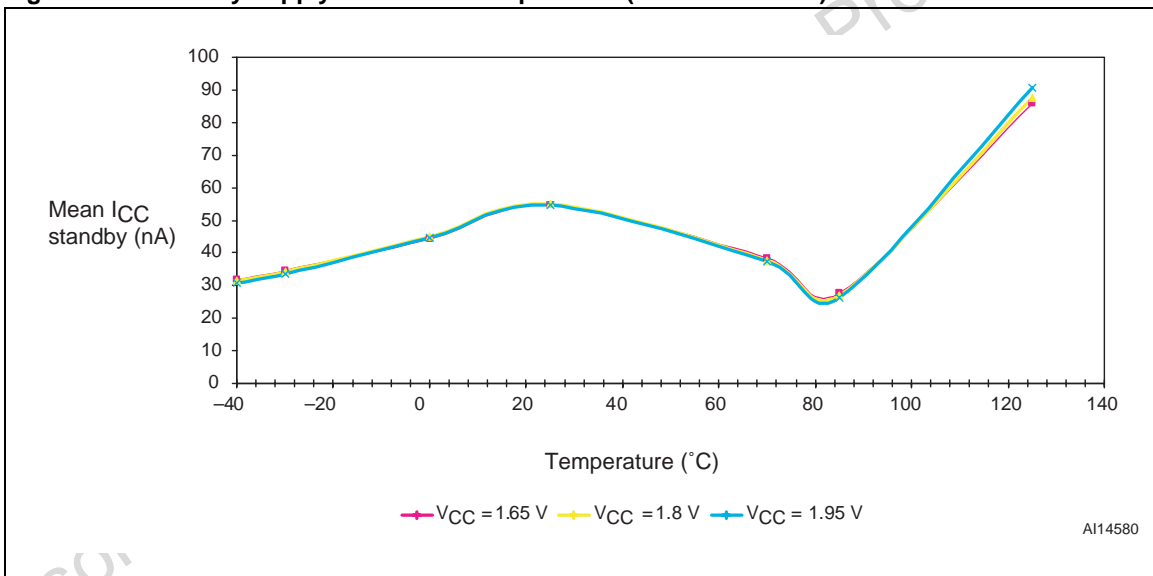


Figure 7. Startup time vs. temperature (STCL132KRxxx)

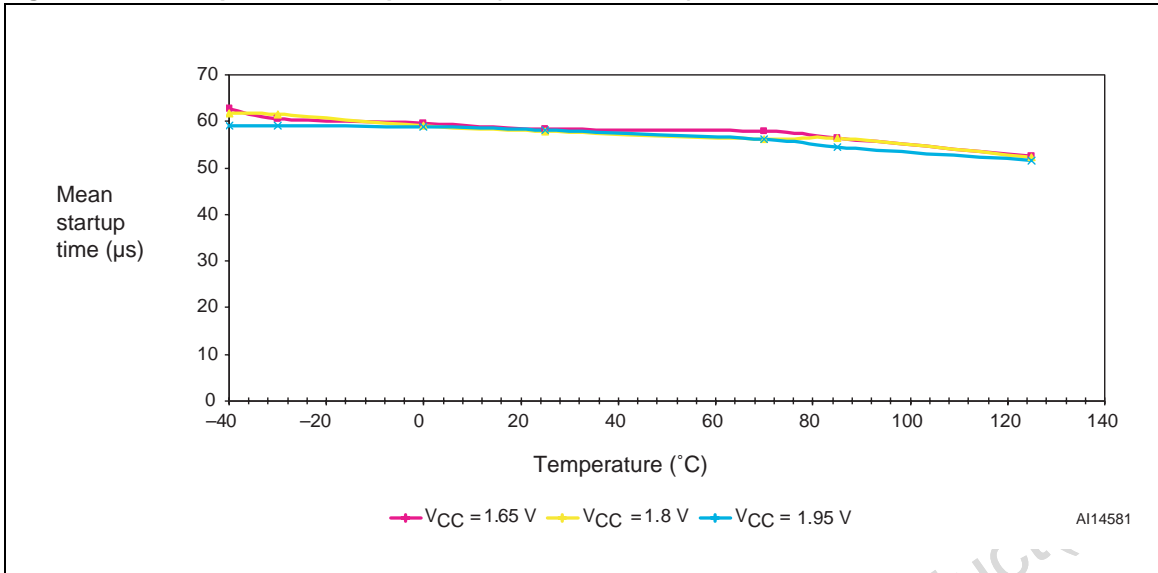
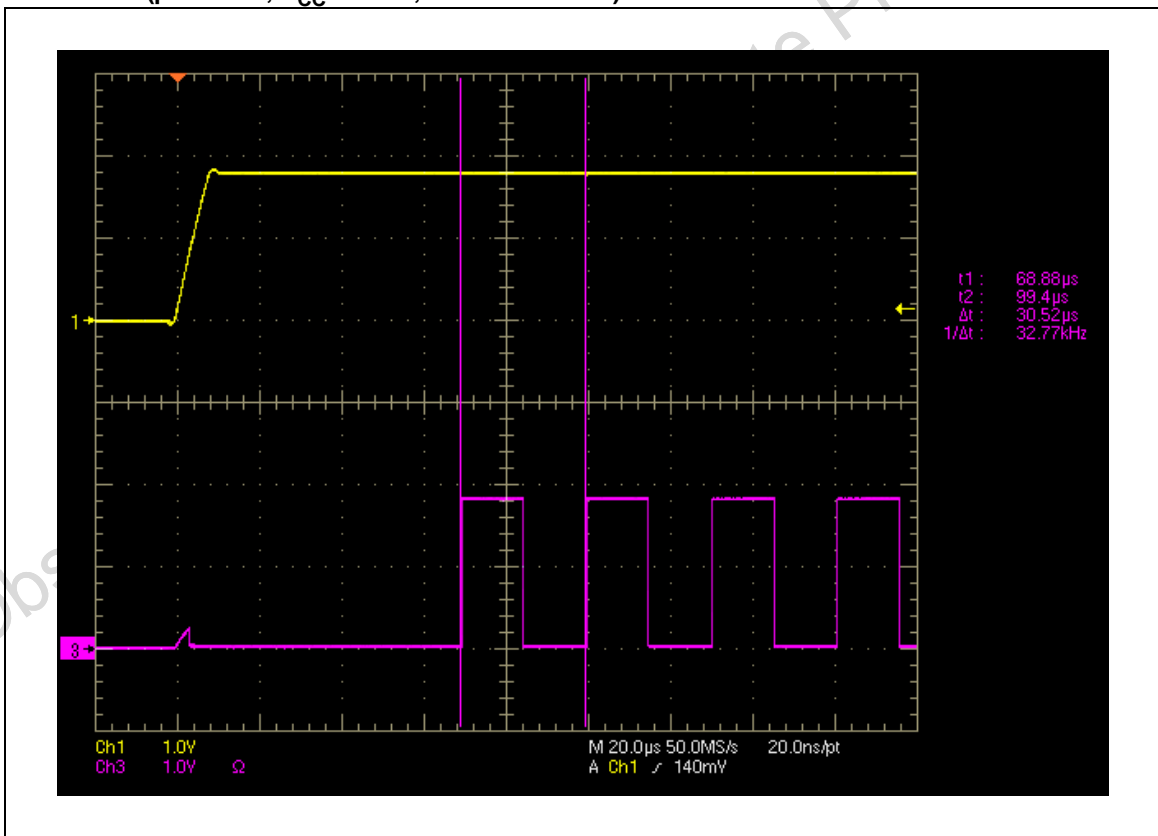


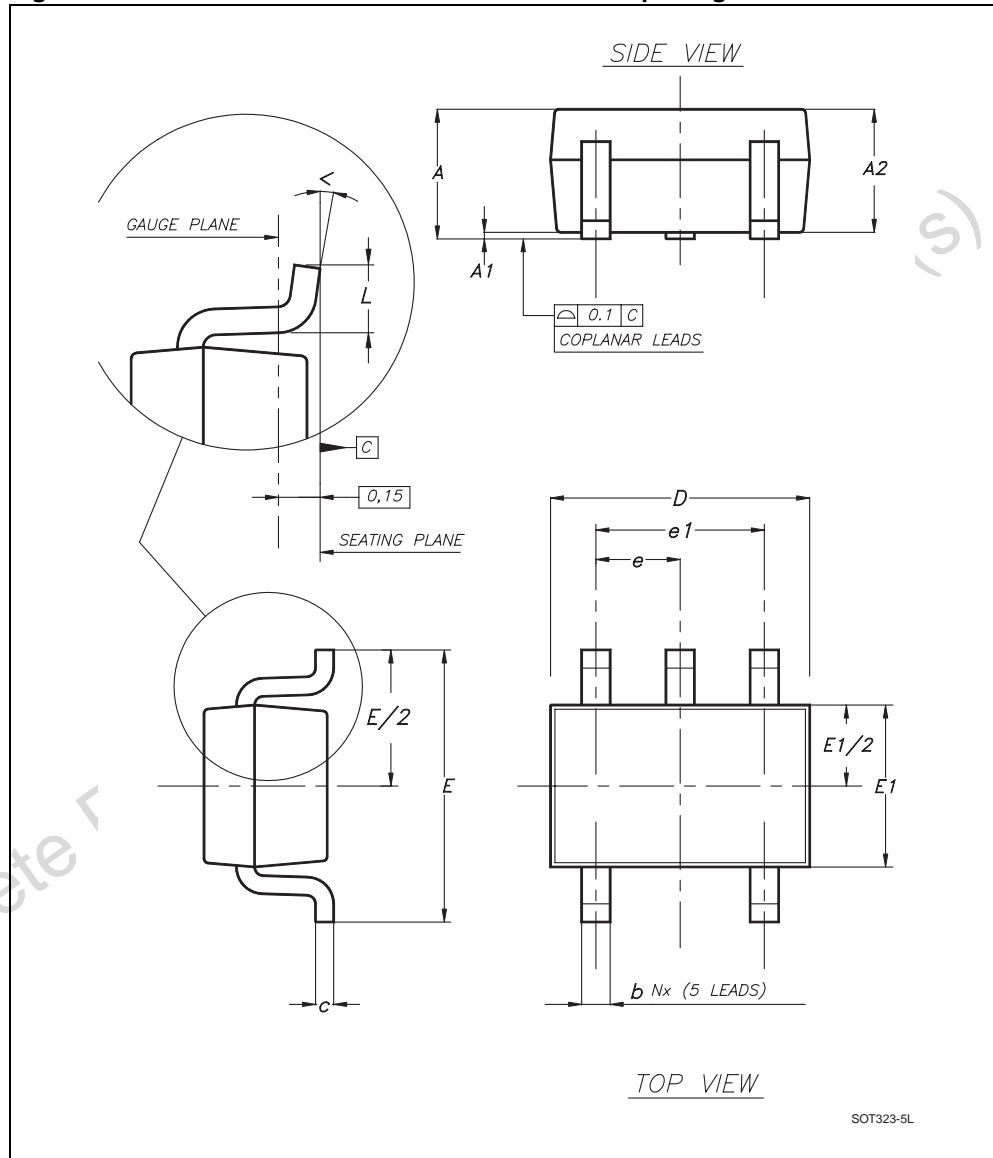
Figure 8. Startup output waveform: already the first cycle is within specifications (power-on, V_{CC} = 1.8 V, STCL132KRxxx)



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 9. SC70-5L – 5-lead small outline transistor package outline



1. Drawing is not to scale.

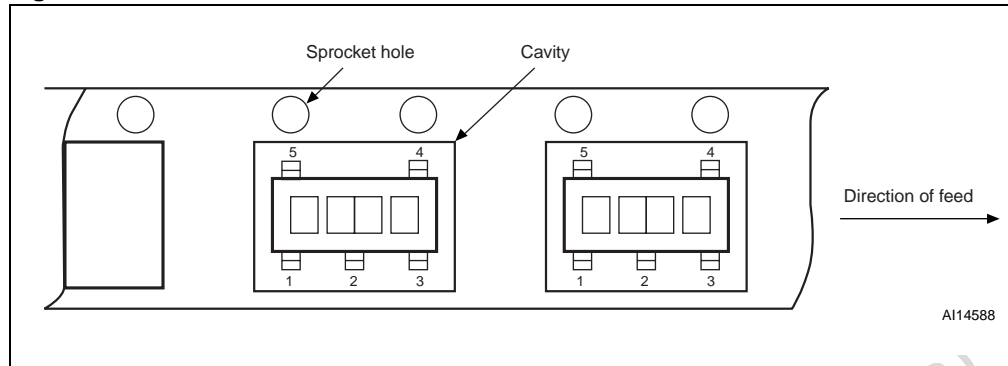
Table 5. SC70-5L – 5-lead small outline transistor package mechanical data

Symbol	mm			Inches		
	Typ	Min	Max	Typ	Min	Max
A	—	0.80	1.10	—	0.031	0.043
A1	—	0	0.10	—	0	0.004
A2	0.90	—	—	0.035	—	—
b	—	0.15	0.30	—	0.006	0.012
C	—	0.10	0.20	—	0.004	0.008
D	2.00	1.80	2.20	0.079	0.071	0.087
E	2.10	1.80	2.40	0.083	0.071	0.094
E1	1.25	1.15	1.35	0.049	0.045	0.053
e	0.65	—	—	0.026	—	—
e1	1.30	—	—	0.051	—	—
L	0.36	0.26	0.46	0.014	0.010	0.018
s	—	0°	5°	—	0°	5°

8 Package details SC70-5L (RoHS compliant)

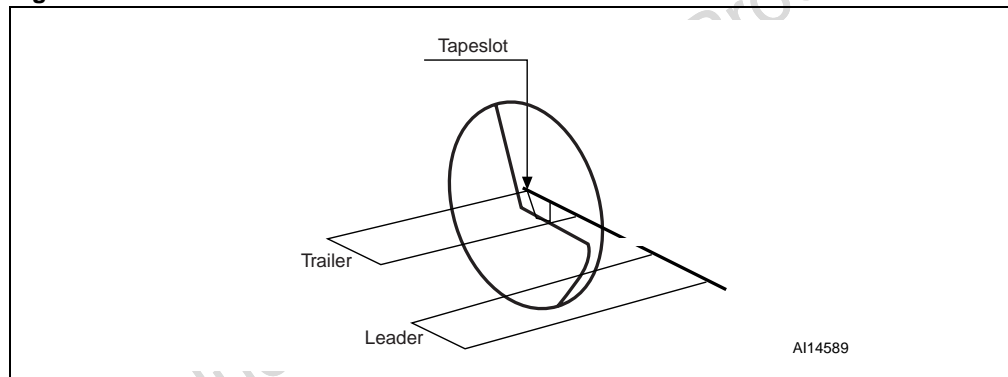
Tape and reel specifications according to EIA-481B standard:

Figure 10. Parts orientation in reel



Pin 1 located opposite to sprocket hole (lower left corner / quadrant 3 with reference to EIA-481B standard).

Figure 11. Reel



Leader length = 500 mm minimum

Trailer length = 160 mm minimum

Peel strength: conforms to EIA 481 standard

Min: 10 gm

Max: 130 gm

9 Part numbering

Table 6. Ordering information scheme

	STCL	1	32K	R	D	E	A	W8	9
Device type									
STCL = Silicon oscillator									
Product family									
1 = Single frequency, fixed									
Frequency									
32K = 32.768 kHz									
Operating voltage									
R = 1.65 to 1.95 V W = 2.7 to 3.6 V ⁽¹⁾									
Accuracy									
D = ±1.2%									
Chip enable⁽²⁾									
E = Single chip enable, active high, pull-down									
Disable mode⁽²⁾									
A = Immediate disable, output low during disable, output low during startup									
Package⁽³⁾									
W8 = SOT323-5 (SC70-5)									
Temperature range									
9 = -30 to +85 °C									

1. Contact local ST sales office for availability of the 3 V V_{CC} range ("W") version.
2. Contact local ST sales office for availability of other product options (chip enable active high or low, with or without internal pull-up or pull-down, possibility of various disable modes, startup procedures, output low or in high-impedance when disabled, etc.).
3. The shipping method is tape and reel only in ECOPACK[®] packages.

10 Package marking

Table 7. Package marking

Part number	V _{CC} range	Topside marking ⁽¹⁾
STCL 1 32K R D E A W8 9	1.65 to 1.95 V	32Ax
STCL 1 32K W D E A W8 9	2.7 to 3.6 V	32Dx

1. x = letter assigned to indicate assembly work week (i.e., A = WW01 and WW02, B = WW03 and WW04, C = WW05 and WW06..., Z = WW51, WW52, and WW53).

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11 Revision history

Table 8. Document revision history

Date	Revision	Changes
23-May-2007	1	Initial release.
09-Aug-2007	2	Updated cover page; frequency accuracy in Table 4 ; Section 7: Package mechanical data ; and Section 9: Part numbering .
28-Feb-2008	3	Document reformatted, added STCL132KWxxx device and commercial temperature range, Chapter 10 , updated Chapter 6 , Chapter 8 , Table 3 and 4 , Figure 10 and 11 , Chapter 9 .
19-Mar-2008	4	Updated cover page, Table 2 , 6 , 7 , and Figure 2 , 8 ; minor text change.
24-Apr-2008	5	Changed status for STCL132K, added note below Table 6 .

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