

## 92HD73E/D/C, 92HDW74E/D/C

## Ten, Eight and Six Channel HD Audio Codecs

# Overview

The current errata and updates for the revision B2 are described below. These items were gathered through *evaluation*, if additional items are identified, notice will be given. Device reliability, life span, and suitability for intended use are not affected. Product covered by this errata carry standard guarantee and warranties.

# **Product Summary**

Product can be identified in several ways. The main part number is located below the IDT Name on the physical chip top marking. The revision code is the first two digits of the fourth line of marking. Products can be identified specifically through the software accessible registers as indicated in the table below. It is recommended that software programmers incorporate identification and adjustment code for the device revisions when updating drivers.

Revision Code Marking	92HD73E 92HDW74E	92HD73D 92HDW74D	92HD73C 92HDW74C1 92HDW74C2
Vendor ID (Parameter 00h (MSB))	111Dh	111Dh	111Dh
Device ID (Parameter 00h (LSB))	7676h	7674h	7675h
Revision ID(Parameter 02h (LSB))	0202h		
Issue Date	April 2008		
Production Status	Production		

Table1. Product Identification

# Errata

Errata Item	Issue Description	Workaround	Status
DMIC out of band noise	Noise may be heard when running digital microphone at or below the standard clock rate (2.58MHz) with the total record gain + boost > ~20dB.	<ul> <li>Option 1. Run digital microphones using the 3.528MHz clock rate (may require a waiver from certain DMIC vendors whose parts are rated with a max clock value below 3.528MHz). This option is implemented with a simple BIOS widget write and does not require any hardware or driver changes.</li> <li>Option 2. Disable the hardware gain inside the driver and implement the boost/gain in SW. This option will require a driver spin, and it will limit the total mic gain to 30dB. Additionally, this option is not available when using the MS Class Driver (which will expose the hardware gain).</li> </ul>	May be addressed in a future silicon revision. Contact IDT sales
DAC-	May experience	These devices are not offered with a productized 3.3V	This will not
MIXER-	clipping and/or	Analog option. If customer chooses to run the device as	be
ADC Path	distortion at -1dB	3.3V, please note that material will not be ATE tested at	addressed.
3.3V	signal levels.	that level and this errata may apply.	

Table 2. Errata

Dynamic Range: Headphone ports with 10k loading have a recommended external filer of 50hms/22nF. With the new WLP requirements, using an external 27nF capacitor or other value is acceptable. Please note that you may have to be "tune" the system for optimal DR behavior by changing this external capacitor during DTM certification. It has no actual effect on audio performance and is only done to compensate for the AP test equipment.

Please note there are no additional known issues or errata items at this time.

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### For Sales

800-345-7015 408-284-8200 Fax: 408-284-2775

### **Corporate Headquarters**

Integrated Device Technology, Inc. 6024 Silver Creek Valley Road San Jose, CA 95138 United States 800 345 7015 +408 284 8200 (outside U.S.)

#### Asia Pacific and Japan

Integrated Device Technology Singapore (1997) Pte. Ltd. Reg. No. 199707558G 435 Orchard Road #20-03 Wisma Atria Singapore 238877 +65 6 887 5505

### Europe

IDT Europe, Limited 321 Kingston R cad Leatherhead, Surrey KT227TU England +44 1372 363 339



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