Simultaneous Sampling Video Rate Codec

ADV7202

FEATURES

Four 10-Bit Video DACs (4:2:2, YCrCb, RGB I/P Supported)
10-Bit Video Rate Digitization at up to 54 MHz
AGC Control (±6 dB)
Front End 3-Channel Clamp Control
Up to Five CVBS Input Channels, Two Component YUV, Three S-Video, or a Combination of the Above. Simultaneous Digitization of Two CVBS Input Channels
Aux 8-Bit SAR ADC @ 843 kHz Sampling Giving up to Eight General-Purpose Inputs
I^2C Compatible Interface with I^2C Filter
RGB Inputs for Picture-on-Picture of the RGB DACs
Optional Internal Reference
Power Save Mode

APPLICATIONS

Picture-on-Picture Video Systems
Simultaneous Video Rate Processing
Hybrid Set-Top Box TV Systems
Direct Digital Synthesis/I-Q Demodulation
Image Processing

GENERAL DESCRIPTION

The ADV7202 is a video rate sampling codec.

It has the capability of sampling up to five NTSC/PAL/SECAM video I/P signals. The resolution on the front end digitizer is 12 bits; 2 bits (12 dB) are used for gain and offset adjustment. The digitizer has a conversion rate of up to 54 MHz.

The ADV7202 can have up to eight auxiliary inputs that can be sampled by an 843 kHz SAR ADC for system monitoring.

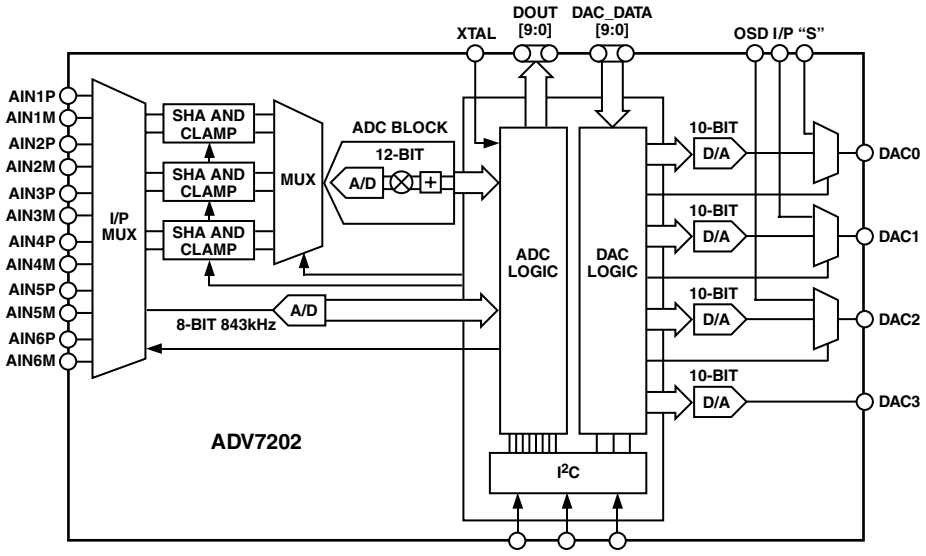
The back end consists of four 10-bit DACs that run at up to 200 MHz and can be used to output CVBS, S-Video, Component YCrCb, and RGB.

This codec also supports Picture-on-Picture.

The ADV7202 can operate at 3.3 V or 5 V. Its monolithic CMOS construction ensures greater functionality with lower power dissipation.

The ADV7202 is packaged in a small 64-lead LQFP package.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADV7202–SPECIFICATIONS

5 V SPECIFICATIONS (AVDD/DVDD = 5 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}[1], unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE_DAC					
Resolution (Each DAC)		10		Bits	
Accuracy (Each DAC)		10		Bits	
Integral Nonlinearity		±0.6		LSB	10-Bit Operation
Differential Nonlinearity	–1.5	–0.6/0.1	+0.5	LSB	10-Bit Operation
VIDEO ADC					
Resolution		12		Bits	(Including 2 Bits for Gain Ranging) 2.2 V Ref.
Accuracy		12		Bits	
Integral Nonlinearity		±2.5		LSB	12 Bit
Differential Nonlinearity		±0.7		LSB	12 Bit
Input Voltage Range[2]	$-V_{REFADC}$		$+V_{REFADC}$		
SNR		62		dB	27 MHz Clock
		57		dB	54 MHz Clock
AUX ADC					
Resolution		8		Bits	
Differential Nonlinearity		±0.4		LSB	Guaranteed No Missing Codes
Integral Nonlinearity		±0.4		LSB	
Input Voltage Range	0		2 V_{REFADC}	V	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Leakage Current, I_{IN}			±2	μA	
Input Capacitance, C_{IN}		6		pF	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 1.6 mA
Three-State Leakage Current			10	μA	
Output Capacitance		10		pF	
Digital Output Access Time, t_{14}		6		ns	See Figure 13
Digital Output Hold Time, t_{15}		5		ns	
ANALOG OUTPUTS					
Output Current Range	4.10	4.33	4.6	mA	R_{SET} = 1.2 kΩ, R_L = 300 Ω
DAC-to-DAC Matching		3		%	
Output Compliance, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		50		kΩ	
Output Capacitance, C_{OUT}		30		pF	I_{OUT} = 0 mA
Analog Output Delay[3]		5.5		ns	
DAC Output Skew		0.06		ns	
VOLTAGE REFERENCE					
Reference Range, V_{REFDAC}	1.17	1.235	1.30	V	
Reference Range, V_{REFADC}	2.1	2.2	2.30	V	Programmable 1.1 V or 2.2 V
Reference Range, V_{REFADC}		1.1		V	

NOTES
[1]0°C to 70°C.
[2]SHA gain = 1, half range for SHA gain = 2, see Table II.
[3]Output delay measured from 50% of the rising edge of the clock to the 50% point of full-scale transition.

Specifications subject to change without notice.

5 V SPECIFICATIONS (AVDD/DVDD = 5 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
POWER REQUIREMENTS[1]					
AVDD/DVDD	4.75	5	5.25	V	
Normal Power Mode					
I_{DAC}[2]			22	mA	R_{SET} = 1.2 kΩ, R_L = 300 Ω
I_{DSC}[3]			12	mA	Inputs at Supply
I_{ADC}[4]		95	115	mA	Max Power YUV Mode
I_{ADC}[4]		65		mA	CVBS Input Mode
Sleep Mode Current[5]		400		µA	
Power-Up Time		4		ms	Internal Reference
MPU PORT[6]—I^2C					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After this period the first clock is generated.
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	

NOTES
[1]All DACs and ADCs on.
[2]I_{DAC} is the DAC supply current.
[3]I_{DSC} is the digital core supply current.
[4]I_{ADC} is the ADC supply current.
[5]This includes I_{ADC}, I_{DAC}, and I_{DSC}.
[6]Guaranteed by characterization.

Specifications subject to change without notice.

ADV7202–SPECIFICATIONS

5 V SPECIFICATIONS (AVDD/DVDD = 4.75 V – 5.25 V, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}[1], unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Condition[2]
PROGRAMMABLE GAIN AMPLIFIER					
Video ADC Gain	–6		+6	dB	Setup Conditions
CLAMP CIRCUITRY[3]					
Clamp Fine Source/Sink Current		4.0		µA	
Clamp Coarse Source/Sink Current		0.8		mA	
CLOCK CONTROL[4]					
DACCLK0/DACCLK1		27		MHz	Dual CLK Dual Edge Mode
DACCLK1[5, 6, 7]			200	MHz	Single Edge Single Clock Mode
DACCLK1		27		MHz	4:2:2 Mode
Data Setup Time, t_{12}[7]	1.5			ns	All Input Modes
Data Hold Time, t_{13}[7]	1.5			ns	
Min Clock High Time, t_{10}[7]		1.5		ns	
Min Clock Low Time, t_{11}[7]		1.5		ns	
Pipeline Delay[8]					
Video ADC		4		Clock Cycles	
RESET CONTROL					
$\overline{\text{RESET}}$ Low Time		10		ns	

NOTES

[1]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[2]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range.

[3]External clamp capacitor = 0.1 µF.

[4]TTL input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF.

[5]Maximum clock speed determined by setup and hold conditions.

[6]Single DAC only.

[7]Guaranteed by characterization.

[8]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Specifications subject to change without notice.

3.3 V SPECIFICATIONS (AVDD/DVDD = 3.3 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}[1], unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE_DAC					
Resolution (Each DAC)		10		Bits	
Accuracy (Each DAC)		10		Bits	
Integral Nonlinearity		±1		LSB	10-Bit Operation
Differential Nonlinearity		–0.8/0.1		LSB	10-Bit Operation
VIDEO ADC					
Resolution		12		Bits	(Including 2 Bits for Gain Ranging) 2.2 V Ref.
Accuracy		12		Bits	
Integral Nonlinearity		±4		LSB	12 Bit
Differential Nonlinearity		±1		LSB	12 Bit
Differential Input Voltage Range[2]	$-V_{REFADC}$		$+V_{REFADC}$		See Table II
SNR		60		dB	27 MHz Clock, f_{IN} = 100 kHz
		55		dB	54 MHz Clock
AUX ADC					
Resolution		8		Bits	
Differential Nonlinearity		±0.5		LSB	
Integral Nonlinearity		±0.5		LSB	
Input Voltage Range	0		2 V_{REFADC}	V	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}		±1		μA	
Input Capacitance, C_{IN}		10		pF	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 1.6 mA
Three-State Leakage Current		10		μA	
Output Capacitance		10		pF	
Digital Output Access Time, t_{14}		6		ns	See Figure 13
Digital Output Hold Time, t_{15}		5		ns	
ANALOG OUTPUTS					
Output Current		4.33		mA	R_{SET} = 1.2 kΩ, R_L = 300 Ω
DAC-to-DAC Matching		4		%	DAC 0, 1, and 2
Output Compliance, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		50		kΩ	
Output Capacitance, C_{OUT}		30		pF	I_{OUT} = 0 mA
Analog Output Delay[3]		5.5		ns	
DAC Output Skew		0.06		ns	
VOLTAGE REFERENCE					
Reference Range, V_{REFADC}		1.100		V	
Reference Range, V_{REFDAC}		1.235		V	

NOTES
[1]0°C to 70°C.
[2]SHA gain = 1, half range for SHA gain = 2, see Table II.
[3]Output delay measured from 50% of the rising edge of the clock to the 50% point of full-scale transition.
Specifications subject to change without notice.

ADV7202–SPECIFICATIONS

3.3 V SPECIFICATIONS (AVDD/DVDD = 3.3 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
POWER REQUIREMENTS[1]					
AVDD/DVDD	3.14	3.3	3.46	V	
Normal Power Mode					
I_{DAC}[2]		18		mA	
I_{DSC}[3]		8		mA	Inputs at Supply
I_{ADC}[4]		80		mA	
Sleep Mode Current[5]		350		µA	
Power-Up Time		4		ms	Internal Reference
MPU PORT[6]—I^2C					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulsewidth, t_1	0.6			µs	
SCLOCK Low Pulsewidth, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After this period, the first clock is generated.
Setup Time (Start Condition), t_4	0.6			µs	Relevant for Repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	

NOTES
[1]All DACs and ADCs on.
[2]I_{DAC} is the DAC supply current.
[3]I_{DSC} is the digital core supply current.
[4]I_{ADC} is the ADC supply current.
[5]This includes I_{ADC}, I_{DAC}, and I_{DSC}.
[6]Guaranteed by characterization.

Specifications subject to change without notice.

3.3 V SPECIFICATIONS (AVDD/DVDD = 3.3 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 1.2 kΩ, all specifications T_{MIN} to T_{MAX}[1], unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Condition[2]
PROGRAMMABLE GAIN AMPLIFIER					
Video ADC Gain	–6		+6	dB	
CLAMP CIRCUITRY[3]					
Clamp Fine Source/Sink Current		4		µA	Up/Down
Clamp Coarse Source/Sink Current		0.8		mA	Up/Down
CLOCK CONTROL[4]					
DACCLK0/DACCLK1		27		MHz	Dual CLK Dual Edge Mode
DACCLK1[5, 6, 7]		180		MHz	Single Edge Single Clock Mode
DACCLK1[7]		27		MHz	4:2:2 Mode
Data Setup Time, t_{12}		2		ns	All Input Modes
Data Hold Time, t_{13}		2		ns	
Min Clock High Time, t_{10}[7]		3		ns	
Min Clock Low Time, t_{11}[7]		3		ns	
Pipeline Delay[8]					
Video ADC		4		Clock Cycles	
RESET CONTROL					
$\overline{\text{RESET}}$ Low Time		10		ns	

NOTES
[1]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[2]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range.
[3]External clamp capacitor = 0.1 µF.
[4]TTL input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF.
[5]Maximum clock speed determined by setup and hold conditions.
[6]Single DAC only.
[7]Guaranteed by characterization.
[8]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

AVDD to AVSS . . . . . 7 V
DVDD to DVSS . . . . . 7 V
Ambient Operating Temperature (T_A) . . . . . 0°C to 70°C
Storage Temperature (T_S) . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . 150°C
Lead Temperature (Soldering, 10 secs) . . . . . 300°C
Vapor Phase Soldering (1 minute) . . . . . 220°C
I_{OUT} to GND[2] . . . . . 0 V to V_{AA}

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Analog output short circuit to any power supply or common can be of an indefinite duration.

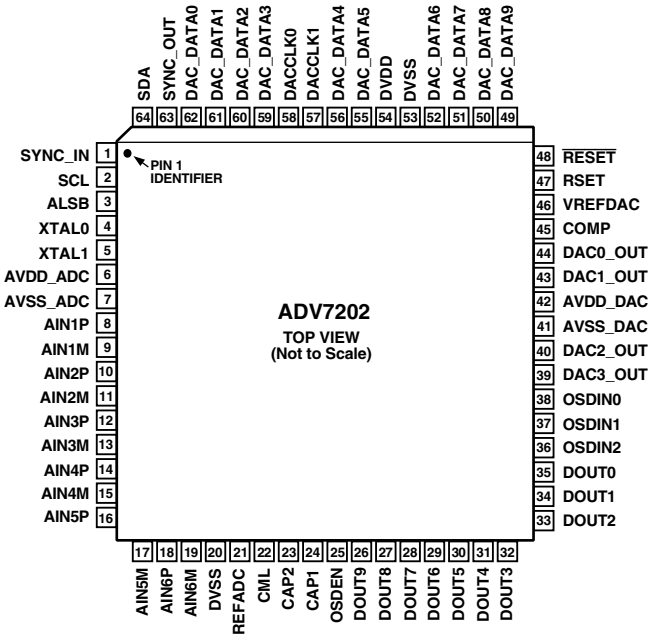
ORDERING INFORMATION

Model	Temperature Range	Package Description	Package Option
ADV7202	0°C to 70°C	64-Lead Plastic Quad Flatpack (LQFP)	ST-64

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7202 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Input/ Output	Function
1	SYNC_IN	I	This signal can be used to synchronize the updating of clamps. Polarity is programmable via I^2C.
2	SCL	I	MPU Port Serial Interface Clock Input
3	ALSB	I	This signal sets up the LSB of the MPU address. MPU address = 2cH, ALSB = 0, MPU address = 2eH, ALSB = 1. When this pin is tied high, the I^2C filter is activated, which reduces noise on the I^2C interface. When this pin is tied low, the input bandwidth on the I^2C lines is increased.
4	XTAL0	I	Input terminal for crystal oscillator or connection for external oscillator with CMOS-compatible square wave clock signal.
5	XTAL1	O	Second Terminal for Crystal Oscillator. Not connected if external clock source is used.
6	AVDD_ADC	P	ADC Supply Voltage (5 V or 3.3 V)
7	AVSS_ADC	G	Ground for ADC Supply
8–19	AIN1–AIN6	I	Analog Signal Inputs. Can be configured differentially or single-ended.
20	DVSS	G	Ground for Digital Core Supply
21	REFADC	I/O	Voltage Reference Input or Programmable Reference Out.
22	CML	O	Common-Mode Level for ADCs. Connect a 0.1 µF capacitor from CML pin to AVSS_ADC.
23, 24	CAP2, CAP1	I	ADC Capacitor Network. Connect a 0.1 µF capacitor from each CAP pin to AVSS_ADC and a 10 µF capacitor across the two CAP pins.
25	OSDEN	I	Enable data from OSDIN0–OSDIN2 to be switched to the outputs when set to a logic high.
26–35	DOUT[9:0]	O	ADC Data Output
36	OSDIN2	I	Third Input Channel for On-Screen Display
37	OSDIN1	I	Second Input Channel for On-Screen Display
38	OSDIN0	I	First Input Channel for On-Screen Display
39	DAC3_OUT	O	General-Purpose Analog Output
40	DAC2_OUT	O	Analog Output. Can be used to output CVBS, R, or U.
41	AVSS_DAC	G	Ground for DAC Supply
42	AVDD_DAC	P	DAC Supply Voltage (5 V or 3.3 V)
43	DAC1_OUT	O	Analog Output. Can be used to output CVBS, Y, G, or Luma.
44	DAC0_OUT	O	Analog Output. Can be used to output CVBS, V, B, or Chroma.
45	COMP	O	Compensation pin for DACs. Connect 0.1 µF capacitor from COMP pin to AVDD_DAC.
46	VREFDAC	I/O	DAC Voltage Reference Output Pin, Nominally 1.235 V. Can be driven by an external voltage reference.
47	RSET	I	Used to control the amplitude of the DAC output current, 1200 Ω resistor gives an I max of 4.33 mA.
48	$\overline{\text{RESET}}$	I	Master Reset (Asynchronous)
49–52, 55, 56, 59–62	DAC_DATA[9:0]	I	DAC Input Data for Four Video Rate DACs
53	DVSS	G	Ground for Digital Core Supply
54	DVDD	P	Supply Voltage for Digital Core (5 V or 3.3 V)
57, 58	DACCLK[1:0]	I	DAC Clocks
63	SYNC_OUT	O	Output Sync Signal, which goes to a high state while Cr data sample from a YCrCb data stream or C data from a Y/C data stream is output on DOUT[9:0].
64	SDA	I/O	MPU Port Serial Data Input/Output

FUNCTIONAL DESCRIPTION

Analog Inputs

The ADV7202 has the capability of sampling up to five CVBS video input signals, two component YUV, or three S-Video inputs. Eight auxiliary general-purpose inputs are also available. Table I shows the analog signal input options available and programmable by I²C. When configured for auxiliary input mode, the CVBS inputs are single-ended with the second differential input internally set to VREFADC. The resolution on the front end digitizer is 12 bits; 2 bits (12 dB) are used for gain and offset adjustment. The digitizer has a conversion rate of up to 54 MHz. The eight auxiliary inputs can be used for system monitoring, etc. and are sampled by an 843 kHz* SAR ADC. The analog input signal range will be dependent on the value of VREFADC and the SHA gain see (Table II). Three on-screen display inputs OSDIN[2:0] mux to the DAC outputs to enable support for Picture-on-Picture applications.

Table I. Analog Input Signal Data

Register Setting	Description	SHA Used	Sync_Out
0000	CVBS in on AIN1	0	Figure 1
0001	CVBS in on AIN2	0	Figure 1
0010	CVBS in on AIN3	1	Figure 1
0011	Reserved	1	
0100	CVBS in on AIN5	0	Figure 1
0101	CVBS in on AIN6	2	Figure 1
0110	Y/C, Y on AIN1, C on AIN4	0, 1	Figure 2
0111	Y/C, Y on AIN2, C on AIN3	0, 1	Figure 2
1000	YUV, Y on AIN2, U on AIN3, V on AIN6	0, 1, 2	Figure 3
1001	CVBS on AIN1 and 8 AUX. I/Ps AIN3–AIN6*.	0	Figure 1
1010	CVBS on AIN2 and 8 AUX. I/Ps AIN3–AIN6*.	0	Figure 1

*AUX inputs are single-ended. All other inputs are differential.

Table II. Analog Input Signal Range

I/P Mode	V_{REFOUT} (V)	SHA Gain	Input Range (V) Min	Max
Differential	2.2	1	–2.2	+2.2
Differential	2.2	2	–1.1	+1.1
Differential	1.1	1	–1.1	+1.1
Differential	1.1	2	–0.55	+0.55
Single-Ended	2.2	1	0	4.4
Single-Ended	2.2	2	1.1	3.3
Single-Ended	1.1	1	0	2.2
Single-Ended	1.1	2	0.55	1.65

Digital Inputs

The DAC digital inputs on the ADV7202 [9:0] are TTL compatible. Data may be latched into the device in three different modes, programmable via I²C.

DAC Mode 1, single clock, single edge (see Figure 10) uses only the rising edge of DACCLK1 to latch data into the device. DACCLK0 is a data line that goes high to indicate that the data is for DAC0. Subsequent data-words go to the next DAC in sequence.

DAC Mode 2, dual edge, dual clock (see Figure 11) clocks data in on both edges of DACCLK0 and DACCLK1. Using this option, data can be latched into the device at four times the clock speed. All four DACs are used in this mode.

DAC Mode 3, 4:2:2 mode (see Figure 12). Using this option, 4:2:2 video data is latched in using DACCLK1, while DACCLK0 is used as a data line that is brought to a high state when Cr data is input; hence Y will appear on DAC1, Cr on DAC2, and Cb on DAC0.

Analog Outputs

Analog outputs [DAC0–DAC3] consist of four 10-bit DACs that run at up to 54 MHz or up to 200 MHz if only DAC0 is used. These outputs can be used to output CVBS, S-Video, Component YCrCb, and RGB.

Digital Outputs

Video data will be clocked out on DOUT[9:0] on the rising edge of XTAL0 (see Figure 13). Auxiliary data can be read out via I²C compatible MPU port.

I²C Control

I²C operation allows both reading and writing of system registers. Its operation is explained in detail in the MPU Port Description section.

*Fclk/32, 843 kHz for nominal 27 MHz

VIDEO CLAMPING AND AGC CONTROL

When analog signal clamping is required, the input signal should be ac-coupled to the input via a capacitor, the clamping control is via the MPU port. The AGC is implemented digitally. For correct operation, the user must program the clamp value to which the signal has been clamped into the ADV7202 I^2C Register. This allows the user to specify which signal level is unaffected by the AGC. The digital output signal will be a function of the *ADC* output, the *AGC Gain,* and the *Clamp Level* and can be represented as follows:

$$D_{OUT} = AGC\ Gain \times [ADC\_DATA - Clamp\ Level] + Clamp\ Level \quad (1)$$

D_{OUT} will be a 10-bit number (0–1023), the *AGC Gain* defaults to 2 and can have a value between 0 to 7.99. The *Clamp Level* is a 10-bit number (0–1023) equal to the 7-bit I^2C value × 16 (Clamp Level CR06-CR00); the ADC value can be regarded as a 10-bit number (0–1023) for the equation. It should be noted that the ADC resolution is 12 bits. The above equation is used to give a basic perspective and is mathematically correct.

When the clamps are operational, Equation 1 shows how the ADV7202 ensures that the level to which the user is clamping is unaffected by the AGC loop. When no clamps are operational, the operation should be regarded as a straightforward gain-and-level shift.

Equation 1 maps the ADC input voltage range to its output.

AGC Gain

The AGC gain can be set to a value from 0 to 7.99. The AGC Gain Register holds a 12-bit number that corresponds to the required gain. The first three MSBs hold the gain integer value while the remaining nine bits hold the gain fractional value. The new AGC multiplier is latched when the MSB register is written to. Example: The user requires a gain of 3.65.

The first three bits give the integer value 3, hence these will be set to '011.' The remaining nine bits will have to be set to give the fractional value 0.65, 512 × 0.65 = 333 = '101001101.' From Equation 2 it can be seen that the *Clamp Level* is subtracted from the signal before *AGC* is applied and then added on again afterwards; hence, if the *AGC Gain* is set to a value of one, the result would be as follows:

(*AGC Gain* = 1)

$$D_{OUT} = ADC\_DATA - Clamp\ Level + Clamp\ Level = ADC\_Data \quad (2)$$

FUNCTIONAL DESCRIPTION

Clamp and AGC Control

The ADV7202 has a front end 3-channel clamp control. To perform an accurate AGC gain operation, it is necessary to know to what level the user is clamping the black level; this value is programmable in Clamp Register 0 CR00–CR06. Each channel has a fine and coarse clamp; the clamp direction and its duration are programmable. Synchronization of the clamps and AGC to the input signal is possible using the SYNC_IN control pin and setting mode Register CR14 to Logic Level "1." Using this method, it is possible to ensure that AGC and clamping are only applied outside the active video area.

Control Signals

The function and operation of the SYNC_IN signal is described in the Clamp and AGC Control section. The SYNC_OUT will go high while Cr data from a YCrCb data stream or C data from a Y/C data stream has been output on DOUT[9:0] (see Figures 1 to 3).

I^2C Filter

A selectable internal I^2C filter allows significant noise reduction on the I^2C interface. In setting ALSB high, the input bandwidth on the I^2C lines is reduced and pulses of less than 50 ns are not passed to the I^2C controller. Setting ALSB low allows greater input bandwidth on the I^2C lines.

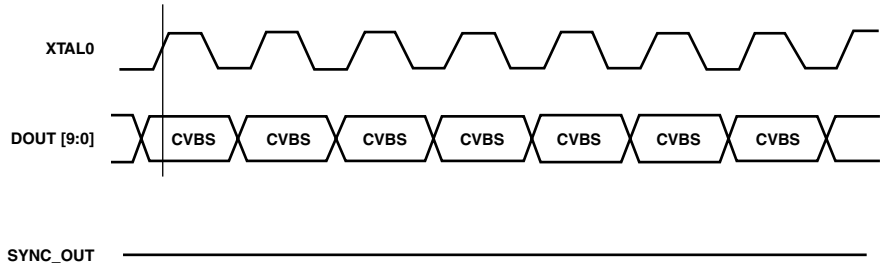


Figure 1. SYNC_OUT Output Timing, CVBS Input

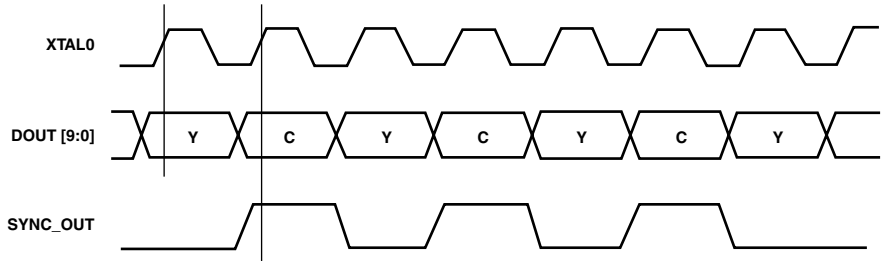


Figure 2. SYNC_OUT Output Timing, Y/C (S-VIDEO) Input

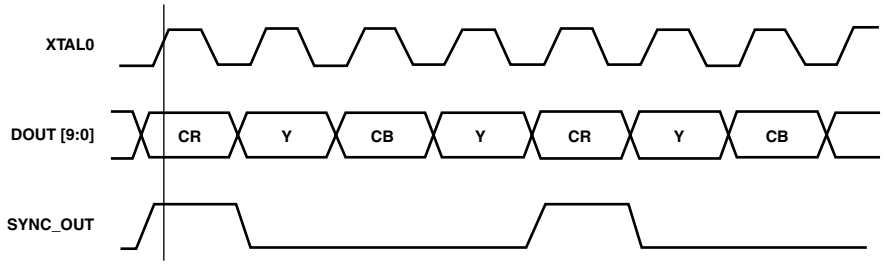


Figure 3. SYNC_OUT Output Timing, YCrCb Input

MPU PORT DESCRIPTION

The ADV7202 supports a 2-wire serial (I^2C-compatible) microprocessor bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCL), carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7202 has four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 4. The LSB sets either a read or write operation. Logic Level "1" corresponds to a read operation, while Logic Level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7202 to Logic Level "0" or Logic Level "1." When ALSB is set to "0," there is greater input bandwidth on the I^2C lines, which allows high speed data transfers on this bus. When ALSB is set to "1," there is reduced input bandwidth on the I^2C lines, which means that pulses of less than 50 ns will not pass into the I^2C internal controller. This mode is recommended for noisy systems.

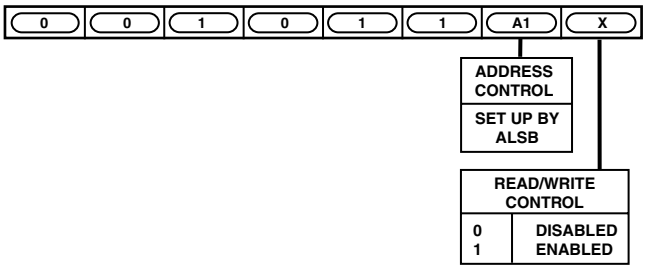


Figure 4. Slave Address

To control the various devices on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a Start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an Acknowledge Bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCL lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data.

A Logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A Logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7202A acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a Stop condition. The user can access any unique subaddress register one-by-one, without updating all the registers.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCL high period, the user should only issue one Start condition, one Stop condition, or a single Stop condition followed by a single Start condition. If an invalid subaddress is issued by the user, the ADV7202 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode, the user exceeds the highest subaddress, the following action will be taken:

1. In read mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
2. In write mode, the data for the invalid byte will not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7202, and the part will return to the idle condition.

Figure 5 illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

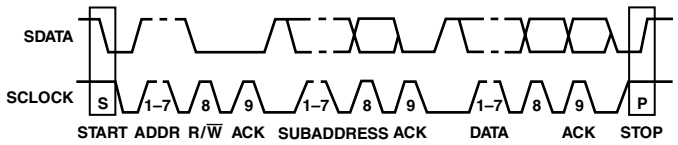


Figure 5. Bus Data Transfer

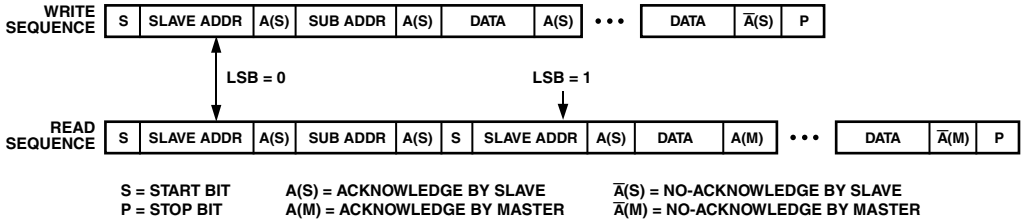


Figure 6. Write and Read Sequence

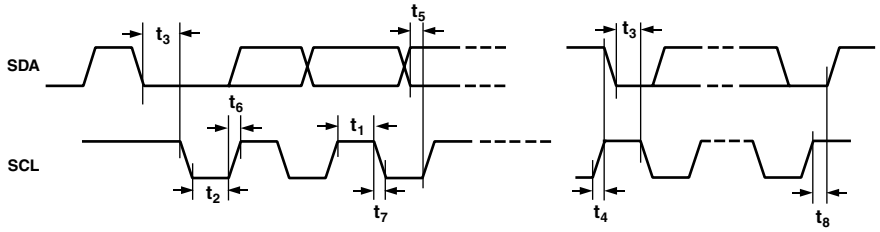


Figure 7. I²C MPU Port Timing Diagram

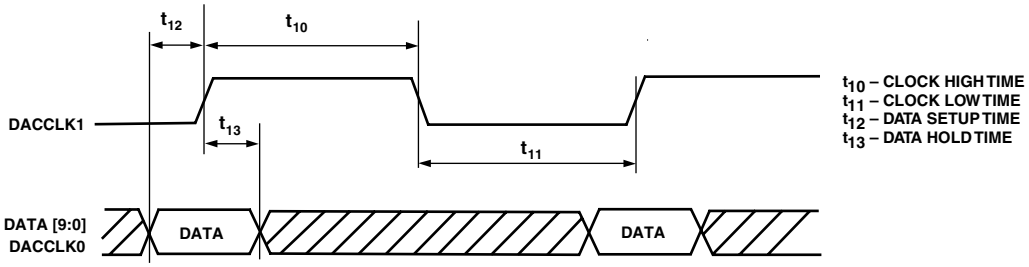


Figure 8. Input Data Format Timing Diagram Single Clock

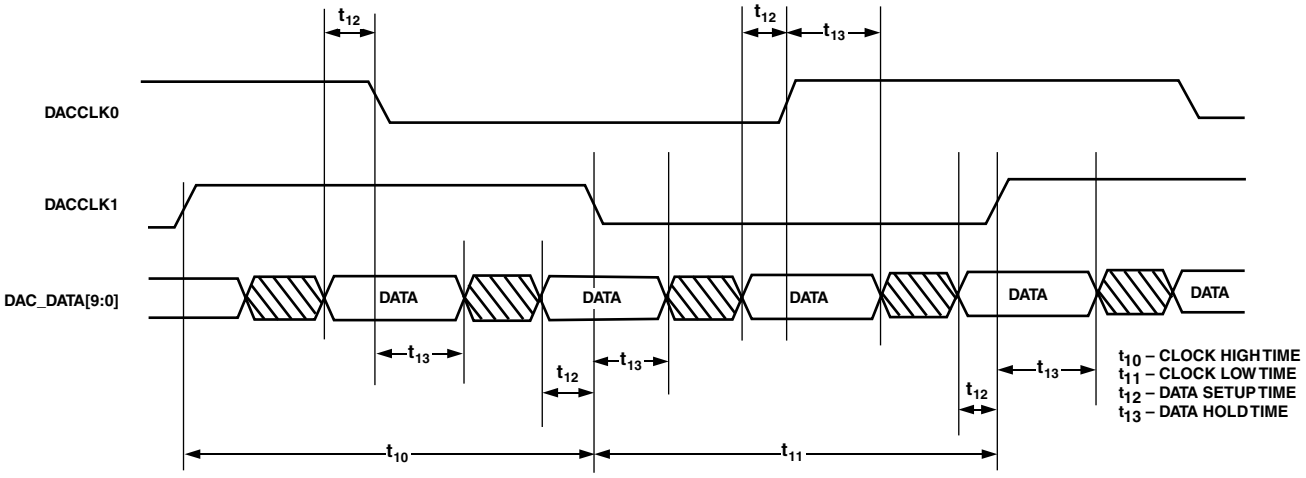


Figure 9. Input Data Format Timing Diagram Dual Clock

DIGITAL DATA INPUT TIMING DIAGRAMS

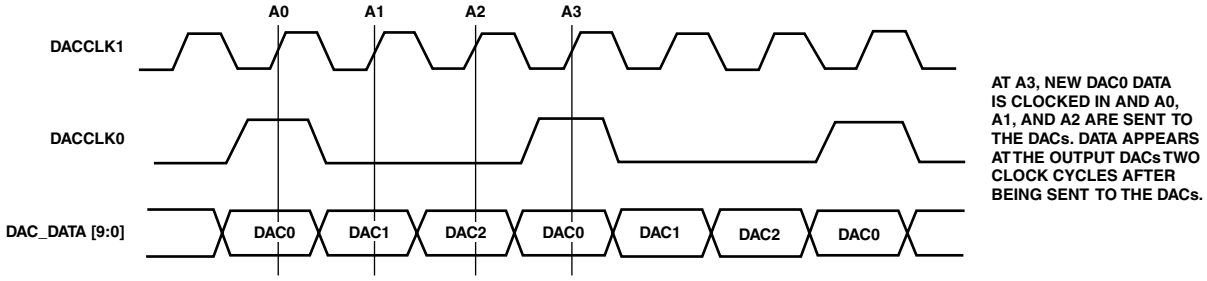


*Figure 10. DAC Mode 1, Single Clock, Single Edge Input Data Format Timing Diagram**

*The figure shows three DAC usages. DACCLK0 is a data line that indicates the data is for DAC0.

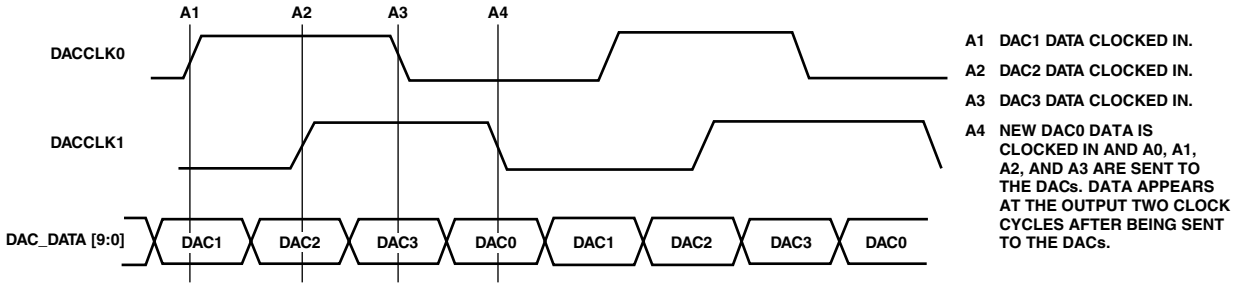


Figure 11. DAC Mode 2, Dual Clock, Dual Edge Input Data Format Timing Diagram

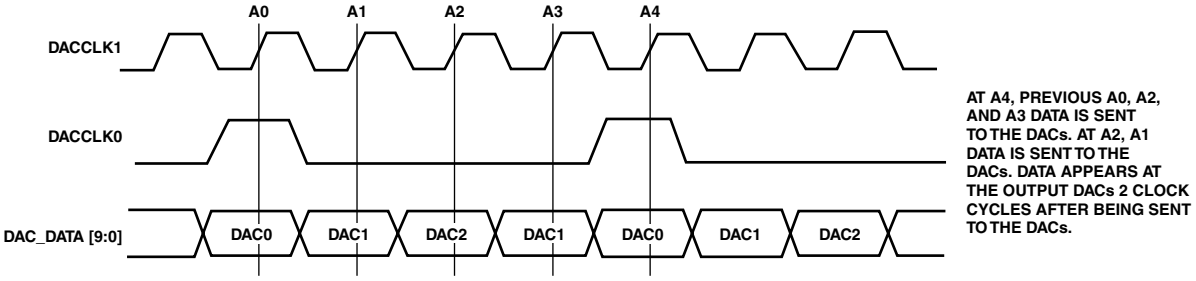


Figure 12. DAC Mode 3, 4:2:2 Input Data Format Timing Diagram

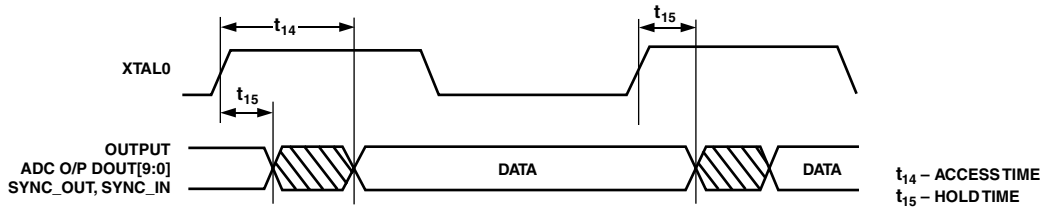


Figure 13. Digital O/P Timing

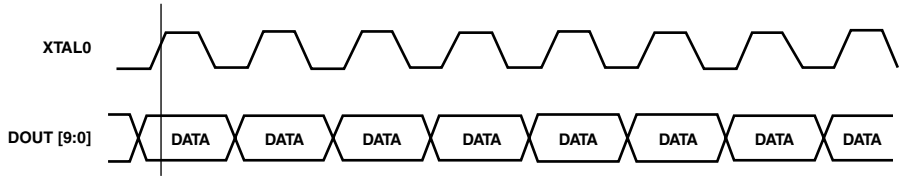


Figure 14. Standard Mode Digital Data O/P Format

REGISTER ACCESS

The MPU can write to or read from all of the registers of the ADV7202 except the Subaddress Registers, which are write-only. The Subaddress Register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the Subaddress Register. A read/write operation is then performed from/to the target address which then increments to the next address until a Stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes the functionality of each register. All registers can be read from as well as written to.

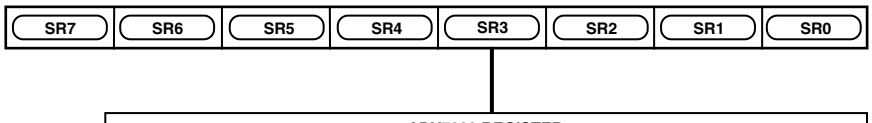
Subaddress Register (SR7–SR0)

The Communications Register is an 8-bit write-only register. After the part has been accessed over the bus, and a read/write operation is selected, the subaddress is set up. The Subaddress Register determines to/from which register the operation takes place.

Figure 15 shows the various operations under the control of the Subaddress Register. "0" should always be written to SR7.

Register Select (SR6–SR0)

These bits are set up to point to the required starting address.



ADV7202 REGISTER								
ADDRESS	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
00h	0	0	0	0	0	0	0	MODE REGISTER 0
01h	0	0	0	0	0	0	1	MODE REGISTER 1
02h	0	0	0	0	0	1	0	MODE REGISTER 2
03h	0	0	0	0	0	1	1	MODE REGISTER 3
04h	0	0	0	0	1	0	0	AGC REGISTER 0
05h	0	0	0	0	1	0	1	AGC REGISTER 1
06h	0	0	0	0	1	1	0	CLAMP REGISTER 0
07h	0	0	0	0	1	1	1	CLAMP REGISTER 1
08h	0	0	0	1	0	0	0	CLAMP REGISTER 2
09h	0	0	0	1	0	0	1	CLAMP REGISTER 3
0Ah	0	0	0	1	0	1	0	TIMING REGISTER
0Bh	0	0	0	1	0	1	1	V_{REF} ADJUST REGISTER
0Ch	0	0	0	1	1	0	0	RESERVED
0Dh	0	0	0	1	1	0	1	RESERVED
0Eh	0	0	0	1	1	1	0	RESERVED
0Fh	0	0	0	1	1	1	1	RESERVED
10h	0	0	1	0	0	0	0	AUX REGISTER 0
11h	0	0	1	0	0	0	1	AUX REGISTER 1
12h	0	0	1	0	0	1	1	AUX REGISTER 2
13h	0	0	1	0	0	0	0	AUX REGISTER 3
14h	0	0	1	0	1	0	0	AUX REGISTER 4
15h	0	0	1	0	1	0	1	AUX REGISTER 5
16h	0	0	1	0	1	1	0	AUX REGISTER 6
17h	0	0	1	0	1	1	1	AUX REGISTER 7

Figure 15. Subaddress Registers

MODE REGISTER 0
MR0 (MR07–MR00)
(Address (SR4–SR0) = 00H)
Figure 16 shows the various operations under the control of Mode Register 0.

MR0 BIT DESCRIPTION
ADC Reference Voltage (MR00)
This control bit is used to select the ADC reference voltage. When this bit is set to "0," a reference voltage of 1.1 V is selected. When the bit is set to "1," a reference voltage of 2.2 V is selected.

External Reference Enable (MR01)
Setting this bit to "1" enables an external voltage reference for the ADC.

Voltage Reference Power-Down (MR02)
Setting this bit to "1" causes the internal DAC voltage reference to power down.

ADC Power-Down (MR03)
Setting this bit to "1" causes the video rate ADC to power down.

Power-Down (MR04)
Setting this bit to "1" puts the device into power-down mode.

Reserved (MR05–MR07)
Zero must be written to these bits.

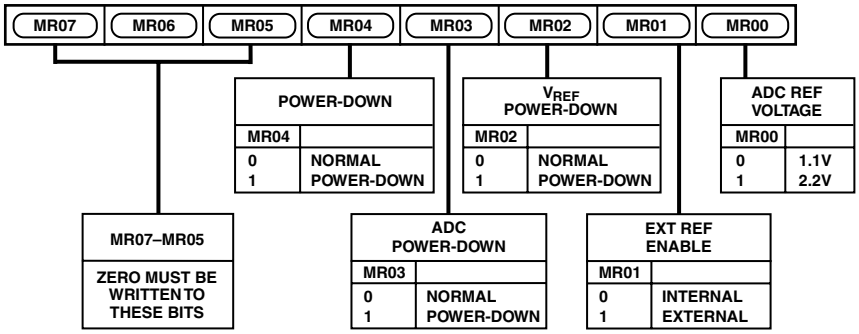


Figure 16. Mode Register 0

MODE REGISTER 1
MR1 (MR17–MR10)
(Address (SR4–SR0) = 01H)
Figure 17 shows the various operations under the control of Mode Register 1.

MR1 BIT DESCRIPTION
DAC0 Control (MR10)
Setting this bit to "0" enables DAC0; otherwise, this DAC is powered down.

DAC1 Control (MR11)
Setting this bit to "0" enables DAC1; otherwise, this DAC is powered down.

DAC2 Control (MR12)
Setting this bit to "0" enables DAC2; otherwise, this DAC is powered down.

DAC3 Control (MR13)
Setting this bit to "0" enables DAC3; otherwise, this DAC is powered down.

Dual Edge Clock (MR14)
Setting this bit to "1" allows data to be read into the DACs on both edges of the clock; hence, data may be read in at twice the clock frequency. See Figure 17. If this bit is set to "0," the data will only be strobed on the rising edge of the clock.

Dual Clock (MR15)
Setting this bit to "1" allows the use of two clocks to strobe data into the DACs. See Figure 17. It is possible to clock data in with only one clock and use the second clock to contain timing information.

4:2:2 Mode (MR16)
Setting this bit to "1" enables data to be input in 4:2:2 format. 4:2:2 mode will only work if MR14 and MR15 register bits are set to zero.

DAC Input Invert (MR17)
Setting this bit to "1" causes the input data to the DACs to be inverted allowing for an external inverting amplifier.

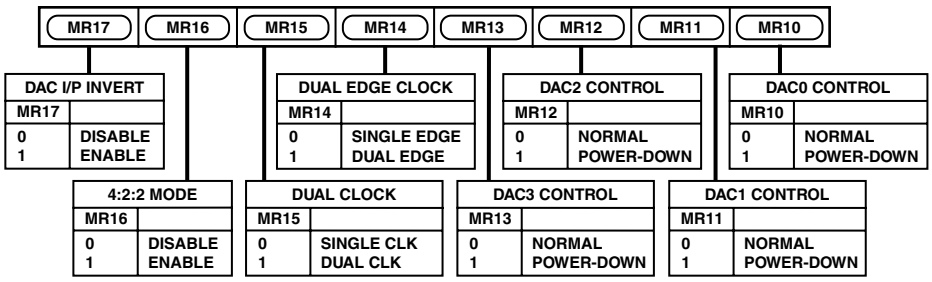


Figure 17. Mode Register 1

MODE REGISTER 2
MR2 (MR20–MR27)
(Address (SR4–SR0) = 02H)
Figure 18 shows the various operations under the control of Mode Register 2.

MR2 BIT DESCRIPTION
Analog Input Configuration (MR20–MR23)
This control selects the analog input configuration, up to five CVBS input channels, or two component YUV, or three S-Video and eight auxiliary inputs. See Figure 18 for details.

SHA0 Control (MR24)
Setting this bit to "0" enables SHA0; otherwise, this SHA is powered down (SHA = Sample and Hold Amplifier).

SHA1 Control (MR25)
Setting this bit to "0" enables SHA1; otherwise, this SHA is powered down.

SHA2 Control (MR26)
Setting this bit to "0" enables SHA2; otherwise, this SHA is powered down.

AUX Control (MR27)
Setting this bit to "0" enables the auxiliary ADC; otherwise, Aux ADC is powered down.

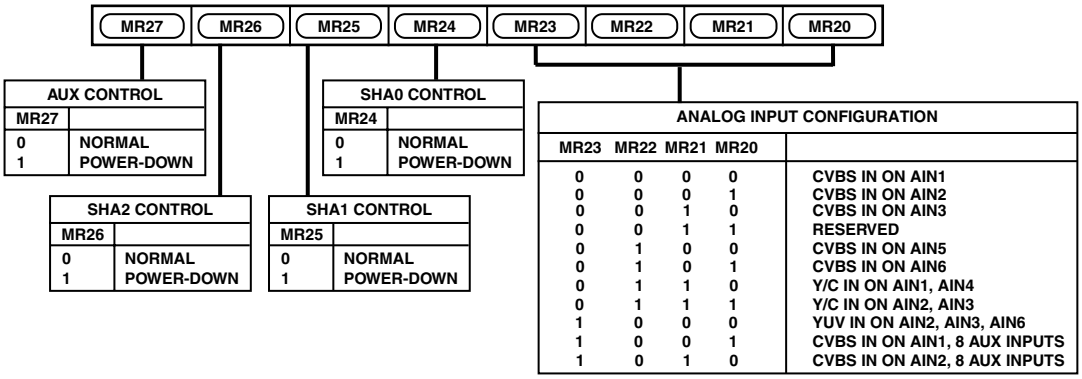


Figure 18. Mode Register 2

MODE REGISTER 3
MR3 (MR30–MR37)
(Address (SR4–SR0) = 03H)
Figure 19 shows the various operations under the control of Mode Register 3.

MR3 BIT DESCRIPTION
Clamp Current (MR30)
Setting this bit to "1" enables the halving of all clamp currents.

Analog Input Mode (MR31)
Setting this bit to "1" enables differential mode for the analog inputs; otherwise, the inputs are single-ended. See Figure 19.

SHA Gain (MR32)
Setting this bit to "0" enables SHA gain of 1. If the bit is set to "1," the SHA gain is 2. The SHA gain will limit the input signal range. See Figure 19.

Voltage Clamp (MR33)
Setting this bit to "1" will enable the voltage clamps.

Output Enable (MR34)
Setting this bit to "1" puts the digital outputs into high impedance.

SYNC Polarity (MR35)
This bit controls the polarity of the SYNC_IN pin. If the bit is set to "0," a logic low pulse corresponds to H-Sync. If the bit is "1," a logic high pulse corresponds to H-Sync. This sync in pulse can then be used to control the synchronization of AGC/Clamping. See AR12.

Reserved (MR36–MR37)
Zero must be written to both these registers.

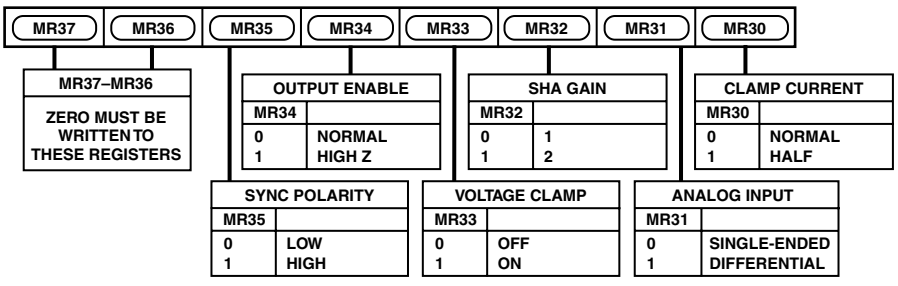


Figure 19. Mode Register 3

AGC REGISTER 0
AR0 (AR00–AR07)
(Address (SR4–SR0) = 04H)
Figure 20 shows the various operations under the control of AGC Register 0.

AR0 BIT DESCRIPTION
AGC Multiplier (AR00–AR07)
This register holds the last eight bits of the 12-bit AGC multiplier word.

AGC REGISTER 1
AR1 (AR08–AR15)
(Address (SR4–SR0) = 05H)
Figure 20 shows the various operations under the control of AGC Register 1.

AR1 BIT DESCRIPTION
AGC Multiplier (AR08–AR11)
These registers hold the first four bits of the 12-bit AGC multiplier word.

AGC Sync Enable (AR12)
Setting this bit to "1" forces the AGC to wait until the next sync pulse before switching on.

Reserved (AR13–AR15)
Zero must be written to these registers.

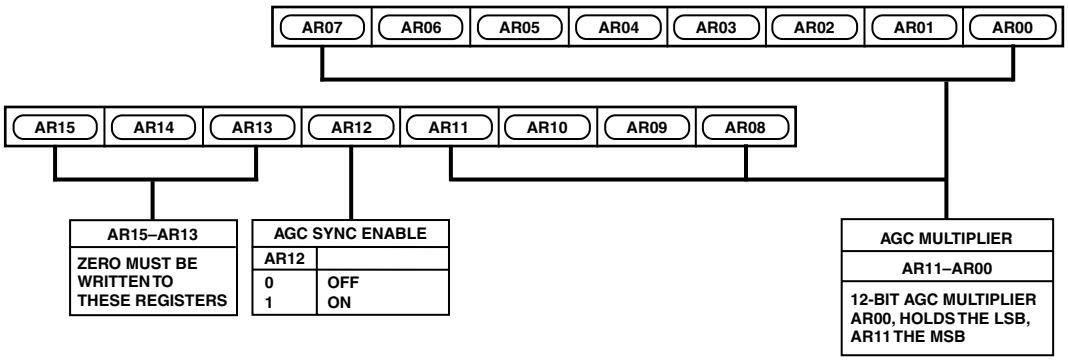


Figure 20. AGC Registers 0–1

CLAMP REGISTER 0
CR0 (CR00–CR07)
(Address (SR4–SR0) = 06H)
Figure 21 shows the various operations under the control of Clamp Register 0.

CR0 BIT DESCRIPTION
Clamp Level/16 (CR00–CR06)
To perform an accurate AGC gain operation, it is necessary to know to what level the user is clamping the black level. This black level is then subtracted from the 10-bit ADC output before gaining. It is then added on again afterwards. It should be noted that this register is seven bit and will hold the value of Clamp Value/16.

Reserved (CR07)
Zero must be written to this bit.

CLAMP REGISTER 1
CR1 (CR10–CR17)
(Address (SR4–SR0) = 07H)
Figure 22 shows the various operations under the control of Clamp Register 1.

CR1 BIT DESCRIPTION
Fine Clamp On Time (CR10–CR12)
There are three fine clamp circuits on the chip. This word controls the number of clock cycles for which the fine clamps are switched on per video line. The clamp is switched on after a SYNC pulse is received on the SYNC_IN pin, provided the relevant enabling bit is set (see CR16).

Coarse Clamp On Time (CR13–CR15)
There are three coarse clamp circuits on the chip. This I^2C word controls the number of clock cycles for which the fine clamps are switched on per video line. The clamp is switched on after a SYNC pulse is received on the SYNC_IN pin, provided the relevant enabling bit is set (see CR16).

Synchronize Clamps (CR16)
Setting this bit to "1" forces the clamps to wait until the next sync pulse before switching on.

Reserved (CR17)
Zero must be written to this bit.

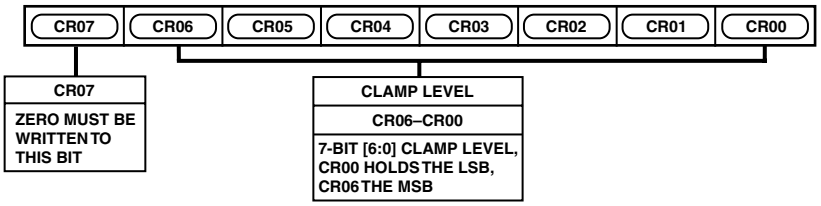


Figure 21. Clamp Register 0

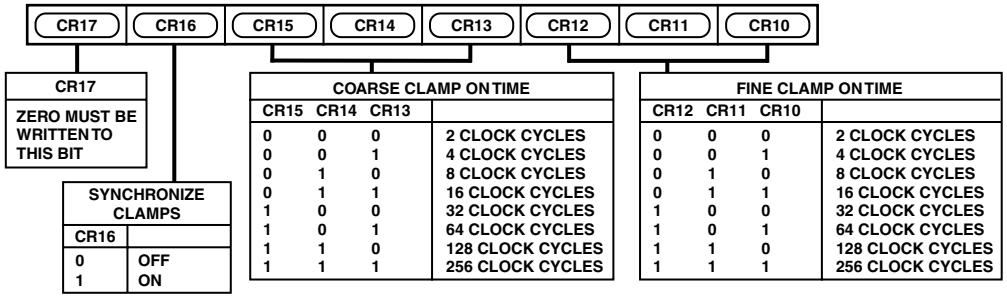


Figure 22. Clamp Register 1

CLAMP REGISTER 2
CR2 (CR20–CR27)
(Address (SR4–SR0) = 08H)
Figure 23 shows the various operations under the control of Clamp Register 2.

CR2 BIT DESCRIPTION
Fine Clamp 0 Up/Down (CR20)
This bit controls the direction of fine clamp number 0, valid only if the clamp is enabled.

Fine Clamp 0 ON/OFF (CR21)
This bit switches fine clamp number 0 on for the prescribed number of clock cycles (CR10–CR12).

Fine Clamp 1 Up/Down (CR22)
This bit controls the direction of fine clamp number 1, valid only if the clamp is enabled.

Fine Clamp 1 ON/OFF (CR23)
This bit switches fine clamp number 1 on for the prescribed number of clock cycles (CR10–CR12).

Fine Clamp 2 Up/Down (CR24)
This bit controls the direction of fine clamp number 2, valid only if the clamp is enabled.

Fine Clamp 2 ON/OFF (CR25)
This bit switches fine clamp number 2 on for the prescribed number of clock cycles (CR10–CR12).

Reserved (CR26–CR27)
Zero must be written to these registers.

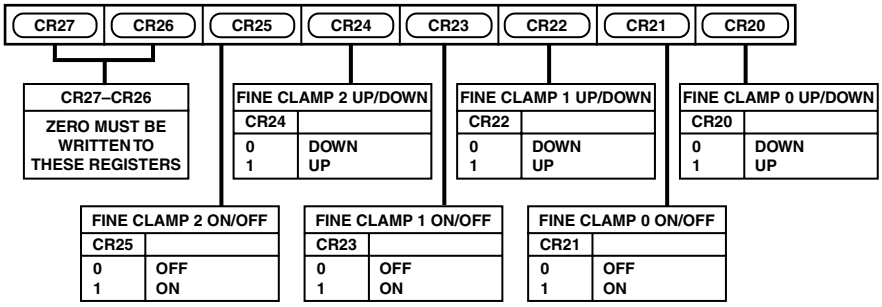


Figure 23. Clamp Register 2

CLAMP REGISTER 3
CR3 (CR30–CR37)
(Address (SR4–SR0) = 09H)
Figure 24 shows the various operations under the control of Clamp Register 3.

CR3 BIT DESCRIPTION
Coarse Clamp 0 Up/Down (CR30)
This bit controls the direction of coarse clamp number 0, valid only if the clamp is enabled.

Coarse Clamp 0 ON/OFF (CR31)
This bit switches coarse clamp number 0 on for the prescribed number of clock cycles (CR13–CR15).

Coarse Clamp 1 Up/Down (CR32)
This bit controls the direction of coarse clamp number 1, valid only if the clamp is enabled.

Coarse Clamp 1 ON/OFF (CR33)
This bit switches coarse clamp number 1 on for the prescribed number of clock cycles (CR13–CR15).

Coarse Clamp 2 Up/Down (CR34)
This bit controls the direction of coarse clamp number 2, valid only if the clamp is enabled.

Coarse Clamp 2 ON/OFF (CR35)
This bit switches coarse clamp number 2 on for the prescribed number of clock cycles (CR13–CR15).

Reserved (CR36–CR37)
Zero must be written to these registers.

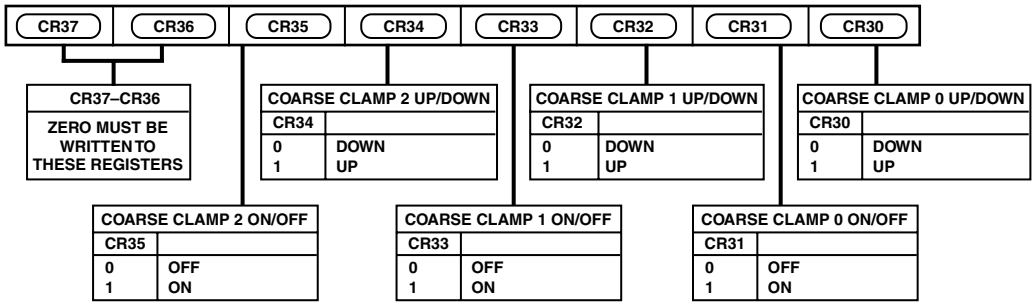


Figure 24. Clamp Register 3

TIMING REGISTER
TR (TR00–TR07)
(Address (SR4–SR0) = 0AH)
Figure 25 shows the various operations under the control of the Timing Register.

TR BIT DESCRIPTION
Crystal Oscillator Circuit (TR00)
If this bit is set to "0," the internal oscillator circuit will be disabled. Disabling the oscillator circuit is possible when an external clock module is used, thus saving power.

ADC Bias Currents (TR01)
If this bit is set to "1," all analog bias currents will be doubled.

Duty Cycle Equalizer (TR03)
When this bit is set to "1," the clock duty cycle equalizer circuit is active. This will only have an effect on the ADC operation. The digital core clock will not be affected.

Clock Delay (TR05–TR06)
Using these two bits, it is possible to insert a delay in the clock signal to the digital core. These bits control the insertion of the delay.

Reserved (TR02, TR04, TR07)
Zero must be written to the bits in these registers.

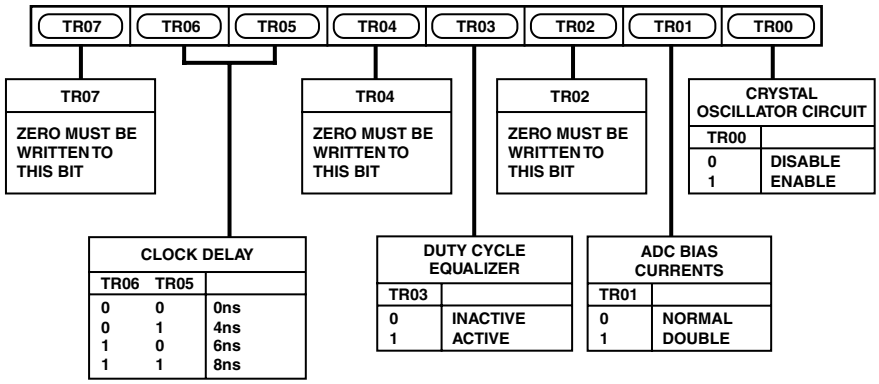


Figure 25. Timing Register 0

VREF ADJUST REGISTER
VR (VR00–VR07)
(Address (SR4–SR0) = 0BH)
Figure 26 shows the various operations under the control of the VREF Adjust Register.

VR BIT DESCRIPTION
Reserved (VR00)
This register is reserved and "1" must be written to this bit.

Reserved (VR01–VR03)
Zero must be written to these registers.

ADC Reference Voltage Adjust (VR04–VR06)
By setting the value of this 3-bit word, it is possible to trim the ADC internal voltage reference VREFADC.

Reserved (VR07)
Zero must be written to this register.

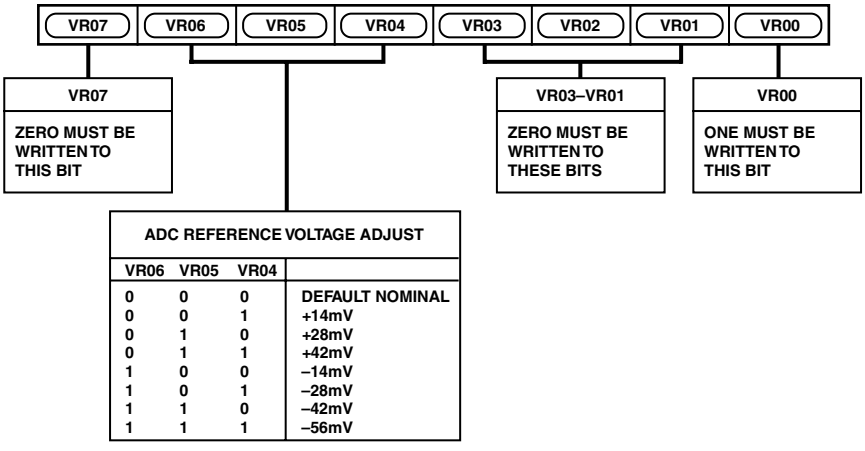


Figure 26. ADC VREF Register

AUXILIARY MONITORING REGISTERS
AU (AU00–AU07)
(Address (SR4–SR0) = 10H)

There are eight Auxiliary Monitoring Registers. These registers are read-only; when the device is configured for auxiliary inputs, they will display a value corresponding to the converted auxiliary input. Auxiliary Register 0 will contain the value of the converted auxiliary 0 input, Auxiliary Register 1 the value of the converted auxiliary 1 input, and so on to Auxiliary Register 7.

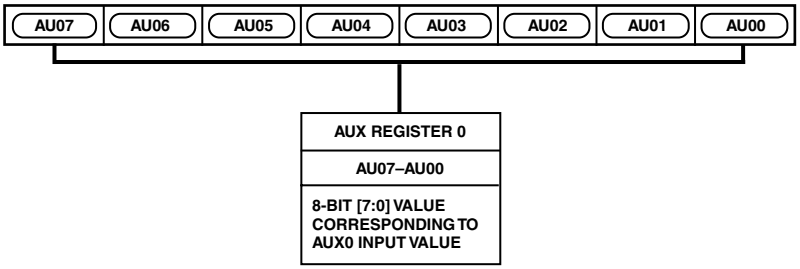


Figure 27. AUX Register 0

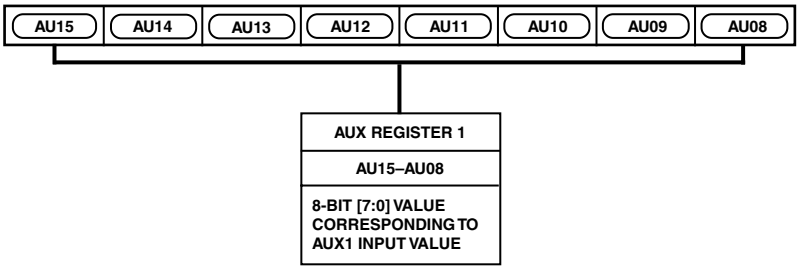


Figure 28. AUX Register 1

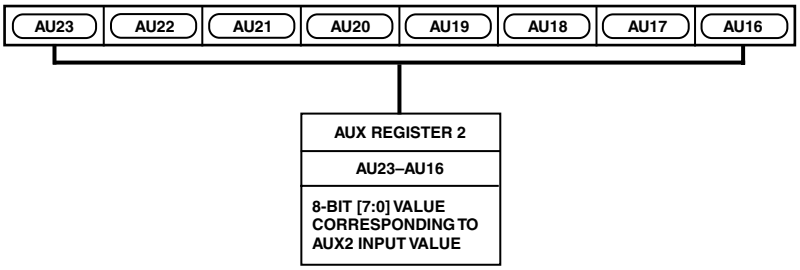


Figure 29. AUX Register 2

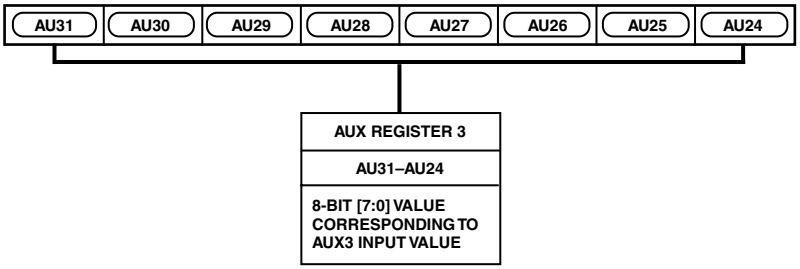


Figure 30. AUX Register 3

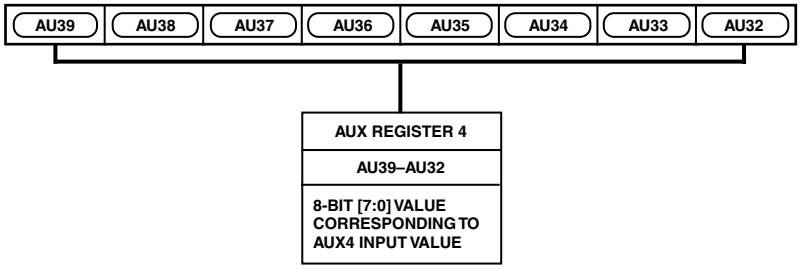


Figure 31. AUX Register 4

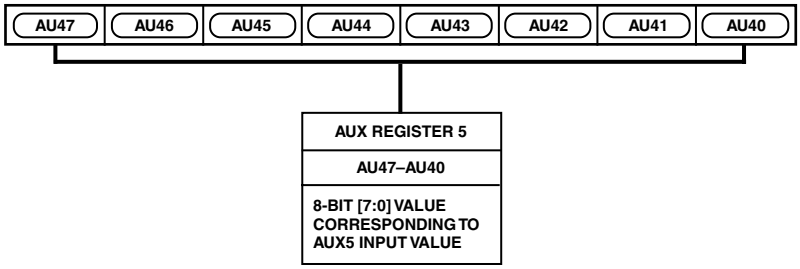


Figure 32. AUX Register 5

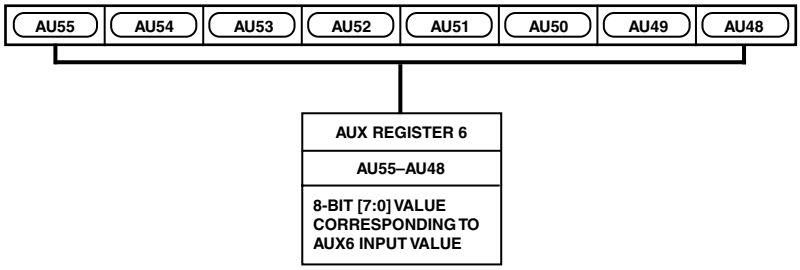


Figure 33. AUX Register 6

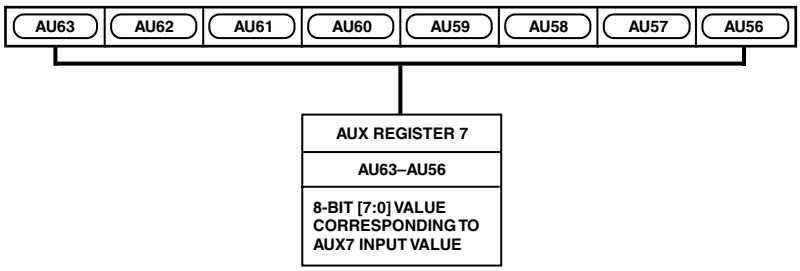


Figure 34. AUX Register 7

CLAMP CONTROL

The clamp control has two modes of operation, if the synchronize clamp control bit CR16 (Bit-6 address 07h) is set, then the clamps that are enabled will be switched on for the programmed time when triggered by the Sync_IN control signal, this control signal is edge detected and its polarity can be set by MR35 (Bit 5 Address 03h). If the synchronize clamp control bit is set to zero, when enabled each clamp will switch on for the programmed time. The clamp control bits are edge detected and the bits must first be reset to zero before the clamps can be switched on again.

DAC TERMINATION AND LAYOUT CONSIDERATIONS

Resistor R_{SET} is connected between the RSET pin and AVSS and is used to control the amplitude of the DAC output current.

$$I_{MAX} = 5.196/R_{SET}\ \ Amps \quad (3)$$

Therefore, a recommended RSET value of 1200 Ω will enable an I_{MAX} of 4.43 mA. $V_{MAX} = R_{LOAD} \times I_{MAX}$, R_{LOAD} should have a value of 300 Ω.

The ADV7202 has four analog outputs—DAC0, DAC1, DAC2, and DAC3. For cable driving the DACs should be used with an external buffer. Suitable op amps are the AD8057 or AD8061.

PC BOARD LAYOUT CONSIDERATIONS

The ADV7202 is optimally designed for the lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7202, it is imperative that great care be given to the PC board layout.

The layout should be optimized for lowest noise on the ADV7202 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of AVDD, AVSS, DVDD, and DVSS pins should be kept as short as possible to minimize inductive ringing.

It is recommended that a four-layer printed circuit board be used, with power and ground planes separating the layer of the signal carrying traces of the components and solder side layer. Placement of components should be considered to separate noisy circuits, such as crystal clocks, high speed logic circuitry, and analog circuitry.

There should be separate analog and digital ground planes (AVSS and DVSS).

Power planes should encompass a digital power plane (DVDD) and an analog power plane (AVDD). The analog power plane should contain the ADCs and all associated circuitry, including VREF circuitry. The digital power plane should contain all logic circuitry. The analog and digital power planes should be individually connected to the common power plane at one single point through a suitable filtering device such as a ferrite bead.

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the DACs be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than three inches). The DAC termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane. As well as minimizing reflections, short analog output traces will reduce noise pickup due to neighboring digital circuitry.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of decoupling capacitors.

Optimum performance is achieved by the use of 0.1 µF ceramic capacitors. Each of the group of AVDD or DVDD pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

Digital Signal Interconnect

The digital signal lines should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7202 should be avoided to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the digital power plane and not the analog power plane.

Analog Signal Interconnect

The ADV7202 should be located as close as possible to the output connectors, thus minimizing noise pickup and reflections due to impedance mismatch.

For optimum performance, the analog outputs should each be source and load terminated, as shown in Figure 35. The termination resistors should be as close as possible to the ADV7202 to minimize reflections.

Any unused inputs should be tied to the ground.

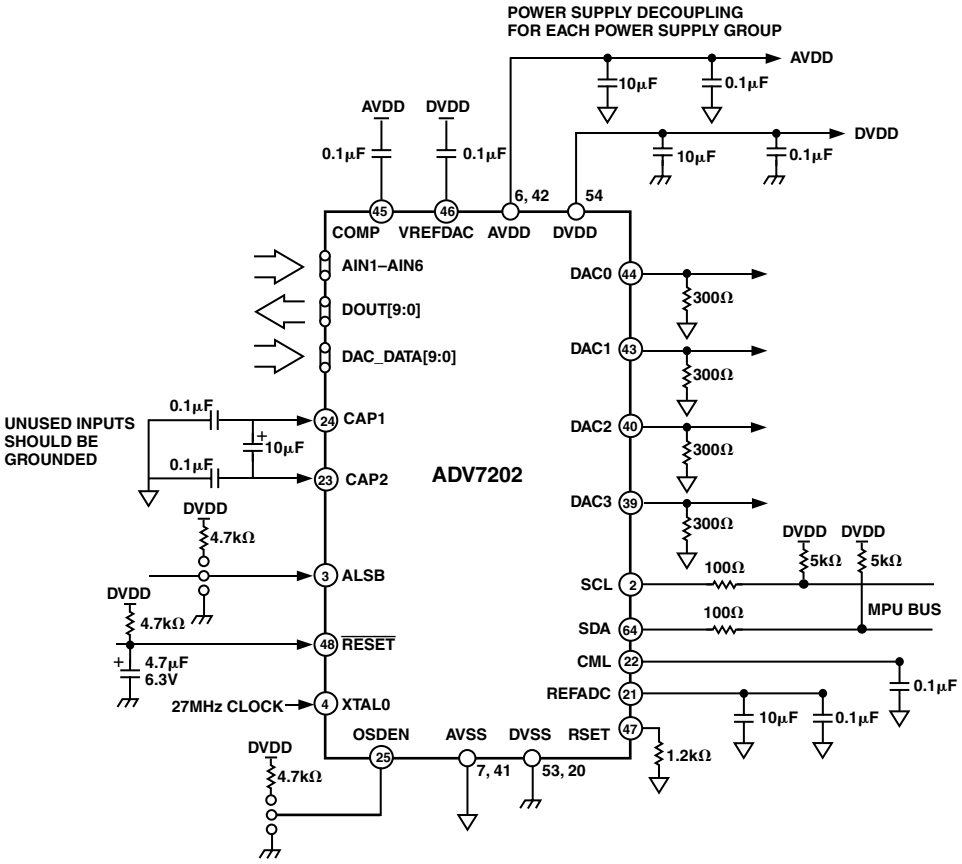
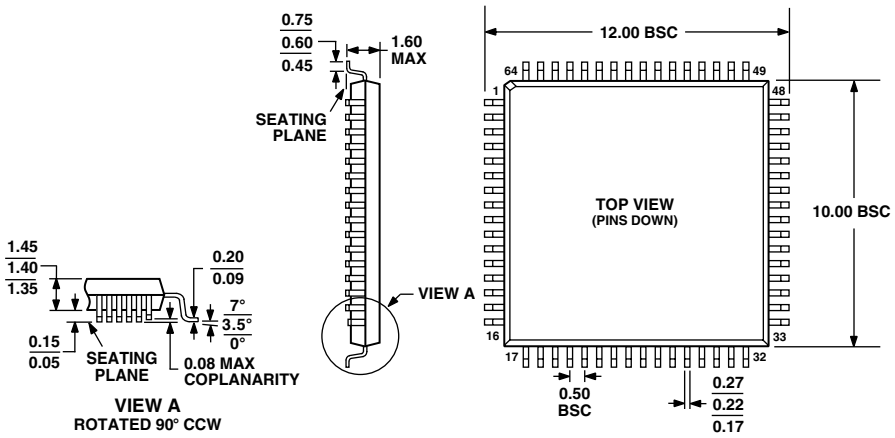


Figure 35. Suggested Schematic

OUTLINE DIMENSIONS

64-Lead Plastic Quad Flatpack [LQFP]
(ST-64B)

Dimensions shown in millimeters



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