

Features

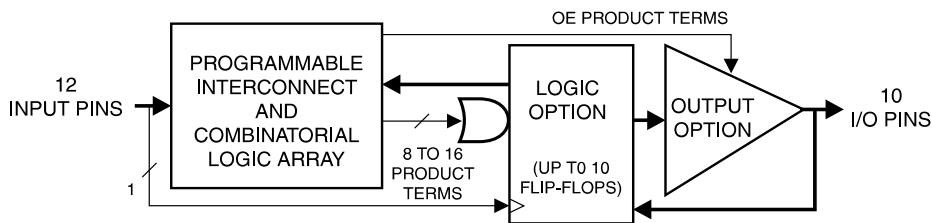
- Low-voltage Programmable Logic Device
 - Wide Power Supply Range - 3.0V to 5.5V
 - Ideal for Battery Powered Systems
- High-speed Operation
 - 20 ns Maximum Propagation Delay at $V_{CC} = 3.0V$
- Commercial and Industrial Temperature Ranges
- Familiar 22V10 Logic Architecture
- Low-power 3-volt CMOS Operation

| | AT22LV10L | AT22LV10 |
|---------------|-----------|-----------|
| Temp | Com./Ind. | Com./Ind. |
| I_{CC} (mA) | 4/5 | 35/45 |

$V_{CC} = 3.6V$

- CMOS and TTL Compatible Inputs and Outputs
 - 10 μA Leakage Maximum
- Reprogrammable – Tested 100% for Programmability
- High-reliability CMOS Technology
 - 2000V ESD Protection
 - 200 mA Latchup Immunity
- Dual-in-line and Surface Mount Packages

Logic Diagram



Description

The AT22LV10 and AT22LV10L are low-voltage compatible CMOS high-performance Programmable Logic Devices (PLDs). Speeds down to 20 ns and power dissipation as low as 14.4 mW are offered. All speed ranges are specified over the 3.0V to 5.5V range. All pins offer a low $\pm 10 \mu A$ leakage.

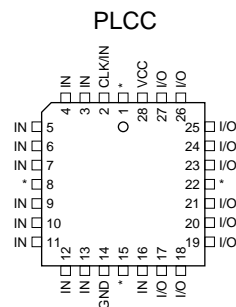
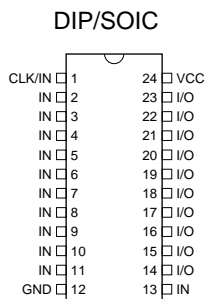
The AT22LV10L provides the optimum low-power CMOS PLD solution, with low DC power (1 mA typical at $V_{CC} = 3.3V$) and full CMOS output levels. The AT22LV10L significantly reduces total system power, allowing battery powered operation.

(continued)

Pin Configurations

All Pinouts Top View

| Pin Name | Function |
|----------|------------------------|
| CLK/IN | Clock and Logic Input |
| IN | Logic Inputs |
| I/O | Bidirectional Buffers |
| * | No Internal Connection |
| VCC | 3.0V to 5.5V Supply |



Rev. 0190E-08/99



Low-voltage UV
Erasable
Programmable
Logic Device

AT22LV10
AT22LV10L



Full CMOS output levels help reduce power in many other system components.

The AT22LV10 and AT22LV10L logic architectures are identical to the familiar 22V10. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all ten registers. All registers are automatically cleared upon power-up.

Register preload simplifies testing. A security fuse prevents unauthorized copying of programmed fuse patterns.

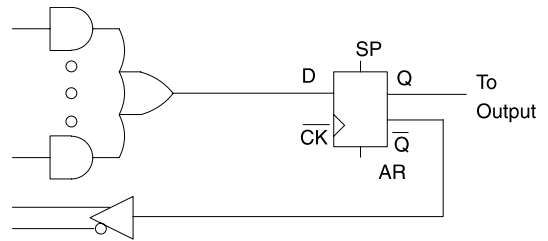
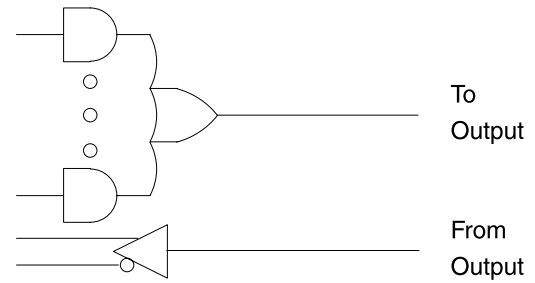
Absolute Maximum Ratings*

| | |
|--|--------------------------------|
| Temperature Under Bias..... | -55°C to +125°C |
| Storage Temperature..... | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground..... | -2.0V to +7.0V ⁽¹⁾ |
| Voltage on Input Pins with Respect to Ground During Programming..... | -2.0V to +14.0V ⁽¹⁾ |
| Programming Voltage with Respect to Ground..... | -2.0V to +14.0V ⁽¹⁾ |
| Integrated UV Erase Dose..... | 7258 W·sec/cm ² |

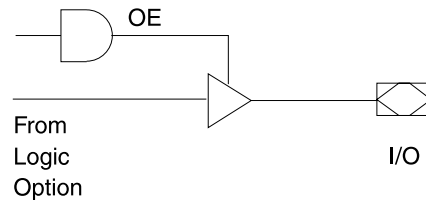
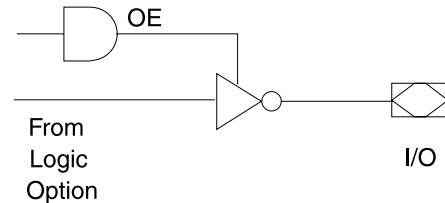
***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum pin voltage is $V_{CC} + 0.75V$ DC which may undershoot to $V_{CC} + 2.0V$ for pulses of less than 20 ns.

Logic Options



Output Options



DC and AC Operating Conditions

| | Commercial | Industrial |
|---------------------------------|--------------|--------------|
| Operating Temperature (Ambient) | 0°C - 70°C | -40°C - 85°C |
| V_{CC} Power Supply | 3.0V to 5.5V | 3.0V to 5.5V |

DC Characteristics

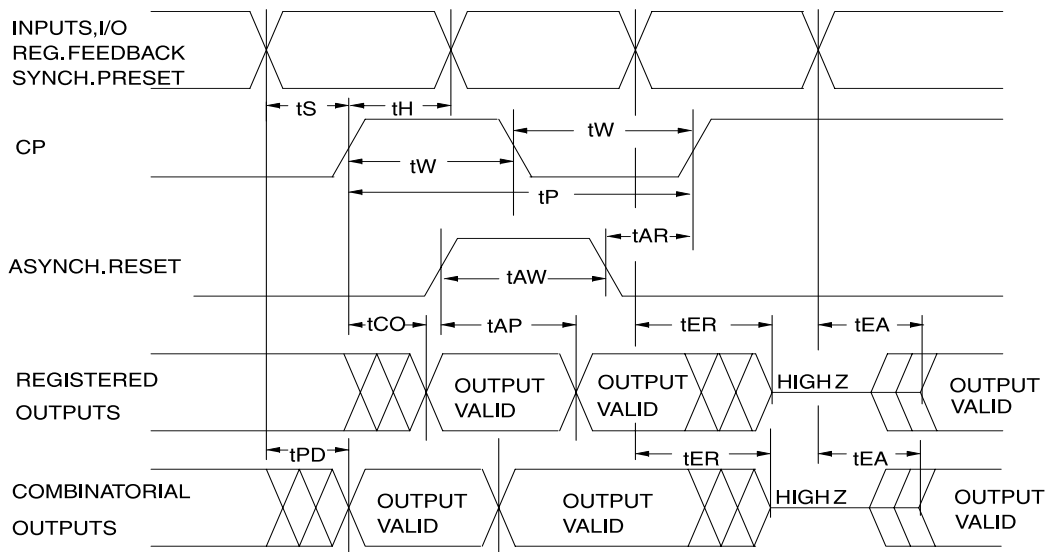
| Symbol | Parameter | Condition ⁽²⁾ | | | Min | Typ | Max | Units |
|----------------|---|--|----------------------------|------------------|----------------|-------|-----------------|---------|
| I_{LI} | Input Load Current | $V_{IN} = -0.1V$ to $V_{CC} + 1V$ | | | | | 10 | μA |
| I_{LO} | Output Leakage Current | $V_{OUT} = -0.1V$ to $V_{CC} + 0.1V$ | | | | | 10 | μA |
| I_{CC} | Power Supply Current | $V_{CC} = 3.6V/5.5V$, $V_{IN} = GND$, Outputs Open | AT22LV10 | Com. | | 20/50 | 35/90 | mA |
| | | | | Ind. | | 20/50 | 45/100 | mA |
| | | | AT22LV10L | Com. | | 1/2 | 4/12 | mA |
| | | | | Ind. | | 1/2 | 5/15 | mA |
| $I_{OS}^{(1)}$ | Output Short Circuit Current | $V_{OUT} = 0.5V$ | | | | | -120 | mA |
| V_{IL1} | Input Low Voltage | $4.5V \leq V_{CC} \leq 5.5V$ | | | -0.6 | | 0.8 | V |
| V_{IL2} | Input Low Voltage | $3.0V \leq V_{CC} < 4.5V$ | | | -0.6 | | 0.6 | V |
| V_{IH} | Input High Voltage | | | | 2.0 | | $V_{CC} + 0.75$ | V |
| V_{OL} | Output Low Voltage $V_{IN} = V_{IH}$ or V_{IL} | $V_{CC} = 3.0V$ | Com., Ind. | $I_{OL} = 8$ mA | | | 0.5 | V |
| | | $V_{CC} = 4.5V$ | Com., Ind. | $I_{OL} = 16$ mA | | | 0.5 | V |
| | | $V_{CC} = 3.0V$ | Com., Ind. | $I_{OL} = 6$ mA | | | 0.35 | V |
| V_{OH} | Output High Voltage | $V_{IN} = V_{IH}$ or V_{IL} , $V_{CC} = 3.0V/4.5V$ | $I_{OH} = -100$ μA | | $V_{CC} - 0.3$ | | | V |
| | | | $I_{OH} = -0.4$ mA/-4.0 mA | | 2.4 | | | V |

- Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. For DC characteristics, the test condition of $V_{CC} = \text{Max}$ corresponds to 3.6V.

AC Characteristics for the AT22LV10

| Symbol | Parameter | AT22LV10-20 | | | AT22LV10-25 | | | Units |
|-----------|---|-------------|-----|-------|-------------|-----|------|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| t_{PD} | Input or Feedback to Non-Registered Output | | 12 | 20 | | 15 | 25 | ns |
| t_{EA} | Input to Output Enable | | | 20 | | 15 | 25 | ns |
| t_{ER} | Input to Output Disable | | | 20 | | 15 | 25 | ns |
| t_{CF} | Clock to Feedback | 0 | 4 | 9 | 0 | 5 | 9 | ns |
| t_{CO} | Clock to Output | 0 | 8 | 14 | 0 | 10 | 17 | ns |
| t_S | Input or Feedback Setup Time | 10 | 6 | | 12 | 7 | | ns |
| t_H | Hold Time | 0 | | | 0 | | | ns |
| t_P | Clock Period | 10 | | | 12 | | | ns |
| t_W | Clock Width | 5 | | | 6 | | | ns |
| F_{MAX} | External Feedback $1/(t_S+t_{CO})$ | | | 41.6 | | | 34.5 | MHz |
| | Internal Feedback $1/(t_S + t_{CF})$ | | | 52.6 | | | 47.6 | MHz |
| | No Feedback $1/(t_P)$ | | | 100.0 | | | 83.3 | MHz |
| t_{AW} | Asynchronous Reset Width | 20 | 12 | | 25 | 15 | | ns |
| t_{AR} | Asynchronous Reset, Synchronous Preset, Recovery Time | 20 | 12 | | 25 | 15 | | ns |
| t_{AP} | Asynchronous Reset to Registered Output Reset | | 15 | 25 | | 18 | 28 | ns |

AC Waveforms⁽¹⁾

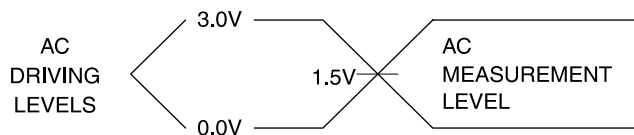


Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

AC Characteristics for the AT22LV10L

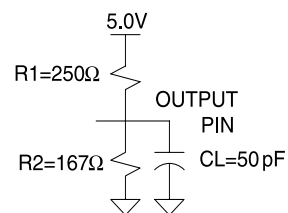
| Symbol | Parameter | AT22LV10L-25 | | | Units |
|-----------|---|--------------|-----|------|-------|
| | | Min | Typ | Max | |
| t_{PD} | Input or Feedback to Non-Registered Output | | 15 | 25 | ns |
| t_{EA} | Input to Output Enable | | 15 | 25 | ns |
| t_{ER} | Input to Output Disable | | 15 | 25 | ns |
| t_{CF} | Clock to Feedback | 0 | 5 | 9 | ns |
| t_{CO} | Clock to Output | 0 | 10 | 14 | ns |
| t_{SF} | Feedback Setup Time | 12 | 7 | | ns |
| t_S | Input Setup Time | 17 | 15 | | ns |
| t_H | Hold Time | 0 | | | ns |
| t_P | Clock Period | 12 | | | ns |
| t_W | Clock Width | 6 | | | ns |
| F_{MAX} | External Feedback $1/(t_S + t_{CO})$ | | | 32.2 | MHz |
| | Internal Feedback $1/(t_{SF} + t_{CF})$ | | | 47.6 | MHz |
| | No Feedback $1/(t_P)$ | | | 83.3 | MHz |
| t_{AW} | Asynchronous Reset Width | 25 | 15 | | ns |
| t_{AR} | Asynchronous Reset Recovery Time | 25 | 15 | | ns |
| t_{AP} | Asynchronous Reset to Registered Output Reset | | 18 | 28 | ns |

Input Test Waveforms and Measurement Levels

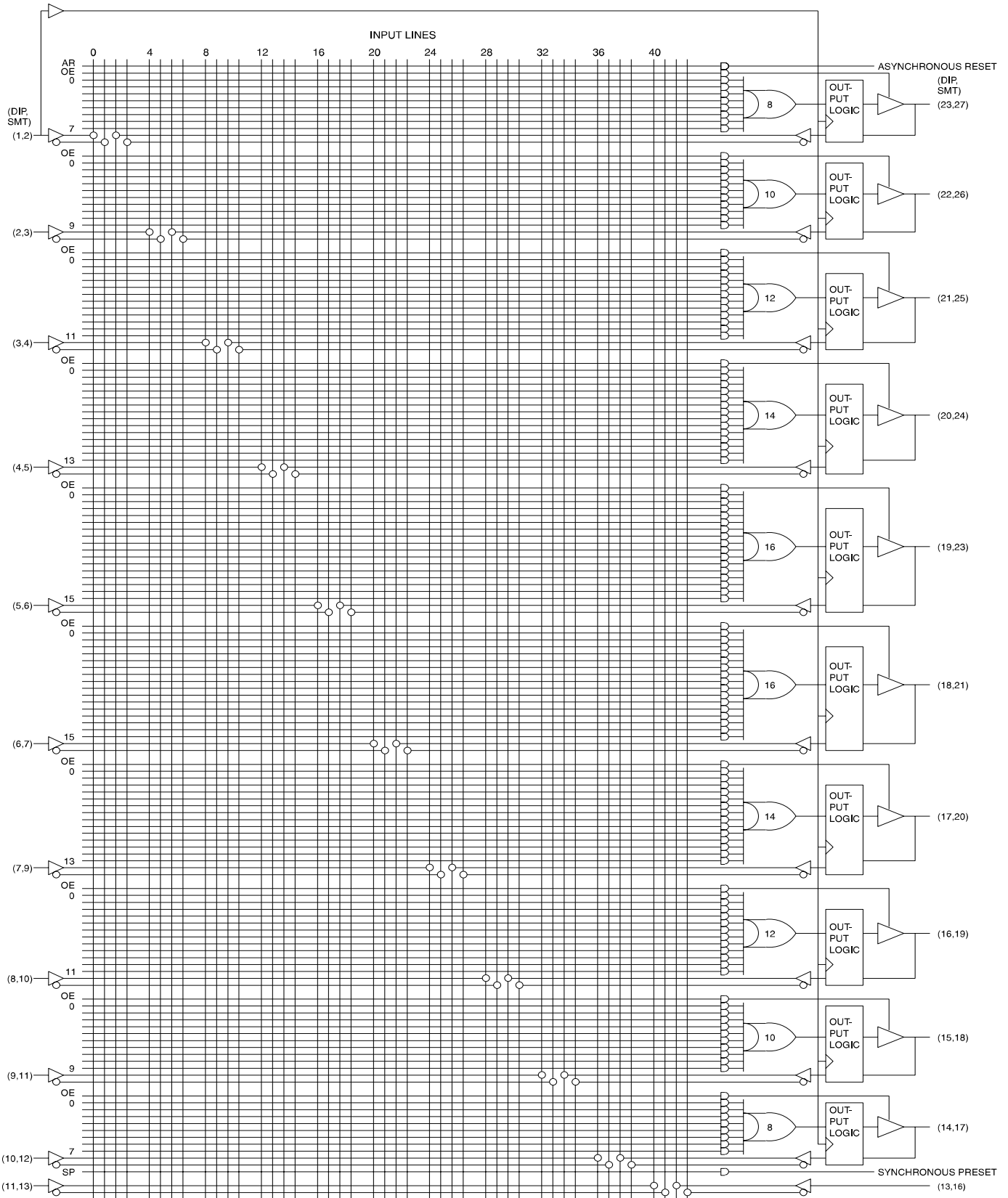


Output Test Loads

Commercial



Functional Logic Diagram AT22LV10(L)

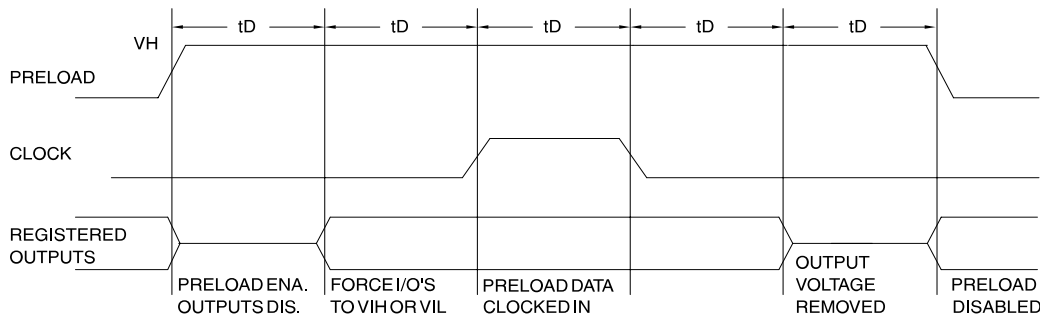


Preload of Registered Outputs

The registers in the AT22LV10 and AT22LV10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The preload state is entered by placing an 11.5V to 13V signal on pin 8 on

DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

| Level Forced on Registered Output Pin During Preload Cycle | Register State After Cycle |
|--|----------------------------|
| V_{IH} | High |
| V_{IL} | Low |

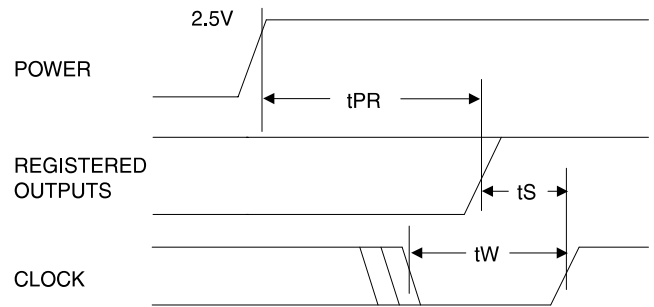


Power-up Reset

The registers in the AT22LV10 and AT22LV10L are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing 2.5V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic;
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3. The clock must remain stable during t_{PR} .



| Parameter | Description | Min | Typ | Max | Units |
|-----------|---------------------|-----|-----|------|-------|
| t_{PR} | Power-up Reset Time | | 600 | 1000 | ns |

Pin Capacitance

($f = 1 \text{ MHz}$, $T = 25^\circ\text{C}$)⁽¹⁾

| | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 5 | 8 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 6 | 8 | pF | $V_{OUT} = 0V$ |

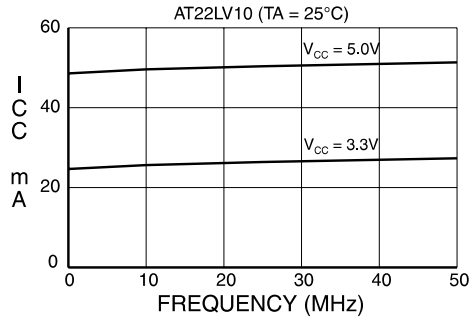
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

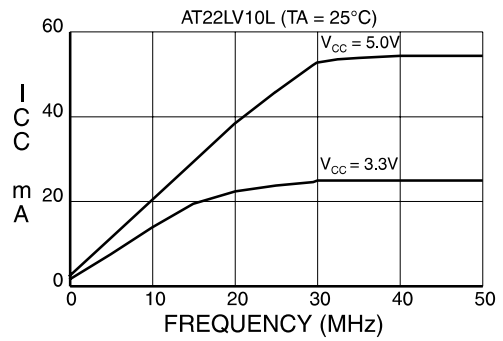
The entire fuse array of an AT22LV10 or AT22LV10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu\text{W}/\text{cm}^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from

the minimum integrated erasure dose of 15 W-sec/cm². To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

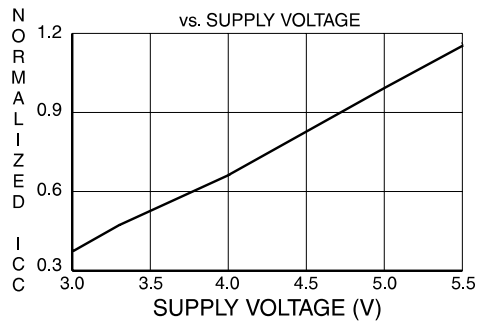
SUPPLY CURRENT vs. INPUT FREQUENCY



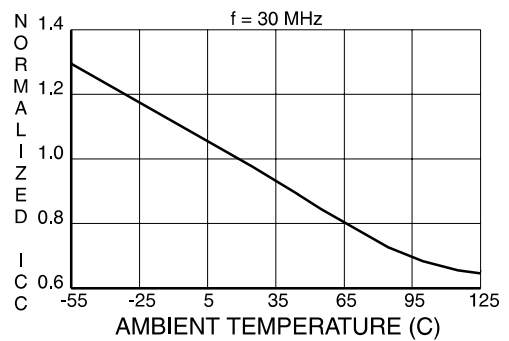
SUPPLY CURRENT vs. INPUT FREQUENCY



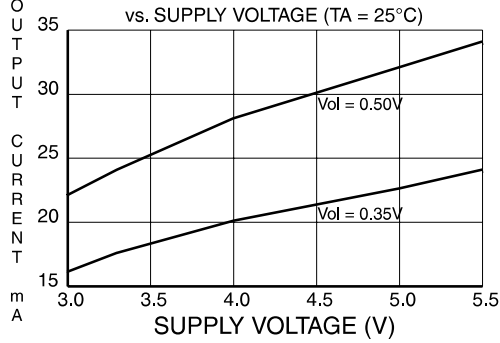
NORMALIZED SUPPLY CURRENT



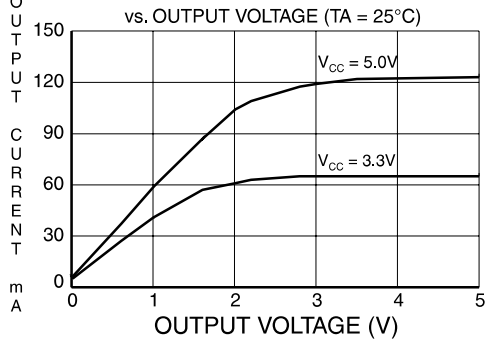
NORMALIZED ICC vs. AMBIENT TEMP.



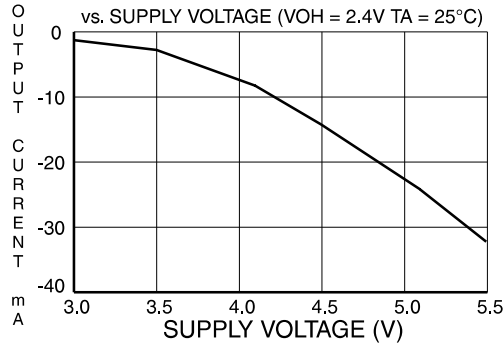
OUTPUT SINK CURRENT



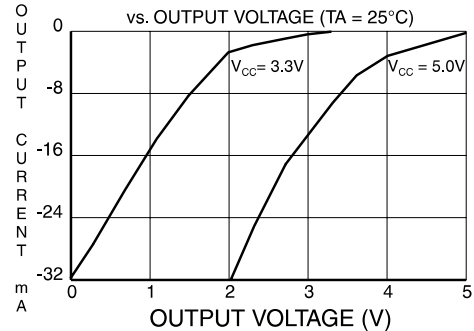
OUTPUT SINK CURRENT

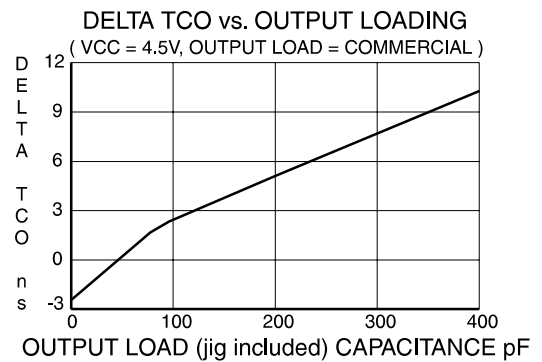
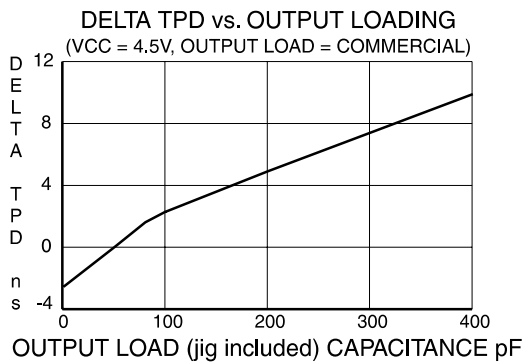
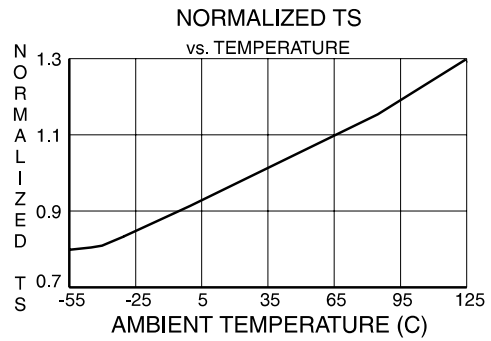
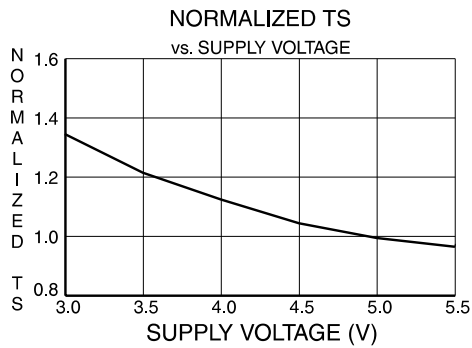
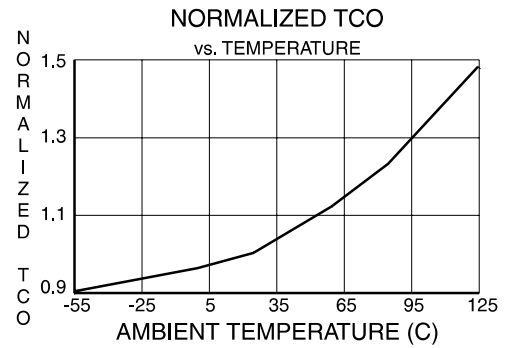
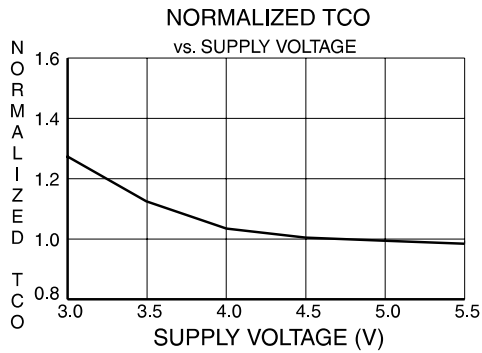
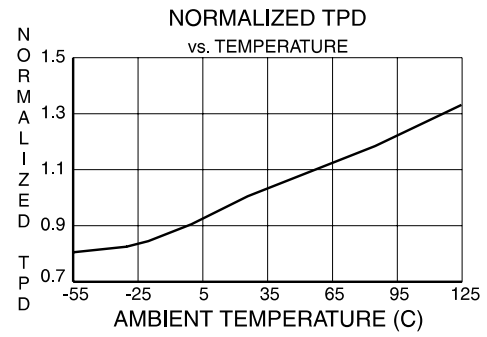
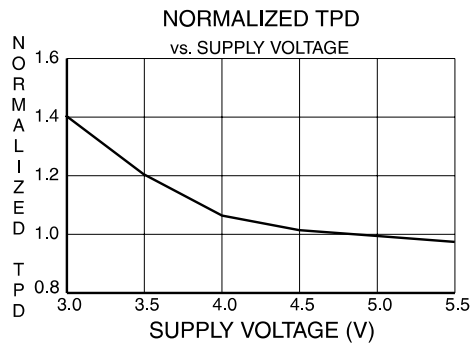


OUTPUT SOURCE CURRENT



OUTPUT SOURCE CURRENT





Ordering Information

| t_{PD} (ns) | t_s (ns) | t_{CO} (ns) | Ordering Code | Package | Operation Range |
|------------------|---------------|------------------|--|--------------------|-------------------------------|
| 20 | 10 | 14 | AT22LV10-20JC AT22LV10-20PC AT22LV10-20SC | 28J 24P3 24S | Commercial (0°C to 70°C) |
| | | | AT22LV10-20JI AT22LV10-20PI AT22LV10-20SI | 28J 24P3 24S | Industrial (-40°C to 85°C) |
| 25 | 12 | 17 | AT22LV10-25JC AT22LV10-25PC AT22LV10-25SC | 28J 24P3 24S | Commercial (0°C to 70°C) |
| | | | AT22LV10-25JI AT22LV10-25PI AT22LV10-25SI | 28J 24P3 24S | Industrial (-40°C to 85°C) |
| 25 | 17 | 14 | AT22LV10L-25JC AT22LV10L-25PC AT22LV10L-25SC | 28J 24P3 24S | Commercial (0°C to 70°C) |
| | | | AT22LV10L-25JI AT22LV10L-25PI AT22LV10L-25SI | 28J 24P3 24S | Industrial (-40°C to 85°C) |

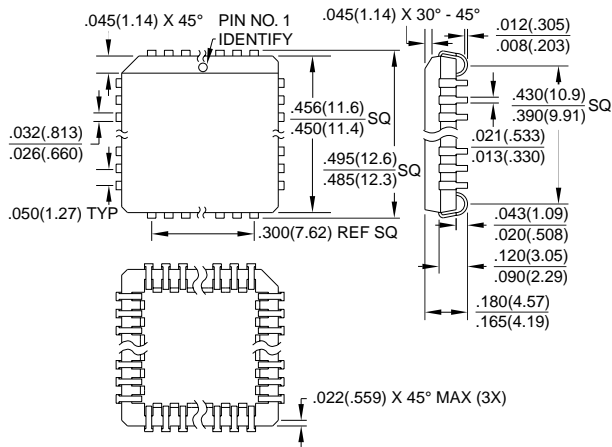
Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

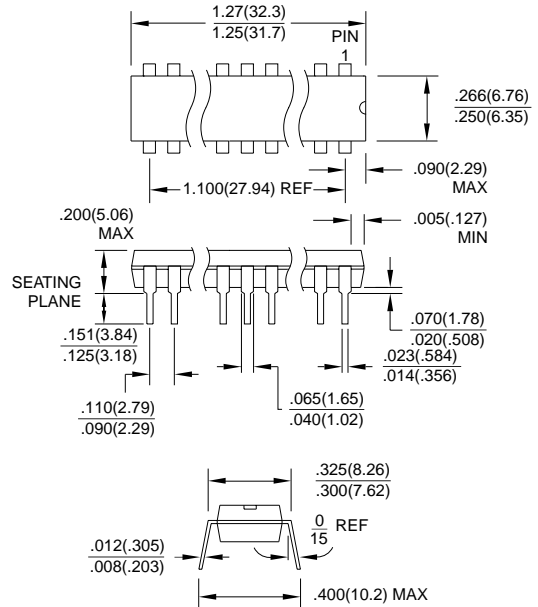
| Package Type | |
|--------------|--|
| 28J | 28-lead, Plastic J-leaded Chip Carrier OTP (PLCC) |
| 24P3 | 24-lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP) |
| 24S | 24-lead, 0.300" Wide, Plastic Gull-Wing Small Outline OTP (SOIC) |

Packaging Information

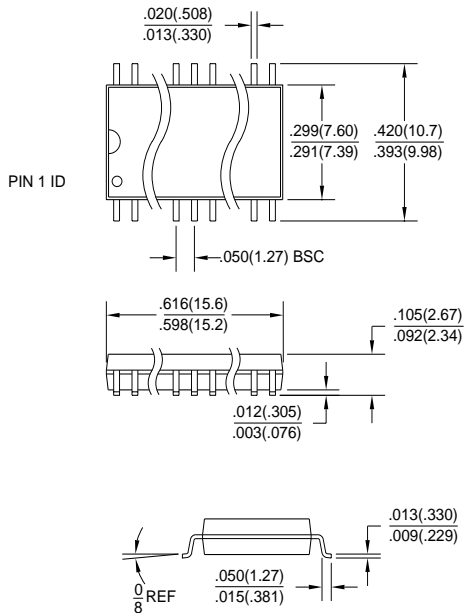
28J, 28-lead, Plastic J-leaded Chip Carrier (PLCC)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-018 AB



24P3, 24-lead, 0.300" Wide. Plastic
 Dual Inline Package (PDIP)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-011 AB



24S, 24-lead, 0.300" Wide, Plastic Gull-Wing Small
 Outline (SOIC)
 Dimensions in Inches and (Millimeters)





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