XS1-G4 512BGA Datasheet

Version 3.5

XMOS

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XS1-G4 Description

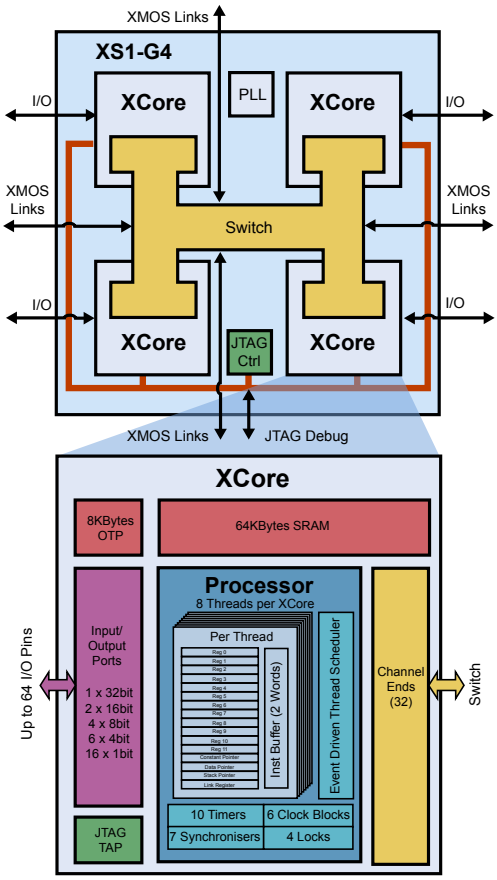
The XS1-G family blends a powerful programmable fabric based on multi-threaded processors with a high-level programming language design flow. XMOS chips are general-purpose programmable devices that can be used in a wide range of applications and systems.

The XS1-G4 device integrates four XCore™ devices. Each XCore contains a 32-bit processor, SRAM memory, I/O ports for communicating with external components and channels for communicating with other devices.

OTP memory is provided for application boot code and security keys, with a secure mode that disables debug and prevents read-back of memory contents.

A high performance switch supports low latency and deterministic communication between the threads in different XCores.

The XMOS architecture is unique in its direct support for concurrent processing (multi-threading), event handling, communication and timed I/O operations.



XS1-G4 Package Features

Four XCores providing 1600MIPS and up to 32 concurrent, deterministic real-time tasks
256 user I/O pins, dynamically configurable as input, output or bi-directional
16 XMOS Links

XCore Resources (per core)

Threads	8
Channel Ends	32
Timers	10
Clock Blocks	6 (includes the reference clock)
Thread Synchronisers	7
Hardware Locks	4
SRAM	64KBytes
OTP Memory	8KBytes

1 Signal Descriptions

This section describes the external signal pins of the XS1-G4 in the 512BGA package.

The following I/O type conventions are used in this document:

I/O Type convention	
I	Input
O	Permanent Output
IO	Bidirectional
OT	Tristatable Output
PU	Pull Up
PD	Pull Down
ST	Schmitt Trigger

1.1 XCore Signals

XCore signals can be used for generic I/O ports or for XMOS Links. All the XCore signals are bidirectional and share the same electrical characteristics:

Signal	I/O	Function	Description
X0D0 : X0D70	IO	XCore 0 I/O	Programmable I/O ports for XCore. See Section 1.2 Port Pin Table
X1D0 : X1D70	IO	XCore 1 I/O	
X2D0 : X2D70	IO	XCore 2 I/O	
X3D0 : X3D70	IO	XCore 3 I/O	

1.1.1 XCore signals as I/O ports

The following table shows the I/O ports available on the four XCore processors. Each port is bidirectional. See Section 1.2 Port Pin Table for details on the signals available for I/O ports in the 512 BGA device.

Signal	I/O	Function	Description
P1A[0] . . . P1P[0]	IO	1-bit port	16 ports per XCore
P4A[3:0] . . . P4F[3:0]	IO	4-bit port	8 ports per XCore
P8A[7:0] . . . P8D[7:0]	IO	8-bit port	4 ports per XCore
P16A[15:0] . . . P16B[15:0]	IO	16-bit port	2 ports per XCore
P32A[31:0]	IO	32-bit port	1 port per XCore

1.1.2 XCore signals as XMOS Links

XMOS Links are full duplex and may operate in either 5wire/direction or 2wire/direction mode. See Section 1.2 Port Pin Table for further information.

5wire fast mode

The following table shows the XMOS link fast interface allocation on each XCore processor:

Signal	Description
XLA[4:0]in XLA[4:0]out	XCore I/O configured as a 5wire link
XLB[4:0]in XLB[4:0]out	XCore I/O configured as a 5wire link
XLC[4:0]in XLC[4:0]out	XCore I/O configured as a 5wire link
XLD[4:0]in XLD[4:0]out	XCore I/O configured as a 5wire link

2wire serial mode

The following table shows the XMOS link serial interface allocation on each XCore processor:

Signal	Description
XLA[1:0]in XLA[1:0]out	XCore I/O configured as a 2wire link
XLB[1:0]in XLB[1:0]out	XCore I/O configured as a 2wire link
XLC[1:0]in XLC[1:0]out	XCore I/O configured as a 2wire link
XLD[1:0]in XLD[1:0]out	XCore I/O configured as a 2wire link

1.1.3 Precedence

Ports and XMOS Links are connected to pins on the XS1-G4 by the program running on the device. The ports and links are multiplexed and follow a defined precedence if they overlap on the same core:

- If an XMOS Link is enabled, the link has access to the pins; the pins of the underlying ports are disabled.
- If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled.

Ports always operate at their specified width, even if they share pins with another port.

1.2 Port Pin Table

	XCORES				XMOS LINKS				PORTS				
Package	Ball Location				A (XCORE1, XCORE3)		B (XCORE0, XCORE2)						
Ball Name	X0	X1	X2	X3	5bit	2bit	5bit	2bit	1b	4b	8b	16b	32b
XnD0	M6	N6	N19	M19					P1A0				
XnD1	M5	N5	N20	M20	XLA4in		XLA4out		P1B0				
XnD2	L6	P6	P19	L19	XLA3in		XLA3out			P4A0	P8A0	P16A0	P32A20
XnD3	L5	P5	P20	L20	XLA2in		XLA2out			P4A1	P8A1	P16A1	P32A21
XnD4	K6	R6	R19	K19	XLA1in	XLA1in	XLA1out	XLA1out		P4B0	P8A2	P16A2	P32A22
XnD5	K5	R5	R20	K20	XLA0in	XLA0in	XLA0out	XLA0out		P4B1	P8A3	P16A3	P32A23
XnD6	J6	T6	T19	J19	XLA0out	XLA0out	XLA0in	XLA0in		P4B2	P8A4	P16A4	P32A24
XnD7	H5	U5	U20	H20	XLA1out	XLA1out	XLA1in	XLA1in		P4B3	P8A5	P16A5	P32A25
XnD8	H6	U6	U19	H19	XLA2out		XLA2in			P4A2	P8A6	P16A6	P32A26
XnD9	G5	V5	V20	G20	XLA3out		XLA3in			P4A3	P8A7	P16A7	P32A27
XnD10	G6	V6	V19	G19	XLA4out		XLA4in		P1C0				
XnD11	F5	W5	W20	F20					P1D0				
XnD12	F7	W7	W18	F18					P1E0				
XnD13	E6	Y6	Y19	E19	XLB4in		XLB4out		P1F0				
XnD14	F8	W8	W17	F17	XLB3in		XLB3out			P4C0	P8B0	P16A8	P32A28
XnD15	E7	Y7	Y18	E18	XLB2in		XLB2out			P4C1	P8B1	P16A9	P32A29
XnD16	F9	W9	W16	F16	XLB1in	XLB1in	XLB1out	XLB1out		P4D0	P8B2	P16A10	
XnD17	E8	Y8	Y17	E17	XLB0in	XLB0in	XLB0out	XLB0out		P4D1	P8B3	P16A11	
XnD18	F10	W10	W15	F15	XLB0out	XLB0out	XLB0in	XLB0in		P4D2	P8B4	P16A12	
XnD19	E10	Y10	Y15	E15	XLB1out	XLB1out	XLB1in	XLB1in		P4D3	P8B5	P16A13	
XnD20	F11	W11	W14	F14	XLB2out		XLB2in			P4C2	P8B6	P16A14	P32A30
XnD21	E11	Y11	Y14	E14	XLB3out		XLB3in			P4C3	P8B7	P16A15	P32A31
XnD22	F12	W12	W13	F13	XLB4out		XLB4in		P1G0				
XnD23	E12	Y12	Y13	E13					P1H0				
XnD24	L4	P4	P21	L21					P1I0				
XnD25	K3	R3	R22	K22					P1J0				
XnD26	K4	R4	R21	K21						P4E0	P8C0	P16B0	
XnD27	J3	T3	T22	J22						P4E1	P8C1	P16B1	
XnD28	J4	T4	T21	J21						P4F0	P8C2	P16B2	
XnD29	H3	U3	U22	H22						P4F1	P8C3	P16B3	
XnD30	G4	V4	V21	G21						P4F2	P8C4	P16B4	
XnD31	F3	W3	W22	F22						P4F3	P8C5	P16B5	
XnD32	F4	W4	W21	F21						P4E2	P8C6	P16B6	
XnD33	E3	Y3	Y22	E22						P4E3	P8C7	P16B7	
XnD34	E4	Y4	Y21	E21					P1K0				
XnD35	D3	AA3	AA22	D22					P1L0				
XnD36	D5	AA5	AA20	D20					P1M0		P8D0	P16B8	
XnD37	C4	AB4	AB21	C21					P1N0		P8D1	P16B9	
XnD38	D6	AA6	AA19	D19					P1O0		P8D2	P16B10	
XnD39	C5	AB5	AB20	C20					P1P0		P8D3	P16B11	
XnD40	D7	AA7	AA18	D18							P8D4	P16B12	
XnD41	C6	AB6	AB19	C19							P8D5	P16B13	
XnD42	D9	AA9	AA16	D16							P8D6	P16B14	
XnD43	C8	AB8	AB17	C17							P8D7	P16B15	
XnD49	J1	T1	T24	J24	XLC4in		XLC4out						P32A0
XnD50	H2	U2	U23	H23	XLC3in		XLC3out						P32A1
XnD51	H1	U1	U24	H24	XLC2in		XLC2out						P32A2
XnD52	G2	V2	V23	G23	XLC1in	XLC1in	XLC1out	XLC1out					P32A3
XnD53	G1	V1	V24	G24	XLC0in	XLC0in	XLC0out	XLC0out					P32A4
XnD54	E2	Y2	Y23	E23	XLC0out	XLC0out	XLC0in	XLC0in					P32A5
XnD55	E1	Y1	Y24	E24	XLC1out	XLC1out	XLC1in	XLC1in					P32A6
XnD56	D2	AA2	AA23	D23	XLC2out		XLC2in						P32A7
XnD57	D1	AA1	AA24	D24	XLC3out		XLC3in						P32A8
XnD58	C2	AB2	AB23	C23	XLC4out		XLC4in						P32A9
XnD61	A3	AD3	AD22	A22	XLD4in		XLD4out						P32A10
XnD62	B4	AC4	AC21	B21	XLD3in		XLD3out						P32A11
XnD63	A4	AD4	AD21	A21	XLD2in		XLD2out						P32A12
XnD64	B5	AC5	AC20	B20	XLD1in	XLD1in	XLD1out	XLD1out					P32A13
XnD65	A5	AD5	AD20	A20	XLD0in	XLD0in	XLD0out	XLD0out					P32A14
XnD66	B7	AC7	AC18	B18	XLD0out	XLD0out	XLD0in	XLD0in					P32A15
XnD67	A7	AD7	AD18	A18	XLD1out	XLD1out	XLD1in	XLD1in					P32A16
XnD68	B8	AC8	AC17	B17	XLD2out		XLD2in						P32A17
XnD69	A8	AD8	AD17	A17	XLD3out		XLD3in						P32A18
XnD70	B9	AC9	AC16	B16	XLD4out		XLD4in						P32A19

1.3 System Service Pin Table

Signal	Ball ID
SS_BYPASS_PLL_LOCK	G9
SS_CLK	H7
SS_DEBUG	M18
SS_EXT_OSC_CONFIG	M7
SS_EXT_OSC_HS_MODE	N7
SS_PLL_BYPASS	G8
SS_RESET	G12
SS_TCK	U18

Signal	Ball ID
SS_TDI	V16
SS_TDO	V13
SS_TEST_ENA	T18
SS_TMS	V12
SS_TRST	V17
SS_XC0_BS0	H18
SS_XC0_BS1	J18
SS_XC0_BS2	N23

Signal	Ball ID
SS_XC0_BS3	P23
SS_XC0_CFG0	L23
SS_XC0_CFG1	M23
SS_XC1_BS0	L24
SS_XC1_BS1	M24
SS_XC1_BS2	N24
SS_XC1_BS3	P24

1.4 Core Power and Ground Pin Table

Signal	Ball ID
VDD	G10
VDD	G11
VDD	G14
VDD	G15
VDD	G16
VDD	K7
VDD	K18
VDD	L7
VDD	L18
VDD	P7
VDD	P18
VDD	R7
VDD	R18
VDD	V10
VDD	V11
VDD	V14
VDD	V15

Signal	Ball ID
VSS	K10
VSS	K11
VSS	K12
VSS	K13
VSS	K14
VSS	K15
VSS	L10
VSS	L11
VSS	L12
VSS	L13
VSS	L14
VSS	L15
VSS	M10
VSS	M11
VSS	M12
VSS	M13
VSS	M14
VSS	M15

Signal	Ball ID
VSS	N10
VSS	N11
VSS	N12
VSS	N13
VSS	N14
VSS	N15
VSS	P10
VSS	P11
VSS	P12
VSS	P13
VSS	P14
VSS	P15
VSS	R10
VSS	R11
VSS	R12
VSS	R13
VSS	R14
VSS	R15

1.5 XCore I/O Power Table

Signal	Ball ID
IO VDD	A1
IO VDD	A2
IO VSS	A6
IO VDD	A10
IO VSS	A15
IO VDD	A19
IO VSS	A23
IO VSS	A24
IO VDD	B1
IO VDD	B2
IO VSS	B6
IO VDD	B10
IO VSS	B15
IO VDD	B19
IO VSS	B23
IO VSS	B24
IO VDD	C3
IO VSS	C7
IO VDD	C11
IO VSS	C14
IO VDD	C18
IO VSS	C22
IO VDD	D4
IO VSS	D8
IO VDD	D17
IO VSS	D21
IO VDD	E5
IO VSS	E9
IO VDD	E16
IO VSS	E20
IO VSS	F1
IO VSS	F2
IO VDD	F6

Signal	Ball ID
IO VSS	F19
IO VDD	F23
IO VDD	F24
IO VSS	G3
IO VDD	G7
IO VSS	G18
IO VDD	G22
IO VSS	H4
IO VDD	H21
IO VSS	J5
IO VDD	J20
IO VDD	K1
IO VDD	K2
IO VSS	K23
IO VSS	K24
IO VDD	L3
IO VSS	P3
IO VSS	R1
IO VSS	R2
IO VDD	R23
IO VDD	R24
IO VDD	T5
IO VSS	T20
IO VDD	U4
IO VSS	U21
IO VDD	V3
IO VSS	V7
IO VDD	V18
IO VSS	V22
IO VDD	W1
IO VDD	W2
IO VSS	W6
IO VDD	W19

Signal	Ball ID
IO VSS	W23
IO VSS	W24
IO VSS	Y5
IO VDD	Y9
IO VSS	Y16
IO VDD	Y20
IO VSS	AA4
IO VDD	AA8
IO VSS	AA17
IO VDD	AA21
IO VSS	AB3
IO VDD	AB7
IO VSS	AB11
IO VDD	AB14
IO VSS	AB18
IO VDD	AB22
IO VSS	AC1
IO VSS	AC2
IO VDD	AC6
IO VSS	AC10
IO VDD	AC15
IO VSS	AC19
IO VDD	AC23
IO VDD	AC24
IO VSS	AD1
IO VSS	AD2
IO VDD	AD6
IO VSS	AD10
IO VDD	AD15
IO VSS	AD19
IO VDD	AD23
IO VDD	AD24

1.6 XMOS Link Pin Table

See Section 1.2 Port Pin Table

2 System Services

System Services are required to support correct device behavior. These signals control clocking, reset and boot behavior of the device.

2.1 Clock control signals

These signals control the PLL of the XS1-G4

Signal	Ball ID	I/O	Function	Description
SS_EXT_OSC_CONFIG	M7	I, PD	Control	PLL input oscillator configuration mode
SS_EXT_OSC_HS_MODE	N7	I, PD	Control	PLL input oscillator high speed mode
SS_PLL_BYPASS	G8	I, PD	Control	Bypasses the PLL, using SS_CLK directly
SS_BYPASS_PLL_LOCK	G9	I, PD	Control	Reserved, connect to ground
SS_PLL_AVDD		pwr		Analog power supply to the PLL
SS_PLL_AGND		pwr		AGND power supply for the PLL
SS_CLK	H7	I, PD, ST	Clock	System clock

Functional description

SS_EXT_OSC_CONFIG The on-chip PLL derives the system clock for the device by multiplication of the input reference on SS_CLK. By default this ratio is set to multiply by 20, giving an internal operating frequency of 400MHz. Achieving a very specific core frequency requires a different reference frequency on SS_CLK. If the SS_CLK frequency is not 20 MHz, this pin should be tied to VDD. See the XS1-G Clock Frequency Control Application Note for further information.

SS_EXT_OSC_HS_MODE When SS_EXT_OSC_CONFIG is set high, this pin must be driven low if the SS_CLK reference frequency is below 50MHz or driven high if the reference frequency is above 50 MHz. This configuration is used to configure the PLL such that the device boots up at a frequency that is not in excess of 400MHz. See the XS1-G Clock Frequency Control Application Note for further information.

SS_PLL_BYPASS When pin is set high, SS_CLK is used as the system clock. Set to IO_VDD.

SS_BYPASS_PLL_LOCK Reserved, connect to ground.

SS_PLL_AVDD The on-chip PLL requires a very clean AVDD power supply. It is recommended that this supply node be separated from the other, noisier, supplies in the board. The supply should be decoupled close to the respective IC power pins. Nominally 1.0V.

SS_PLL_AGND Analogue ground for the PLL. Connect directly to board ground.

SS_CLK Reference clock signal for the on-chip PLL. A default frequency of 20MHz is typically used by XS1 family devices. However other frequencies can be derived from SS_CLK using the SS_EXT_OSC_CONFIG and SS_EXT_OSC_HS_MODE pins. Clock frequencies of ≤20 MHz and ≥25 MHz are supported.

2.2 Miscellaneous control signals

Signal	Ball ID	I/O	Function	Description
SS_XC0_BS[3:0]	P23, N23, J18, H18	IO, PU	Boot status XCore0	See Boot status pins below
SS_XC1_BS[3:0]	P24, N24,M24, L24	IO, PU	Boot Status XCore1	See Boot status pins below
SS_DEBUG	M18	IO, PU, ST	Debug	Activates multicore debug
SS_RESET	G12	I, PD, ST	Reset	Asynchronous system reset
SS_XC0_CFG[1:0]	M23, L23	I, PD		Reserved, tie to IO_VDD
SS_TEST_ENA	T18	I, PD		Reserved, tie pin to ground
SS_RESERVED				Reserved, leave unconnected

Functional description

SS_XC0_BS[3:0], SS_XC1_BS[3:0] Boot status pins.

The boot status pins are dual function.

Prior to reset, bits 1:0 function as inputs prior to the de-assertion of reset. The XS1-G4 latches the value driven on these two pins on the rising edge (de-assertion) of SS_RESET. The value driven should be static and configured using pullup or pulldown resistors, as the XS1-G4 drives the boot status on these pins after reset. The value configured on these two pins defines the boot mode for XCore 0 as follows:

Value	Description
00	Reserved
01	Reserved
10	Boot from SPI
11	Boot from JTAG

NOTE: If secure boot from OTP is enabled by programming the OTP, the boot mode indicated on the XC0_BS[1:0] and XC1_BS[1:0] pins is ignored.

After reset is complete, bits 2:0 become outputs and indicate the XCore0 or XCore1 boot mode. Bit 3 indicates boot has completed. Codes for bits 2:0 are:

Value	Description
001	Boot from OTP
010	Reserved
011	Reserved
100	Boot from SPI
101	Boot from JTAG

For further details on booting XCores see the XS1-G System Specification document (http://xmos.com/published/xsystem).

SS_DEBUG This pin is used to synchronize the debugging of multiple G4 devices. This pin can operate in both output and input mode. In output mode and when configured to do so, SS_DEBUG is driven low by the device when one or more internal XCore processors hit a debug break point. Prior to this point the pin is tri-stated. In input mode and when configured to do so, driving this pin low puts all internal CPUs into debug mode. Software can set the behavior of each internal XCore based on this pin. This pin should have an external pull up to IO_VDD(3.3V) of 4K7 ohms.

SS_RESET Active low asynchronous-assertion reset signal. At power-up, this pin must be activated for at least 5us after the power supplies are stable to ensure reliable boot up. Following a reset the PLL re-establishes lock after which the XCores boot up according to the BOOT_MODE (see SS_XC0_BS1, SS_XC0_BS0).

SS_XC0_CFG0 Reserved, tie pin to IO_VDD

SS_TEST_ENA Reserved, tie pin to ground.

SS_RESERVED Reserved, leave unconnected.

2.3 JTAG Operation

The XS1-G family supports a generic 5pin JTAG interface, which can be used to provide hardware testing including:

- Boundary scan testing for correct board connectivity
- Onboard source level debugging from remote terminals
- Boundary scanning for OTP ROM

The JTAG connectors on the XCore are:

Signal	Pin ID	I/O	Function	Description
SS_TCK	U18	I, PU, ST	TCK	Test clock
SS_TMS	V12	I, PU	TMS	Test mode select
SS_TRST	V17	I, PU, ST	TRST	Test reset (optional)
SS_TDI	V16	I, PU	TDI	Test data in
SS_TDO	V13	OT, PU	TDO	Test data out

Each XCore and Switch has a JTAG controller with a 10-bit instruction register (IR) and a 32-bit data register (DR). A mux controller selects the XCore the TMS is routed to, and which device TDO is wired to the chip level output. TDO can output in tristate in accordance with the JTAG specification. The JTAG controller supports the following commands:

Symbol	Function	Description
1111111111	BYPASS	See IEEE 1149.1 documentation
0000000100	SAMPLE	
0000001000	PRELOAD	
0000001100	EXTEST	
aaaaaaaa01	PEEK	Copies shared register contents, into data register (a=address register bits)
aaaaaaaa10	POKE	Copies data register contents into shared register (a=address register bits)

The JTAG controller has access to the following registers for an XCore:

Register	Number	JTAG Perm	Description
DEVICE_ID0	0x00	RO	XCore ID register
DEVICE_ID1	0x01	RO	XCore ID register
DEVICE_ID2	0x02	RO	XCore ID register
DEVICE_ID3	0x03	RO	XCore ID register
DBG_CTRL	0x04	RW	Control internal switch permissions to debug register
DBG_INT	0x05	RW	Trigger debug interrupts
PLL_CLK_DIVIDER	0x06	RO	PLL clock divider register
SECURITY_CONFIG	0x07	RO	OTP security configuration register
PLINK[3:0]	0x10 : 0x13	RO	Internal link status
DBG_SCRATCH[7:0]	0x20 : 0x27	RW	Scratch register for debug software protocols
T[7:0]_PC	0x40 : 0x47	RO	Copy of PC
T[7:0]_SR	0x60 : 0x67	RO	Copy of SR

The JTAG controller can read from the DBG_SCRATCH registers at the same time as the XCore, but if both devices write at the same time, the XCore write completes and the JTAG controller is ignored.

The TRST_N pin must be driven low for at least 100ns at power up to reset the JTAG port. If JTAG debug is not required, the TRST_N pin can be tied low with a 1k resistor to hold the JTAG port in reset.

3 DC and Switching Characteristics

3.1 Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
IO_VDD	I/O DC supply voltage	3.0	3.3	3.6	V	1
VDD	Core DC supply voltage	0.95	1.0	1.05	V	2
SS_PLL_AVDD	PLL analogue supply	0.95	1.0	1.05	V	
SS_PLL_DVDD	PLL Digital DC Supply	0.95	1.0	1.05	V	
SS_OTP_VPP	OTP external programming voltage	6.18	6.5	6.83	V	3
Cl	XCore I/O load capacitance			25	pF	
Ta	Operating temperature range (Commercial)	0		70	Degrees C	
	Operating temperature range (Industrial)	-40		85	Degrees C	
Tj	Junction temperature			125	Degrees C	
Tstg	Storage temperature	-65		150	Degrees C	

Notes:

1. Voltages with respect to IO VSS
2. Voltages with respect to VSS
3. Program only

3.2 DC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(IH)	Signal pin input high voltage	2.0		5.5	V	1,2,3
V(IL)	Signal pin input low voltage	-0.3		0.8	V	1,2,3
V(OH)	Signal pin output high voltage	2.4			V	1,2,3
V(OL)	Signal pin output low voltage			0.4	V	1,2,3
I(OL)	Signal pin low level output current		4		mA	1,3
I(OH)	Signal pin high level output current		4		mA	1,3
R(PU)	Signal pin pull-up resistance			100k	Ohms	1,4

Notes:

1. Signal pin may be any pin except power supply pins

2. Voltages with respect to IO VSS
3. Internal pull-up resistors are fitted to general purpose XCore I/O pins. Applies to both XCore I/O and XCore link I/Os.
4. Use for unused I/O only—the internal pull up resistor is not recommended as a substitute for an external pull-up resistor.

3.3 ESD Stress Voltage

ESD Model	ESD Stress Voltage	Notes
HBM	± 2.0 KV	
MM	± 200 V	

3.4 Reset Timing

Parameters	MIN	TYP	MAX	UNITS	Notes
Reset pulse width for correct start-up	100			ns	
PLL Lock			1	ms	
ISA (BOOT)			< 100	μs	

User code must wait for the device to reset, the PLL to be locked and system code to be started, before it can be run.

3.5 Power Supply

Power is applied to the device through the IO_VDD and VDD balls. Several balls of each type are provided to minimize the effect of inductance within the package. All supply pins must be connected. Each supply should be decoupled close to the chip by several 100nF low inductance (for example, ceramic) capacitors between IO_VDD and GND, and VDD and GND.

Input voltages must not exceed specification with respect to IO_VDD, VDD and GND, even during power up and power down ramping. Permanent damage can occur if the operation exceeds these ranges.

3.5.1 Power Supply Sequencing

To ensure correct device operation, the VDDIO and OTP_VDDIO supplies should be present before the VDD supply. Specifically, the VDDIO and OTP_VDDIO supplies should rise to their nominal operating range with VDD held at 0V. The VDD supply should then rise to its nominal operating range with a rise time of less than 10ms.

Quiescent Current

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
I(DDCQ)	Quiescent VDD(core) Current		120		mA	
I(PLLQ)	Quiescent PLL Total Current		4		mA	

Power consumption

The power consumption of the XS1-G4 is highly application dependant. The following figures should be used for budgetary purposes only:

Commercial Qualification						
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
PD	Power dissipation		1.6		Watts	1,2,3

Industrial Qualification						
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
PD	Power dissipation		1.6		Watts	1,2,3

Notes:

1. Assumes typical core and I/O voltages, operating at 400MHz with nominal activity on all cores.
2. P(TYP) value is the usage power consumption under typical operating conditions.
3. P(TYP) value includes quiescent current.

For further details on power consumption for XS1-G devices see the Estimating Power Consumption For XS1-G Devices Application Note

3.6 Clock

XS1-G devices use an input clock frequency, supplied by the user on the SS_CLK pin, to drive the PLL and obtain the system clock. The nominal frequency of the clock for all XS1 family components is 20MHz but other clock frequencies can be derived from SS_CLK using the MODE pins and internal PLL. For further details on setting the clock frequency see the XS1-G Clock Frequency Control Application Note.

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
	Frequency	12.5	20	100	MHz	1
	Slew rate	1		2	ns	
	Frequency jitter					

Notes:

1. Clock frequencies between 20 and 25 MHz are not supported.

A set of system clock dividers are applied to the system clock frequency allowing specific clock frequencies to be derived for each XCore, the switch and the reference clock.

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
	System Clock Frequency			400	MHz	

Clock edges must be monotonic and remain within the specified voltage and time limits.

3.7 Memory

3.7.1 Internal static memory

The XS1-G4 has a total of 256K bytes of fast internal static memory for high rates of data throughput, divided into 64k bytes per XCore. Each internal memory access consumes one core clock cycle. There is no dedicated external memory interface, although memory can be expanded through appropriate use of the ports.

3.7.2 Internal one-time programmable memory

Each XCore has 64K bits of one-time programmable memory that can be programmed using the JTAG interface.

3.7.3 OTP voltage ramp requirement

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(PP)	OTP VPP Programming Voltage Ramp Rate			1	V/μs	

The OTP may be programmed using its internal charge pump or by supplying a 6.5V VPP programming voltage on the OTP_VPP pin. Unless a programming cycle is underway the OTP_VPP pins should be left undriven.

For further information on security and OTP programming, see the relevant application note.

3.8 Port Timing

Ports timing is explained in a separate application note. Please see http://xmos.com/documentation for more details.

3.8.1 XCore I/O AC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(XOINVALID)	XCore I/O Minimum Output Data Invalid window which can be achieved using Port/ClkBlk combination	9			ns	
T(XOVALID)	XCore I/O Minimum Input Data Valid window to allow safe acquisition of data using Port/ClkBlk combination	8			ns	
T(XIFMAX)	Maximum XCore I/O toggle frequency which can be safely acquired and used as a clock source using a ClkBlk			60	MHz	

The Input Valid window parameter relates to the capability of the XS1-G4 family devices to capture data input to the chip with respect to an external clock source. This parameter can be calculated as the sum of the input setup time and input hold time with regard to the external clock as measured at the G4 device pins. The output invalid window specifies the time for which an output will be invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the G4 provides functionality to delay the incoming clock with respect to the incoming data. For further details on these parameters and on interfacing to higher speed synchronous interfaces see the relevant application note.

3.9 XMOS Link Interface Performance

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
B(2blink_5)	2wire link bandwidth (Nominal load)			160	Mb/s	
B(5blink_5)	5wire link bandwidth (Nominal load)			400	Mb/s	

The asynchronous nature of links means that the relative phasing of SS_CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

3.10 JTAG Timing

The JTAG interface may be operated in either synchronous or asynchronous mode.

Parameters	MIN	TYP	MAX	UNITS	Notes
SS_TCLK period	30			ns	
TSU	5			ns	1
TH			10	ns	1
TCO			15	ns	2

Notes:

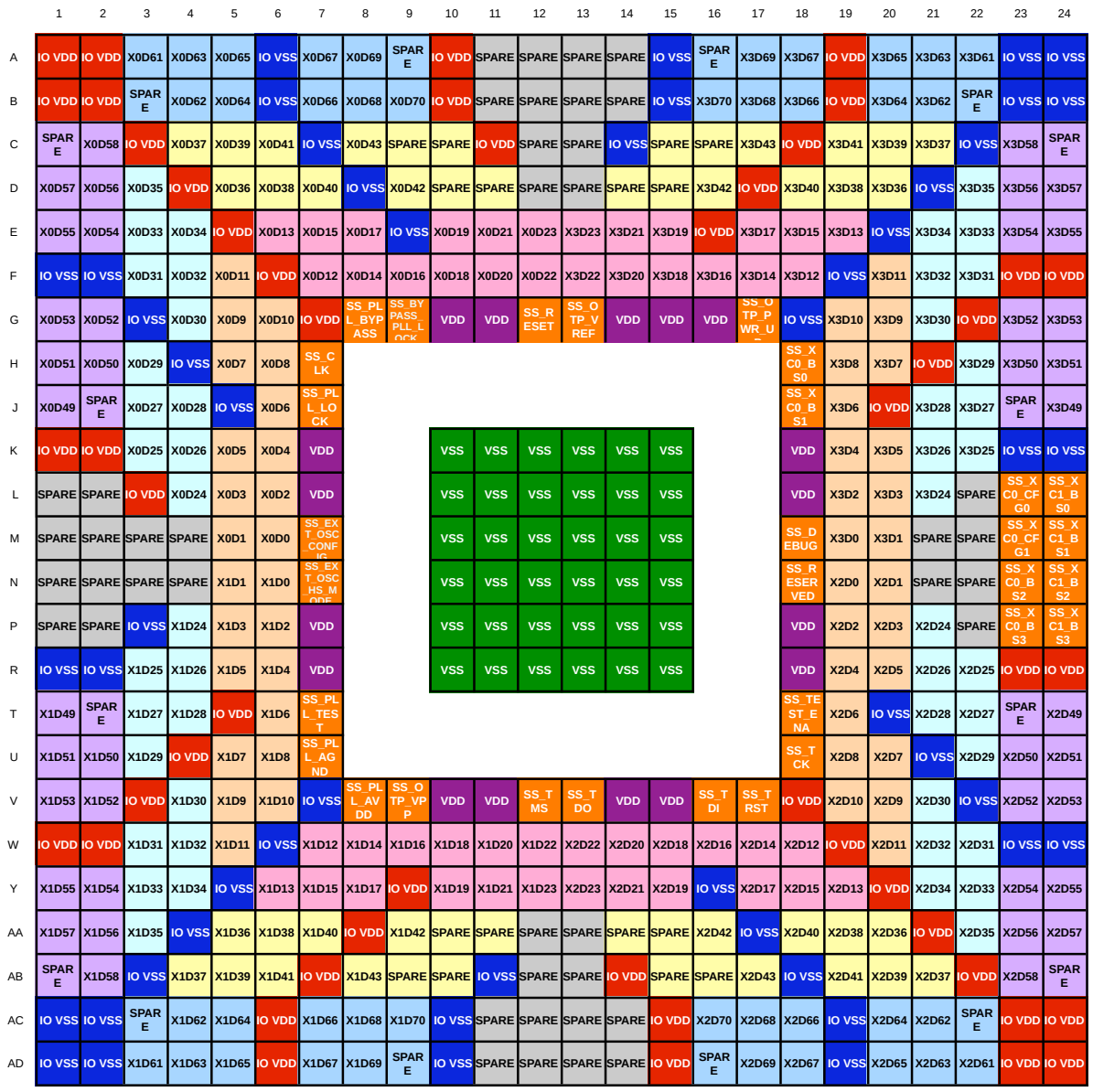
1. Timing applies to SS_TMS, SS_TRST, SS_TDI inputs
2. Timing applies to SS_TDO output

4 Package Details

4.1 Package Pin Layout

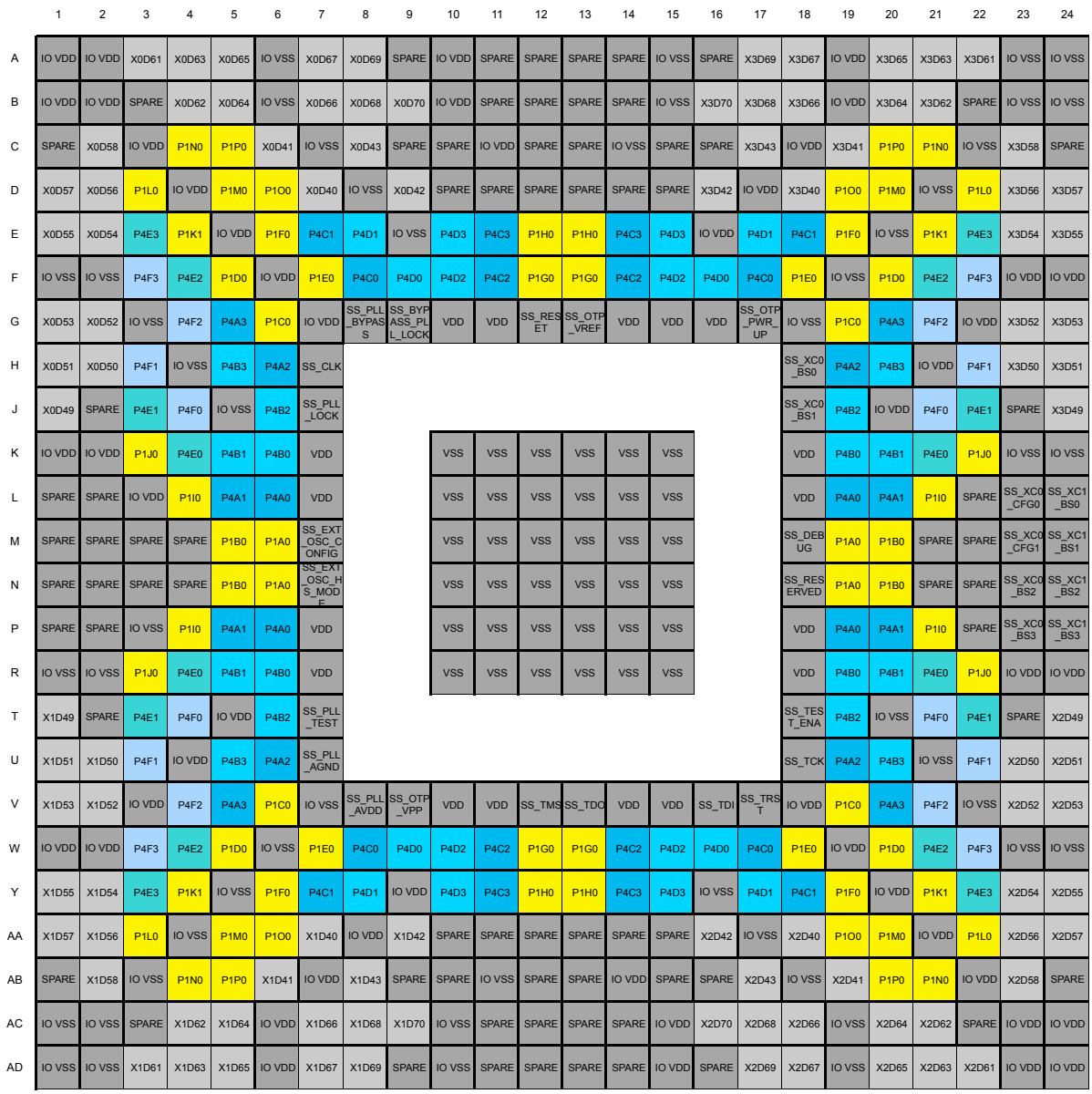
The following diagrams show the ball name and location for the BGA512 Package. The pin layout is designed to allow each XCore port configuration to use the same socket—the footprint for each set of port widths is shown on the following pages.

Pin layout



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	IO VDD	IO VDD	X0D61	X0D63	X0D65	IO VSS	X0D67	X0D69	SPARE	IO VDD	SPARE	SPARE	SPARE	SPARE	IO VSS	SPARE	X3D69	X3D67	IO VDD	X3D65	X3D63	X3D61	IO VSS	IO VSS
B	IO VDD	IO VDD	SPARE	X0D62	X0D64	IO VSS	X0D66	X0D68	X0D70	IO VDD	SPARE	SPARE	SPARE	SPARE	IO VSS	X3D70	X3D68	X3D66	IO VDD	X3D64	X3D62	SPARE	IO VSS	IO VSS
C	SPARE	X0D58	IO VDD	X0D37	X0D39	X0D41	IO VSS	X0D43	SPARE	SPARE	IO VDD	SPARE	SPARE	IO VSS	SPARE	SPARE	X3D43	IO VDD	X3D41	X3D39	X3D37	IO VSS	X3D58	SPARE
D	X0D57	X0D56	X0D35	IO VDD	X0D36	X0D38	X0D40	IO VSS	X0D42	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	X3D42	IO VDD	X3D40	X3D38	X3D36	IO VSS	X3D35	X3D56	X3D57
E	X0D55	X0D54	X0D33	X0D34	IO VDD	X0D13	X0D15	X0D17	IO VSS	X0D19	X0D21	X0D23	X3D23	X3D21	X3D19	IO VDD	X3D17	X3D15	X3D13	IO VSS	X3D34	X3D33	X3D54	X3D55
F	IO VSS	IO VSS	X0D31	X0D32	X0D11	IO VDD	X0D12	X0D14	X0D16	X0D18	X0D20	X0D22	X3D22	X3D20	X3D18	X3D16	X3D14	X3D12	IO VSS	X3D11	X3D32	X3D31	IO VDD	IO VDD
G	X0D53	X0D52	IO VSS	X0D30	X0D9	X0D10	IO VDD	SS_PLL_BYPASS	SS_BYPASS_PLL_LOCK	VDD	VDD	SS_RESET	SS_OTP_VREF	VDD	VDD	VDD	SS_OTP_PWR_U	IO VSS	X3D10	X3D9	X3D30	IO VDD	X3D52	X3D53
H	X0D51	X0D50	X0D29	IO VSS	X0D7	X0D8	SS_CLK											SS_XC0_BS0	X3D8	X3D7	IO VDD	X3D29	X3D50	X3D51
J	X0D49	SPARE	X0D27	X0D28	IO VSS	X0D6	SS_PLL_LOCK											SS_XC0_BS1	X3D6	IO VDD	X3D28	X3D27	SPARE	X3D49
K	IO VDD	IO VDD	X0D25	X0D26	X0D5	X0D4	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	X3D4	X3D5	X3D26	X3D25	IO VSS	IO VSS
L	SPARE	SPARE	IO VDD	X0D24	X0D3	X0D2	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	X3D2	X3D3	X3D24	SPARE	SS_XC0_CFG0	SS_XC1_BS0
M	SPARE	SPARE	SPARE	SPARE	X0D1	X0D0	SS_EXT_OSC_CONFIG			VSS	VSS	VSS	VSS	VSS	VSS			SS_DEBUG	X3D0	X3D1	SPARE	SPARE	SS_XC0_CFG1	SS_XC1_BS1
N	SPARE	SPARE	SPARE	SPARE	X1D1	X1D0	SS_EXT_OSC_HS_MODE			VSS	VSS	VSS	VSS	VSS	VSS			SS_RESERVED	X2D0	X2D1	SPARE	SPARE	SS_XC0_BS2	SS_XC1_BS2
P	SPARE	SPARE	IO VSS	X1D24	X1D3	X1D2	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	X2D2	X2D3	X2D24	SPARE	SS_XC0_BS3	SS_XC1_BS3
R	IO VSS	IO VSS	X1D25	X1D26	X1D5	X1D4	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	X2D4	X2D5	X2D26	X2D25	IO VDD	IO VDD
T	X1D49	SPARE	X1D27	X1D28	IO VDD	X1D6	SS_PLL_TEST											SS_TEST_ENA	X2D6	IO VSS	X2D28	X2D27	SPARE	X2D49
U	X1D51	X1D50	X1D29	IO VDD	X1D7	X1D8	SS_PLL_AGND											SS_TCK	X2D8	X2D7	IO VSS	X2D29	X2D50	X2D51
V	X1D53	X1D52	IO VDD	X1D30	X1D9	X1D10	IO VSS	SS_PLL_AVDD	SS_OTP_VPP	VDD	VDD	SS_TMS	SS_TDO	VDD	VDD	SS_TDI	SS_TRST	IO VDD	X2D10	X2D9	X2D30	IO VSS	X2D52	X2D53
W	IO VDD	IO VDD	X1D31	X1D32	X1D11	IO VSS	X1D12	X1D14	X1D16	X1D18	X1D20	X1D22	X2D22	X2D20	X2D18	X2D16	X2D14	X2D12	IO VDD	X2D11	X2D32	X2D31	IO VSS	IO VSS
Y	X1D55	X1D54	X1D33	X1D34	IO VSS	X1D13	X1D15	X1D17	IO VDD	X1D19	X1D21	X1D23	X2D23	X2D21	X2D19	IO VSS	X2D17	X2D15	X2D13	IO VDD	X2D34	X2D33	X2D54	X2D55
AA	X1D57	X1D56	X1D35	IO VSS	X1D36	X1D38	X1D40	IO VDD	X1D42	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	X2D42	IO VSS	X2D40	X2D38	X2D36	IO VDD	X2D35	X2D56	X2D57
AB	SPARE	X1D58	IO VSS	X1D37	X1D39	X1D41	IO VDD	X1D43	SPARE	SPARE	IO VSS	SPARE	SPARE	IO VDD	SPARE	SPARE	X2D43	IO VSS	X2D41	X2D39	X2D37	IO VDD	X2D58	SPARE
AC	IO VSS	IO VSS	SPARE	X1D62	X1D64	IO VDD	X1D66	X1D68	X1D70	IO VSS	SPARE	SPARE	SPARE	SPARE	IO VDD	X2D70	X2D68	X2D66	IO VSS	X2D64	X2D62	SPARE	IO VDD	IO VDD
AD	IO VSS	IO VSS	X1D61	X1D63	X1D65	IO VDD	X1D67	X1D69	SPARE	IO VSS	SPARE	SPARE	SPARE	SPARE	IO VDD	SPARE	X2D69	X2D67	IO VSS	X2D65	X2D63	X2D61	IO VDD	IO VDD

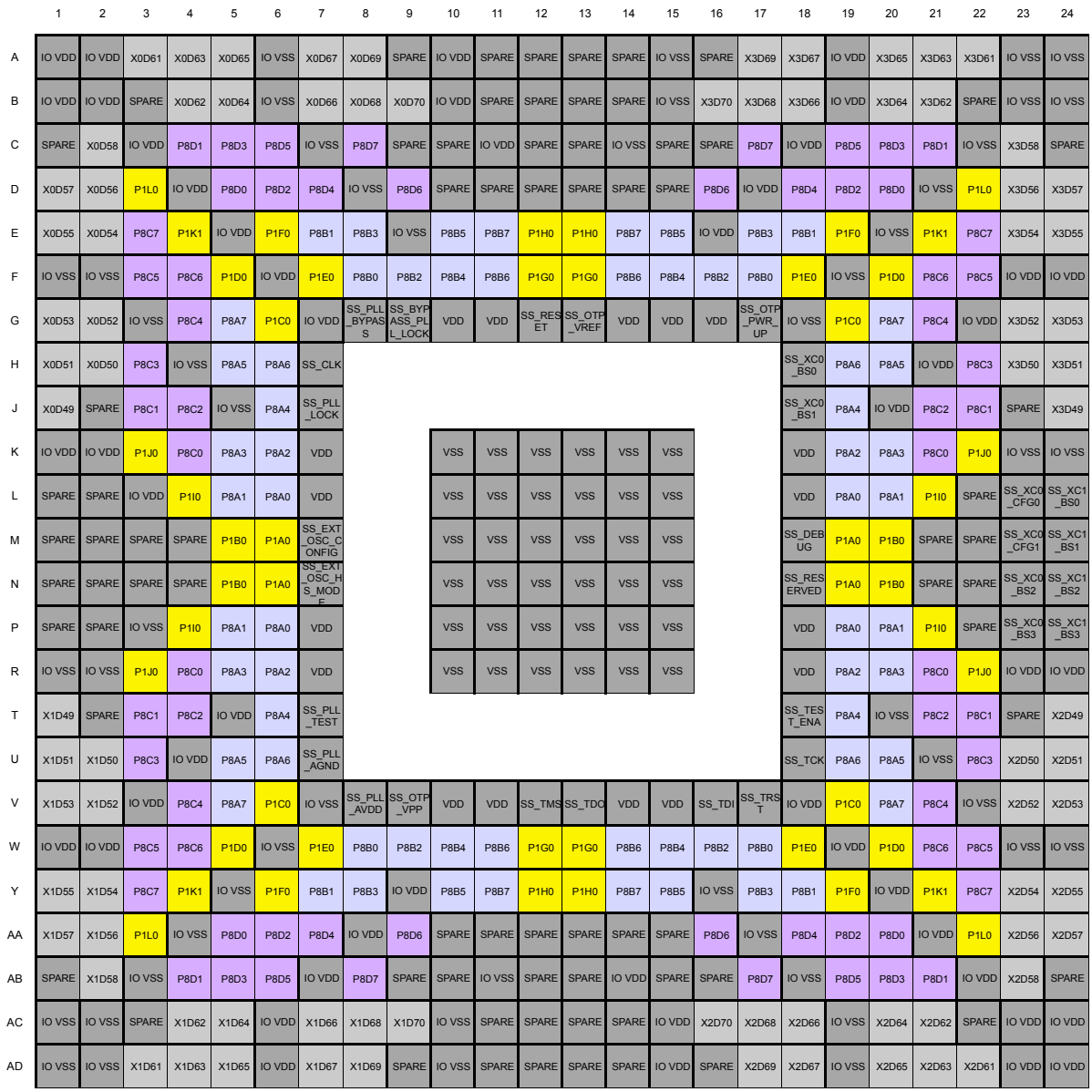
4-bit and 1-bit ports



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	IO VDD	IO VDD	X0D61	X0D63	X0D65	IO VSS	X0D67	X0D69	SPARE	IO VDD	SPARE	SPARE	SPARE	SPARE	IO VSS	SPARE	X3D69	X3D67	IO VDD	X3D65	X3D63	X3D61	IO VSS	IO VSS
B	IO VDD	IO VDD	SPARE	X0D62	X0D64	IO VSS	X0D66	X0D68	X0D70	IO VDD	SPARE	SPARE	SPARE	SPARE	IO VSS	X3D70	X3D68	X3D66	IO VDD	X3D64	X3D62	SPARE	IO VSS	IO VSS
C	SPARE	X0D58	IO VDD	P1N0	P1P0	X0D41	IO VSS	X0D43	SPARE	SPARE	IO VDD	SPARE	SPARE	IO VSS	SPARE	SPARE	X3D43	IO VDD	X3D41	P1P0	P1N0	IO VSS	X3D58	SPARE
D	X0D57	X0D56	P1L0	IO VDD	P1M0	P1O0	X0D40	IO VSS	X0D42	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	X3D42	IO VDD	X3D40	P1O0	P1M0	IO VSS	P1L0	X3D56	X3D57
E	X0D55	X0D54	P4E3	P1K1	IO VDD	P1F0	P4C1	P4D1	IO VSS	P4D3	P4C3	P1H0	P1H0	P4C3	P4D3	IO VDD	P4D1	P4C1	P1F0	IO VSS	P1K1	P4E3	X3D54	X3D55
F	IO VSS	IO VSS	P4F3	P4E2	P1D0	IO VDD	P1E0	P4C0	P4D0	P4D2	P4C2	P1G0	P1G0	P4C2	P4D2	P4D0	P4C0	P1E0	IO VSS	P1D0	P4E2	P4F3	IO VDD	IO VDD
G	X0D53	X0D52	IO VSS	P4F2	P4A3	P1C0	IO VDD	SS_PLL_BYPASS	SS_BYPASS_PLL_LOCK	VDD	VDD	SS_RESET	SS_OTP_VREF	VDD	VDD	VDD	SS_OTP_PWR_UP	IO VSS	P1C0	P4A3	P4F2	IO VDD	X3D52	X3D53
H	X0D51	X0D50	P4F1	IO VSS	P4B3	P4A2	SS_CLK											SS_XC0_BS0	P4A2	P4B3	IO VDD	P4F1	X3D50	X3D51
J	X0D49	SPARE	P4E1	P4F0	IO VSS	P4B2	SS_PLL_LOCK											SS_XC0_BS1	P4B2	IO VDD	P4F0	P4E1	SPARE	X3D49
K	IO VDD	IO VDD	P1J0	P4E0	P4B1	P4B0	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	P4B0	P4B1	P4E0	P1J0	IO VSS	IO VSS
L	SPARE	SPARE	IO VDD	P1I0	P4A1	P4A0	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	P4A0	P4A1	P1I0	SPARE	SS_XC0_CFG0	SS_XC1_BS0
M	SPARE	SPARE	SPARE	SPARE	P1B0	P1A0	SS_EXT_OSC_CONFIG			VSS	VSS	VSS	VSS	VSS	VSS			SS_DEBUG	P1A0	P1B0	SPARE	SPARE	SS_XC0_CFG1	SS_XC1_BS1
N	SPARE	SPARE	SPARE	SPARE	P1B0	P1A0	SS_EXT_OSC_HS_MODE			VSS	VSS	VSS	VSS	VSS	VSS			SS_RESERVED	P1A0	P1B0	SPARE	SPARE	SS_XC0_BS2	SS_XC1_BS2
P	SPARE	SPARE	IO VSS	P1I0	P4A1	P4A0	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	P4A0	P4A1	P1I0	SPARE	SS_XC0_BS3	SS_XC1_BS3
R	IO VSS	IO VSS	P1J0	P4E0	P4B1	P4B0	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	P4B0	P4B1	P4E0	P1J0	IO VDD	IO VDD
T	X1D49	SPARE	P4E1	P4F0	IO VDD	P4B2	SS_PLL_TEST											SS_TEST_ENA	P4B2	IO VSS	P4F0	P4E1	SPARE	X2D49
U	X1D51	X1D50	P4F1	IO VDD	P4B3	P4A2	SS_PLL_AGND											SS_TCK	P4A2	P4B3	IO VSS	P4F1	X2D50	X2D51
V	X1D53	X1D52	IO VDD	P4F2	P4A3	P1C0	IO VSS	SS_PLL_AVDD	SS_OTP_VPP	VDD	VDD	SS_TMS	SS_TDO	VDD	VDD	SS_TDI	SS_TRST	IO VDD	P1C0	P4A3	P4F2	IO VSS	X2D52	X2D53
W	IO VDD	IO VDD	P4F3	P4E2	P1D0	IO VSS	P1E0	P4C0	P4D0	P4D2	P4C2	P1G0	P1G0	P4C2	P4D2	P4D0	P4C0	P1E0	IO VDD	P1D0	P4E2	P4F3	IO VSS	IO VSS
Y	X1D55	X1D54	P4E3	P1K1	IO VSS	P1F0	P4C1	P4D1	IO VDD	P4D3	P4C3	P1H0	P1H0	P4C3	P4D3	IO VSS	P4D1	P4C1	P1F0	IO VDD	P1K1	P4E3	X2D54	X2D55
AA	X1D57	X1D56	P1L0	IO VSS	P1M0	P1O0	X1D40	IO VDD	X1D42	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	X2D42	IO VSS	X2D40	P1O0	P1M0	IO VDD	P1L0	X2D56	X2D57
AB	SPARE	X1D58	IO VSS	P1N0	P1P0	X1D41	IO VDD	X1D43	SPARE	SPARE	IO VSS	SPARE	SPARE	IO VDD	SPARE	SPARE	X2D43	IO VSS	X2D41	P1P0	P1N0	IO VDD	X2D58	SPARE
AC	IO VSS	IO VSS	SPARE	X1D62	X1D64	IO VDD	X1D66	X1D68	X1D70	IO VSS	SPARE	SPARE	SPARE	SPARE	IO VDD	X2D70	X2D68	X2D66	IO VSS	X2D64	X2D62	SPARE	IO VDD	IO VDD
AD	IO VSS	IO VSS	X1D61	X1D63	X1D65	IO VDD	X1D67	X1D69	SPARE	IO VSS	SPARE	SPARE	SPARE	SPARE	IO VDD	SPARE	X2D69	X2D67	IO VSS	X2D65	X2D63	X2D61	IO VDD	IO VDD

XCore	1-bit port pins	4-bit port pins	Spare pins
0	16	24	20
1	16	24	20
2	16	24	17
3	16	24	17

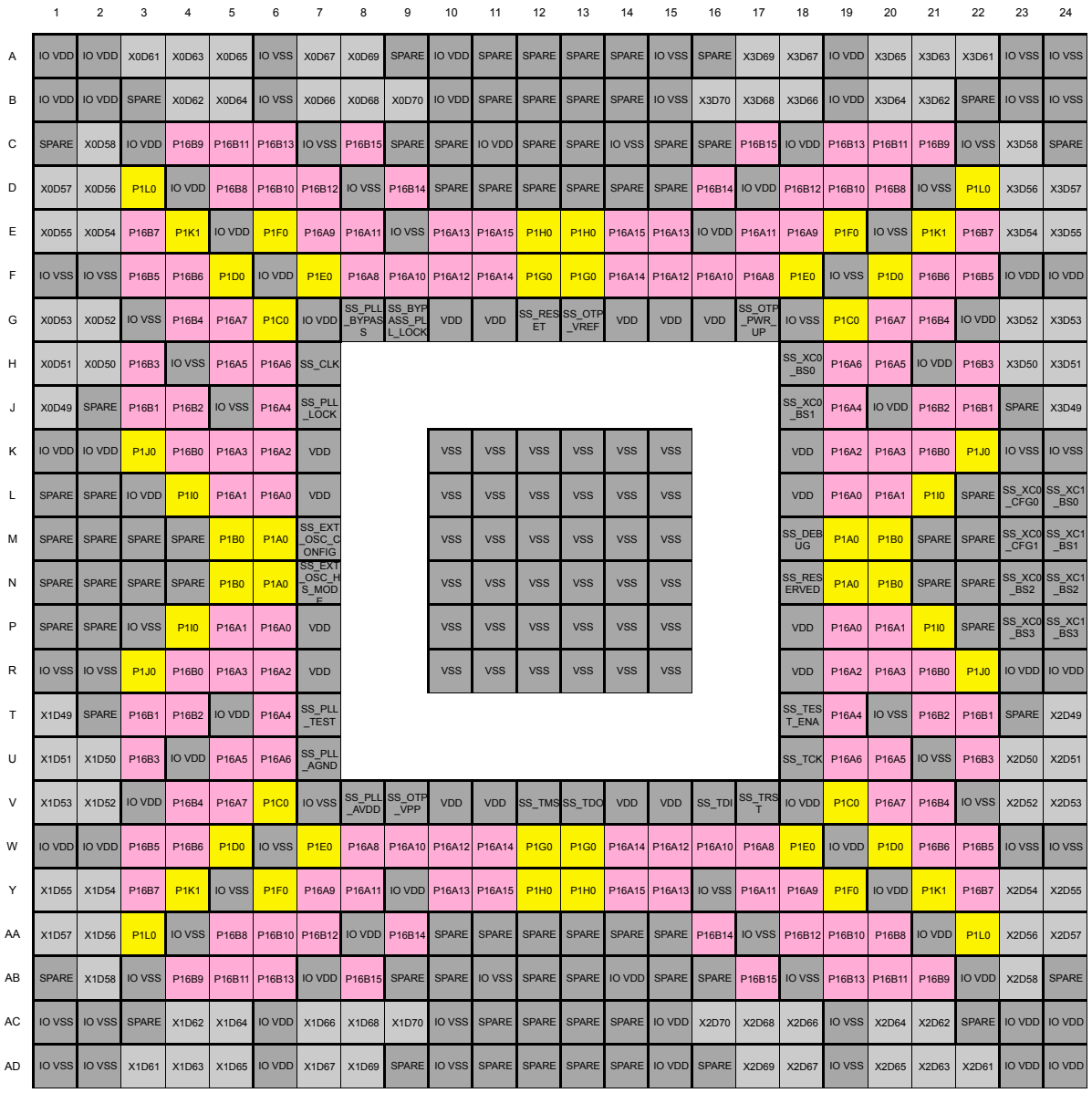
8-bit and 1-bit ports



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
IO VDD	IO VDD	X0D61	X0D63	X0D65	IO VSS	X0D67	X0D69	SPARE	IO VDD	SPARE	SPARE	SPARE	SPARE	IO VSS	SPARE	X3D69	X3D67	IO VDD	X3D65	X3D63	X3D61	IO VSS	IO VSS	A
IO VDD	IO VDD	SPARE	X0D62	X0D64	IO VSS	X0D66	X0D68	X0D70	IO VDD	SPARE	SPARE	SPARE	SPARE	IO VSS	X3D70	X3D68	X3D66	IO VDD	X3D64	X3D62	SPARE	IO VSS	IO VSS	B
SPARE	X0D58	IO VDD	P8D1	P8D3	P8D5	IO VSS	P8D7	SPARE	SPARE	IO VDD	SPARE	SPARE	IO VSS	SPARE	SPARE	P8D7	IO VDD	P8D5	P8D3	P8D1	IO VSS	X3D58	SPARE	C
X0D57	X0D56	P1L0	IO VDD	P8D0	P8D2	P8D4	IO VSS	P8D6	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	P8D6	IO VDD	P8D4	P8D2	P8D0	IO VSS	P1L0	X3D56	X3D57	D
X0D55	X0D54	P8C7	P1K1	IO VDD	P1F0	P8B1	P8B3	IO VSS	P8B5	P8B7	P1H0	P1H0	P8B7	P8B5	IO VDD	P8B3	P8B1	P1F0	IO VSS	P1K1	P8C7	X3D54	X3D55	E
IO VSS	IO VSS	P8C5	P8C6	P1D0	IO VDD	P1E0	P8B0	P8B2	P8B4	P8B6	P1G0	P1G0	P8B6	P8B4	P8B2	P8B0	P1E0	IO VSS	P1D0	P8C6	P8C5	IO VDD	IO VDD	F
X0D53	X0D52	IO VSS	P8C4	P8A7	P1C0	IO VDD	SS_PLL_BYPASS	SS_BYPASS_PLL_LOCK	VDD	VDD	SS_RESET	SS_OTP_VREF	VDD	VDD	VDD	SS_OTP_PWR_UP	IO VSS	P1C0	P8A7	P8C4	IO VDD	X3D52	X3D53	G
X0D51	X0D50	P8C3	IO VSS	P8A5	P8A6	SS_CLK											SS_XC0_BS0	P8A6	P8A5	IO VDD	P8C3	X3D50	X3D51	H
X0D49	SPARE	P8C1	P8C2	IO VSS	P8A4	SS_PLL_LOCK											SS_XC0_BS1	P8A4	IO VDD	P8C2	P8C1	SPARE	X3D49	J
IO VDD	IO VDD	P1J0	P8C0	P8A3	P8A2	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	P8A2	P8A3	P8C0	P1J0	IO VSS	IO VSS	K
SPARE	SPARE	IO VDD	P1I0	P8A1	P8A0	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	P8A0	P8A1	P1I0	SPARE	SS_XC0_CFG0	SS_XC1_BS0	L
SPARE	SPARE	SPARE	SPARE	P1B0	P1A0	SS_EXT_OSC_CONFIG			VSS	VSS	VSS	VSS	VSS	VSS			SS_DEBUG	P1A0	P1B0	SPARE	SPARE	SS_XC0_CFG1	SS_XC1_BS1	M
SPARE	SPARE	SPARE	SPARE	P1B0	P1A0	SS_EXT_OSC_HS_MODE			VSS	VSS	VSS	VSS	VSS	VSS			SS_RESERVED	P1A0	P1B0	SPARE	SPARE	SS_XC0_BS2	SS_XC1_BS2	N
SPARE	SPARE	IO VSS	P1I0	P8A1	P8A0	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	P8A0	P8A1	P1I0	SPARE	SS_XC0_BS3	SS_XC1_BS3	P
IO VSS	IO VSS	P1J0	P8C0	P8A3	P8A2	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	P8A2	P8A3	P8C0	P1J0	IO VDD	IO VDD	R
X1D49	SPARE	P8C1	P8C2	IO VDD	P8A4	SS_PLL_TEST											SS_TEST_ENA	P8A4	IO VSS	P8C2	P8C1	SPARE	X2D49	T
X1D51	X1D50	P8C3	IO VDD	P8A5	P8A6	SS_PLL_AGND											SS_TCK	P8A6	P8A5	IO VSS	P8C3	X2D50	X2D51	U
X1D53	X1D52	IO VDD	P8C4	P8A7	P1C0	IO VSS	SS_PLL_AVDD	SS_OTP_VPP	VDD	VDD	SS_TMS	SS_TDO	VDD	VDD	SS_TDI	SS_TRST	IO VDD	P1C0	P8A7	P8C4	IO VSS	X2D52	X2D53	V
IO VDD	IO VDD	P8C5	P8C6	P1D0	IO VSS	P1E0	P8B0	P8B2	P8B4	P8B6	P1G0	P1G0	P8B6	P8B4	P8B2	P8B0	P1E0	IO VDD	P1D0	P8C6	P8C5	IO VSS	IO VSS	W
X1D55	X1D54	P8C7	P1K1	IO VSS	P1F0	P8B1	P8B3	IO VDD	P8B5	P8B7	P1H0	P1H0	P8B7	P8B5	IO VSS	P8B3	P8B1	P1F0	IO VDD	P1K1	P8C7	X2D54	X2D55	Y
X1D57	X1D56	P1L0	IO VSS	P8D0	P8D2	P8D4	IO VDD	P8D6	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	P8D6	IO VSS	P8D4	P8D2	P8D0	IO VDD	P1L0	X2D56	X2D57	AA
SPARE	X1D58	IO VSS	P8D1	P8D3	P8D5	IO VDD	P8D7	SPARE	SPARE	IO VSS	SPARE	SPARE	IO VDD	SPARE	SPARE	P8D7	IO VSS	P8D5	P8D3	P8D1	IO VDD	X2D58	SPARE	AB
IO VSS	IO VSS	SPARE	X1D62	X1D64	IO VDD	X1D66	X1D68	X1D70	IO VSS	SPARE	SPARE	SPARE	SPARE	IO VDD	X2D70	X2D68	X2D66	IO VSS	X2D64	X2D62	SPARE	IO VDD	IO VDD	AC
IO VSS	IO VSS	X1D61	X1D63	X1D65	IO VDD	X1D67	X1D69	SPARE	IO VSS	SPARE	SPARE	SPARE	SPARE	IO VDD	SPARE	X2D69	X2D67	IO VSS	X2D65	X2D63	X2D61	IO VDD	IO VDD	AD

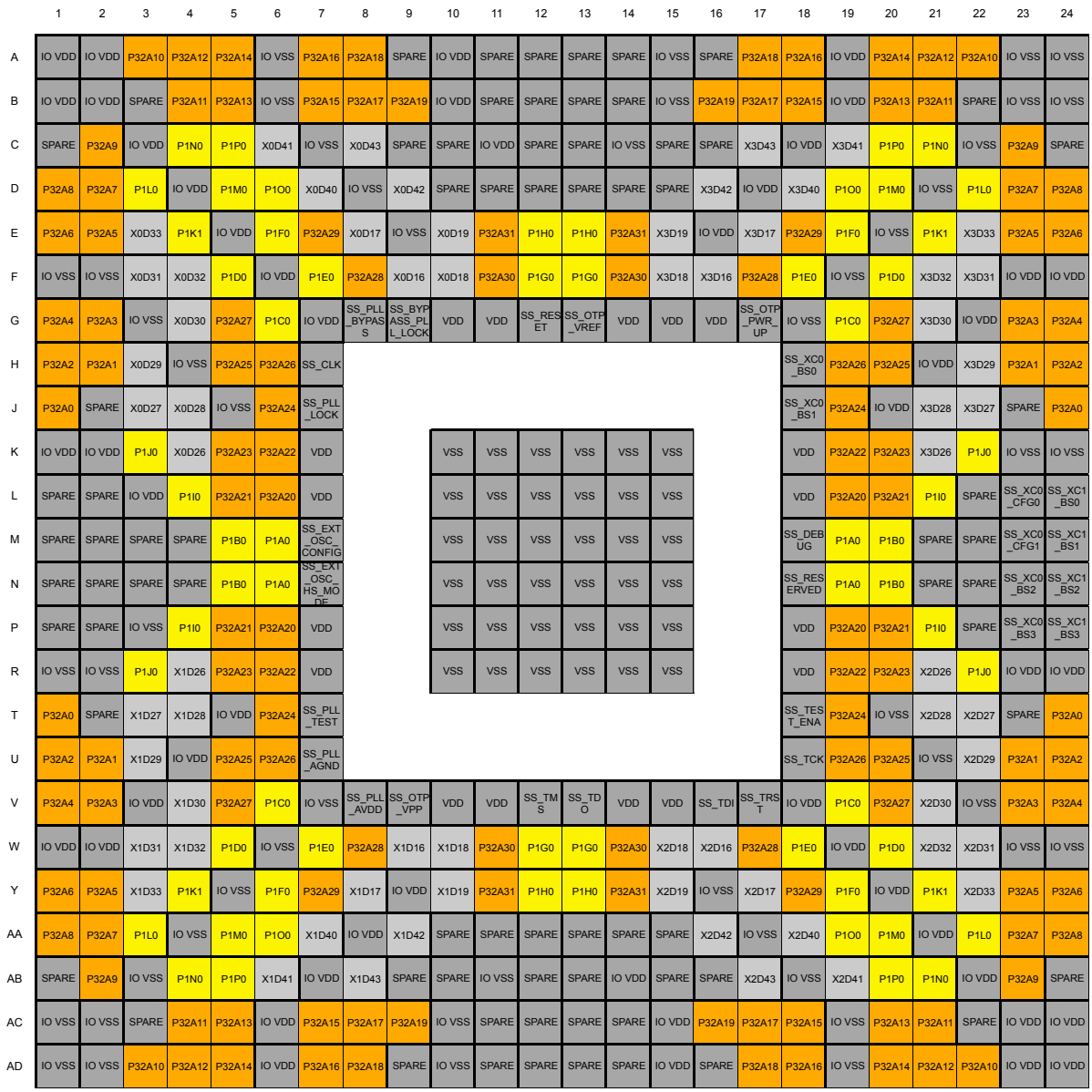
XCore	1-bit port pins	8-bit port pins	Spare pins
0	12	32	20
1	12	32	20
2	12	32	16
3	12	32	16

16-bit and 1-bit ports



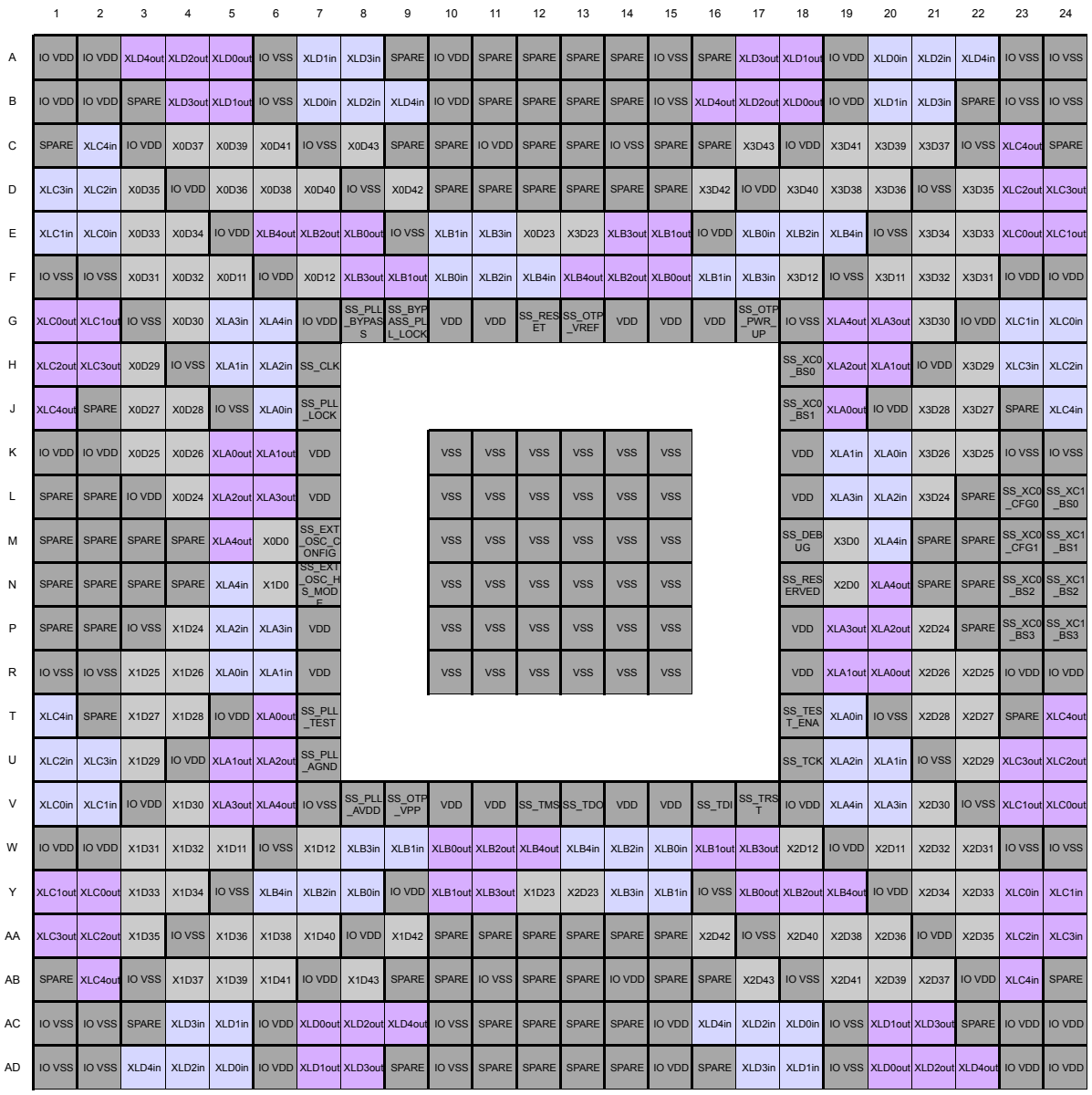
XCore	1-bit port pins	16-bit port pins	Spare pins
0	12	32	20
1	12	32	20
2	12	32	16
3	12	32	16

32-bit and 1-bit ports



XCore	1-bit port pins	32-bit port pins	Spare pins
0	12	32	20
1	12	32	20
2	12	32	16
3	12	32	16

5bit XMOS Links

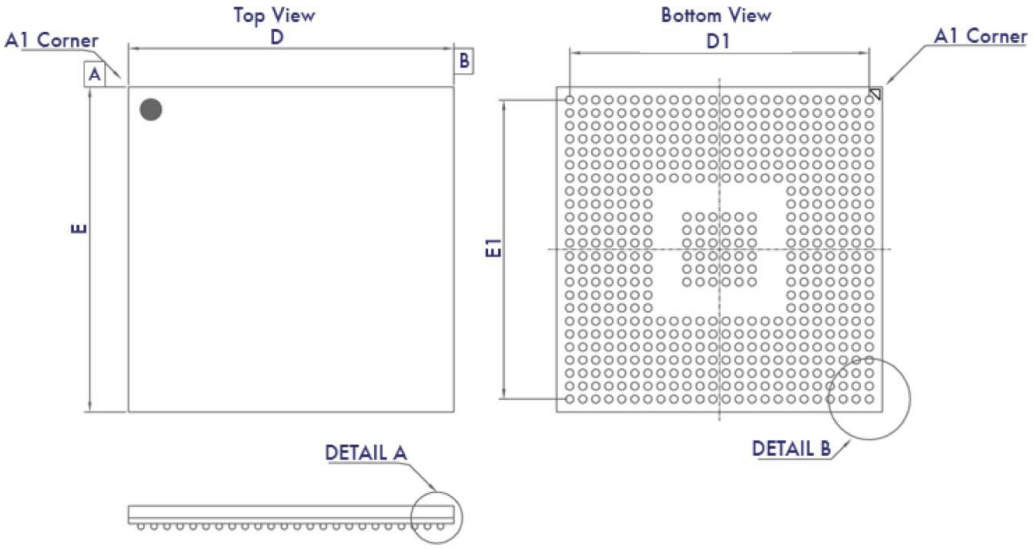


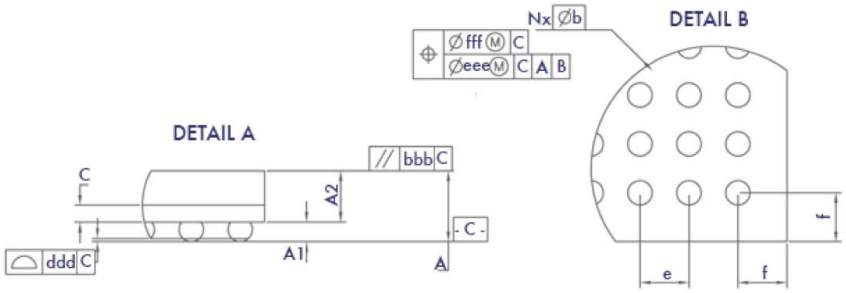
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	IO VDD	IO VDD	XLD4out	XLD2out	XLD0out	IO VSS	XLD1in	XLD3in	SPARE	IO VDD	SPARE	SPARE	SPARE	SPARE	IO VSS	SPARE	XLD3out	XLD1out	IO VDD	XLD0in	XLD2in	XLD4in	IO VSS	IO VSS
B	IO VDD	IO VDD	SPARE	XLD3out	XLD1out	IO VSS	XLD0in	XLD2in	XLD4in	IO VDD	SPARE	SPARE	SPARE	SPARE	IO VSS	XLD4out	XLD2out	XLD0out	IO VDD	XLD1in	XLD3in	SPARE	IO VSS	IO VSS
C	SPARE	XLC4in	IO VDD	X0D37	X0D39	X0D41	IO VSS	X0D43	SPARE	SPARE	IO VDD	SPARE	SPARE	IO VSS	SPARE	SPARE	X3D43	IO VDD	X3D41	X3D39	X3D37	IO VSS	XLC4out	SPARE
D	XLC3in	XLC2in	X0D35	IO VDD	X0D36	X0D38	X0D40	IO VSS	X0D42	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	X3D42	IO VDD	X3D40	X3D38	X3D36	IO VSS	X3D35	XLC2out	XLC3out
E	XLC1in	XLC0in	X0D33	X0D34	IO VDD	XLB4out	XLB2out	XLB0out	IO VSS	XLB1in	XLB3in	X0D23	X3D23	XLB3out	XLB1out	IO VDD	XLB0in	XLB2in	XLB4in	IO VSS	X3D34	X3D33	XLC0out	XLC1out
F	IO VSS	IO VSS	X0D31	X0D32	X0D11	IO VDD	X0D12	XLB3out	XLB1out	XLB0in	XLB2in	XLB4in	XLB4out	XLB2out	XLB0out	XLB1in	XLB3in	X3D12	IO VSS	X3D11	X3D32	X3D31	IO VDD	IO VDD
G	XLC0out	XLC1out	IO VSS	X0D30	XLA3in	XLA4in	IO VDD	SS_PLL_BYPASS	SS_BYPASS_PLL_LOCK	VDD	VDD	SS_RESET	SS_OTP_VREF	VDD	VDD	VDD	SS_OTP_PWR_UP	IO VSS	XLA4out	XLA3out	X3D30	IO VDD	XLC1in	XLC0in
H	XLC2out	XLC3out	X0D29	IO VSS	XLA1in	XLA2in	SS_CLK											SS_XC0_BS0	XLA2out	XLA1out	IO VDD	X3D29	XLC3in	XLC2in
J	XLC4out	SPARE	X0D27	X0D28	IO VSS	XLA0in	SS_PLL_LOCK											SS_XC0_BS1	XLA0out	IO VDD	X3D28	X3D27	SPARE	XLC4in
K	IO VDD	IO VDD	X0D25	X0D26	XLA0out	XLA1out	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	XLA1in	XLA0in	X3D26	X3D25	IO VSS	IO VSS
L	SPARE	SPARE	IO VDD	X0D24	XLA2out	XLA3out	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	XLA3in	XLA2in	X3D24	SPARE	SS_XC0_CFG0	SS_XC1_BS0
M	SPARE	SPARE	SPARE	SPARE	XLA4out	X0D0	SS_EXT_OSC_CONFIG			VSS	VSS	VSS	VSS	VSS	VSS			SS_DEBUG	X3D0	XLA4in	SPARE	SPARE	SS_XC0_CFG1	SS_XC1_BS1
N	SPARE	SPARE	SPARE	SPARE	XLA4in	X1D0	SS_EXT_OSC_HS_MODE			VSS	VSS	VSS	VSS	VSS	VSS			SS_RESERVED	X2D0	XLA4out	SPARE	SPARE	SS_XC0_BS2	SS_XC1_BS2
P	SPARE	SPARE	IO VSS	X1D24	XLA2in	XLA3in	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	XLA3out	XLA2out	X2D24	SPARE	SS_XC0_BS3	SS_XC1_BS3
R	IO VSS	IO VSS	X1D25	X1D26	XLA0in	XLA1in	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	XLA1out	XLA0out	X2D26	X2D25	IO VDD	IO VDD
T	XLC4in	SPARE	X1D27	X1D28	IO VDD	XLA0out	SS_PLL_TEST											SS_TEST_ENA	XLA0in	IO VSS	X2D28	X2D27	SPARE	XLC4out
U	XLC2in	XLC3in	X1D29	IO VDD	XLA1out	XLA2out	SS_PLL_AGND											SS_TCK	XLA2in	XLA1in	IO VSS	X2D29	XLC3out	XLC2out
V	XLC0in	XLC1in	IO VDD	X1D30	XLA3out	XLA4out	IO VSS	SS_PLL_AVDD	SS_OTP_VPP	VDD	VDD	SS_TMS	SS_TDO	VDD	VDD	SS_TDI	SS_TRST	IO VDD	XLA4in	XLA3in	X2D30	IO VSS	XLC1out	XLC0out
W	IO VDD	IO VDD	X1D31	X1D32	X1D11	IO VSS	X1D12	XLB3in	XLB1in	XLB0out	XLB2out	XLB4out	XLB4in	XLB2in	XLB0in	XLB1out	XLB3out	X2D12	IO VDD	X2D11	X2D32	X2D31	IO VSS	IO VSS
Y	XLC1out	XLC0out	X1D33	X1D34	IO VSS	XLB4in	XLB2in	XLB0in	IO VDD	XLB1out	XLB3out	X1D23	X2D23	XLB3in	XLB1in	IO VSS	XLB0out	XLB2out	XLB4out	IO VDD	X2D34	X2D33	XLC0in	XLC1in
AA	XLC3out	XLC2out	X1D35	IO VSS	X1D36	X1D38	X1D40	IO VDD	X1D42	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	X2D42	IO VSS	X2D40	X2D38	X2D36	IO VDD	X2D35	XLC2in	XLC3in
AB	SPARE	XLC4out	IO VSS	X1D37	X1D39	X1D41	IO VDD	X1D43	SPARE	SPARE	IO VSS	SPARE	SPARE	IO VDD	SPARE	SPARE	X2D43	IO VSS	X2D41	X2D39	X2D37	IO VDD	XLC4in	SPARE
AC	IO VSS	IO VSS	SPARE	XLD3in	XLD1in	IO VDD	XLD0out	XLD2out	XLD4out	IO VSS	SPARE	SPARE	SPARE	SPARE	IO VDD	XLD4in	XLD2in	XLD0in	IO VSS	XLD1out	XLD3out	SPARE	IO VDD	IO VDD
AD	IO VSS	IO VSS	XLD4in	XLD2in	XLD0in	IO VDD	XLD1out	XLD3out	SPARE	IO VSS	SPARE	SPARE	SPARE	SPARE	IO VDD	SPARE	XLD3in	XLD1in	IO VSS	XLD0out	XLD2out	XLD4out	IO VDD	IO VDD

2bit XMOS Links

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	IO VDD	IO VDD	X0D61	X0D63	XLD0out	IO VSS	XLD1in	X0D69	SPARE	IO VDD	SPARE	SPARE	SPARE	SPARE	IO VSS	SPARE	X3D69	XLD1out	IO VDD	XLD0in	X3D63	X3D61	IO VSS	IO VSS
B	IO VDD	IO VDD	SPARE	X0D62	XLD1out	IO VSS	XLD0in	X0D68	X0D70	IO VDD	SPARE	SPARE	SPARE	SPARE	IO VSS	X3D70	X3D68	XLD0out	IO VDD	XLD1in	X3D62	SPARE	IO VSS	IO VSS
C	SPARE	X0D58	IO VDD	X0D37	X0D39	X0D41	IO VSS	X0D43	SPARE	SPARE	IO VDD	SPARE	SPARE	IO VSS	SPARE	SPARE	X3D43	IO VDD	X3D41	X3D39	X3D37	IO VSS	X3D58	SPARE
D	X0D57	X0D56	X0D35	IO VDD	X0D36	X0D38	X0D40	IO VSS	X0D42	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	X3D42	IO VDD	X3D40	X3D38	X3D36	IO VSS	X3D35	X3D56	X3D57
E	XLC1in	XLC0in	X0D33	X0D34	IO VDD	X0D13	X0D15	XLB0out	IO VSS	XLB1in	X0D21	X0D23	X3D23	X3D21	XLB1out	IO VDD	XLB0in	X3D15	X3D13	IO VSS	X3D34	X3D33	XLC0out	XLC1out
F	IO VSS	IO VSS	X0D31	X0D32	X0D11	IO VDD	X0D12	X0D14	XLB1out	XLB0in	X0D20	X0D22	X3D22	X3D20	XLB0out	XLB1in	X3D14	X3D12	IO VSS	X3D11	X3D32	X3D31	IO VDD	IO VDD
G	XLC0out	XLC1out	IO VSS	X0D30	X0D9	X0D10	IO VDD	SS_PLL_BYPASS	SS_BYPASS_PLL_LOCK	VDD	VDD	SS_RESET	SS_OTP_VREF	VDD	VDD	VDD	SS_OTP_PWR_UP	IO VSS	X3D10	X3D9	X3D30	IO VDD	XLC1in	XLC0in
H	X0D51	X0D50	X0D29	IO VSS	XLA1in	X0D8	SS_CLK											SS_XC0_BS0	X3D8	XLA1out	IO VDD	X3D29	X3D50	X3D51
J	X0D49	SPARE	X0D27	X0D28	IO VSS	XLA0in	SS_PLL_LOCK											SS_XC0_BS1	XLA0out	IO VDD	X3D28	X3D27	SPARE	X3D49
K	IO VDD	IO VDD	X0D25	X0D26	XLA0out	XLA1out	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	XLA1in	XLA0in	X3D26	X3D25	IO VSS	IO VSS
L	SPARE	SPARE	IO VDD	X0D24	X0D3	X0D2	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	X3D2	X3D3	X3D24	SPARE	SS_XC0_CFG0	SS_XC1_BS0
M	SPARE	SPARE	SPARE	SPARE	X0D1	X0D0	SS_EXT_OSC_CONFIG			VSS	VSS	VSS	VSS	VSS	VSS			SS_DEBUG	X3D0	X3D1	SPARE	SPARE	SS_XC0_CFG1	SS_XC1_BS1
N	SPARE	SPARE	SPARE	SPARE	X1D1	X1D0	SS_EXT_OSC_HS_MODE			VSS	VSS	VSS	VSS	VSS	VSS			SS_RESERVED	X2D0	X2D1	SPARE	SPARE	SS_XC0_BS2	SS_XC1_BS2
P	SPARE	SPARE	IO VSS	X1D24	X1D3	X1D2	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	X2D2	X2D3	X2D24	SPARE	SS_XC0_BS3	SS_XC1_BS3
R	IO VSS	IO VSS	X1D25	X1D26	XLA0in	XLA1in	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	XLA1out	XLA0out	X2D26	X2D25	IO VDD	IO VDD
T	X1D49	SPARE	X1D27	X1D28	IO VDD	XLA0out	SS_PLL_TEST											SS_TEST_ENA	XLA0in	IO VSS	X2D28	X2D27	SPARE	X2D49
U	X1D51	X1D50	X1D29	IO VDD	XLA1out	X1D8	SS_PLL_AGND											SS_TCK	X2D8	XLA1in	IO VSS	X2D29	X2D50	X2D51
V	XLC0in	XLC1in	IO VDD	X1D30	X1D9	X1D10	IO VSS	SS_PLL_AVDD	SS_OTP_VPP	VDD	VDD	SS_TMS	SS_TDO	VDD	VDD	SS_TDI	SS_TRST	IO VDD	X2D10	X2D9	X2D30	IO VSS	XLC1out	XLC0out
W	IO VDD	IO VDD	X1D31	X1D32	X1D11	IO VSS	X1D12	X1D14	XLB1in	XLB0out	X1D20	X1D22	X2D22	X2D20	XLB0in	XLB1out	X2D14	X2D12	IO VDD	X2D11	X2D32	X2D31	IO VSS	IO VSS
Y	XLC1out	XLC0out	X1D33	X1D34	IO VSS	X1D13	X1D15	XLB0in	IO VDD	XLB1out	X1D21	X1D23	X2D23	X2D21	XLB1in	IO VSS	XLB0out	X2D15	X2D13	IO VDD	X2D34	X2D33	XLC0in	XLC1in
AA	X1D57	X1D56	X1D35	IO VSS	X1D36	X1D38	X1D40	IO VDD	X1D42	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	X2D42	IO VSS	X2D40	X2D38	X2D36	IO VDD	X2D35	X2D56	X2D57
AB	SPARE	X1D58	IO VSS	X1D37	X1D39	X1D41	IO VDD	X1D43	SPARE	SPARE	IO VSS	SPARE	SPARE	IO VDD	SPARE	SPARE	X2D43	IO VSS	X2D41	X2D39	X2D37	IO VDD	X2D58	SPARE
AC	IO VSS	IO VSS	SPARE	X1D62	XLD1in	IO VDD	XLD0out	X1D68	X1D70	IO VSS	SPARE	SPARE	SPARE	SPARE	IO VDD	X2D70	X2D68	XLD0in	IO VSS	XLD1out	X2D62	SPARE	IO VDD	IO VDD
AD	IO VSS	IO VSS	X1D61	X1D63	XLD0in	IO VDD	XLD1out	X1D69	SPARE	IO VSS	SPARE	SPARE	SPARE	SPARE	IO VDD	SPARE	X2D69	XLD1in	IO VSS	XLD0out	X2D63	X2D61	IO VDD	IO VDD

4.2 Package Mechanical Details





Dimensional Ref			
REF	Min	Nom	Max
A			1.6
A1	0.27		
A2	1.02	1.06	1.1
D		20.0	
D1		18.4	
E		20.0	
E1		18.4	
b		0.5	
c	0.32	0.36	0.40
e		0.8	
f		0.8	
m		24	
n		512	

Dimensional Tol	
aaa	0.15
bbb	0.10
ddd	0.20
eee	0.15
fff	0.08

Notes	
1.	All dimensions in mm.
2.	‘e’ represents the basic solder ball pitch.
3.	‘m’ represents the basic solder ball matrix size. ‘n’ is the number of attached solder balls.
4.	‘b’ is measurable at the maximum solder ball diameter parallel the primary datum – C –.
5.	Dimension ‘aaa’ is measured parallel to primary datum – C –.
6.	Primary datum – C – and the seating plane are defined by the spherical crowns of the solder balls.
7.	The package surface shall be matte finish charmilles 24 to 27.
8.	The over package thickness ‘A’ already considers collapse balls.

5 Device Configuration

Example schematic diagrams detailing minimal system configurations may be found at: http://xmos.com/support/silicon

6 Device ID

6.1 XMOS JEDEC Manufacturer ID

JEDEC is an international organization that manages standards in the electronic and semiconductor industries. XMOS has a unique Manufacturers ID which is:

7F7F7F7F7F7F19H

or:

01111111011111110111111101111111011111110111111100011000B

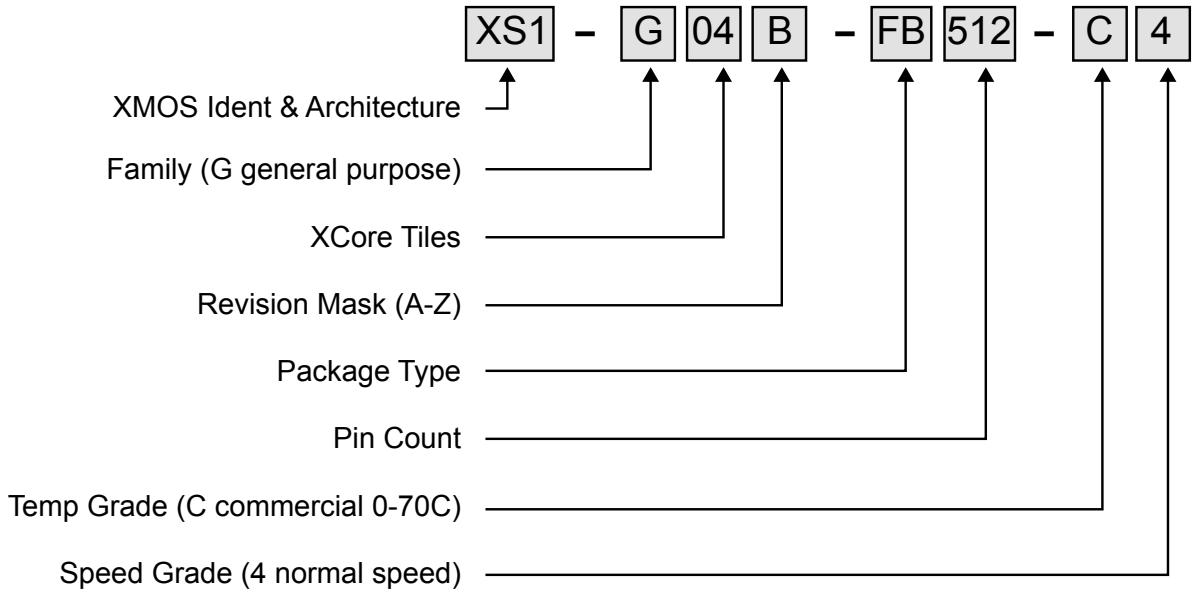
6.2 XMOS JTAG ID

A modified version of the XMOS JEDEC Manufacturers ID is installed in the JTAG ID field. It appears in the JTAG ID as:

Bit31																												Bit0
Unused				Device Part No.																Manufacturer's ID									1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	1	0	0	1	1

7 Ordering information

Part numbering and ordering information



7.1 Orderable part numbers

Part Number	Package	Qualification
XS1-G04B-FB512-C4	PBGA512 0.8mm pitch	Commercial $0°C$ to $+70°C$
XS1-G04B-FB512-I4	PBGA512 0.8mm pitch	Industrial $-40°C$ to $+85°C$

8 Related Documents

Information about XMOS technology is primarily available from the XMOS web site; please see http://xmos.com/documentation for the latest documents or click on one of the links below to find out more information.

Document title	Document reference
The XMOS XS1 Architecture	xs1_en
Programming XC on XMOS Devices	xc_en
XS1-G System Specification	xsystem
XMOS Tools User Guide	xtools_en
XS1 Assembly Language Manual	xas_en
XMOS XS1 32-Bit Application Binary Interface	abi_en
XS1-G Clock Frequency Control Application Note	xs1g_clk
Estimating Power Consumption For XS1-G Devices	xs1g_power

Document History

Date	Release	Comment
2009-12-18	3.4	Revised format
2010-06-07	3.5	Fixed pin list on page 8/30. Updated power consumption section

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