XS1-G2 144BGA Datasheet

Version 2.6

XMOS

Publication Date: 2010/06/07

Description

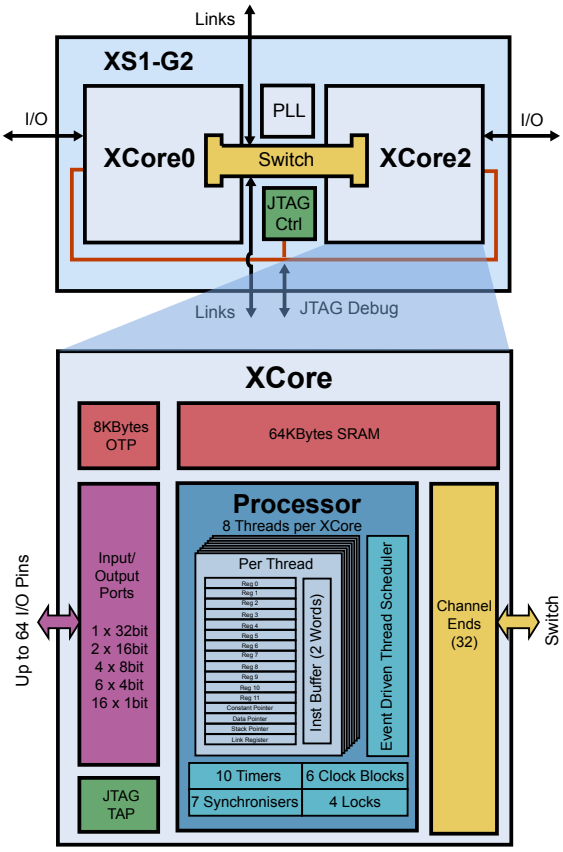
The XS1-G family blends a powerful programmable fabric based on multi-threaded processors with a high-level programming language design flow. XMOS chips are general-purpose programmable devices that can be used in a wide range of applications and systems.

The XS1-G2 device integrates two XCore™ devices. Each XCore contains a 32-bit processor, SRAM memory, I/O ports for communicating with external components and channels for communicating with other devices.

OTP memory is provided for application boot code and security keys, with a secure mode that disables debug and prevents read-back of memory contents.

A high performance switch supports low latency and deterministic communication between the threads in different XCores.

The XMOS architecture is unique in its direct support for concurrent processing (multi-threading), event handling, communication and timed I/O operations.



XS1-G2 Package Features

Two XCores providing 800MIPS and up to 16 concurrent, deterministic real-time tasks
88 user I/O pins, dynamically configurable as input, output or bi-directional
4 XMOS Links

XCore Resources (per core)

Threads	8
Channel Ends	32
Timers	10
Clock Blocks	6 (includes the reference clock)
Thread Synchronisers	7
Hardware Locks	4
SRAM	64KBytes
OTP Memory	8KBytes

1 Signal Descriptions

This section describes the external signal pins of the XS1-G2 in the 144BGA package.

The following I/O type conventions are used in this document:

I/O Type convention	
I	Input
O	Permanent Output
IO	Bidirectional
OT	Tristatable Output
PU	Pull Up
PD	Pull Down
ST	Schmitt Trigger

1.1 XCore Signals

XCore signals can be used for generic I/O ports or for XMOS Links. All the XCore signals are bidirectional and share the same electrical characteristics:

Signal	I/O	Function	Description
X0D0 : X0D43	IO	XCore 0 I/O	Programmable I/O ports for XCore. See Section 1.2 Port Pin Table
X2D0 : X2D43	IO	XCore 2 I/O	

1.1.1 XCore signals as I/O ports

The following table shows the I/O ports available on the two XCore processors. Each port is bidirectional. See Section 1.2 Port Pin Table for details on the signals available for I/O ports in the 144BGA device.

Signal	I/O	Function	Description
P1A[0] . . . P1P[0]	IO	1-bit port	16 ports per XCore
P4A[3:0] . . . P4F[3:0]	IO	4-bit port	8 ports per XCore
P8A[7:0] . . . P8D[7:0]	IO	8-bit port	4 ports per XCore
P16A[15:0] . . . P16B[15:0]	IO	16-bit port	2 ports per XCore

1.1.2 XCore signals as XMOS Links

XMOS Links are full duplex and may operate in either 5wire/direction or 2wire/direction mode. See Section 1.2 Port Pin Table for further information.

5wire fast mode

The following table shows the XMOS link fast interface allocation on each XCore processor:

Signal	Description
XLA[4:0]in XLA[4:0]out	XCore I/O configured as a 5wire link
XLB[4:0]in XLB[4:0]out	XCore I/O configured as a 5wire link

2wire serial mode

The following table shows the XMOS link serial interface allocation on each XCore processor:

Signal	Description
XLA[1:0]in XLA[1:0]out	XCore I/O configured as a 2wire link
XLB[1:0]in XLB[1:0]out	XCore I/O configured as a 2wire link

1.1.3 Precedence

Ports and XMOS Links are connected to pins on the XS1-G2 by the program running on the device. The ports and links are multiplexed and follow a defined precedence if they overlap on the same core:

- If an XMOS Link is enabled, the link has access to the pins; the pins of the underlying ports are disabled.
- If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled.

Ports always operate at their specified width, even if they share pins with another port.

1.2 Port Pin Table

	XCORES		XMOS LINKS		PORTS			
Package	Ball Location		XCORE0, XCORE2					
Ball Name	X0	X2	5bit	2bit	1b	4b	8b	16b
XnD0	J3	D10			P1A0			
XnD1	H3	E10	XLA4in		P1B0			
XnD2	G3	F10	XLA3in			P4A0	P8A0	P16A0
XnD3	F3	G10	XLA2in			P4A1	P8A1	P16A1
XnD4	E3	H10	XLA1in	XLA1in		P4B0	P8A2	P16A2
XnD5	D3	J10	XLA0in	XLA0in		P4B1	P8A3	P16A3
XnD6	C4	K9	XLA0out	XLA0out		P4B2	P8A4	P16A4
XnD7	C5	K8	XLA1out	XLA1out		P4B3	P8A5	P16A5
XnD8	C6	K7	XLA2out			P4A2	P8A6	P16A6
XnD9	C7	K6	XLA3out			P4A3	P8A7	P16A7
XnD10	C8	K5	XLA4out		P1C0			
XnD11	C9	K4			P1D0			
XnD12	K2	C11			P1E0			
XnD13	J2	D11	XLB4in		P1F0			
XnD14	H2	E11	XLB3in			P4C0	P8B0	P16A8
XnD15	E2	H11	XLB2in			P4C1	P8B1	P16A9
XnD16	D2	J11	XLB1in	XLB1in		P4D0	P8B2	P16A10
XnD17	C2	K11	XLB0in	XLB0in		P4D1	P8B3	P16A11
XnD18	B3	L10	XLB0out	XLB0out		P4D2	P8B4	P16A12
XnD19	B4	L9	XLB1out	XLB1out		P4D3	P8B5	P16A13
XnD20	B5	L8	XLB2out			P4C2	P8B6	P16A14
XnD21	B8	L5	XLB3out			P4C3	P8B7	P16A15
XnD22	B9	L4	XLB4out		P1G0			
XnD23	B10	L3			P1H0			
XnD24	L1	B12			P1I0			
XnD25	K1	C12			P1J0			
XnD26	J1	D12				P4E0	P8C0	P16B0
XnD27	H1	E12				P4E1	P8C1	P16B1
XnD28	G1	F12				P4F0	P8C2	P16B2
XnD29	F1	G12				P4F1	P8C3	P16B3
XnD30	E1	H12				P4F2	P8C4	P16B4
XnD31	D1	J12				P4F3	P8C5	P16B5
XnD32	C1	K12				P4E2	P8C6	P16B6
XnD33	B1	L12				P4E3	P8C7	P16B7
XnD34	A2	M11			P1K0			
XnD35	A3	M10			P1L0			
XnD36	A4	M9			P1M0		P8D0	P16B8
XnD37	A5	M8			P1N0		P8D1	P16B9
XnD38	A6	M7			P1O0		P8D2	P16B10
XnD39	A7	M6			P1P0		P8D3	P16B11
XnD40	A8	M5					P8D4	P16B12
XnD41	A9	M4					P8D5	P16B13
XnD42	A10	M3					P8D6	P16B14
XnD43	A11	M2					P8D7	P16B15

1.3 System Service Pin Table

Signal	Ball ID
SS_CLK	E4
SS_DEBUG	E9
SS_PLL_BYPASS	D4
SS_RESET	D5
SS_TCK	H9
SS_TDI	J8

Signal	Ball ID
SS_TDO	J6
SS_TEST_ENA	G9
SS_TMS	J5
SS_TRST	J9
SS_XC0_BS0	D8
	D9

1.4 Core Power and Ground Pin Table

Signal	Ball ID
VDD	C3
VDD	C10
VDD	D6
VDD	F9
VDD	G4
VDD	J7
VDD	K3
VDD	K10

Signal	Ball ID
VSS	E5
VSS	E6
VSS	E7
VSS	E8
VSS	F5
VSS	F6
VSS	F7
VSS	F8
VSS	G5
VSS	G6
VSS	G7
VSS	G8
VSS	H5
VSS	H6
VSS	H7
VSS	H8

1.5 XCore I/O Power Table

Signal	Ball ID
IO VDD	A1
IO VDD	B6
IO VDD	B11
IO VDD	F2
IO VDD	G11
IO VDD	L2
IO VDD	L7
IO VDD	M12

Signal	Ball ID
IO VSS	A12
IO VSS	B2
IO VSS	B7
IO VSS	F11
IO VSS	G2
IO VSS	L6
IO VSS	L11
IO VSS	M1

1.6 XMOS Link Pin Table

See Section 1.2 Port Pin Table

2 System Services

System Services are required to support correct device behavior. These signals control clocking, reset and boot behavior of the device.

2.1 Clock control signals

These signals control the PLL of the XS1-G2

Signal	Ball ID	I/O	Function	Description
SS_PLL_BYPASS	D4	I, PD	Control	Bypasses the PLL, using SS_CLK directly
SS_PLL_AVDD		pwr		Analog power supply to the PLL
SS_PLL_AGND		pwr		AGND power supply for the PLL
SS_CLK	E4	I, PD, ST	Clock	System clock

Functional description

SS_PLL_BYPASS When pin is set high, SS_CLK is used as the system clock. Set to IO_VDD.

SS_PLL_AVDD The on-chip PLL requires a very clean AVDD power supply. It is recommended that this supply node be separated from the other, noisier, supplies in the board. The supply should be decoupled close to the respective IC power pins. Nominally 1.0V.

SS_PLL_AGND Analogue ground for the PLL. Connect directly to board ground.

SS_CLK Reference clock signal for the on-chip PLL. A default frequency of 20MHz is typically used by XS1 family devices but other frequencies can be derived from SS_CLK using an onboard PLL. Clock frequencies of $\leq$20 MHz and $\geq$25 MHz are supported.

2.2 Miscellaneous control signals

Signal	Ball ID	I/O	Function	Description
SS_XC0_BS0	D8	IO, PU	Boot status XCore0	See Boot status pins below
SS_DEBUG	E9	IO, PU, ST	Debug	Activates multicore debug
SS_RESET	D5	I, PD, ST	Reset	Asynchronous system reset
SS_XC0_CFG0	D9	I, PD		Reserved, tie to IO_VDD
SS_TEST_ENA	G9	I, PD		Reserved, tie pin to ground

Functional description

SS_XC0_BS0 Boot status pin

The boot status pin is dual function.

SS_XC0_BS0 functions as an input prior to the de-assertion of reset. The XS1-G2 latches the value driven onto this pin on the rising edge (de-assertion) of SS_RESET. The value driven should be static and configured using a pullup or pulldown resistor, as the XS1-G2 drives the boot status on this pin after reset. The value configured on this pin defines the boot mode for core 0 as follows:

Value	Description
0	Boot from SPI
1	Boot from JTAG

NOTE: If secure boot from OTP is enabled by programming the OTP, the boot mode indicated on the SS_XC0_BS0 pin is ignored.

After reset is complete, SS_XC0_BS0 becomes an output and the value on this pin indicates the XCore0 boot mode:

Value	Description
0	Boot from SPI
1	Boot from OTP or JTAG

SS_XC0_BS0 should be tied to IO_VDD.

For further details on booting XCores see the XS1-G System Specification document (http://xmos.com/published/xsystem).

SS_DEBUG This pin is used to synchronize the debugging of multiple G2 devices. This pin can operate in both output and input mode. In output mode and when configured to do so, SS_DEBUG is driven low by the device when one or more internal XCore processors hit a debug break point. Prior to this point the pin is tri-stated. In input mode and when configured to do so, driving this pin low puts all internal CPUs into debug mode. Software can set the behavior of each internal XCore based on this pin. This pin should have an external pull up to IO_VDD(3.3V) of 4K7 ohms.

SS_RESET Active low asynchronous-assertion reset signal. At power-up, this pin must be activated for at least 5us after the power supplies are stable to ensure reliable boot up. Following a reset the PLL re-establishes lock after which the XCores boot up according to the BOOT_MODE (see SS_XC0_BS1, SS_XC0_BS0).

SS_XC0_CFG0 Reserved, tie pin to IO_VDD

SS_TEST_ENA Reserved, tie pin to ground.

2.3 JTAG Operation

The XS1-G family supports a generic 5pin JTAG interface, which can be used to provide hardware testing including:

- Boundary scan testing for correct board connectivity
- Onboard source level debugging from remote terminals
- Boundary scanning for OTP ROM

The JTAG connectors on the XCore are:

Signal	Pin ID	I/O	Function	Description
SS_TCK	H9	I, PU, ST	TCK	Test clock
SS_TMS	J5	I, PU	TMS	Test mode select
SS_TRST	J9	I, PU, ST	TRST	Test reset (optional)
SS_TDI	J8	I, PU	TDI	Test data in
SS_TDO	J6	OT, PU	TDO	Test data out

Each XCore and Switch has a JTAG controller with a 10-bit instruction register (IR) and a 32-bit data register (DR). A mux controller selects the XCore the TMS is routed to, and which device TDO is wired to the chip level output. TDO can output in tristate in accordance with the JTAG specification. The JTAG controller supports the following commands:

Symbol	Function	Description
1111111111	BYPASS	See IEEE 1149.1 documentation
0000000100	SAMPLE	
0000001000	PRELOAD	
0000001100	EXTEST	
aaaaaaaa01	PEEK	Copies shared register contents, into data register (a=address register bits)
aaaaaaaa10	POKE	Copies data register contents into shared register (a=address register bits)

The JTAG controller has access to the following registers for an XCore:

Register	Number	JTAG Perm	Description
DEVICE_ID0	0x00	RO	XCore ID register
DEVICE_ID1	0x01	RO	XCore ID register
DEVICE_ID2	0x02	RO	XCore ID register
DEVICE_ID3	0x03	RO	XCore ID register
DBG_CTRL	0x04	RW	Control internal switch permissions to debug register
DBG_INT	0x05	RW	Trigger debug interrupts
PLL_CLK_DIVIDER	0x06	RO	PLL clock divider register
SECURITY_CONFIG	0x07	RO	OTP security configuration register
PLINK[3:0]	0x10 : 0x13	RO	Internal link status
DBG_SCRATCH[7:0]	0x20 : 0x27	RW	Scratch register for debug software protocols
T[7:0]_PC	0x40 : 0x47	RO	Copy of PC
T[7:0]_SR	0x60 : 0x67	RO	Copy of SR

The JTAG controller can read from the DBG_SCRATCH registers at the same time as the XCore, but if both devices write at the same time, the XCore write completes and the JTAG controller is ignored.

The TRST_N pin must be driven low for at least 100ns at power up to reset the JTAG port. If JTAG debug is not required, the TRST_N pin can be tied low with a 1k resistor to hold the JTAG port in reset.

3 DC and Switching Characteristics

3.1 Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
IO_VDD	I/O DC supply voltage	3.0	3.3	3.6	V	1
VDD	Core DC supply voltage	0.95	1.0	1.05	V	2
SS_PLL_AVDD	PLL analogue supply	0.95	1.0	1.05	V	
SS_PLL_DVDD	PLL Digital DC Supply	0.95	1.0	1.05	V	
SS_OTP_VPP	OTP external programming voltage	6.18	6.5	6.83	V	3
Cl	XCore I/O load capacitance			25	pF	
Ta	Operating temperature range (Commercial)	0		70	Degrees C	
	Operating temperature range (Industrial)	-40		85	Degrees C	
Tj	Junction temperature			125	Degrees C	
Tstg	Storage temperature	-65		150	Degrees C	

Notes:

1. Voltages with respect to IO VSS
2. Voltages with respect to VSS
3. Program only

3.2 DC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(IH)	Signal pin input high voltage	2.0		5.5	V	1,2,3
V(IL)	Signal pin input low voltage	-0.3		0.8	V	1,2,3
V(OH)	Signal pin output high voltage	2.4			V	1,2,3
V(OL)	Signal pin output low voltage			0.4	V	1,2,3
I(OL)	Signal pin low level output current		4		mA	1,3
I(OH)	Signal pin high level output current		4		mA	1,3
R(PU)	Signal pin pull-up resistance			100k	Ohms	1,4

Notes:

1. Signal pin may be any pin except power supply pins

2. Voltages with respect to IO VSS
3. Internal pull-up resistors are fitted to general purpose XCore I/O pins. Applies to both XCore I/O and XCore link I/Os.
4. Use for unused I/O only—the internal pull up resistor is not recommended as a substitute for an external pull-up resistor.

3.3 ESD Stress Voltage

ESD Model	ESD Stress Voltage	Notes
HBM	± 2.0 KV	
MM	± 200 V	

3.4 Reset Timing

Parameters	MIN	TYP	MAX	UNITS	Notes
Reset pulse width for correct start-up	100			ns	
PLL Lock			1	ms	
ISA (BOOT)			< 100	μs	

User code must wait for the device to reset, the PLL to be locked and system code to be started, before it can be run.

3.5 Power Supply

Power is applied to the device through the IO_VDD and VDD balls. Several balls of each type are provided to minimize the effect of inductance within the package. All supply pins must be connected. Each supply should be decoupled close to the chip by several 100nF low inductance (for example, ceramic) capacitors between IO_VDD and GND, and VDD and GND.

Input voltages must not exceed specification with respect to IO_VDD, VDD and GND, even during power up and power down ramping. Permanent damage can occur if the operation exceeds these ranges.

3.5.1 Power Supply Sequencing

To ensure correct device operation, the VDDIO and OTP_VDDIO supplies should be present before the VDD supply. Specifically, the VDDIO and OTP_VDDIO supplies should rise to their nominal operating range with VDD held at 0V. The VDD supply should then rise to its nominal operating range with a rise time of less than 10ms.

Quiescent Current

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
I(DDCQ)	Quiescent VDD(core) Current		120		mA	
I(PLLQ)	Quiescent PLL Total Current		4		mA	

Power consumption

The power consumption of the XS1-G2 is highly application dependant. The following figures should be used for budgetary purposes only:

Commercial Qualification						
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
PD	Power dissipation		0.86		Watts	1,2,3

Industrial Qualification						
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
PD	Power dissipation		0.8		Watts	1,2,3

Notes:

1. Assumes typical core and I/O voltages, operating at 400MHz with nominal activity on all cores.
2. P(TYP) value is the usage power consumption under typical operating conditions.
3. P(TYP) value value includes quiescent current.

For further details on power consumption for XS1-G devices see the Estimating Power Consumption For XS1-G Devices Application Note

3.6 Clock

XS1-G devices use an input clock frequency, supplied by the user on the SS_CLK pin, to drive the PLL and obtain the system clock. The nominal frequency of the clock for all XS1 family components is 20MHz but other clock frequencies can be derived from SS_CLK using the MODE pins and internal PLL. For further details on setting the clock frequency see the XS1-G Clock Frequency Control Application Note.

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
	Frequency	12.5	20	100	MHz	1
	Slew rate	1		2	ns	
	Frequency jitter					

Notes:

1. Clock frequencies between 20 and 25 MHz are not supported.

A set of system clock dividers are applied to the system clock frequency allowing specific clock frequencies to be derived for each XCore, the switch and the reference clock.

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
	System Clock Frequency			400	MHz	

Clock edges must be monotonic and remain within the specified voltage and time limits.

3.7 Memory

3.7.1 Internal static memory

The XS1-G2 has a total of 128K bytes of fast internal static memory for high rates of data throughput, divided into 64k bytes per XCore. Each internal memory access consumes one core clock cycle. There is no dedicated external memory interface, although memory can be expanded through appropriate use of the ports.

3.7.2 Internal one-time programmable memory

Each XCore has 64K bits of one-time programmable memory that can be programmed using the JTAG interface.

3.7.3 OTP voltage ramp requirement

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(PP)	OTP VPP Programming Voltage Ramp Rate			1	V/μs	

The OTP may be programmed using its internal charge pump or by supplying a 6.5V VPP programming voltage on the OTP_VPP pin. Unless a programming cycle is underway the OTP_VPP pins should be left undriven.

For further information on security and OTP programming, see the relevant application note.

3.8 Port Timing

Ports timing is explained in a separate application note. Please see http://xmos.com/documentation for more details.

3.8.1 XCore I/O AC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(XOINVALID)	XCore I/O Minimum Output Data Invalid window which can be achieved using Port/ClkBlk combination	9			ns	
T(XOVALID)	XCore I/O Minimum Input Data Valid window to allow safe acquisition of data using Port/ClkBlk combination	8			ns	
T(XIFMAX)	Maximum XCore I/O toggle frequency which can be safely acquired and used as a clock source using a ClkBlk			60	MHz	

The Input Valid window parameter relates to the capability of the XS1-G2 family devices to capture data input to the chip with respect to an external clock source. This parameter can be calculated as the sum of the input setup time and input hold time with regard to the external clock as measured at the G2 device pins. The output invalid window specifies the time for which an output will be invalid with respect to the external clock. Note that these parameters are specified as a window rather than

absolute numbers since the G2 provides functionality to delay the incoming clock with respect to the incoming data. For further details on these parameters and on interfacing to higher speed synchronous interfaces see the relevant application note.

3.9 XMOS Link Interface Performance

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
B(2blink_5)	2b link bandwidth (Nominal load)			160	Mb/s	
B(5blink_5)	5b link bandwidth (Nominal load)			400	Mb/s	

The asynchronous nature of links means that the relative phasing of SS_CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

3.10 JTAG Timing

The JTAG interface may be operated in either synchronous or asynchronous mode.

Parameters	MIN	TYP	MAX	UNITS	Notes
SS_TCLK period	30			ns	
TSU	5			ns	1
TH			10	ns	1
TCO			15	ns	2

Notes:

1. Timing applies to SS_TMS, SS_TRST, SS_TDI inputs
2. Timing applies to SS_TDO output

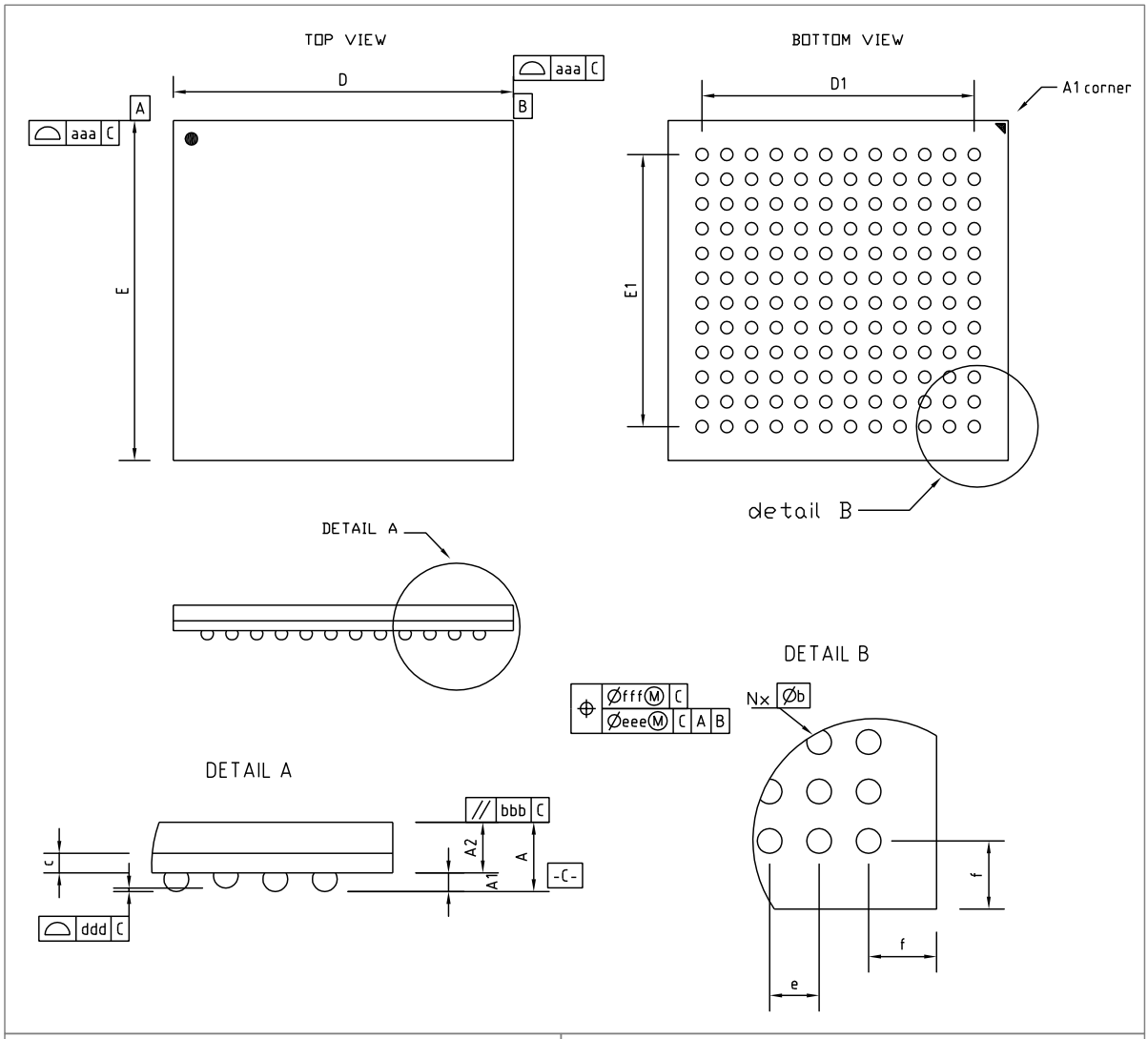
4 Package Details

4.1 Package Pin Layout

The following diagrams show the ball name and location for the BGA144 Package.

	1	2	3	4	5	6	7	8	9	10	11	12
A	IO VDD	X0D34	X0D35	X0D36	X0D37	X0D38	X0D39	X0D40	X0D41	X0D42	X0D43	IO VSS
B	X0D33	IO VSS	X0D18	X0D19	X0D20	IO VDD	IO VSS	X0D21	X0D22	X0D23	IO VDD	X2D24
C	X0D32	X0D17	VDD	X0D6	X0D7	X0D8	X0D9	X0D10	X0D11	VDD	X2D12	X2D25
D	X0D31	X0D16	X0D5	SS_PLL_BYPASS	SS_RESET	VDD	SS_OTP_VPP	SS_XC0_BS0	SS_XC0_CFG0	X2D0	X2D13	X2D26
E	X0D30	X0D15	X0D4	SS_CLK	VSS	VSS	VSS	VSS	SS_DEBUG	X2D1	X2D14	X2D27
F	X0D29	IO VDD	X0D3	SS_PLL_AGND	VSS	VSS	VSS	VSS	VDD	X2D2	IO VSS	X2D28
G	X0D28	IO VSS	X0D2	VDD	VSS	VSS	VSS	VSS	SS_TEST_ENA	X2D3	IO VDD	X2D29
H	X0D27	X0D14	X0D1	SS_PLL_AVDD	VSS	VSS	VSS	VSS	SS_TCK	X2D4	X2D15	X2D30
J	X0D26	X0D13	X0D0	SS_PLL_LOCK	SS_TMS	SS_TDO	VDD	SS_TDI	SS_TRST	X2D5	X2D16	X2D31
K	X0D25	X0D12	VDD	X2D11	X2D10	X2D9	X2D8	X2D7	X2D6	VDD	X2D17	X2D32
L	X0D24	IO VDD	X2D23	X2D22	X2D21	IO VSS	IO VDD	X2D20	X2D19	X2D18	IO VSS	X2D33
M	IO VSS	X2D43	X2D42	X2D41	X2D40	X2D39	X2D38	X2D37	X2D36	X2D35	X2D34	IO VDD

4.2 Package Mechanical Details



Dimensional Ref.			
REF.	Min.	Nom	Max.
A			1.7
A1	0.21		
A2		1.06	
D		11.0	
D1		8.8	
E		11.0	
E1		8.8	
b		0.4	
c	0.32	0.36	0.40
e		0.8	
f		1.1	
m		12	
n		144	

Dimensional Tol.	
aaa	0.15
bbb	0.20
ddd	0.10
eee	0.15
fff	0.08

Notes
1. All dimensions in MM
2. 'e' represents the basic solder ball pitch
3. 'm' represents the basic solder ball matrix size. And 'n' is the number of attached solder balls
4. 'b' is measurable at the maximum solder ball diameter parallel the the primary datum -C-
5. Dimension 'aaa' is measured parallel to primary datum -C-
6. Primary datum -C- and the seating plane are defined by the spherical crowns of the solder balls
7. The package surface shall be matte finish charmilles 24 to 27
8. The over package thickness 'A' already considers collapse balls
11. Reference Jedec Design Guide 4.5 and M0-275

5 Device Configuration

Example schematic diagrams detailing minimal system configurations may be found at: http://xmos.com/support/silicon

6 Device ID

6.1 XMOS JEDEC Manufacturer ID

JEDEC is an international organization that manages standards in the electronic and semiconductor industries. XMOS has a unique Manufacturers ID which is:

7F7F7F7F7F7F19H

or:

01111111011111110111111101111111011111110111111100011000B

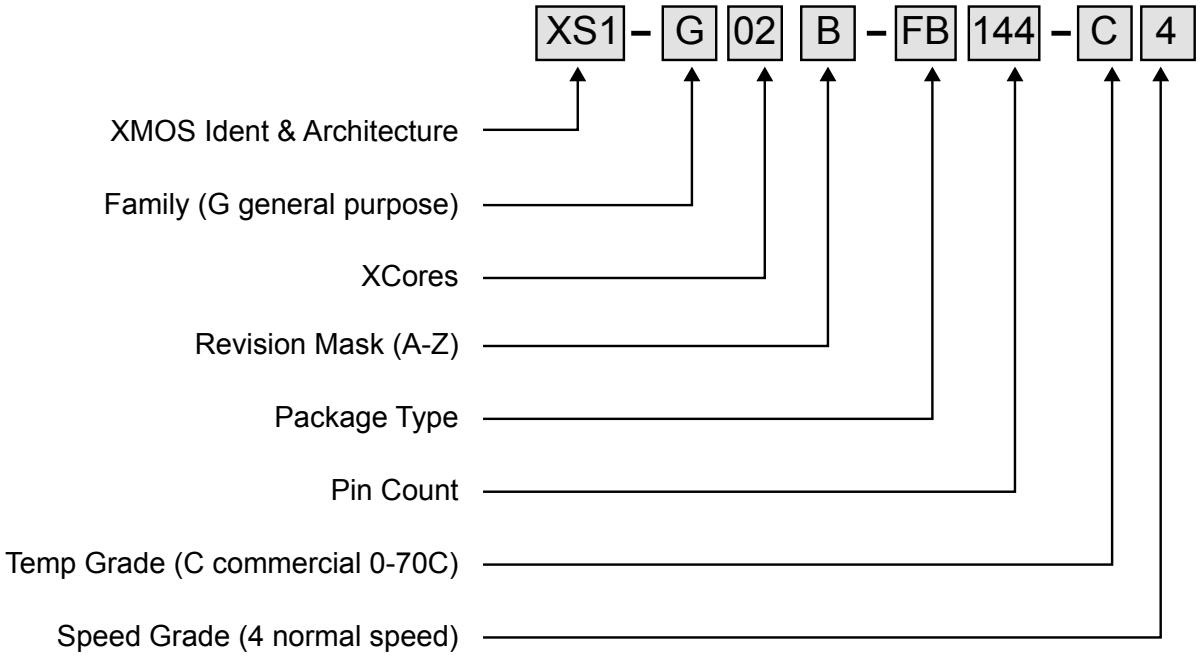
6.2 XMOS JTAG ID

A modified version of the XMOS JEDEC Manufacturers ID is installed in the JTAG ID field. It appears in the JTAG ID as:

Bit31																												Bit0
Unused				Device Part No.																Manufacturer's ID									1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	1	0	0	1	1

7 Ordering information

Part numbering and ordering information



7.1 Orderable part numbers

Part Number	Package	Qualification
XS1-G02B-FB144-C4	FBGA 144 0.8mm pitch	Commercial $0°$C to $+70°$C
XS1-G02B-FB144-I4	FBGA 144 0.8mm pitch	Industrial $-40°$C to $+85°$C

8 Related Documents

Information about XMOS technology is primarily available from the XMOS web site; please see http://xmos.com/documentation for the latest documents or click on one of the links below to find out more information.

Document title	Document reference
The XMOS XS1 Architecture	xs1_en
Programming XC on XMOS Devices	xc_en
XS1-G System Specification	xsystem
XMOS Tools User Guide	xtools_en
XS1 Assembly Language Manual	xas_en
XMOS XS1 32-Bit Application Binary Interface	abi_en
XS1-G Clock Frequency Control Application Note	xs1g_clk
Estimating Power Consumption For XS1-G Devices	xs1g_power

Document History

Date	Release	Comment
2010-06-07	2.6	Revised format Updated power consumption section

Disclaimer